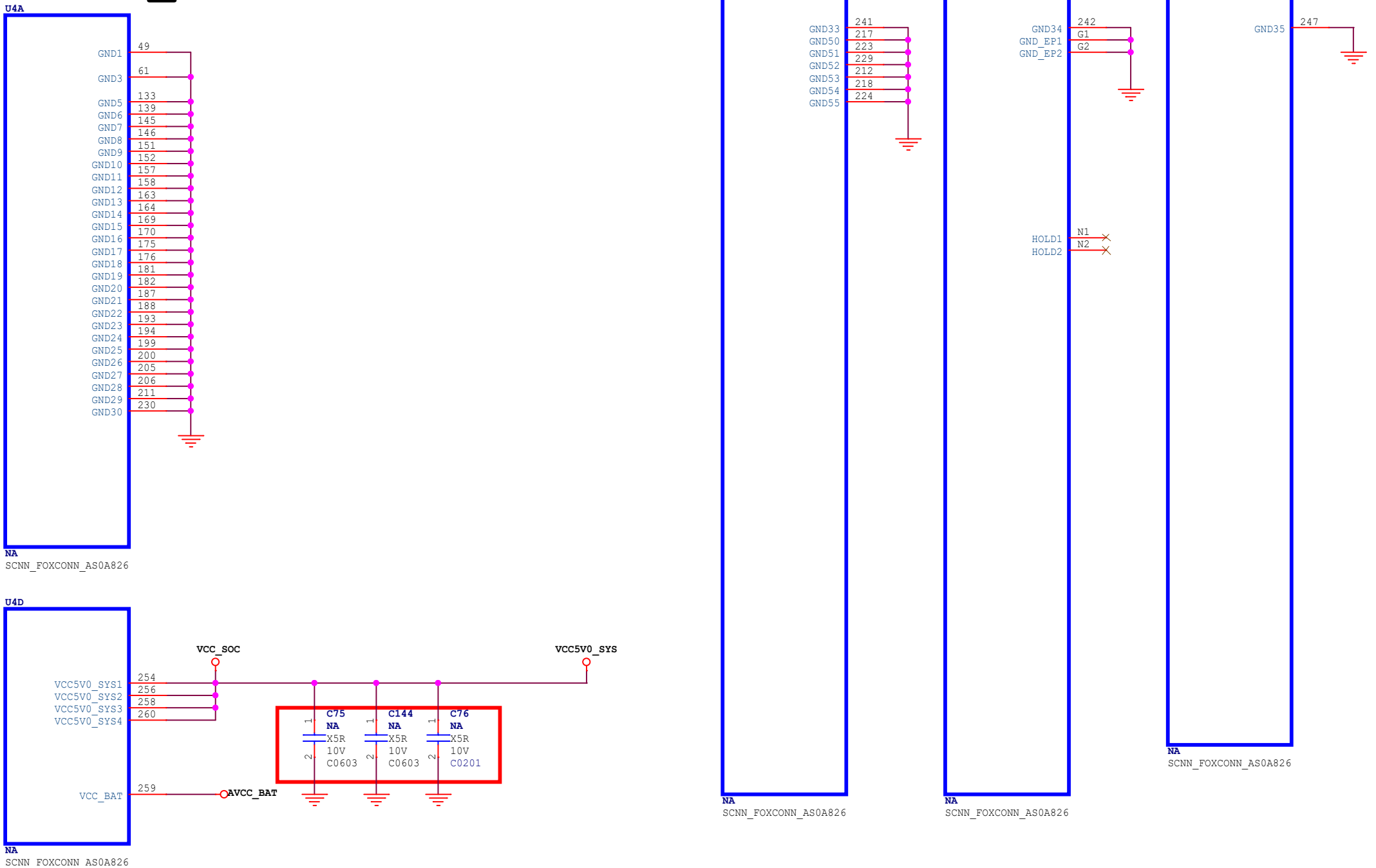
RK3568_ABCDE (Power&Gnd)



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RK3568_F (DDR PHY)

U4F

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15
DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14
DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10
DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9
DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13
DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12
DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8
DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11
DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1
DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P
DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N
DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25
DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24
DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ28
DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29
DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26
DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31
DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30
DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27
DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3
DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P
DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N
DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1
DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5
DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6
DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4
DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2
DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3
DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7
DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0
DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0
DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P
DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N
DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18
DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19
DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22
DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23
DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16
DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17
DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20
DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21
DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2
DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P
DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N
DDR4_ECC_DQ7	--	DDR3_ECC_DQ0	
DDR4_ECC_DQ0	--	DDR3_ECC_DQ1	
DDR4_ECC_DQ2	--	DDR3_ECC_DQ2	
DDR4_ECC_DQ1	--	DDR3_ECC_DQ3	
DDR4_ECC_DQ6	--	DDR3_ECC_DQ4	
DDR4_ECC_DQ4	--	DDR3_ECC_DQ5	
DDR4_ECC_DQ3	--	DDR3_ECC_DQ6	
DDR4_ECC_DQ5	--	DDR3_ECC_DQ7	
DDR4_ECC_DM	--	DDR3_ECC_DM	
DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P	
DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N	

NA

SCNN_FOXCONN_AS0A826

DDR4	LPDDR4	DDR3	LPDDR3
DDR4_A0	**LPDDR4_CLKP_B**	DDR3_A9	---
DDR4_A1	----	DDR3_A2	---
DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6
DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	---
DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3
DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2
DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1
DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	---
DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9
DDR4_A9	**LPDDR4_CLKN_B**	DDR3_A5	---
DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	---
DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8
DDR4_A12	LPDDR4_A3_A	DDR3_BA2	---
DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0
DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5
DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	---
DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7
DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	---
DDR4_BA0	LPDDR4_A2_B	DDR3_A1	---
DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4
DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	---
DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	---
DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE
DDR4_CLKP	**LPDDR4_CLKP_A**	**DDR3_CLKP**	**LPDDR3_CLKP**
DDR4_CLKN	**LPDDR4_CLKN_A**	**DDR3_CLKN**	**LPDDR3_CLKN**
DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0
DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1
DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n
DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n
DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	---

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences
can not be swap

GND31 235

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x =1.1V

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x **=0.6V**

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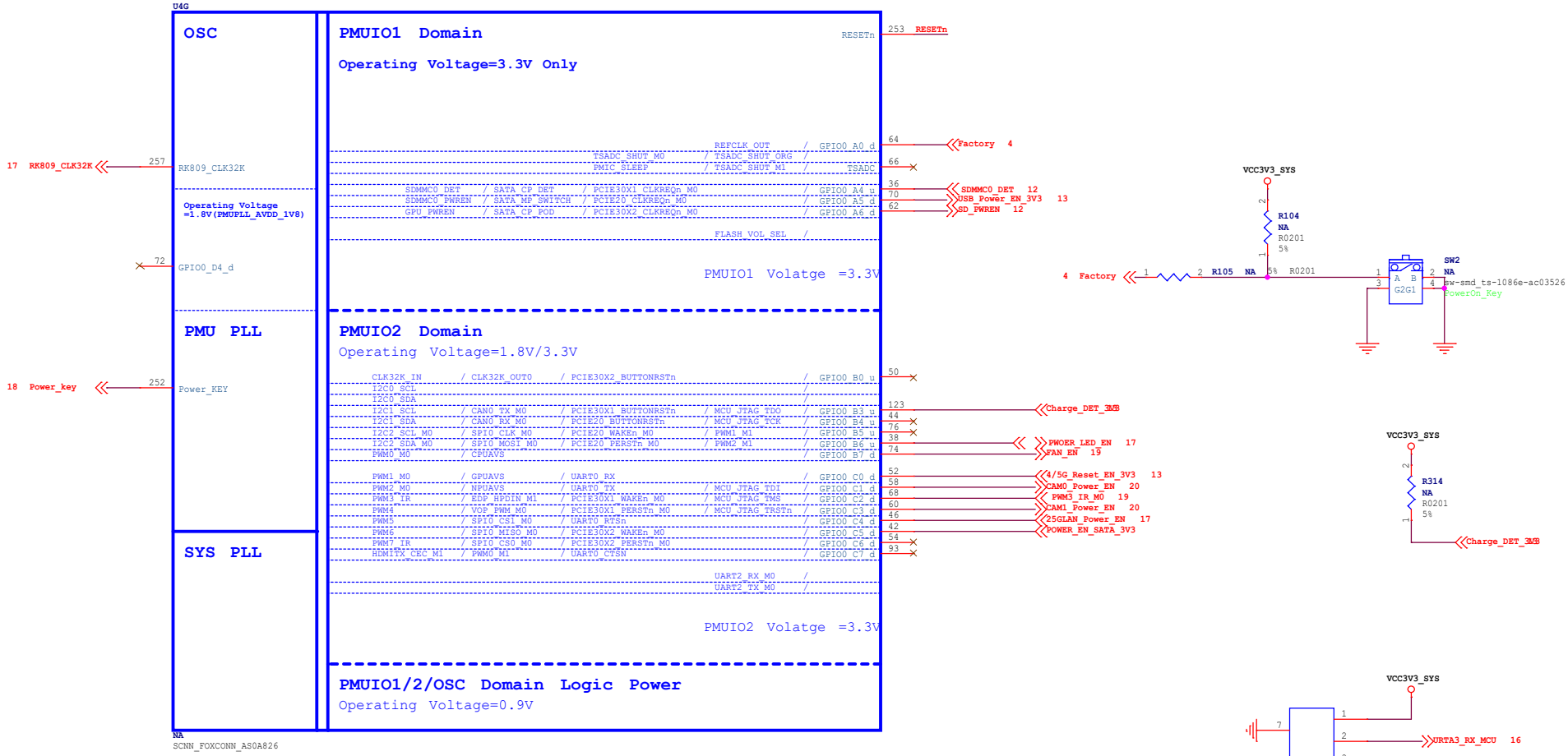
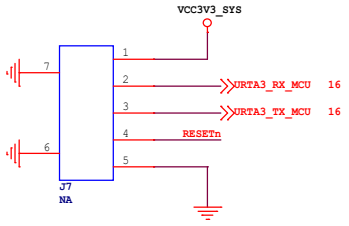
RK3568_G(OSC/PLL/PMUIO1/2)





Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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RK3568_I(VCCIO2 Domain)

U4I

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

EMMC_D0	/ FLASH_D0	/	
EMMC_D1	/ FLASH_D1	/	Update
EMMC_D2	/ FLASH_D2	/	
EMMC_D3	/ FLASH_D3	/	
EMMC_D4	/ FLASH_D4	/	
EMMC_D5	/ FLASH_D5	/	
EMMC_D6	/ FLASH_D6	/	
EMMC_D7	/ FLASH_D7	/	
EMMC_CMD	/ FLASH_WRn	/	
EMMC_CLKOUT	/ FLASH_DQS	/	
EMMC_DATA_STROBE	/ FSPI_CS1n / FLASH_CLE	/	
EMMC_RSTn	/ FSPI_D2 / FLASH_WPn	/	
	FSPI_CLK / FLASH_ALE	/	
	FSPI_D0 / FLASH_RDY	/	
	FSPI_D1 / FLASH_RDn	/	
	FSPI_CS0n / FLASH_CS0n	/	
	FSPI_D3 / FLASH_CS1n	/	

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

GND32

VCCIO2 Volatge =1.8V

NA

SCNN_FOXCONN_AS0A826

55 Update 5

5 Update 1 2 R102 NA 5% R0201 2 1 3

KEY2 NA TC-1321

RK3568_J(VCCIO3 Domain)

U4J

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

SDMMC0_D0	/ UART2_TX_M1 / UART6_TX_M1	/ PWM8_M1	/	GPIO1_D5_u
SDMMC0_D1	/ UART2_RX_M1 / UART6_RX_M1	/ PWM9_M1	/	GPIO1_D6_u
SDMMC0_D2	/ ARMJTAG_TCK / UART5_CTSn_M0		/	GPIO1_D7_u
SDMMC0_D3	/ ARMJTAG_TMS / UART5_RTSn_M0		/	GPIO2_A0_u
SDMMC0_CMD	/ PWM10_M1	/ UART5_RX_M0 / CAN0_TX_M1	/	GPIO2_A1_u
SDMMC0_CLK	/ TEST_CLKOUT / UART5_TX_M0	/ CAN0_RX_M1	/	GPIO2_A2_d

VCCIO3 Volatge =3.3V

NA

SCNN_FOXCONN_AS0A826

6 SDMMC0_D0 12
4 SDMMC0_D1 12
8 SDMMC0_D2 12
2 SDMMC0_D3 12
25 SDMMC0_CMD 12
27 SDMMC0_CLK 12

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

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RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)

U4U

USB3.0
OTG0_HS/FS/LS
(USB Download)

USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_VBUSDET
USB3_OTG0_ID

237 M237_USB3_OTG0_DP 13
239 M239_USB3_OTG0_DM 13
34 M034_USB3_OTG_VBUSDET 13
32

90 Ohm ± 10 %

USB3.0
HOST1_HS/FS/LS

USB3_HOST1_DP
USB3_HOST1_DM

238 M238_USB3_HOST1_DP 13
240 M240_USB3_HOST1_DM 13

90 Ohm ± 10 %

USB3.0
OTG0/HOST1_
HS/FS/LS
Power

USB3 AVDD 0V9
USB3 AVDD 1V8
USB3 AVDD 3V3

MULTI_PHY0/1/2

USB3.0 OTG0_SS
and SATA0 Mux

USB3_OTG0_SSTXP/SATA0_TXP
USB3_OTG0_SSTXN/SATA0_TXN
USB3_OTG0_SSRXP/SATA0_RXP
USB3_OTG0_SSRXN/SATA0_RXN

243 M243_USB3_OTG0_SSTXP
245 M245_USB3_OTG0_SSTXN
246 M246_USB3_OTG0_SSRXP
244 M244_USB3_OTG0_SSRXN

TO SATA

USB3.0 HOST1_SS and SATA1
and QSGMII_M0 Mux

USB3_HOST1_SSTXP/SATA1_TXP/QSGMII_TXP_M0
USB3_HOST1_SSTXN/SATA1_TXN/QSGMII_TXN_M0
USB3_HOST1_SSRXP/SATA1_RXP/QSGMII_RXP_M0
USB3_HOST1_SSRXN/SATA1_RXN/QSGMII_RXN_M0

250 M250_USB3_HOST1_SSTXP 13
248 M248_USB3_HOST1_SSTXN 13
249 M249_USB3_HOST1_SSRXP 13
251 M251_USB3_HOST1_SSRXN 13

TO USB3.0-A
5G LTE

PCIe2.0 and SATA2
and QSGMII_M1 Mux

PCIE20_TXP/SATA2_TXP/QSGMII_TXP_M1
PCIE20_TXN/SATA2_TXN/QSGMII_TXN_M1
PCIE20_RXP/SATA2_RXP/QSGMII_RXP_M1
PCIE20_RXN/SATA2_RXN/QSGMII_RXN_M1
PCIE20_REFCLKP
PCIE20_REFCLKN

232 PCIE20_SATA2_TXP 17
234 PCIE20_SATA2_TXN 17
233 PCIE20_SATA2_RXP 17
231 PCIE20_SATA2_RXN 17
208 PCIE20_REFCLKP 17
210 PCIE20_REFCLKN 17

TO M2 WIFI

MULTI_PHY
REFCLK

MULTI PHY AVDD 0V9
MULTI PHY AVDD 1V8

NA
SCNN_FOXCONN_AS0A826

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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RK3568_V(USB2.0 HOST)

U4V

USB2.0 HOST

USB2_HOST2_DP
USB2_HOST2_DM

53 M053_USB2_HOST2_DP 17
51 M051_USB2_HOST2_DM 17

90 Ohm ± 10 %

TO USB A

USB2_HOST3_DP
USB2_HOST3_DM

59 M059_USB2_HOST3_DP 13
57 M057_USB2_HOST3_DM 13

90 Ohm ± 10 %

TO USB A

USB2 AVDD 0V9
USB2 AVDD 1V8
USB2 AVDD 3V3

NA
SCNN_FOXCONN_AS0A826

RK3568_W(PCIe3.0 x2)

U4W

PCIe3.0 x 2

PCIE30_TX0P
PCIE30_TX0N
PCIE30_TX1P
PCIE30_TX1N
PCIE30_RX0P
PCIE30_RX0N
PCIE30_RX1P
PCIE30_RX1N
PCIE30_REFCLKP_IN
PCIE30_REFCLKN_IN

225 PCIE30_TX0P 17
227 PCIE30_TX0N 17
219 PCIE30_TX1P 17
221 PCIE30_TX1N 17
222 PCIE30_RX0P 17
220 PCIE30_RX0N 17
216 PCIE30_RX1P 17
214 PCIE30_RX1N 17
228 PCIE30_REFCLKP_IN 17
226 PCIE30_REFCLKN_IN 17

TO 2.5G ETH

TO 2.5G ETH

PCIE3.0 AVDD 0V9
PCIE3.0 AVDD 1V8

NA
SCNN_FOXCONN_AS0A826

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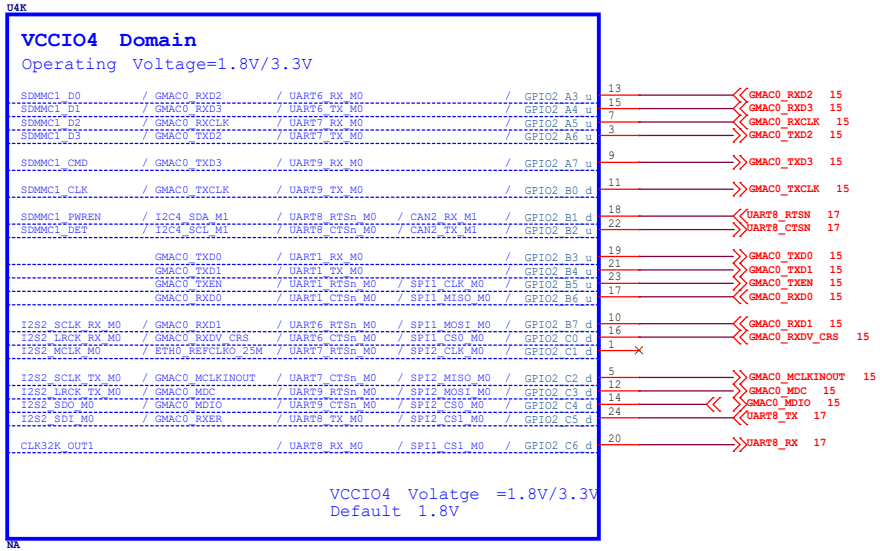
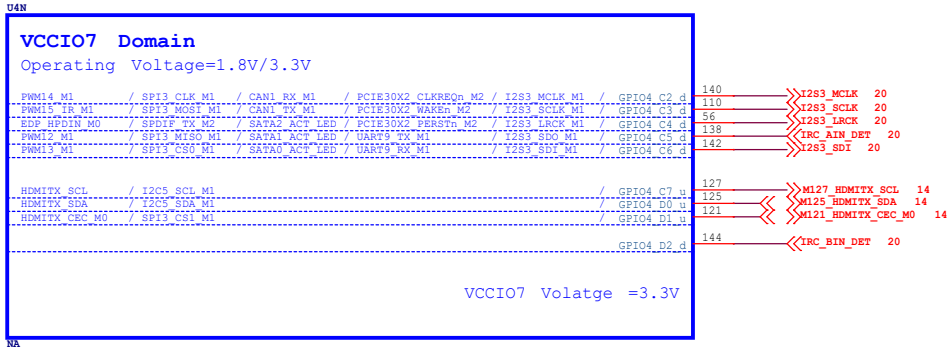
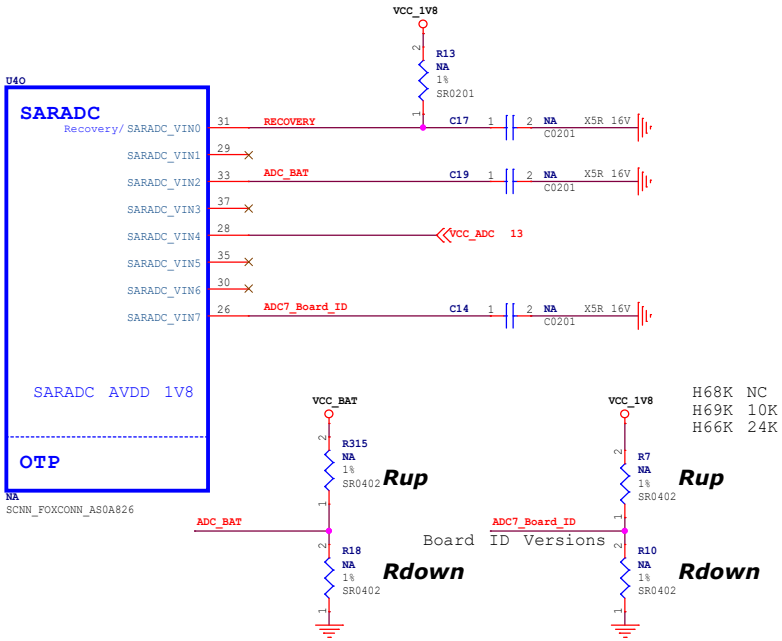
RK3568_K(VCCIO4 Domain)



RK3568_N(VCCIO7 Domain)



RK3568_O(SARADC/OTP)



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RK3568_P(MIPI_CSI_RX)

U4P

MIPI CSI RX

MIPI_CSI_RX_D0P	147	MIPI_CSI_RX0_D0P 20
MIPI_CSI_RX_D0N	149	MIPI_CSI_RX0_D0N 20
MIPI_CSI_RX_D1P	141	MIPI_CSI_RX0_D1P 20
MIPI_CSI_RX_D1N	143	MIPI_CSI_RX0_D1N 20
MIPI_CSI_RX_D2P	154	MIPI_CSI_RX0_D2P 20
MIPI_CSI_RX_D2N	156	MIPI_CSI_RX0_D2N 20
MIPI_CSI_RX_D3P	150	MIPI_CSI_RX0_D3P 20
MIPI_CSI_RX_D3N	148	MIPI_CSI_RX0_D3N 20
MIPI_CSI_RX_CLK0P	135	MIPI_CSI_RX0_CLKP 20
MIPI_CSI_RX_CLK0N	137	MIPI_CSI_RX0_CLKN 20
MIPI_CSI_RX_CLK1P	129	MIPI_CSI_RX1_CLKP 20
MIPI_CSI_RX_CLK1N	131	MIPI_CSI_RX1_CLKN 20

MIPI CSI RX AVDD 0V9

MIPI CSI RX AVDD 1V8

MIPI CSI

NA
SCNN_FOXCONN_AS0A826

RK3568_M(VCCIO6 Domain)

U4M

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

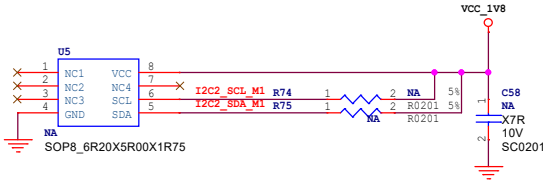
CIF_D0	EBC_SDDO0	SDMMC2_D0_M0	I2S1_MCLK_M1	VOP_BT656_D0_M1	GPIO3_C6_d
CIF_D1	EBC_SDDO1	SDMMC2_D1_M0	I2S1_SCLK_TX_M1	VOP_BT656_D1_M1	GPIO3_C7_d
CIF_D2	EBC_SDDO2	SDMMC2_D2_M0	I2S1_LRCK_TX_M1	VOP_BT656_D2_M1	GPIO3_D0_d
CIF_D3	EBC_SDDO3	SDMMC2_D3_M0	I2S1_SDO0_M1	VOP_BT656_D3_M1	GPIO3_D1_d
CIF_D4	EBC_SDDO4	SDMMC2_CMD_M0	I2S1_SDI0_M1	VOP_BT656_D4_M1	GPIO3_D2_d
CIF_D5	EBC_SDDO5	SDMMC2_CLK_M0	I2S1_SDI1_M1	VOP_BT656_D5_M1	GPIO3_D3_d
CIF_D6	EBC_SDDO6	SDMMC2_DET_M0	I2S1_SDI2_M1	VOP_BT656_D6_M1	GPIO3_D4_d
CIF_D7	EBC_SDDO7	SDMMC2_PWREN_M0	I2S1_SDI3_M1	VOP_BT656_D7_M1	GPIO3_D5_d
CIF_D8	EBC_SDDO8	GMAC1_TXD2_M1	UART1_TX_M1	PDM_CLK0_M1	GPIO3_D6_d
CIF_D9	EBC_SDDO9	GMAC1_TXD3_M1	UART1_RX_M1	PDM_SDI0_M1	GPIO3_D7_d
CIF_D10	EBC_SDDO10	GMAC1_TXCLK_M1		PDM_CLK1_M1	GPIO4_A0_d
CIF_D11	EBC_SDDO11	GMAC1_RXD2_M1		PDM_SDI1_M1	GPIO4_A1_d
CIF_D12	EBC_SDDO12	GMAC1_RXD3_M1	UART7_TX_M2	PDM_SDI2_M1	GPIO4_A2_d
CIF_D13	EBC_SDDO13	GMAC1_RXCLK_M1	UART7_RX_M2	PDM_SDI3_M1	GPIO4_A3_d
CIF_D14	EBC_SDDO14	GMAC1_TXD0_M1	UART9_TX_M2	I2S2_LRCK_TX_M1	GPIO4_A4_d
CIF_D15	EBC_SDDO15	GMAC1_TXD1_M1	UART9_RX_M2	I2S2_LRCK_RX_M1	GPIO4_A5_d
ISP_FLASHTRIGOUT	EBC_SDCE0	GMAC1_TXEN_M1	SPI3_CS0_M0	I2S1_SCLK_RX_M1	GPIO4_A6_d
CAM_CLKOUT0	EBC_SDCE1	GMAC1_RXD0_M1	SPI3_CS1_M0	I2S1_LRCK_RX_M1	GPIO4_A7_d
CAM_CLKOUT1	EBC_SDCE2	GMAC1_RXD1_M1	SPI3_MISO_M0	I2S1_SDO1_M1	GPIO4_B0_d
ISP_PRELIGHT_TRIG	EBC_SDCE3	GMAC1_RXDV_CRS_M1		I2S1_SDO2_M1	GPIO4_B1_d
I2C4_SDA_M0	EBC_VCOM	GMAC1_RXER_M1	SPI3_MOSI_M0	I2S2_SDI_M1	GPIO4_B2_d
I2C4_SCL_M0	EBC_GDOE	ETH1_REFCLKO_25M_M1	SPI3_CLK_M0	I2S2_SDO_M1	GPIO4_B3_d
I2C2_SDA_M1	EBC_GDSP	CAN2_RX_M0	ISP_FLASH_TRIGIN	VOP_BT656_CLK_M1	GPIO4_B4_d
I2C2_SCL_M1	EBC_SDSHR	CAN2_TX_M0		I2S1_SDO3_M1	GPIO4_B5_d
CIF_HREF	EBC_SDLE	GMAC1_MDC_M1	UART1_RTSn_M1	I2S2_MCLK_M1	GPIO4_B6_d
CIF_VSYNC	EBC_SDOE	GMAC1_MDIO_M1		I2S2_SCLK_TX_M1	GPIO4_B7_d
CIF_CLKOUT	EBC_GDCLK		PWM11_IR_M1		GPIO4_C0_d
CIF_CLKIN	EBC_SDCLK	GMAC1_MCLKINOUT_M1	UART1_CTSn_M1	I2S2_SCLK_RX_M1	GPIO4_C1_d

VCCIO6 Volatge =1.8V/3.3V
Default 1.8V

118	SDIO_D0	17
106	SDIO_D1	17
83	SDIO_D2	17
81	SDIO_D3	17
92	SDIO_CMD	17
85	SDIO_CLK	17
77	WIFI_WAKE_HOST	17
104	HOST_WAKE_WIFI	17
94	GMAC1_TXD2	16
100	GMAC1_TXD3	16
102	GMAC1_TXCLK	16
79	GMAC1_RXD2	16
96	GMAC1_RXD3	16
98	GMAC1_RXCLK	16
75	GMAC1_TXD0	16
73	GMAC1_TXD1	16
71	GMAC1_TXEN	16
69	GMAC1_RXD0	16
78	GMAC1_RXD1	16
67	GMAC1_RXDV_CRS	16
90	MIPICAM0_RST_L	20
65	MIPICAM1_RST_L	20
86	I2C2_SDA_M1	20
88	I2C2_SCL_M1	20
80	GMAC1_MDC	16
82	GMAC1_MDIO	16
84		
63	GMAC1_MCLKINOUT	16

MIPI CSI

NA
SCNN_FOXCONN_AS0A826



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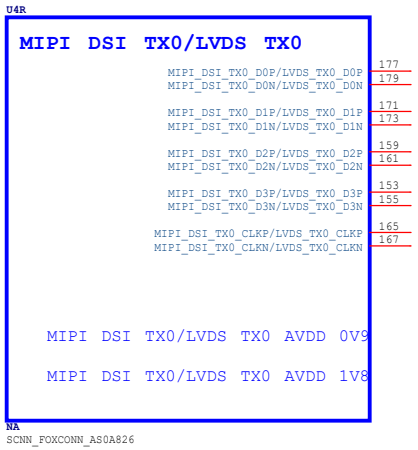
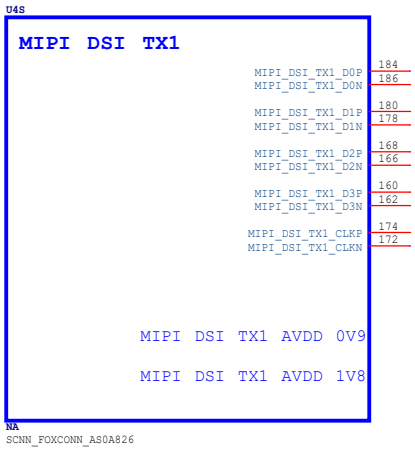
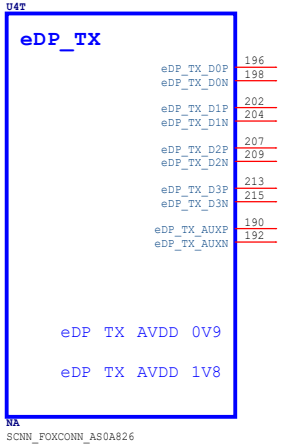
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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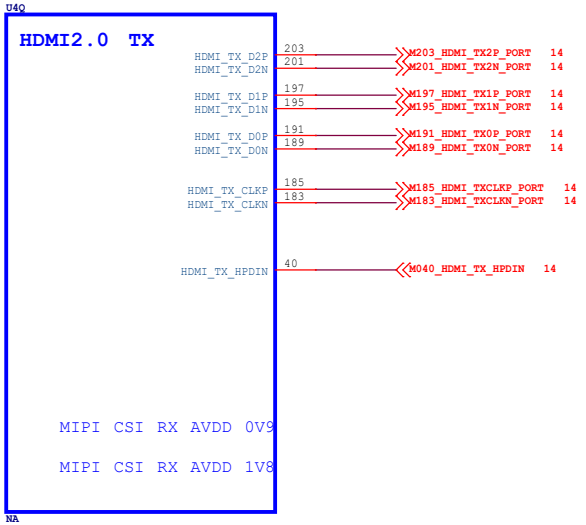
RK3568_Q(HDMI2.0 TX)

HDMI TMDS trace
100 Ohm ± 10 %



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RK3568_H(VCCIO1 Domain)

U4H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u	43
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u	47
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/	
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/	
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d	39
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/	
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/	
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/	
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d	41
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d	45
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d	255
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/	

VCCIO1 Volatge =1.8V/3.3V
Default 3.3V

URTA3_RX_MCU 16
URTA3_TX_MCU 16
GMAC1_RSTn 16

NA

SCNN_FOXCONN_AS0A826

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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RK3568_L(VCCIO5 Domain)

U4L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

VCCIO5 Volatge =1.8V/3.3V
Default 1.8V

金手指要 改为 3V 3

NA
SCNN_FOXCONN_AS0A826

119 25GLAN_ResetB 17
134 I2S1_SCLK_TX 20
136 I2S1_LRCK_TX 20
120 GMAC_RSTn 11
126 I2S1_SDI1 11
130 PCIE30X2_WAKEn_M1 17
128 PCIE30X2_PERSTn_M1 17
117 PCIE30X2_CLKREQn_M1 17
115 BT_RST 17
132 BT_WAKE_HOST 17
124 HOST_WAKE_BT 17
113
122 25GLAN_ResetB 17
111 Green_LED
109
107 RED_LED
105 WORK_LED
101
103
97 I2C5_SCL_3V3
95 I2C5_SDA_3V3
48 25GLAN_Power_EN_NEW 19
99
116
91
89
108
114
112
87

OLD=GPIO2_D3

OLD=GPIO2_D4

11 GMAC_RSTn — R300 NA / R301 NA (R0201 5%) → GMAC0_RSTn 11,15 / I2S1_SDI 11,20

11 I2S1_SDI1 — R302 NA / R303 NA (R0201 5%) → I2S1_SDI 11,20 / GMAC0_RSTn 11,15

VCC3V3_SYS
R97 NA SR0201
D16 NA LED0603W
HDD
Green_LED — R91 NA 5% R0201 — Q11 NA SOT_323
R90 NA R0201 5%

VCC3V3_SYS
R85 NA SR0201
D15 NA LED0603W
RED_LED — R83 NA 5% R0201 — Q8 NA SOT_323
R81 NA R0201 5%

VCC3V3_SYS
R66 NA SR0201
D12 NA LED0603W
WORK
WORK_LED — R51 NA 5% R0201 — Q5 NA SOT_323
R52 NA R0201 5%

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

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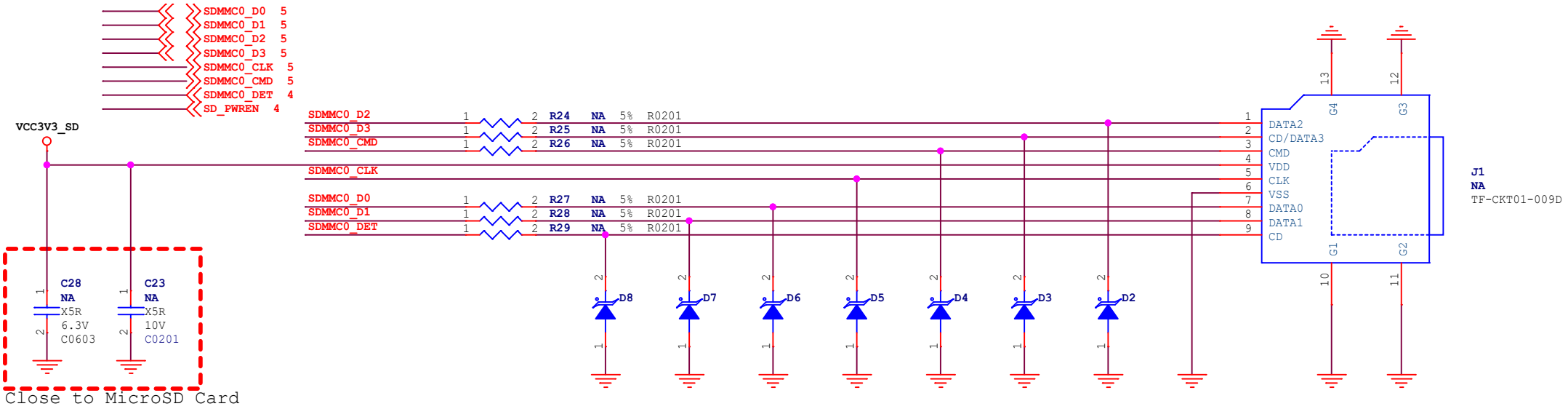
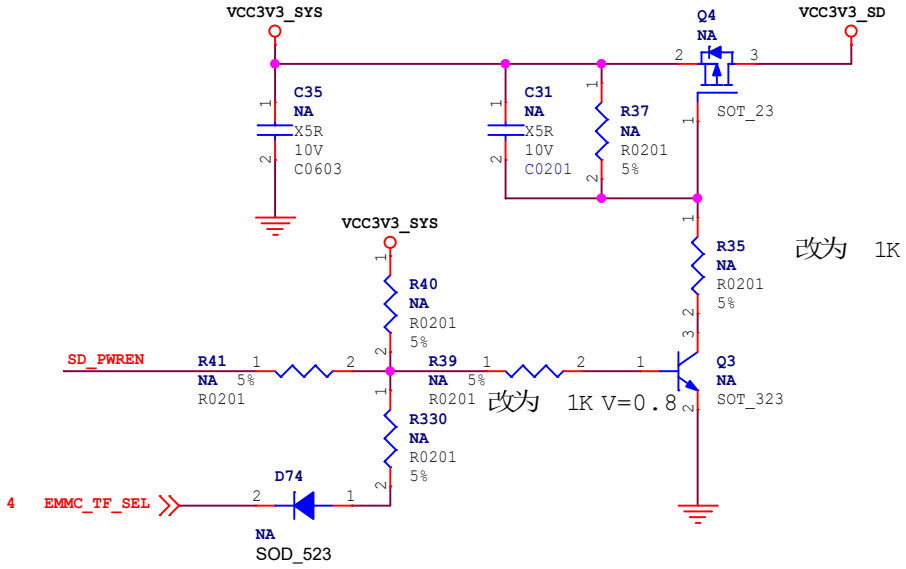


MicroSD Card



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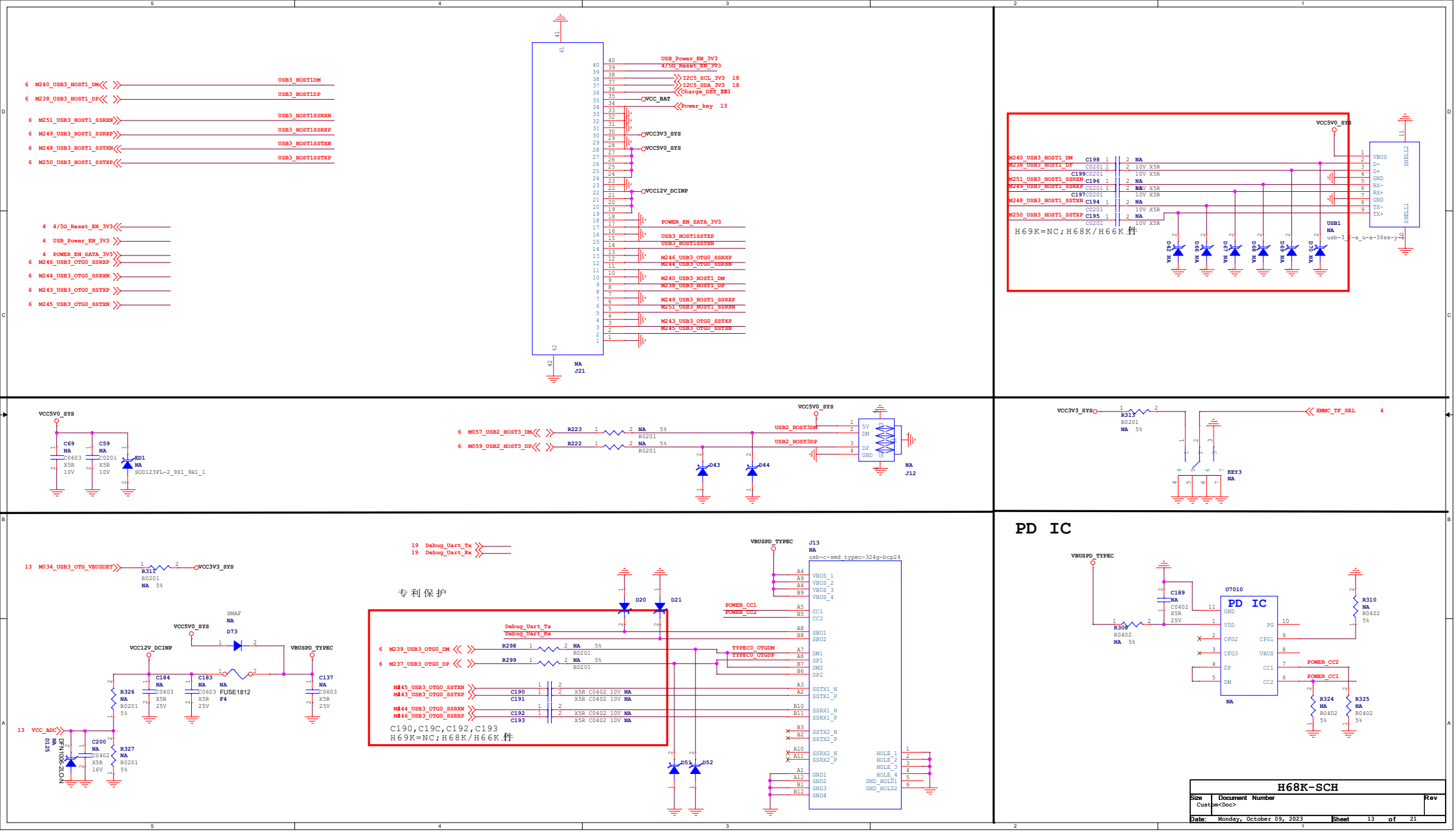
6 M240_USB3_HOST1_DM
6 M238_USB3_HOST1_DP
6 M251_USB3_HOST1_SSRXN
6 M249_USB3_HOST1_SSRXP
6 M248_USB3_HOST1_SSTXN
6 M250_USB3_HOST1_SSTXP
USB3_HOST1DM
USB3_HOST1DP
USB3_HOST1SSRXN
USB3_HOST1SSRXP
USB3_HOST1SSTXN
USB3_HOST1SSTXP
4 4/5G_Reset_EN_3V3
4 USB_Power_EN_3V3
4 POWER_EN_SATA_3V3
6 M246_USB3_OTG0_SSRXP
6 M244_USB3_OTG0_SSRXN
6 M243_USB3_OTG0_SSTXP
6 M245_USB3_OTG0_SSTXN
USB_Power_EN_3V3
4/5G_Reset_EN_3V3
I2C5_SCL_3V3 18
I2C5_SDA_3V3 18
Charge_DET_3V3
VCC_BAT
Power_key 13
VCC3V3_SYS
VCC5V0_SYS
VCC12V_DCINP
POWER_EN_SATA_3V3
USB3_HOST1SSTXP
USB3_HOST1SSTXN
M246_USB3_OTG0_SSRXP
M244_USB3_OTG0_SSRXN
M240_USB3_HOST1_DM
M238_USB3_HOST1_DP
M249_USB3_HOST1_SSRXP
M251_USB3_HOST1_SSRXN
M243_USB3_OTG0_SSTXP
M245_USB3_OTG0_SSTXN
NA
J21
VCC5V0_SYS
M240_USB3_HOST1_DM
M238_USB3_HOST1_DP
M251_USB3_HOST1_SSRXN
M249_USB3_HOST1_SSRXP
M248_USB3_HOST1_SSTXN
M250_USB3_HOST1_SSTXP
C198 C0201 NA 10V X5R
C199 C0201 NA 10V X5R
C196 C0201 NA 10V X5R
C197 C0201 NA 10V X5R
C194 C0201 NA 10V X5R
C195 C0201 NA 10V X5R
D42 NA
D69 NA
D67 NA
D68 NA
D66 NA
D70 NA
USB1
NA
usb-3.0-a_u-a-39ss-y-1
VBUS
D-
D+
GND
RX-
RX+
GND
TX-
TX+
SHELL2
SHELL1
H69K=NC;H68K/H66K 件
VCC5V0_SYS
C69 NA C0603 X5R 10V
C59 NA C0201 X5R 10V
ED1 NA SOD123FL-2_9X1_9H1_1
6 M057_USB2_HOST3_DM
6 M059_USB2_HOST3_DP
R223 R0201 NA 5%
R222 R0201 NA 5%
D43
D44
USB2_HOST3DM
USB2_HOST3DP
5V
DM
DP
GND
NA
J12
VCC3V3_SYS
R313 R0201 NA 5%
EMMC_TF_SEL 4
KEY3
NA
13 M034_USB3_OTG_VBUSDET
R311 R0201 NA 5%
VCC3V3_SYS
VCC5V0_SYS
SMAF
NA
D73
VCC12V_DCINP
VBUSPD_TYPEC
C184 NA C0603 X5R 25V
C183 NA C0603 X5R 25V
FUSE1812
F4
R326 NA R0201 5%
C137 NA C0603 X5R 25V
13 VCC_ADC
DFN1006-2L-ON
D125
C200 NA C0402 X5R 16V
R327 NA R0201 5%
19 Debug_Uart_Tx
19 Debug_Uart_Rx
专利保护
D20
D21
Debug_Uart_Tx
Debug_Uart_Rx
6 M239_USB3_OTG0_DM
6 M237_USB3_OTG0_DP
R298 R0201 NA 5%
R299 R0201 NA 5%
M245_USB3_OTG0_SSTXN
M243_USB3_OTG0_SSTXP
M244_USB3_OTG0_SSRXN
M246_USB3_OTG0_SSRXP
C190 C191 C192 C193
X5R C0402 10V NA
C190,C19C,C192,C193
H69K=NC;H68K/H66K 件
D51
D52
VBUSPD_TYPEC
J13
NA
usb-c-smd typec-324g-bcp24
POWER_CC1
POWER_CC2
TYPEC0_OTGDM
TYPEC0_OTGDP
VBUS_1
VBUS_2
VBUS_3
VBUS_4
CC1
CC2
SBU1
SBU2
DM1
DP1
DM2
DP2
SSTX1_N
SSTX1_P
SSRX1_N
SSRX1_P
SSTX2_N
SSTX2_P
SSRX2_N
SSRX2_P
GND1
GND2
GND3
GND4
HOLE_1
HOLE_2
HOLE_3
HOLE_4
GND_HOLD1
GND_HOLD2
PD IC
VBUSPD_TYPEC
C189 NA C0402 X5R 25V
R308 R0402 NA 5%
U7010
PD IC
GND
VDD
CFG2
CFG3
DP
DM
PG
CFG1
VBUS
CC1
CC2
POWER_CC2
POWER_CC1
NA
R310 NA R0402 5%
R324 NA R0402 5%
R325 NA R0402 5%
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HDMI_TX2P_PORT
HDMI_TX2N_PORT
M203_HDMI_TX2P_PORT 9
M201_HDMI_TX2N_PORT 9

HDMI_TX1P_PORT
HDMI_TX1N_PORT
M197_HDMI_TX1P_PORT 9
M195_HDMI_TX1N_PORT 9

HDMI_TX0P_PORT
HDMI_TX0N_PORT
M191_HDMI_TX0P_PORT 9
M189_HDMI_TX0N_PORT 9

HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
M185_HDMI_TXCLKP_PORT 9
M183_HDMI_TXCLKN_PORT 9

HDMITX_SCL
HDMITX_SDA
HDMITX_CEC_M0
HDMI_TX_HPDIN
M127_HDMITX_SCL 7
M125_HDMITX_SDA 7
M121_HDMITX_CEC_M0 7
M040_HDMI_TX_HPDIN 9

VCC5V0_SYS
D22 NA SOD_123
VCC5V_HDMI_TX
C74 NA SC0402 X5R 10V

U16 NA ESD2510H0_75
U15 NA ESD2510H0_75
Cj<=0.4pF

HDMI_TX2P_PORT
HDMI_TX2N_PORT
HDMI_TX1P_PORT
HDMI_TX1N_PORT
HDMI_TX0P_PORT
HDMI_TX0N_PORT
HDMI_TXCLKP_PORT
HDMI_TXCLKN_PORT
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT
VCC5V_HDMI_TX

ED6 NA ESD0402
ED5 NA ESD0402
ED4 NA ESD0402
ED3 NA ESD0402

D2P D2_G D2N D1P D1_G D1N D0P D0_G D0N CLKP CLK_G CLKN CEC Utility SCL SDA GND +5V HPD
Type A
J20 NA HDMIA19_HDMI_01A

HDMI TX DDC

VCC5V0_SYS
D23 NA SOD_323
VCC3V3_SYS
R122 NA 5% R0201
Q16 NA SOT_323
R117 NA 5% R0201
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC3V3_SYS
R123 NA 5% R0201
Q17 NA SOT_323
R118 NA 5% R0201
HDMITX_SDA
HDMI_TXDDC_SDA_PORT

HDMI TX CEC

VCC3V3_SYS VCC5V0_SYS
R121 NA 5% R0201
Q15 NA SOT_323
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

HDMI TX HPD

HDMI_TX_HPDIN R119 NA 5% R0201 HDMI_TX_HPD_PORT
R120 NA 5% R0201

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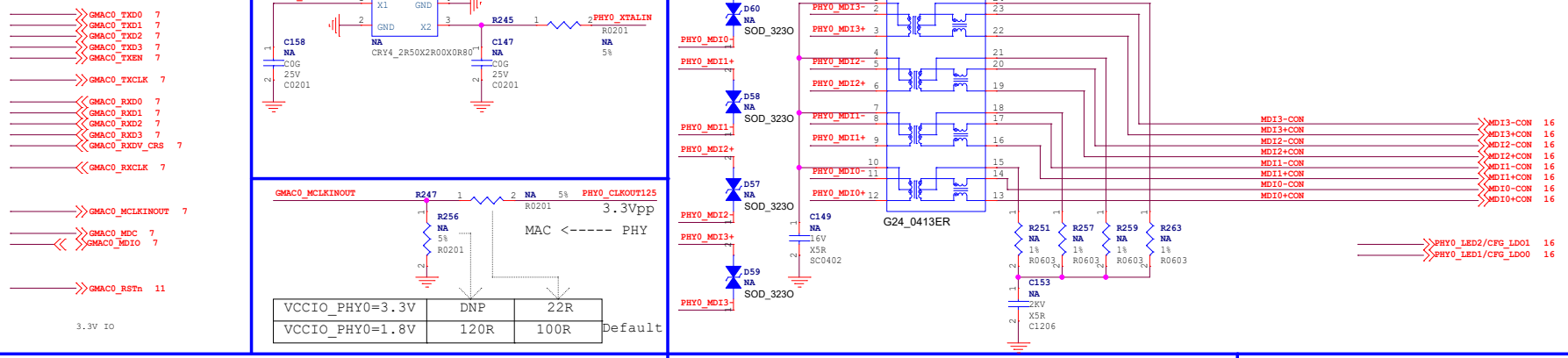
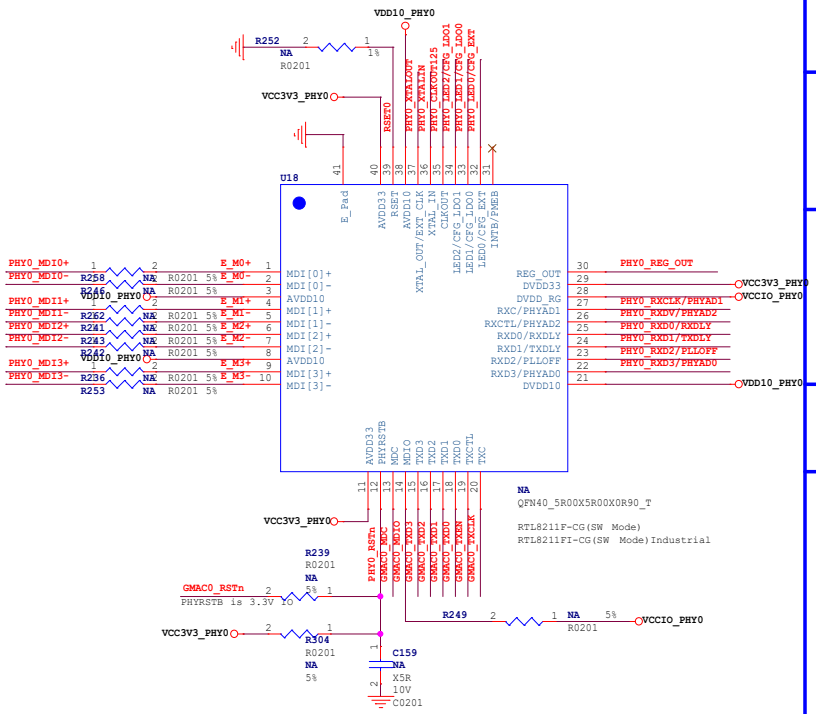
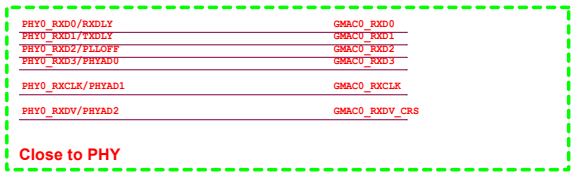
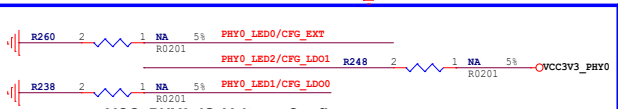
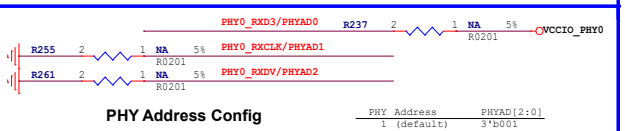


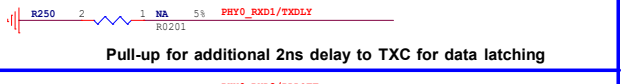


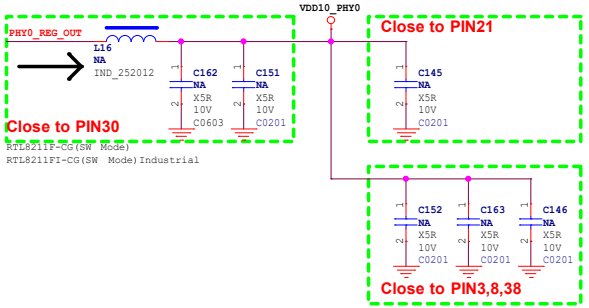


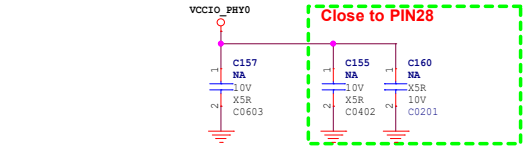


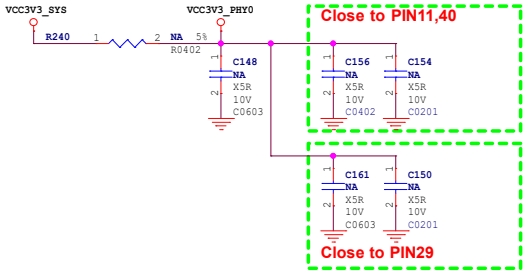
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V (default)	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	











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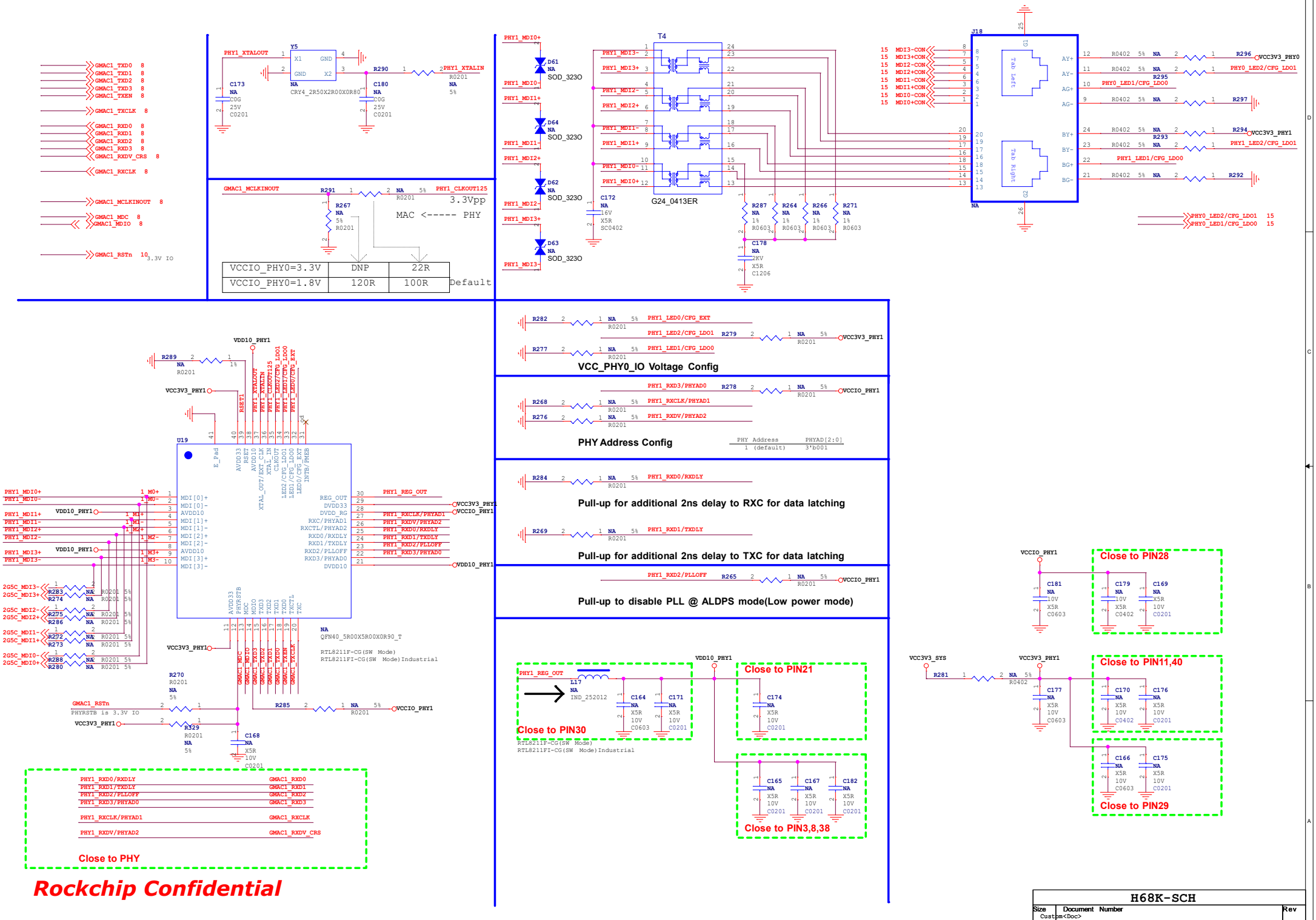
GMAC1_TXD0 8
GMAC1_TXD1 8
GMAC1_TXD2 8
GMAC1_TXD3 8
GMAC1_TXEN 8
GMAC1_TXCLK 8
GMAC1_RXD0 8
GMAC1_RXD1 8
GMAC1_RXD2 8
GMAC1_RXD3 8
GMAC1_RXDV_CRS 8
GMAC1_RXCLK 8
GMAC1_MCLKINOUT 8
GMAC1_MDC 8
GMAC1_MDIO 8
GMAC1_RSTn 10
3.3V IO
PHY1_XTALOUT
Y5
X1 GND
GND X2
CRY4_2R50X2R00X0R80
C173 NA 20G 25V C0201
C180 NA 20G 25V C0201
R290 NA R0201 5%
PHY1_XTALIN
GMAC1_MCLKINOUT
R291 NA 5% R0201
PHY1_CLKOUT125
R267 NA 5% R0201
3.3Vpp
MAC <----- PHY
VCCIO_PHY0=3.3V DNP 22R
VCCIO_PHY0=1.8V 120R 100R Default
PHY1_MDI0+
PHY1_MDI0-
PHY1_MDI1+
PHY1_MDI1-
PHY1_MDI2+
PHY1_MDI2-
PHY1_MDI3+
PHY1_MDI3-
D61 NA SOD_323O
D64 NA SOD_323O
D62 NA SOD_323O
D63 NA SOD_323O
T4
G24_0413ER
C172 NA 16V X5R SC0402
C178 NA 2KV X5R C1206
R287 NA 1% R0603
R264 NA 1% R0603
R266 NA 1% R0603
R271 NA 1% R0603
J18
MDI3-CON
MDI3+CON
MDI2-CON
MDI2+CON
MDI1-CON
MDI1+CON
MDI0-CON
MDI0+CON
Tab Left
Tab Right
AY+ AY- AG+ AG- BY+ BY- BG+ BG-
R0402 5% NA
R296 VCC3V3_PHY0
R295
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
R297
R294 VCC3V3_PHY1
R293
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
R292
VDD10_PHY1
R289 NA R0201
VCC3V3_PHY1
RSET1
PHY1_XTALOUT
PHY1_XTALIN
PHY1_CLKOUT125
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
PHY1_LED0/CFG_EXT
U19
E_Pad
AVDD33 RSET AVDD10 XTAL_OUT XTAL_IN CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PWEB
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-
REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY1_REG_OUT
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
PHY1_RXD0/RXDLY
PHY1_RXD1/TXDLY
PHY1_RXD2/PLLOFF
PHY1_RXD3/PHYAD0
VCC3V3_PHY1
VCCIO_PHY1
VDD10_PHY1
AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
GMAC1_MDC GMAC1_MDIO GMAC1_TXD3 GMAC1_TXD2 GMAC1_TXD1 GMAC1_TXD0 GMAC1_TXEN GMAC1_TXCLK
NA QFN40_5R00X5R00X0R90_T
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
R270 R0201 NA 5%
GMAC1_RSTn
PHYRSTB is 3.3V IO
R285 NA R0201 VCCIO_PHY1
R329 R0201 NA 5%
C168 NA X5R 10V C0201
2G5C_MDI3-
2G5C_MDI3+
2G5C_MDI2-
2G5C_MDI2+
2G5C_MDI1-
2G5C_MDI1+
2G5C_MDI0-
2G5C_MDI0+
R283 R274 R275 R286 R272 R273 R288 R280
NA R0201 5%
PHY1_RXD0/RXDLY GMAC1_RXD0
PHY1_RXD1/TXDLY GMAC1_RXD1
PHY1_RXD2/PLLOFF GMAC1_RXD2
PHY1_RXD3/PHYAD0 GMAC1_RXD3
PHY1_RXCLK/PHYAD1 GMAC1_RXCLK
PHY1_RXDV/PHYAD2 GMAC1_RXDV_CRS
Close to PHY
R282 R277 NA R0201
PHY1_LED0/CFG_EXT
PHY1_LED2/CFG_LDO1
PHY1_LED1/CFG_LDO0
R279 VCC3V3_PHY1
VCC_PHY0_IO Voltage Config
R268 R276 NA R0201
PHY1_RXD3/PHYAD0
PHY1_RXCLK/PHYAD1
PHY1_RXDV/PHYAD2
R278 VCCIO_PHY1
PHY Address Config
PHY Address PHYAD[2:0]
1 (default) 3'b001
R284 NA R0201 PHY1_RXD0/RXDLY
Pull-up for additional 2ns delay to RXC for data latching
R269 NA R0201 PHY1_RXD1/TXDLY
Pull-up for additional 2ns delay to TXC for data latching
PHY1_RXD2/PLLOFF
R265 NA R0201 VCCIO_PHY1
Pull-up to disable PLL @ ALDPS mode(Low power mode)
PHY1_REG_OUT
L17 NA IND_252012
C164 NA X5R 10V C0603
C171 NA X5R 10V C0201
Close to PIN30
Close to PIN21
C174 NA X5R 10V C0201
C165 NA X5R 10V C0201
C167 NA X5R 10V C0201
C182 NA X5R 10V C0201
Close to PIN3,8,38
VCCIO_PHY1
C181 NA 10V X5R C0603
C179 NA 10V X5R C0402
C169 NA X5R 10V C0201
Close to PIN28
VCC3V3_SYS
R281 NA R0402
C177 NA X5R 10V C0603
C170 NA X5R 10V C0402
C176 NA X5R 10V C0201
Close to PIN11,40
C166 NA X5R 10V C0603
C175 NA X5R 10V C0201
Close to PIN29
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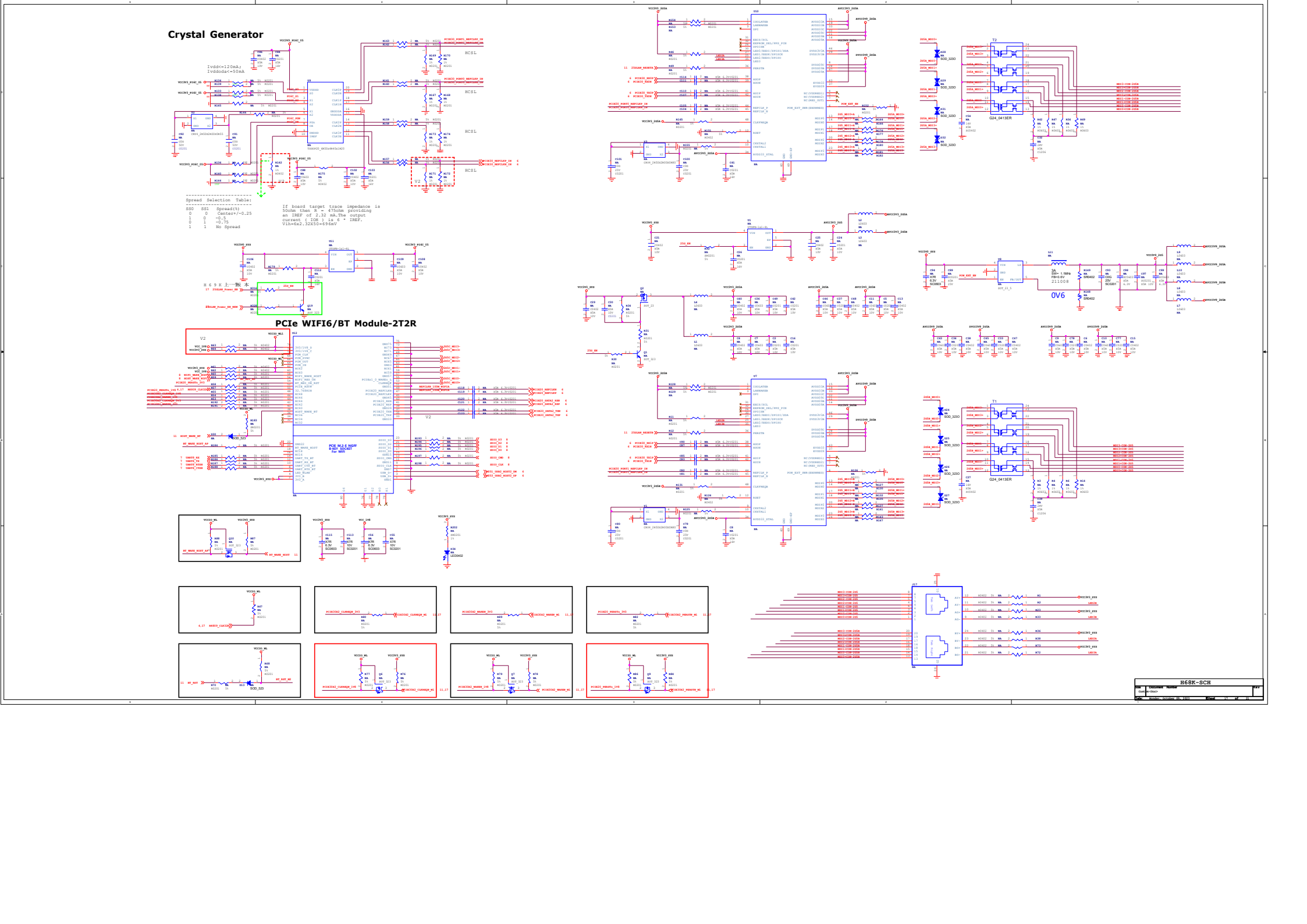
Crystal Generator
PCIe WIFI6/BT Module-2T2R
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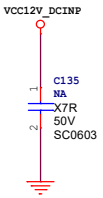
12-24V/1A DCIN



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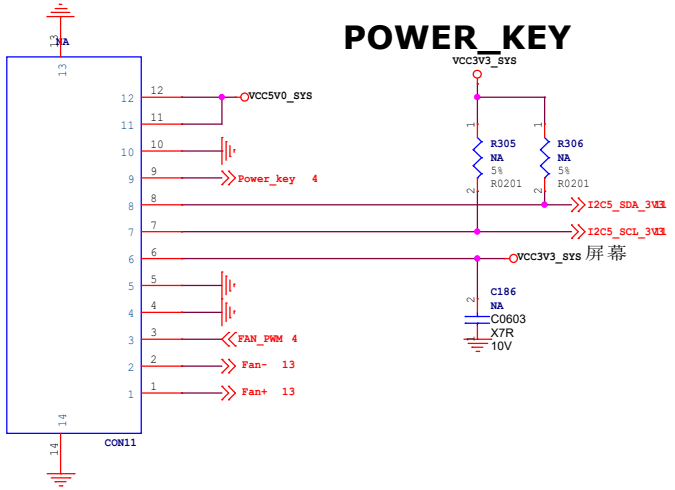
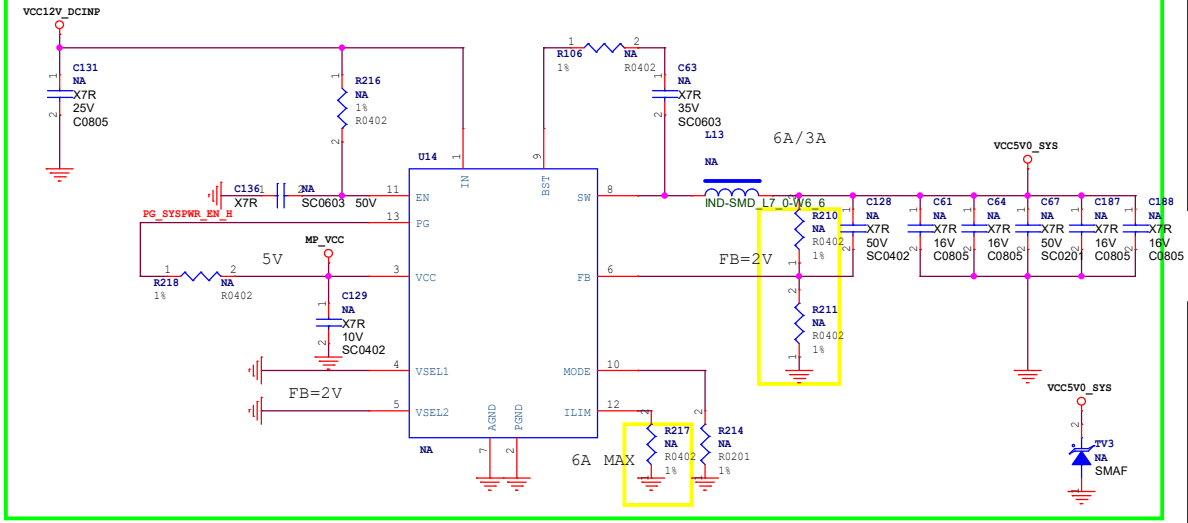
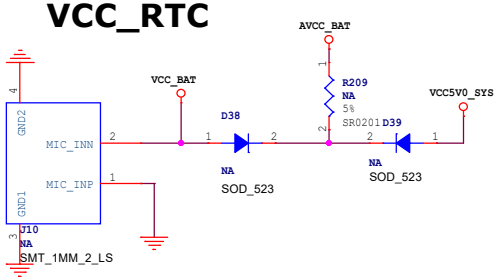


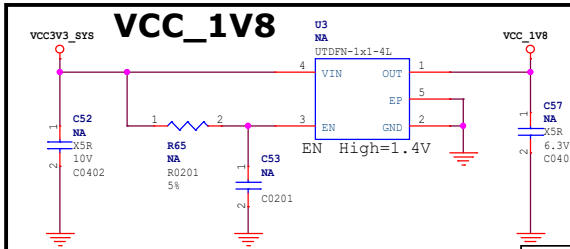
VCC5V0_SYS

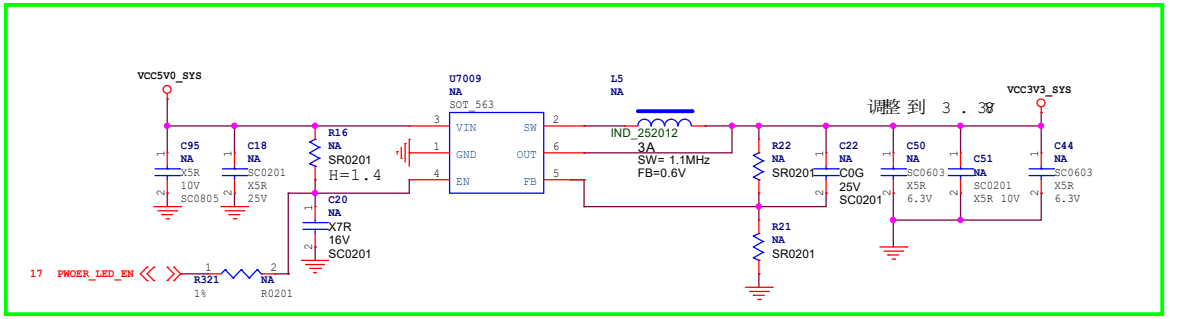


VCC_RTC



VCC_1V8





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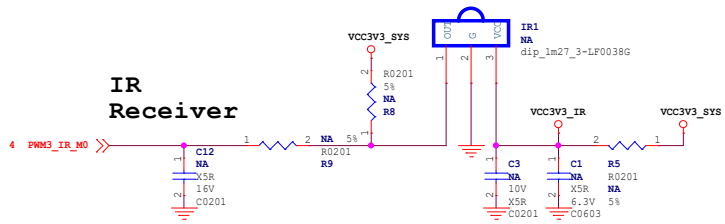

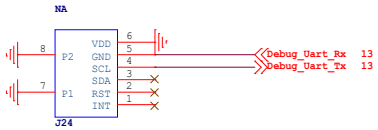

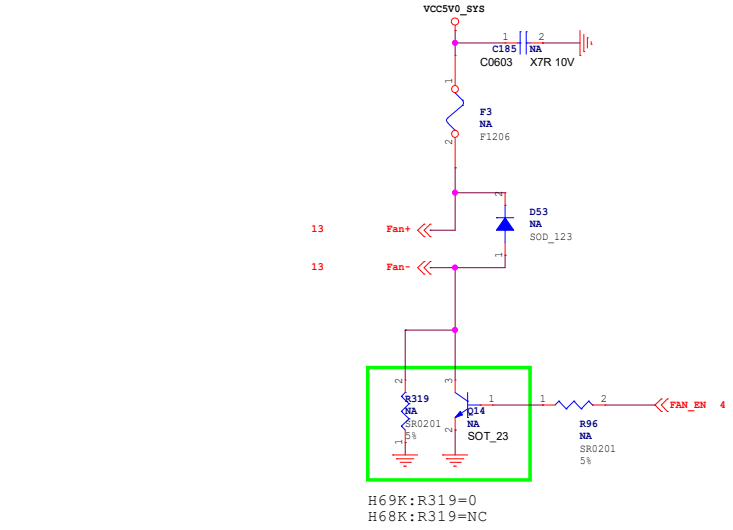

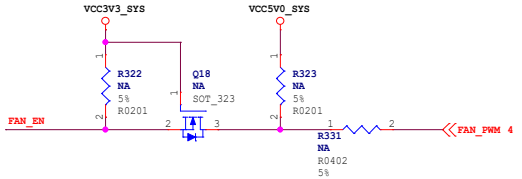

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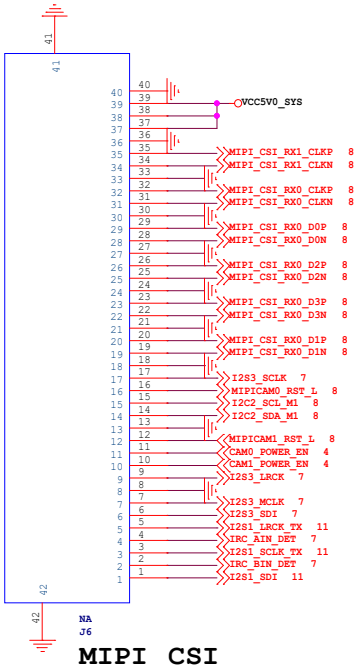

MIPI CSI

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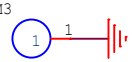
M3



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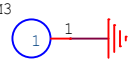

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