

Economy Primary Side Controller

FEATURES

- User Programmable Soft Start With Active Low Shutdown
- User Programmable Maximum Duty Cycle
- Accessible 5V Reference
- Undervoltage Lockout
- Operation to 1MHz
- 0.4A Source/0.8A Sink FET Driver
- Low 100 μ A Startup Current

DESCRIPTION

The UCC3809 family of BCDMOS economy low power integrated circuits contains all the control and drive circuitry required for off-line and isolated DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100 μ A, a user accessible voltage reference, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

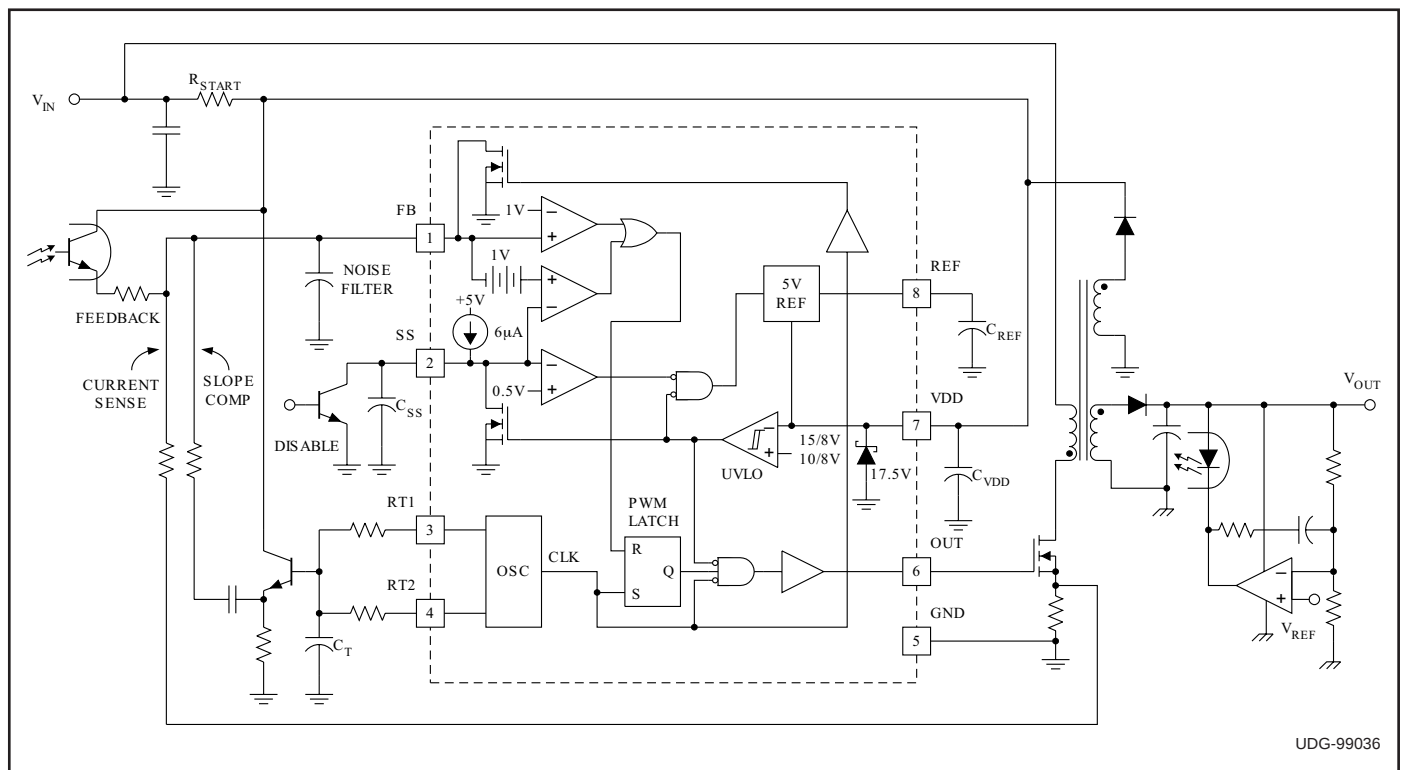
Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3809 family also features full cycle soft start.

The family has UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems as shown in the table to the left.

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCX809-1	10V	8V
UCCX809-2	15V	8V

The UCC3809 and the UCC2809 are offered in the 8 pin SOIC (D), PDIP (N), TSSOP (PW), and MSOP (P) packages. The small TSSOP and MSOP packages make the device ideal for applications where board space and height are at a premium.

TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

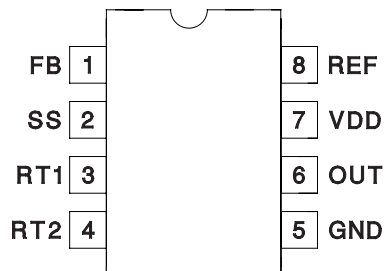
VDD	19V
I _{VDD}	25mA
I _{OUT} (tpw < 1μs and Duty Cycle < 10%)	−0.4A to 0.8A
RT1, RT2, SS	−0.3V to REF + 0.3V
I _{REF}	−15mA
Storage Temperature	−65°C to +150°C
Junction Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

* Values beyond which damage may occur.

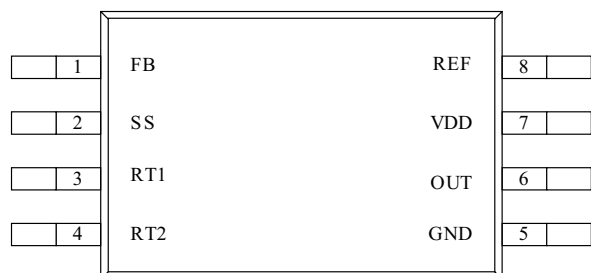
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

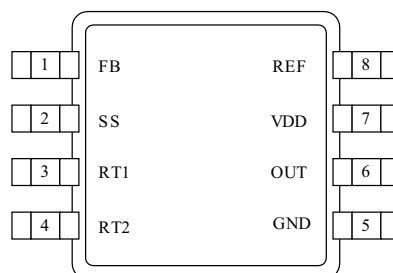
SOIC-8, DIL-8 (Top View) D, N and J Packages



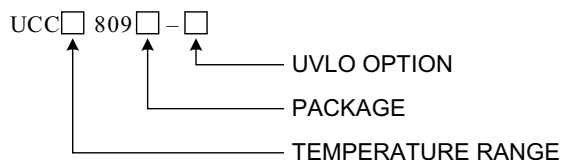
TSSOP-8 (Top View) PW Package



MSOP-8 (Top View) P Package



ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS Unless otherwise specified, $C_{VREF} = 0.47 \mu F$, $V_{DD} = 12V$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft Start Section					
I_{SS}	$V_{DD} = 16V$, $V_{SS} = 0V$; $-40^{\circ}C$ to $+85^{\circ}C$	-4.9	-7.0	-9.1	μA
	$V_{DD} = 16V$, $V_{SS} = 0V$; $< -40^{\circ}C$; $> +85^{\circ}C$	-4.0	-7.0	-10.0	μA
V_{SS} Low	$V_{DD} = 7.5V$, $I_{SS} = 200\mu A$			0.2	V
Shutdown Threshold		0.44	0.48	0.52	V
Oscillator Section					
Frequency	$RT1 = 10k$, $RT2 = 4.32k$, $C_T = 820pF$	90	100	110	kHz
Frequency Change with Voltage	$V_{DD} = 10V$ to $15V$		0.1	</	

APPLICATION INFORMATION

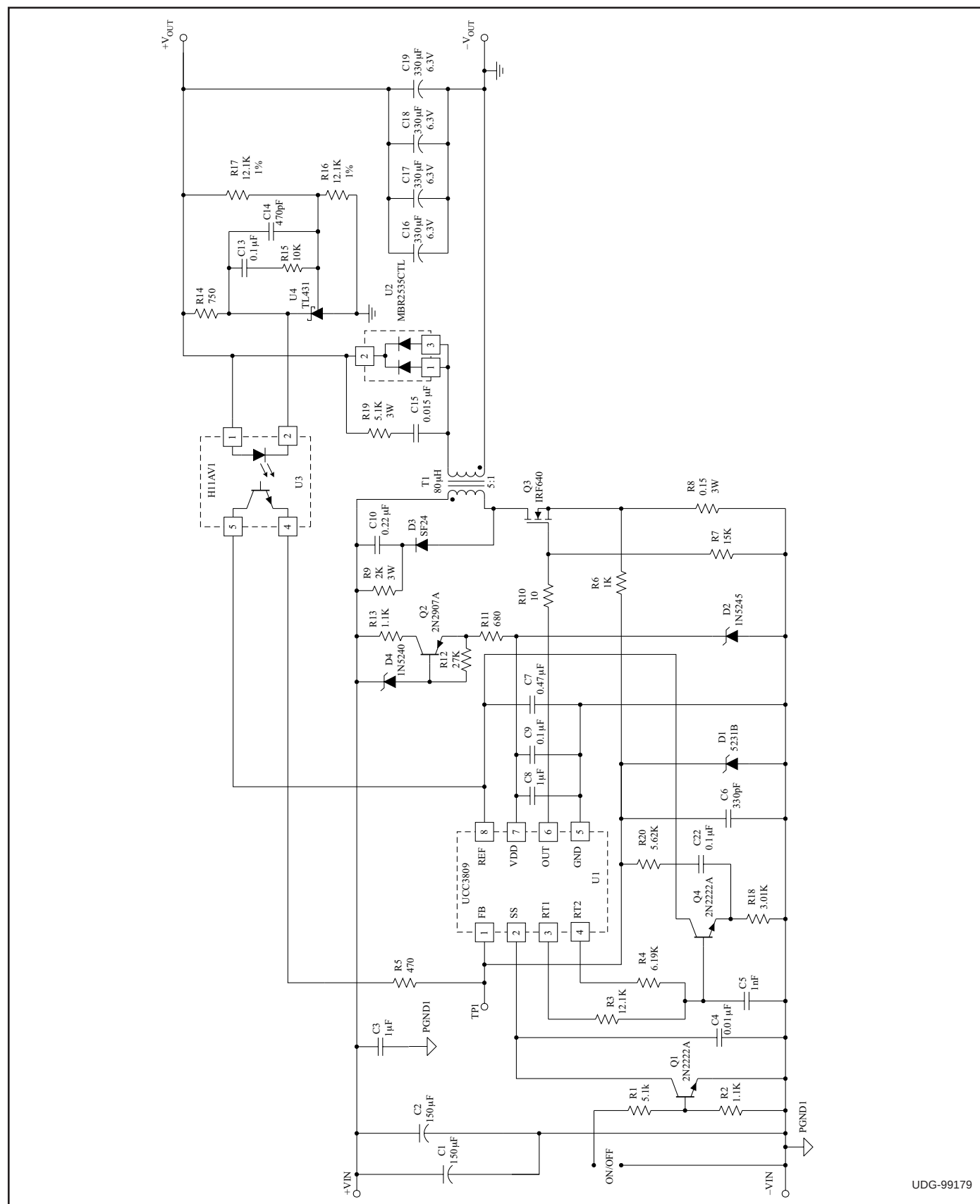


Figure 1. Isolated 50W flyback converter utilizing the UCC3809. The switching frequency is 70kHz, $V_{in} = -32V$ to $-72V$, $V_{out} = +5V$, $I_{out} = 0A$ to $10A$

APPLICATION INFORMATION (cont.)

The Typical Application Diagram shows an isolated flyback converter utilizing the UCC3809. Note that the capacitors C_{REF} and C_{VDD} are local decoupling capacitors for the reference and IC input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close to the IC pins as possible, and returned directly to the ground pin of the chip for best stability. REF provides the internal bias to many of the IC functions and C_{REF} should be at least $0.47\mu F$ to prevent REF from drooping.

FB Pin

The basic premise of the UCC3809 is that the voltage sense feedback signal originates from an optocoupler that is modulated by an external error amplifier located on the secondary side. This signal is summed with the current sense signal and any slope compensation at the FB pin and compared to a 1V threshold, as shown in the Typical Application Diagram. Crossing this 1V threshold resets the PWM latch and modulates the output driver on-time much like the current sense comparator used in the UC3842. In the absence of a FB signal, the output will follow the programmed maximum on-time of the oscillator.

When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the FB pin. By correctly selecting the emitter resistor of the optocoupler, the voltage sense signal can force the FB node to exceed the 1V threshold when the output that is being compared exceeds a desired level. Doing so drives the UCC3809 to zero percent duty cycle.

Oscillator

The following equation sets the oscillator frequency:

$$F_{OSC} = [0.74 \cdot (CT + 27pF) \cdot (RT1 + RT2)]^{-1}$$

APPLICATION INFORMATION (cont.)

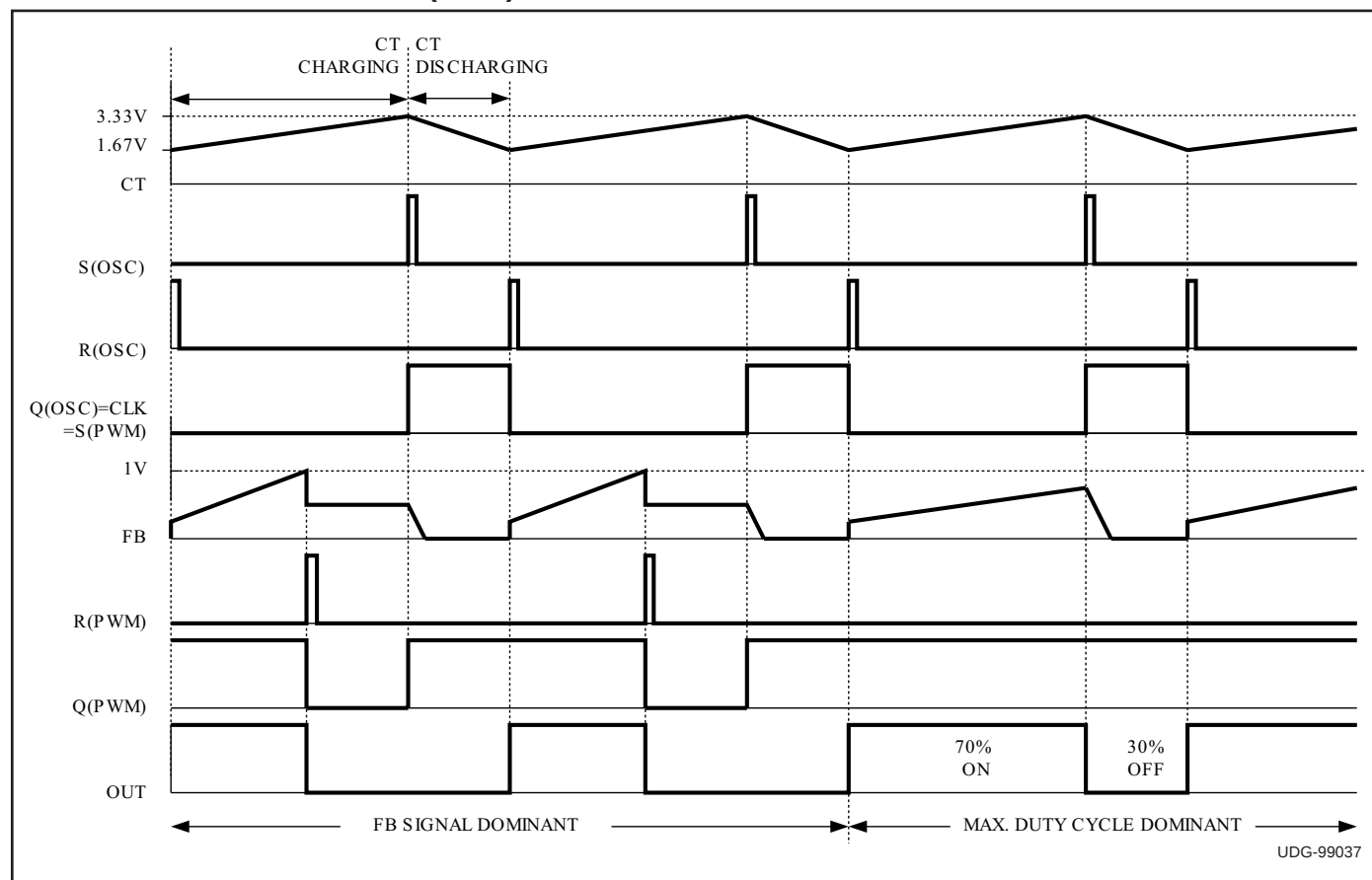


Figure 3. Waveforms associated with the oscillator latch and the PWM latch.

The recommended value for CT is 1nF for frequencies in the 100 kHz or less range and smaller CT for higher frequencies. The minimum recommended values of RT1 and RT2 are 10k Ω and 4.32k Ω , respectively. Using these values maintains a ratio of at least 20:1 between the $R_{DS(on)}$ of the internal F

APPLICATION INFORMATION (cont.)

Synchronization

Both of the synchronization schemes shown in Figure 5 can be successfully implemented with the internal oscillator of the UCC3809. Both schemes allow access to the timing ramp needed for slope compensation and have minimal impact on the programmed maximum duty cycle. In the absence of a sync pulse, the PWM controller will run independently at the frequency set by RT1, RT2, and CT. This free running frequency must be approximately 15 to 20% lower than the sync pulse frequency to insure the free running oscillator does not cross the comparator threshold before the desired sync pulse.

Option I uses the synchronization pulse to pull pin 3 low, triggering the internal 1.67V comparator to reset the RS latch and initiate a charging cycle. The valley voltage of the CT waveform is higher when synchronized using this configuration, decreasing the ramp charge and discharge times, thereby increasing the operating frequency; otherwise the overall shape of the CT voltage waveform is un-

changed.

Option II uses the synchronization pulse to superimpose the sync voltage onto the peak of the CT waveform. This triggers the internal 3.33V comparator, initiating a discharge cycle. The sync pulse is summed with the free running oscillator waveform at the CT node, resulting in a spike on top of the CT peak voltage.

ADDITIONAL INFORMATION

Please refer to the following Unitrode application topics for additional information.

[1] Application Note U-165, Design Review: Isolated 50W Flyback Converter with the UCC3809 Primary Side Controller by Lisa Dinwoodie.

[2] Design Note DN-89, Comparing the UC3842, UCC3802, and UCC3809 Primary Side PWM Controllers by Lisa Dinwoodie.

TYPICAL CHARACTERISTICS CURVES

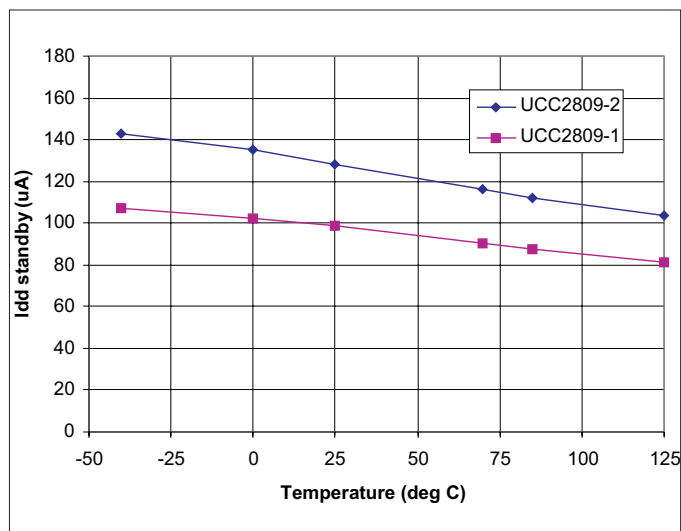
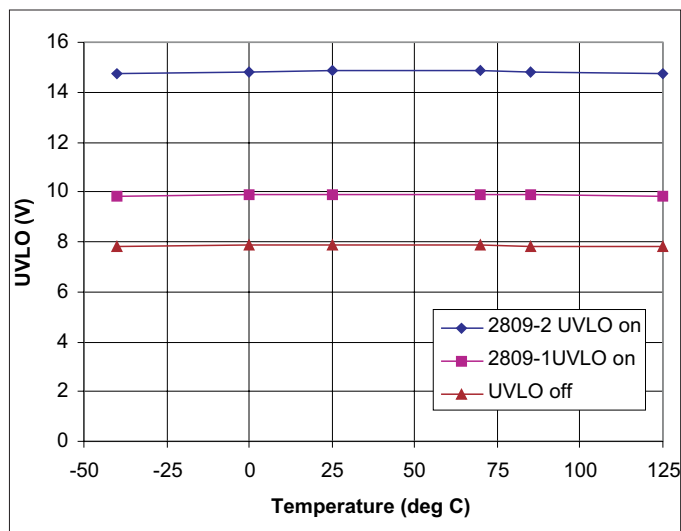


Figure 6. I_{DD} (standby) vs. temperature.



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2809D-1	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-1 D-1
UCC2809D-1.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-1 D-1
UCC2809D-2	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-2 D-2
UCC2809D-2.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2809-2 D-2
UCC2809DTR-1	Active	Production	SOIC						

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2809PWTR-1.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	28091
UCC3809D-1	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-1 D-1
UCC3809D-1.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-1 D-1
UCC3809D-2	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-2 D-2
UCC3809D-2.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	3809-2 D-2

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2809DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	1	

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2809DTR-1	SOIC	D	8	2500	353.0	353.0	32.0
UCC2809DTR-2	SOIC	D	8	2500	353.0	353.0	32.0
UCC2809PTR-1	VSSOP	DGK	8	2500	366.0	364.0	50.0
UCC2809PTR-1G4	VSSOP	DGK	8	2500	366.0	364.0	50.0</

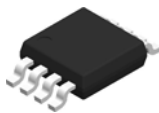
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
UCC2809D-1	D	SOIC	8	75	507	8	3940	4.32
UCC2809D-1.A	D	SOIC	8	75	507	8	3940	4.32
UCC2809D-2	D	SOIC	8	75	507	8	3940	4.32
UCC2809D-2.A	D	SOIC						

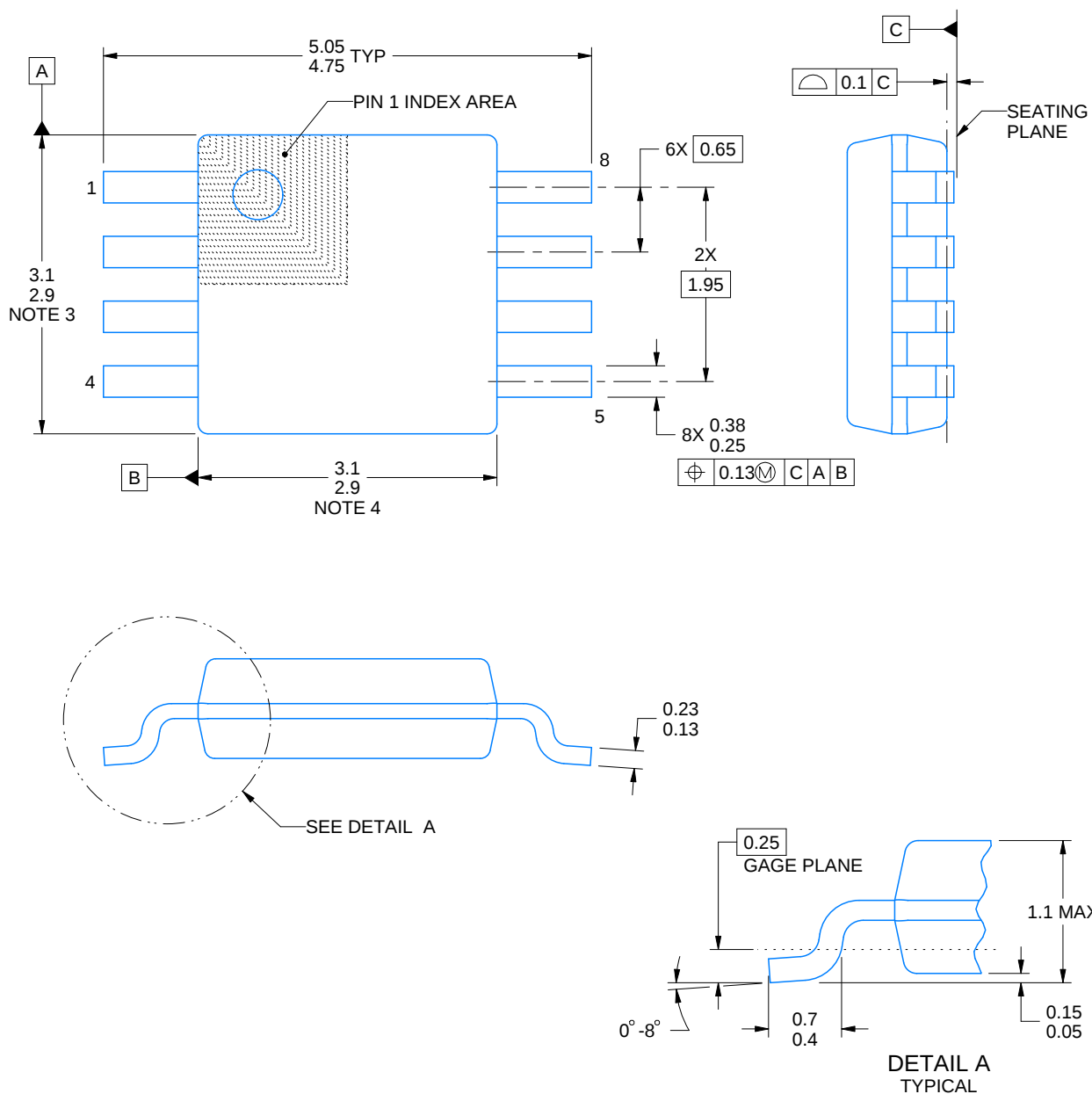
DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

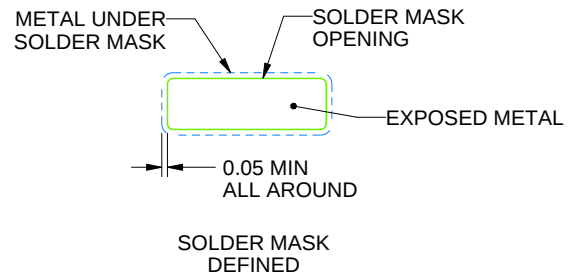
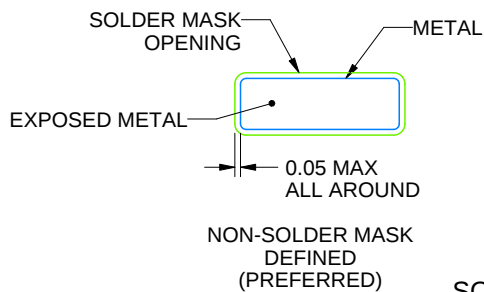
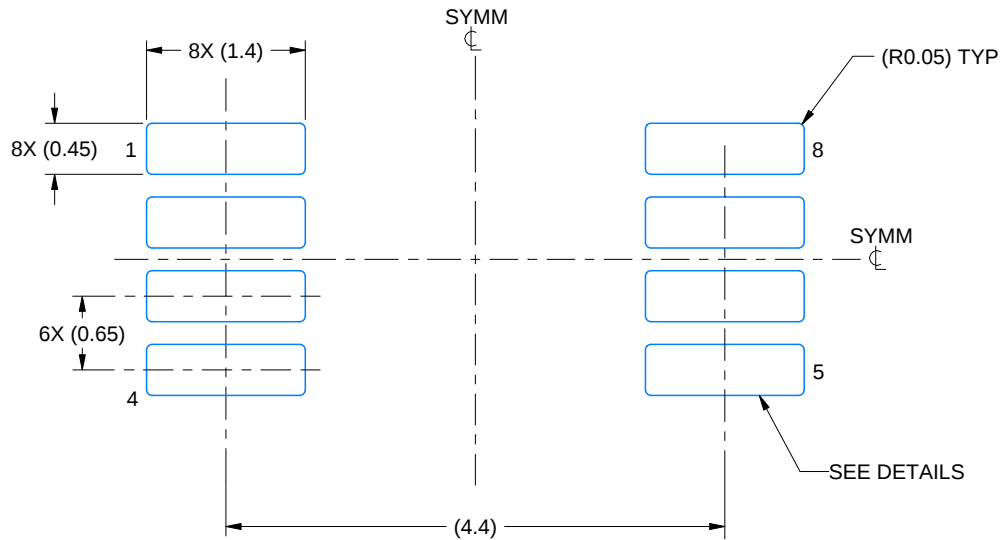


EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

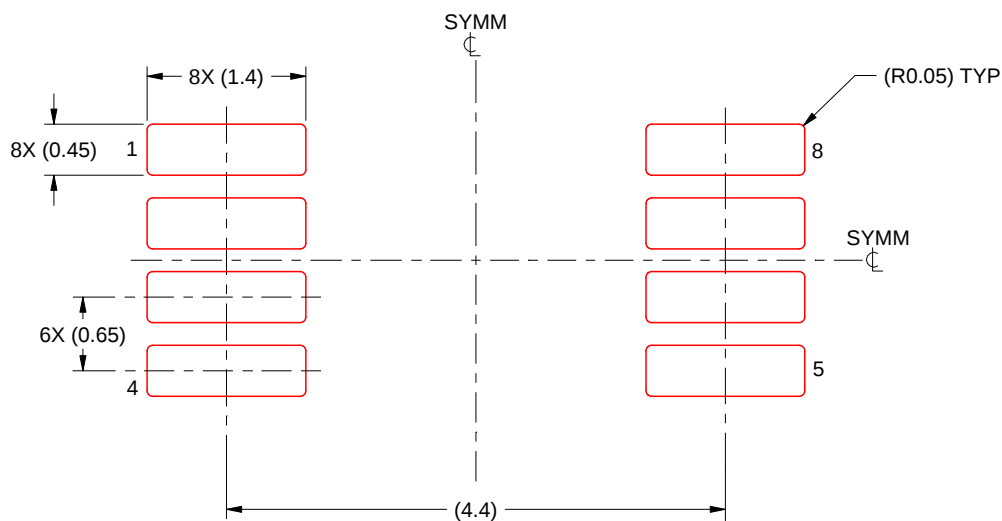


EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

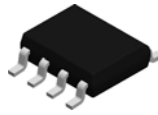


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

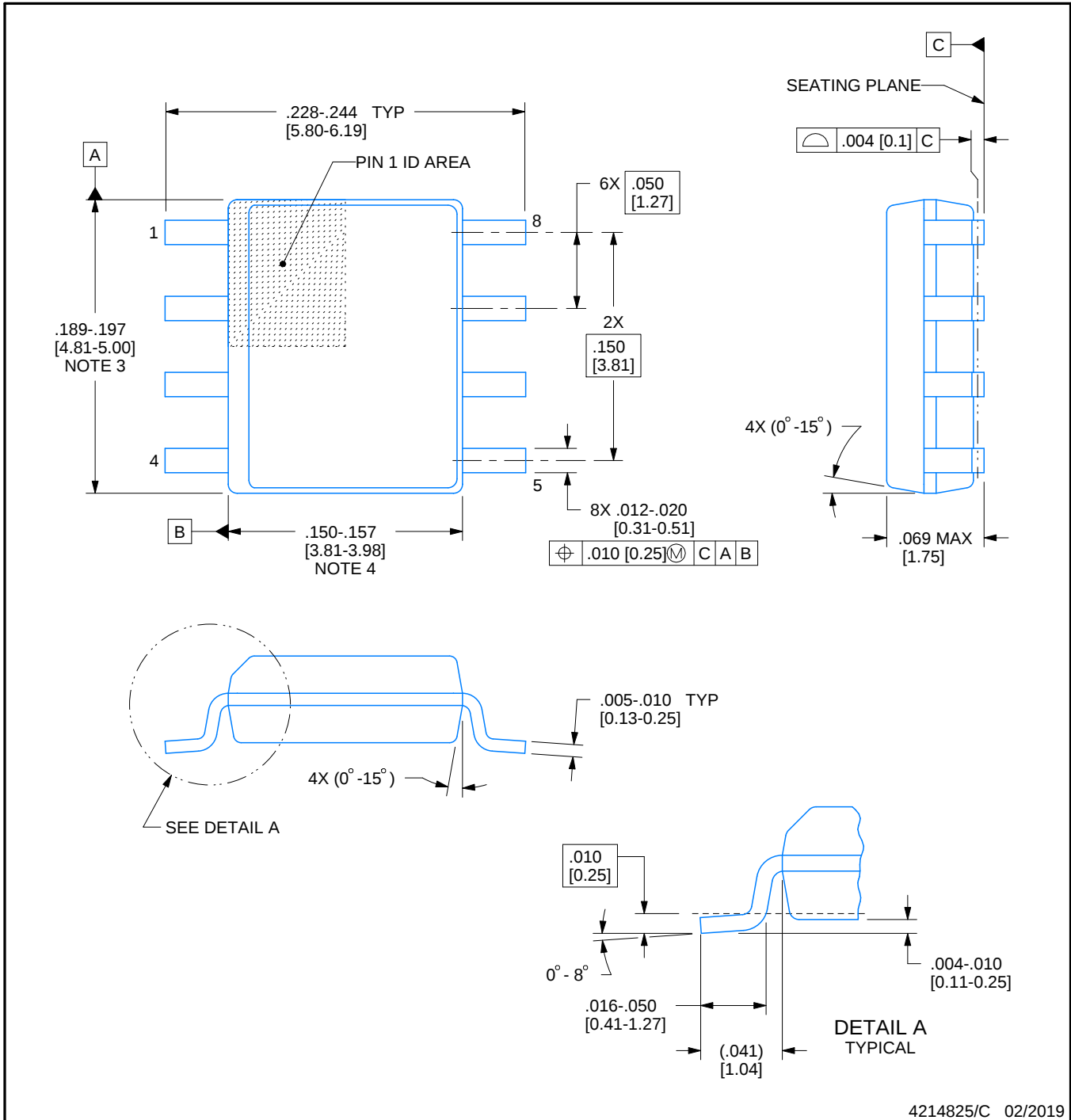


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

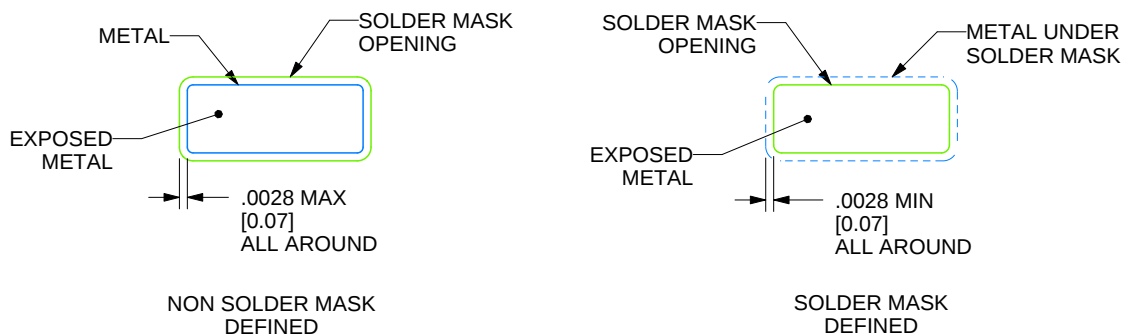
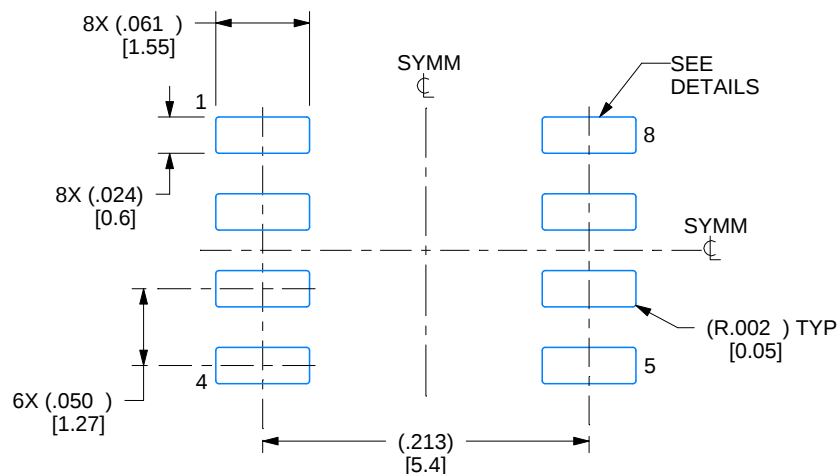


EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

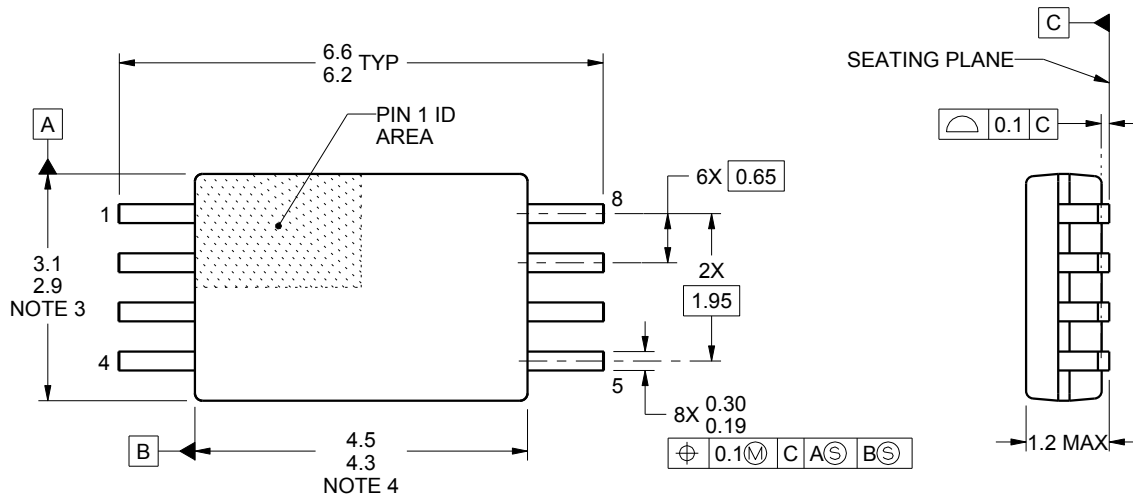
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

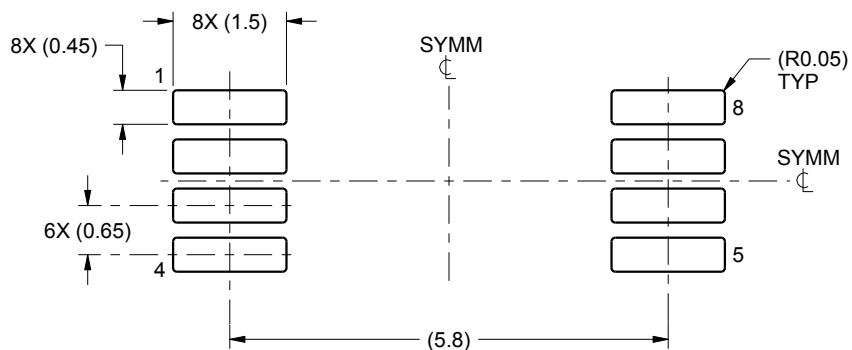


EXAMPLE BOARD LAYOUT

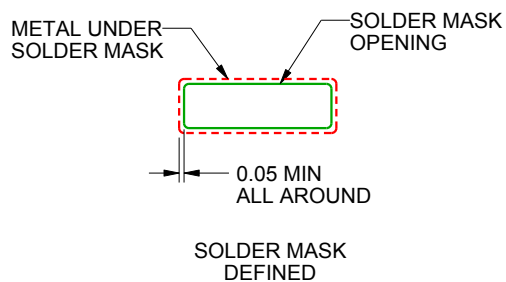
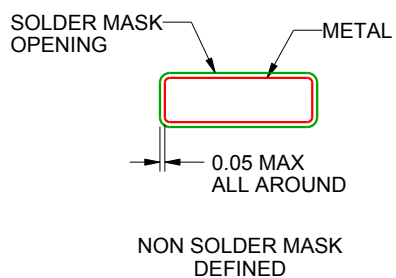
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X

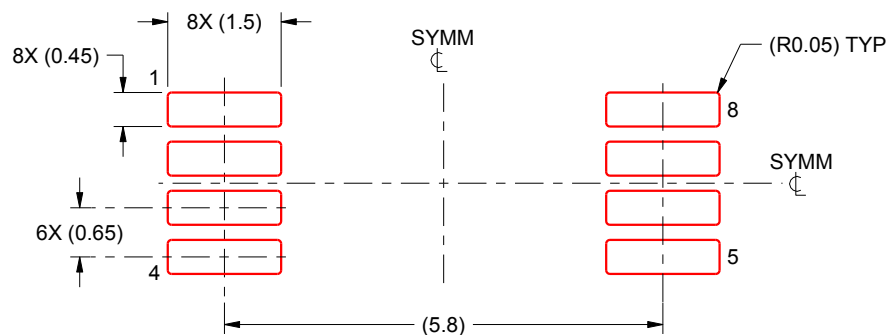


EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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