TPA0103
1.75-W 3-CHANNEL STEREO AUDIO POWER AMPLIFIER

- **Desktop Computer Amplifier Solution**
  - **1.75-W Bridge Tied Load (BTL) Center Channel**
  - **500-mW L/R Single-Ended Channels**
- **Low Distortion Output**
  - **< 0.05% THD+N at Full Power**
- **Full 3.3-V and 5-V Specifications**
- **Surface-Mount Power Package 24-Pin TSSOP**
- **L/R Input MUX Feature**
- **Shutdown Control . . . I$_{DD}$ = 5 μA**
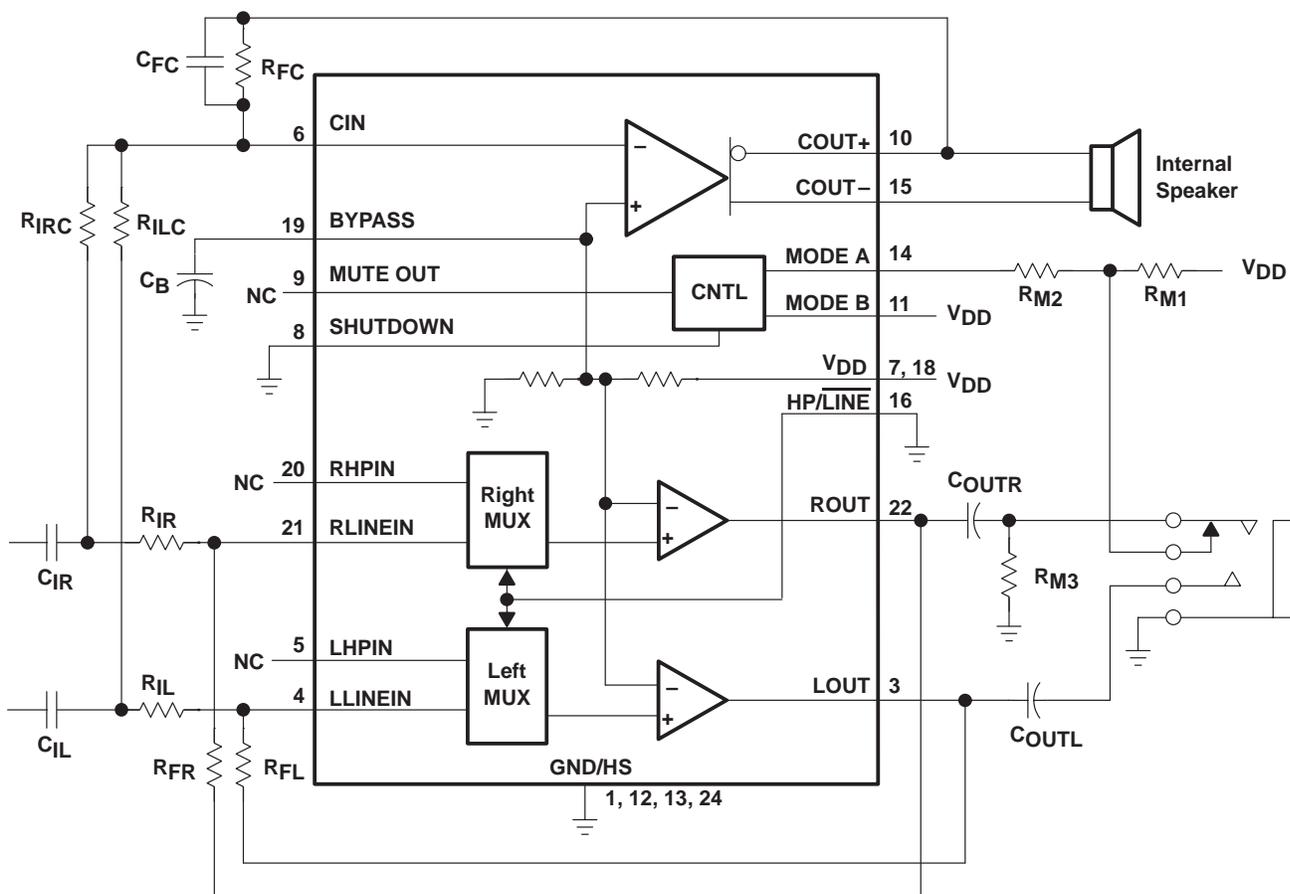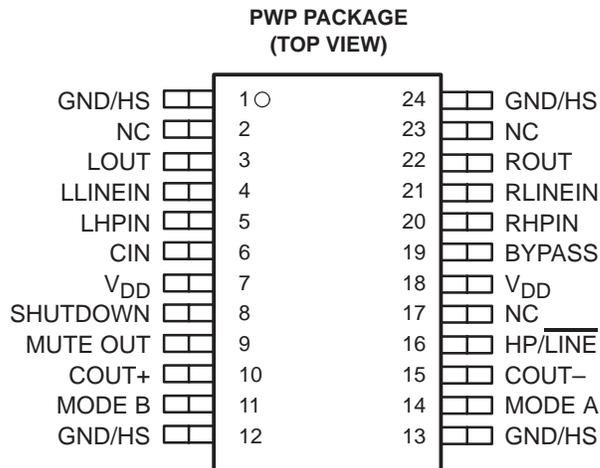
PWP PACKAGE
(TOP VIEW)

GND/HS	1	24	GND/HS
NC	2	23	NC
LOUT	3	22	ROUT
LLINEIN	4	21	RLINEIN
LHPIN	5	20	RHPIN
CIN	6	19	BYPASS
V$_{DD}$	7	18	V$_{DD}$
SHUTDOWN	8	17	NC
MUTE OUT	9	16	HP/$\overline{LINE}$
COUT+	10	15	COUT–
MODE B	11	14	MODE A
GND/HS	12	13	GND/HS

Copyright © 2000, Texas Instruments Incorporated

TEXAS INSTRUMENTS

TPA0103
1.75-W 3-CHANNEL STEREO AUDIO POWER AMPLIFIER

description

The TPA0103 is a 3-channel audio power amplifier in a 24-pin TSSOP thermal package primarily targeted at desktop PC or notebook applications. The left/right (L/R) channel outputs are single ended (SE) and capable of delivering 500 mW of continuous RMS power per channel into 4-Ω loads. The center channel output is a bridged tied load (BTL) configuration for delivering maximum output power from PC power supplies. Combining the SE line drivers and high power center channel amplifiers in a single TSSOP package simplifies design and frees up board space for other features. Full power distortion levels of less than 0.25% THD+N into 4-Ω loads from a 5-V supply voltage are typical. Low-voltage application are also well served by the TPA0103 providing 800 mW to the center channel into 4-Ω loads with a 3.3-V supply voltage.

Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10. A two channel input MUX circuit is integrated on the L/R channel inputs to allow two sets of stereo inputs to the amplifier. In the typical application, the center channel amplifier is driven from a mix of the L/R inputs to produce a monaural representation of the stereo signal. The center channel amplifier can be shut down independently of the L/R output for speaker muting in headphone applications. The TPA0103 also features a full shutdown function for power sensitive applications holding the bias current to 5 μA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of less than 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0103 to operate at full power at ambient temperature of up to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE
	TSSOP† **(PWP)**
−40°C to 85°C	TPA0103PWP

† The PWP package is available in left-ended tape and reel only (e.g., TPA0103PWPLE).

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
BYPASS	19		Bypass. BYPASS is a tap to the voltage divider for the internal mid-supply bias.
CIN	6	I	Center channel input
COUT+	10	O	Center channel + output. COUT+ is in an active or high-impedance state unless the device is in a mute state when the MODE A terminal (14) is high and the MODE B terminal (11) is low.
COUT–	15	O	Center channel – output. COUT– is in an active or high-impedance state unless the device is in a mute state when the MODE A terminal (14) is high and the MODE B terminal (11) is low.
GND/HS	1, 12, 13, 24		Ground. GND/HS is the ground connection for circuitry, directly connected to thermal pad.
MODE A, MODE B	14, 11	I	Mode select. MODE A and MODE B determine the output modes of the TPA0103.

TERMINAL	3 CHANNEL	MUTE	CENTER ONLY	L/R ONLY
MODE A	L	H	L	H
MODE B	L	L	H	H

TERMINAL NAME	NO.	I/O	DESCRIPTION
HP/LINE	16	I	Input MUX control input, hold high to select (L/R) HPIN (5, 20), hold low to select (L/R) LINEIN (4, 21). HP/LINE is normally connected to ground when inputs are connected to (L/R) LINEIN.
LHPIN	5	I	Left channel headphone input, selected when the HP/LINE terminal (16) is held high
LLINEIN	4	I	Left channel line input, selected when the HP/LINE terminal (16) is held low
LOUT	3	O	Left channel output. LOUT is active when the MODE A terminal (14) is low and the MODE B terminal (11) is don't care.
MUTE OUT	9	O	When the MODE A terminal (14) is high and the MODE B terminal (11) is low, MUTE OUT is high and the device is in a mute state. Otherwise MUTE OUT is low.
NC	2, 17, 23		No internal connection
RHPIN	20	I	Right channel headphone input, selected when the HP/LINE terminal (16) is held high
RLINEIN	21	I	Right channel line input, selected when the HP/LINE terminal (16) is held low
ROUT	22	O	Right channel output. ROUT is active when the MODE A terminal (14) is low and the MODE B terminal (11) is don't care.
SHUTDOWN	8	I	Places entire IC in shutdown mode when held high, I_{DD} = 5 µA
V_{DD}	7, 18	I	Supply voltage input. The V_{DD} terminals must be connected together.

TPA0103
1.75-W 3-CHANNEL STEREO AUDIO POWER AMPLIFIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . 6 V

Continuous output current (COUT+, COUT−, LOUT, ROUT) . . . . 2 A

Continuous total power dissipation . . . . internally limited

Operating virtual junction temperature range, T_J . . . . −40°C to 150°C

Operating virtual case temperature range, T_C . . . . −40°C to 125°C

Storage temperature range, T_{stg} . . . . −65°C to 150°C

Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP‡	2.7 W	21.8 mW/°C	1.7 W	1.4 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	3	5	5.5	V
Operating junction temperature, T_J		125		°C

dc electrical characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		NOM	TYP	MAX	UNIT
I_{DD}	Supply current	V_{DD} = 5 V	3 Channel		19	25	mA
			L and R or Center only		9	15	mA
		V_{DD} = 3.3 V	3 Channel		13	20	mA
			L and R or Center only		3	10	mA
V_{OO}	Output offset voltage (measured differentially)	V_{DD} = 5 V, Gain = 2, See Note 1			5	35	mV
$I_{DD(MUTE)}$	Supply current in mute mode	V_{DD} = 5 V			800		μA
$I_{DD(SD)}$	I_{DD} in shutdown	V_{DD} = 5 V			5	15	μA

NOTE 1:   At 3 V < V_{DD} < 5 V the dc output voltage is approximately V_{DD}/2.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

ac operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel) (see Note 2)	THD = 0.2%, BTL, Center channel			1.75		W
		THD = 1%, BTL, Center channel			2.1		
		THD = 0.2%, SE, L/R channels			535		mW
		THD = 1%, SE, L/R channels			575		
THD+N	Total harmonic distortion plus noise	P_O = 1.5 W, f = 20 to 20 kHz			0.25%		
B_{OM}	Maximum output power bandwidth	G = 10, THD < 5 %			>20		kHz
	Phase margin	Open loop			85		°
	Supply ripple rejection ratio	f = 1 kHz	Center channel		80		dB
			L/R channels		58		
		f = 20 – 20 kHz	Center channel		60		
			L/R channels		30		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz			95		dB
	Line/HP input separation				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	V_O = 1 V(rms)	BTL, Center channel		94		dB
			SE, L/R channels		100		
V_n	Output noise voltage	BTL, Center channel			20		μV(rms)
		SE, L/R channels			9		

NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

ac operating characteristics, V_{DD} = 3.3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power (each channel) (see Note 2)	THD = 0.2% BTL, Center channel			800		mW
		THD = 1% BTL, Center channel			850		
		THD = 0.2%, SE, L/R channels			215		
		THD = 1%, SE, L/R channels			235		
THD+N	Total harmonic distortion plus noise	P_O = 750 mW, f = 20 to 20 kHz			0.8%		
B_{OM}	Maximum output power bandwidth	G = 10, THD < 5 %			>20		kHz
	Phase margin	Open loop			85		°
	Supply ripple rejection ratio	f = 1 kHz	Center channel		70		dB
			L/R channels		62		
		f = 20 – 20 kHz	Center channel		55		
			L/R channels		30		
	Mute attenuation				85		dB
	Channel-to-channel output separation	f = 1 kHz			95		dB
	Line/HP input separation				100		dB
Z_I	Input impedance				2		MΩ
	Signal-to-noise ratio	V_O = 1 V(rms)	BTL, Center channel		93		dB
			SE, L/R channels		100		
V_n	Output noise voltage	BTL, Center channel			21		μV(rms)
		SE, L/R channels			10		

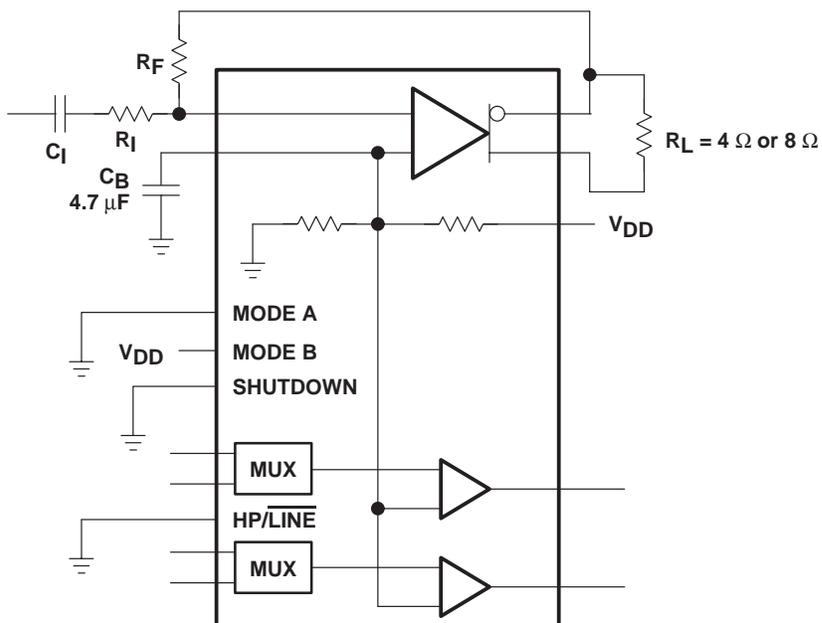NOTE 2: Output power is measured at the output terminals of the IC at 1 kHz.

PARAMETER MEASUREMENT INFORMATION

Figure 1. BTL Test Circuit
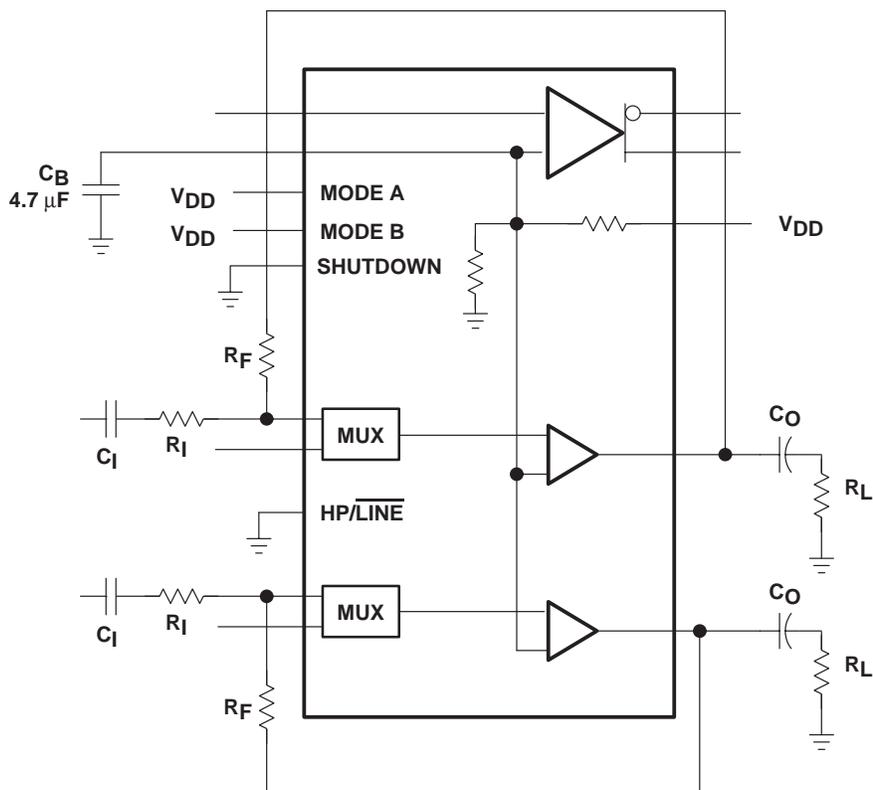
Figure 2. SE Test Circuit

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD + N	Total harmonic distortion plus noise	vs Output power	3, 4, 7, 10–12, 15, 18, 21, 24, 27, 30, 33, 36
		vs Frequency	5, 6, 8, 9, 13, 14, 16, 17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35
V_n	Output noise voltage	vs Frequency	37, 38
	Supply ripple rejection ratio	vs Frequency	39, 40
	Crosstalk	vs Frequency	41, 42
	Open loop response	vs Frequency	43, 44
	Closed loop response	vs Frequency	45 – 48
I_{DD}	Supply current	vs Supply voltage	49
P_O	Output power	vs Supply voltage	50, 51
		vs Load resistance	52, 53
P_D	Power dissipation	vs Output power	54 – 57
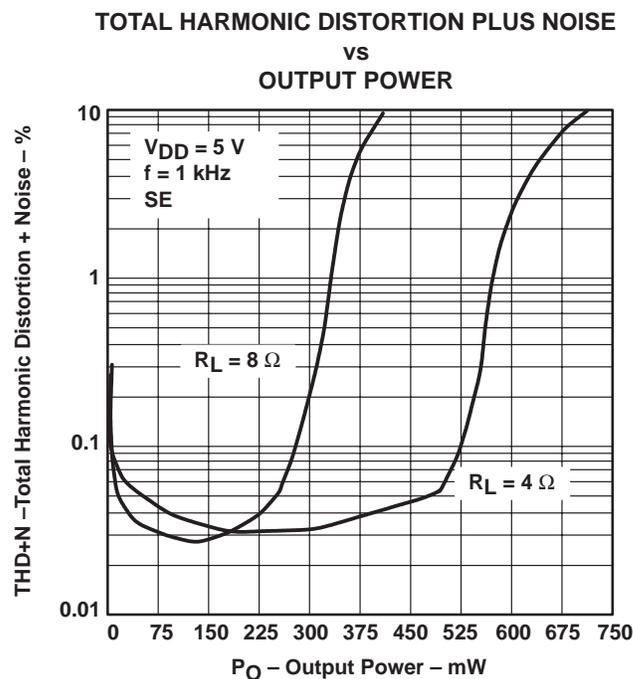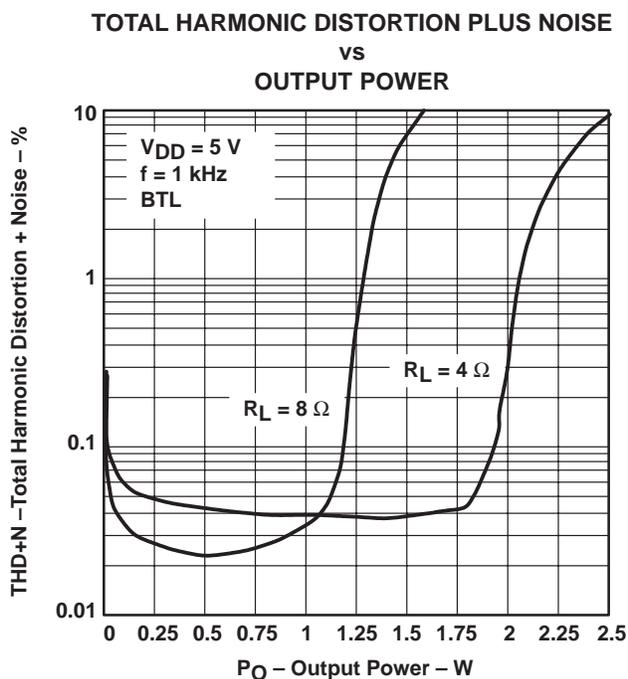
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 4

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

V_{DD} = 5 V
P_O = 1.5 W
R_L = 4 Ω
BTL

A_V = −10 V/V
A_V = −20 V/V
A_V = −2 V/V
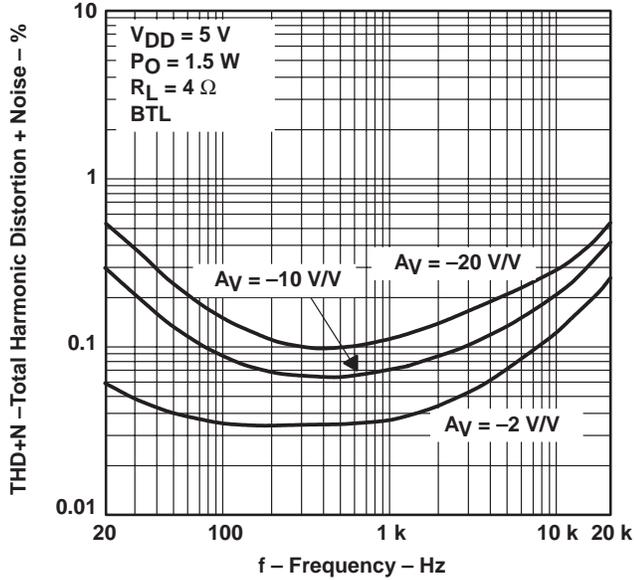
Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

V_{DD} = 5 V
R_L = 4 Ω
A_V = −2 V/V
BTL

P_O = 1.5 W
P_O = 0.75 W
P_O = 0.25 W
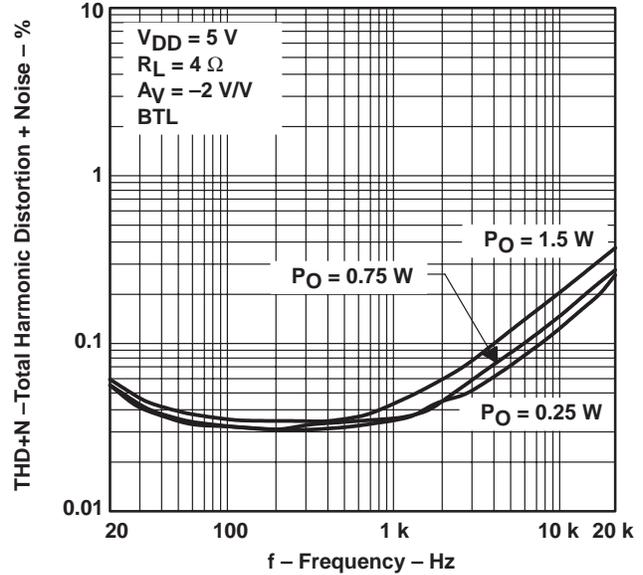
Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

V_{DD} = 5 V
R_L = 4 Ω
BTL

f = 20 kHz
f = 1 kHz
f = 20 Hz
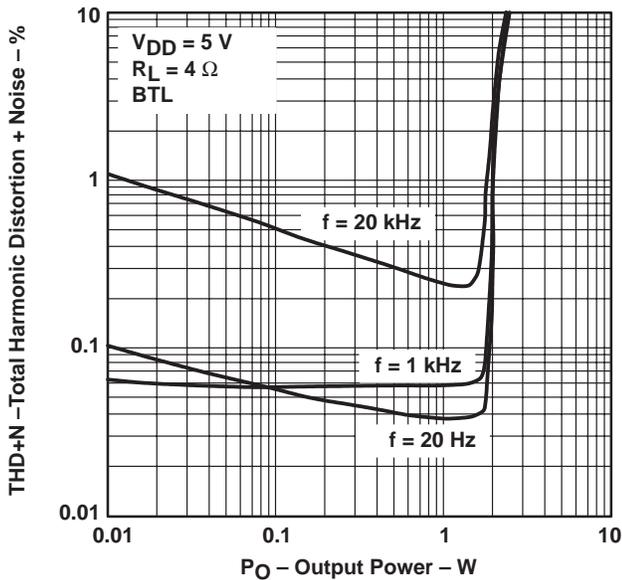
Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
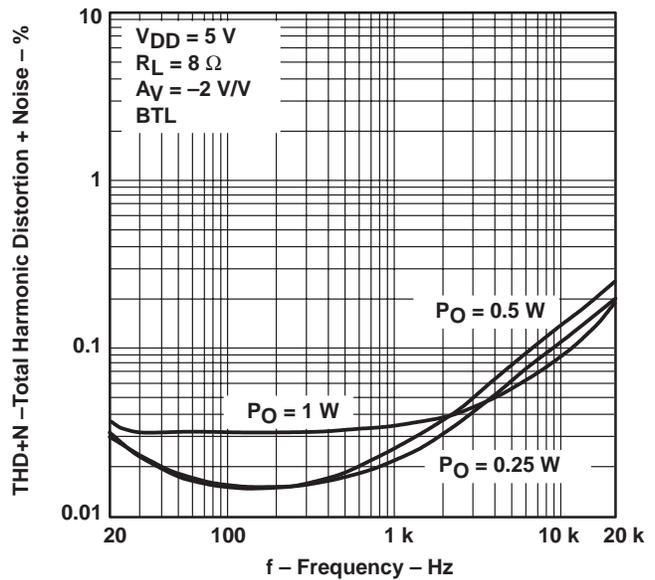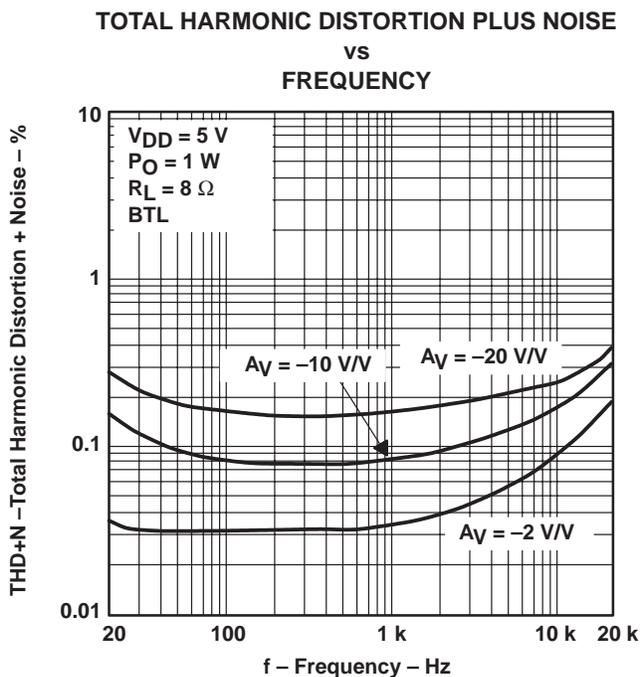
V_{DD} = 5 V
R_L = 8 Ω
A_V = −2 V/V
BTL

P_O = 0.5 W
P_O = 1 W
P_O = 0.25 W

Figure 8

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
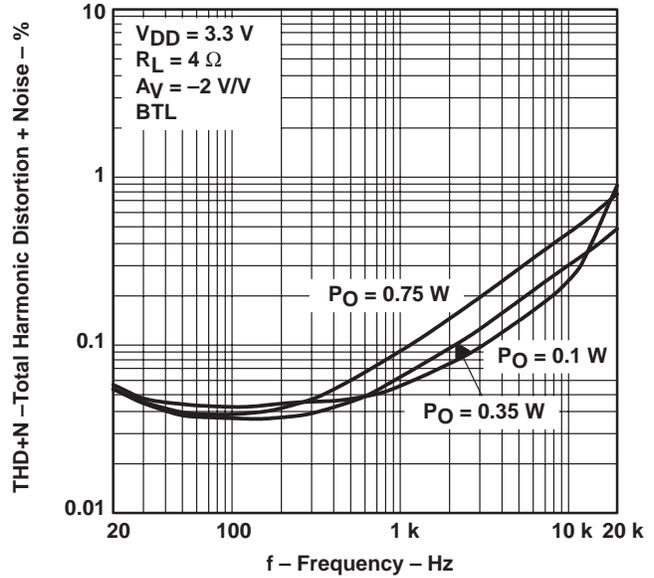

Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER
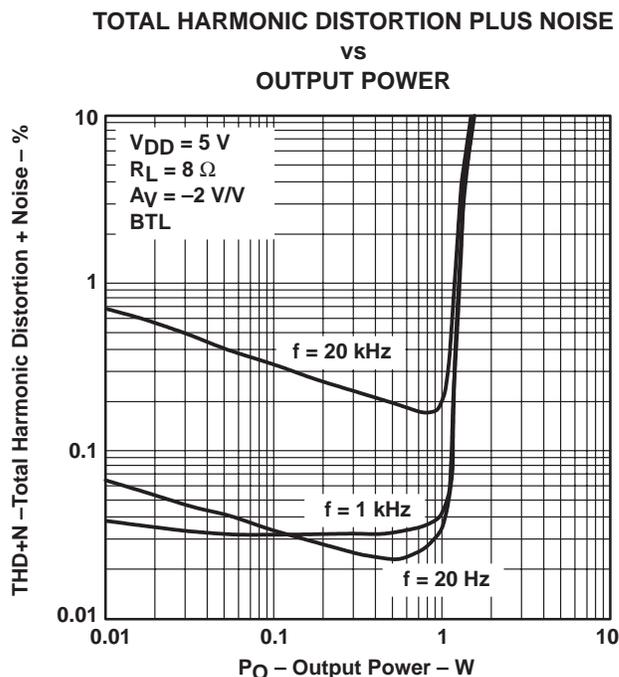
Figure 10
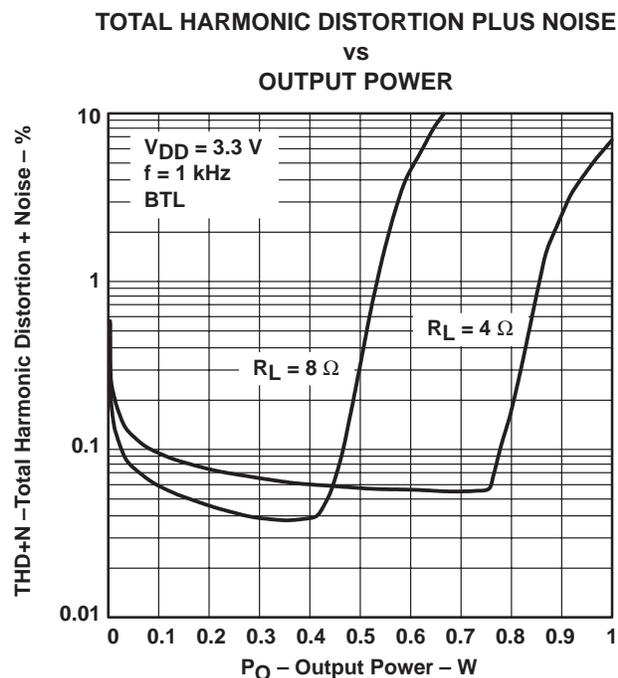
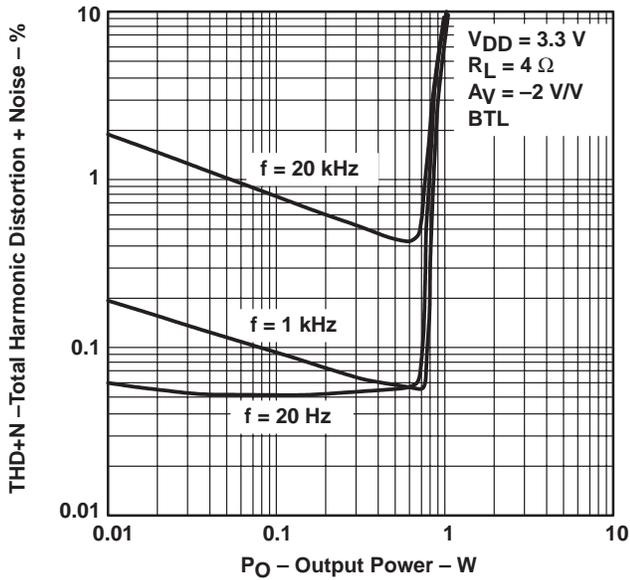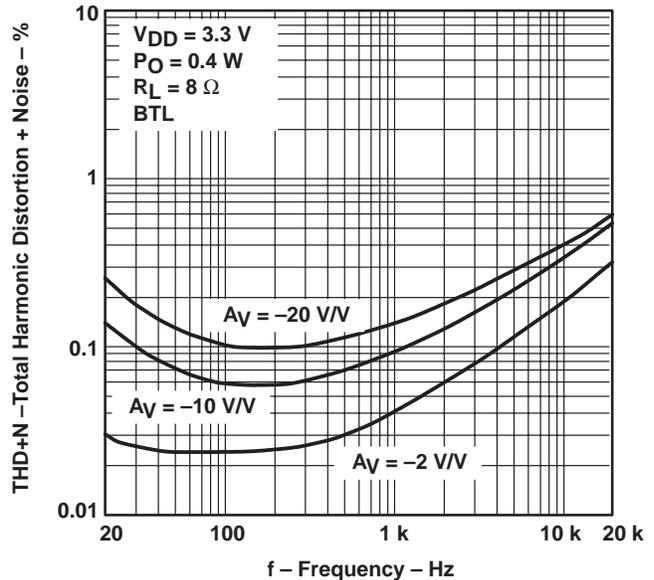TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER
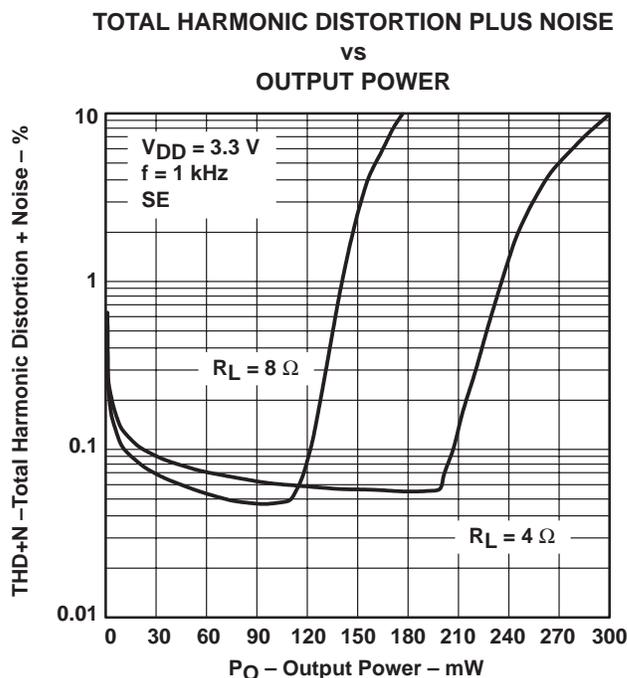
Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

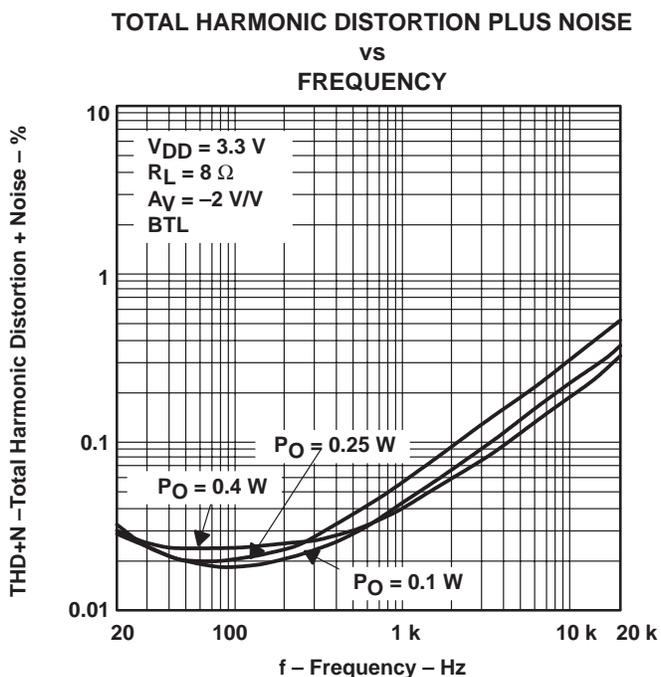Figure 12

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
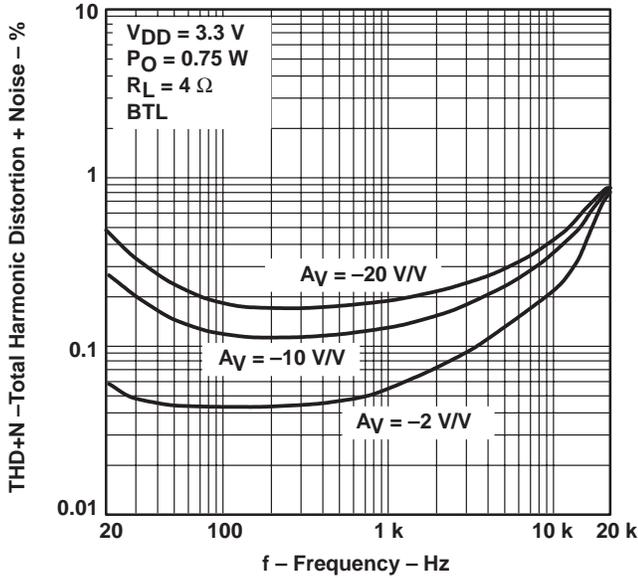
Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 16

TYPICAL CHARACTERISTICS
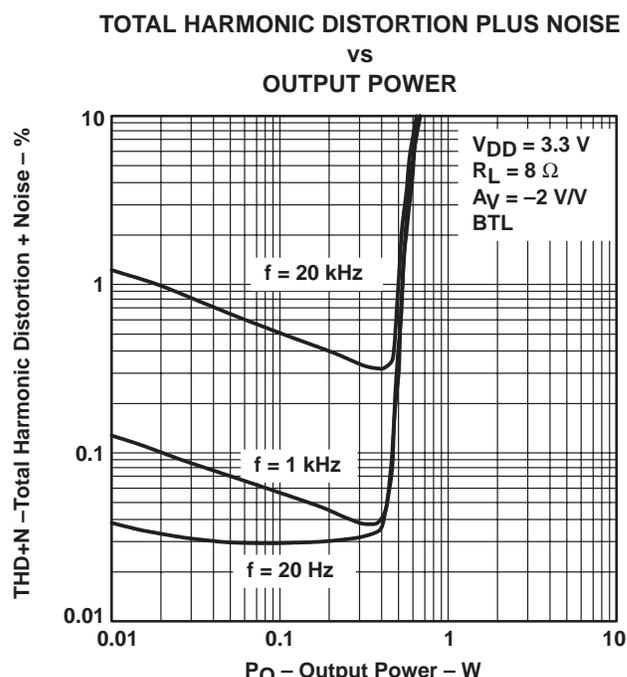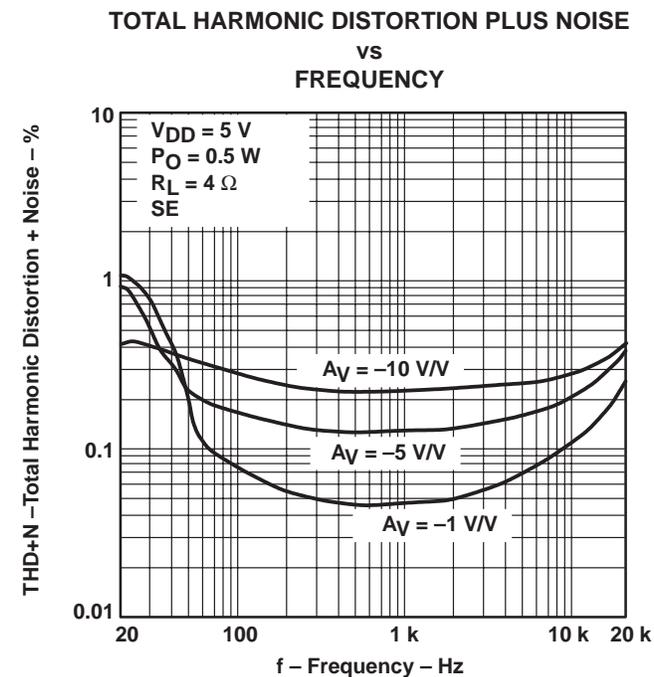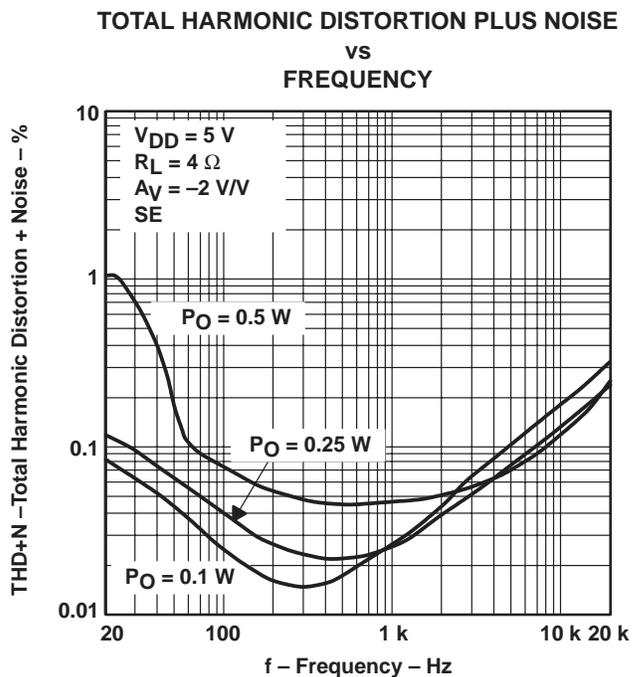
TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 20

TEXAS
INSTRUMENTS

TOTAL HARMONIC DISTORTION PLUS NOISE
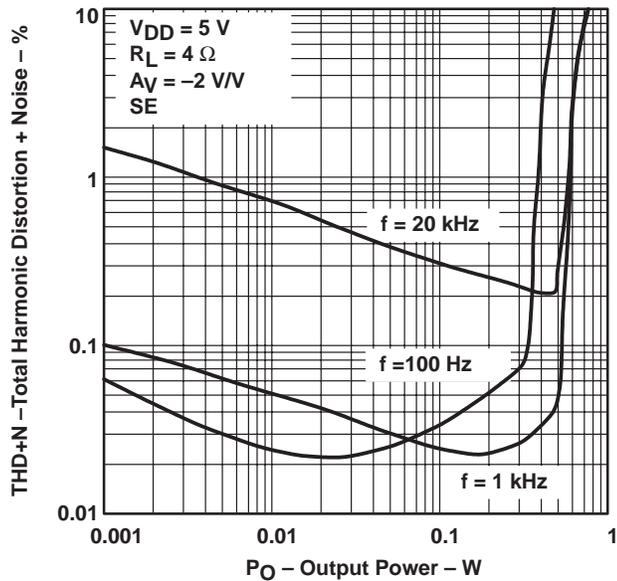**vs**
OUTPUT POWER

Figure 21

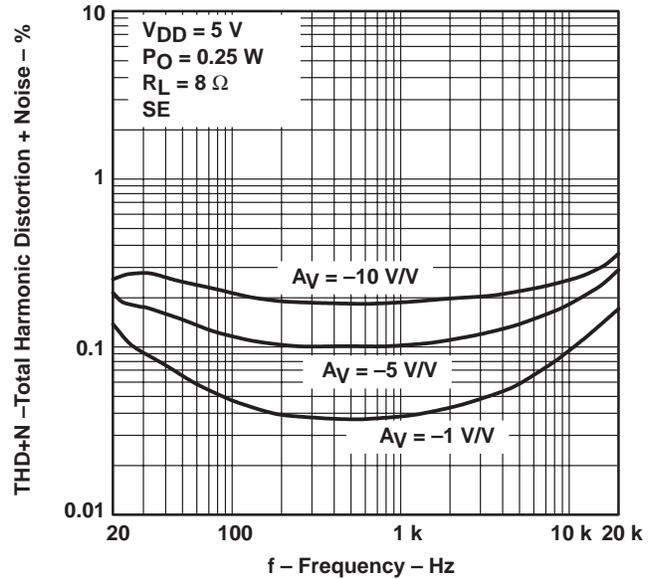**TOTAL HARMONIC DISTORTION PLUS NOISE**
vs
FREQUENCY

Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
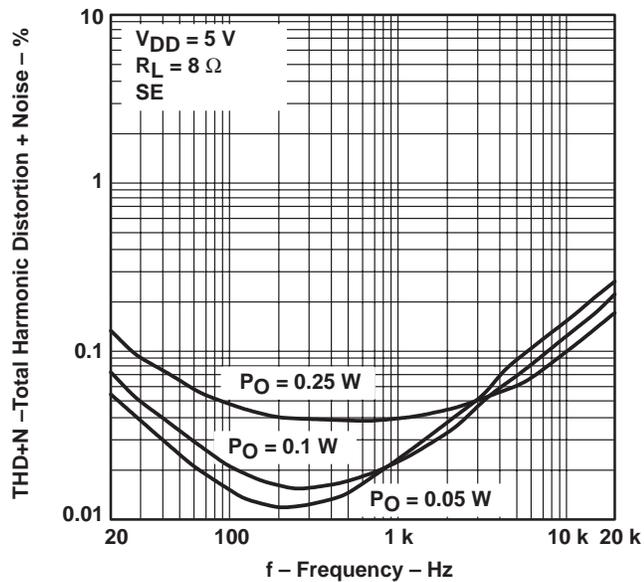**FREQUENCY**

Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 24

TEXAS
INSTRUMENTS
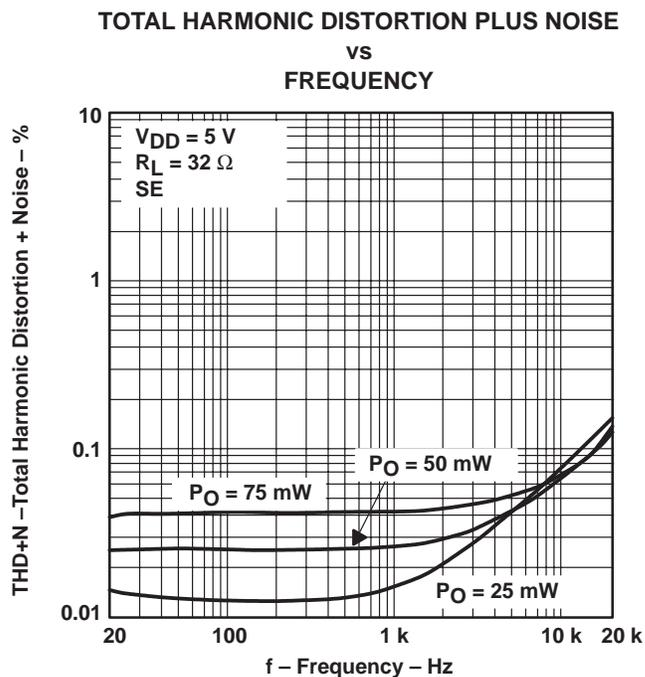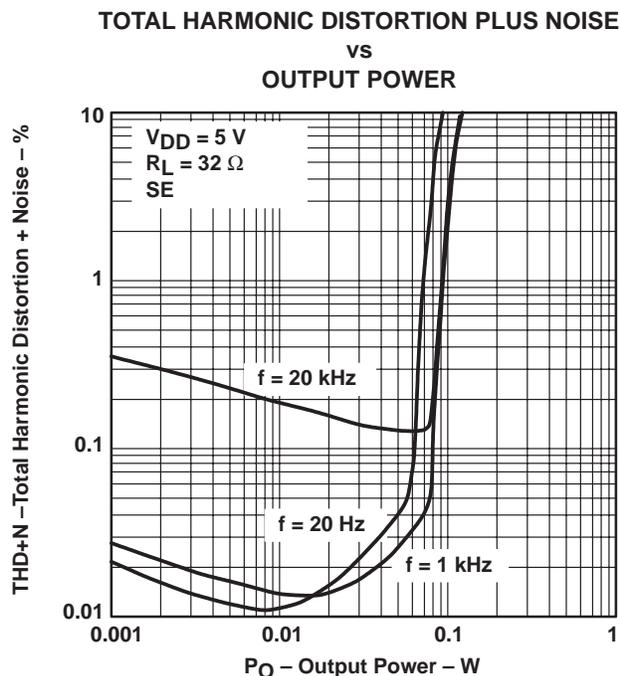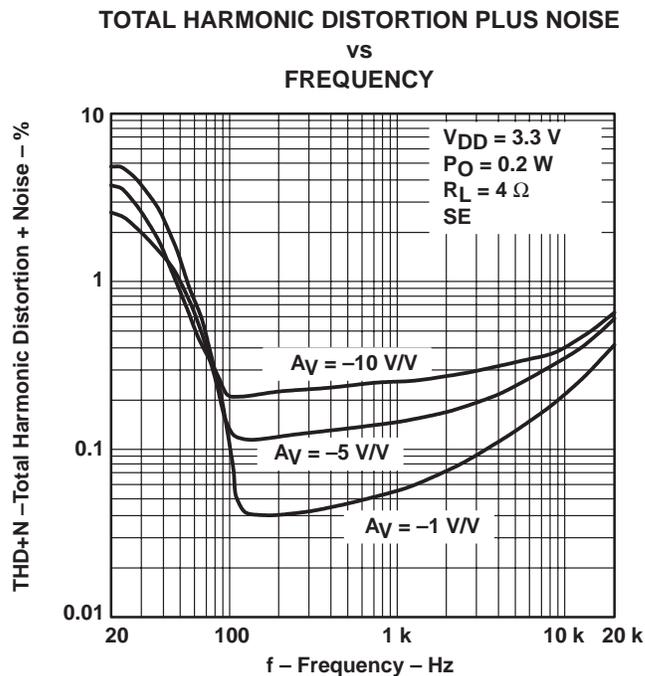
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

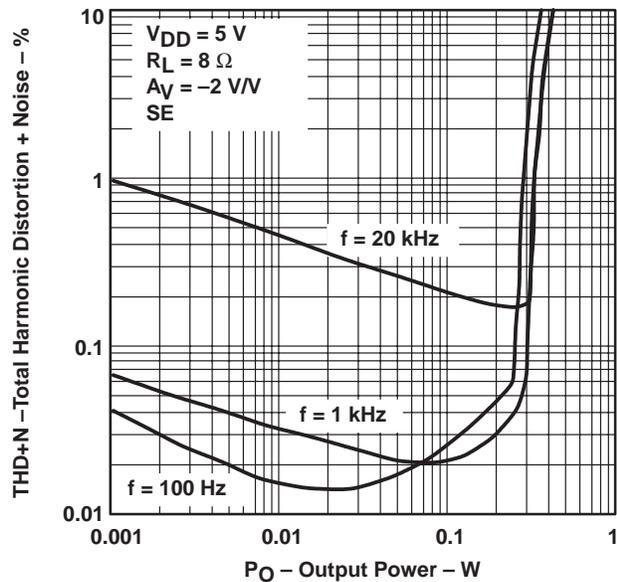Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 28

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
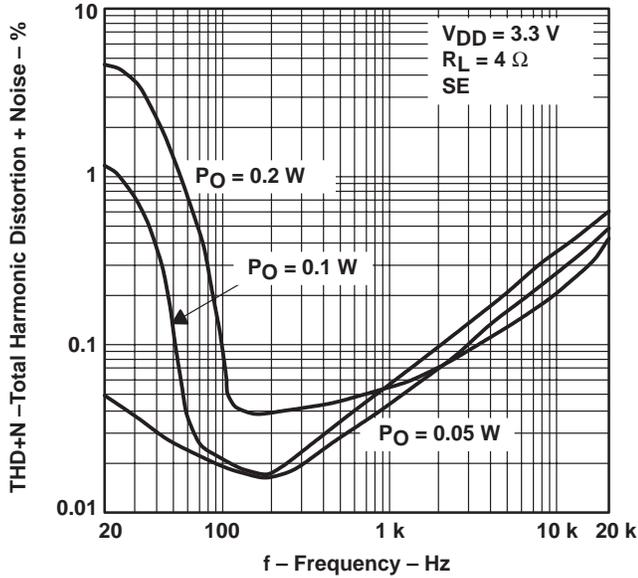
Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE
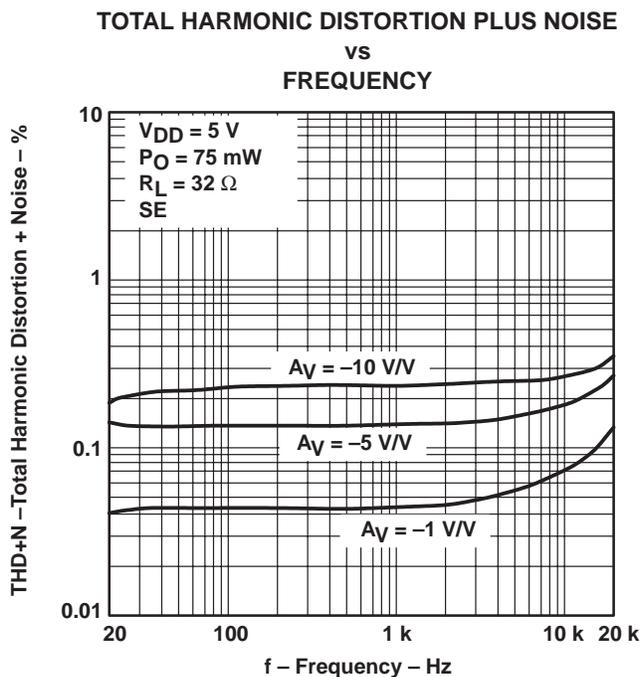vs
OUTPUT POWER
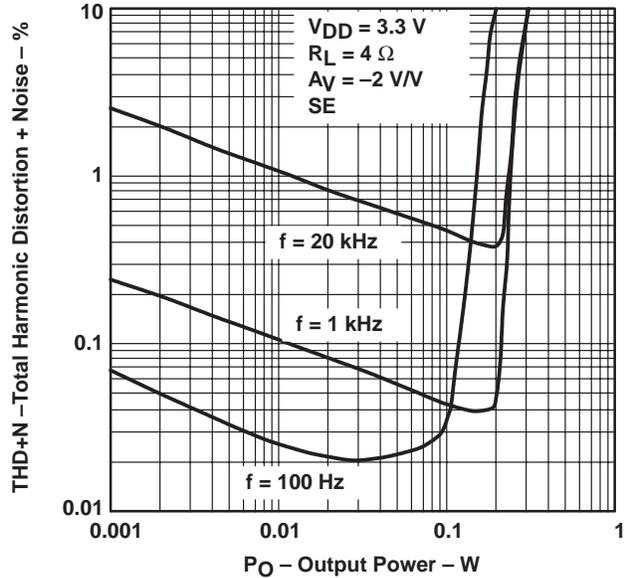
Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
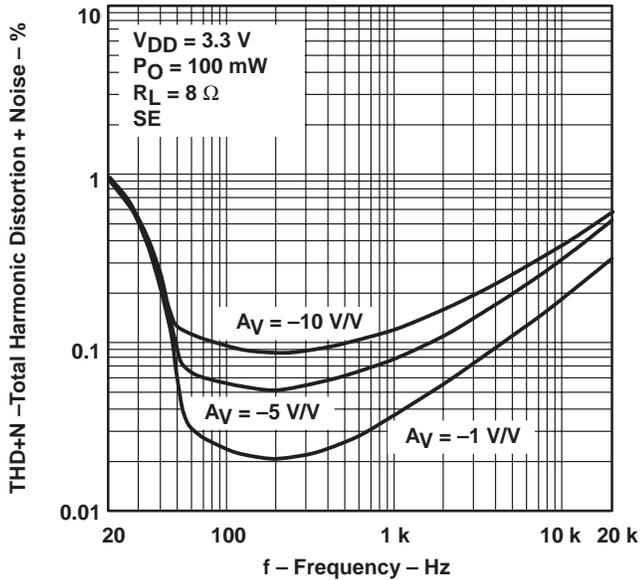
Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
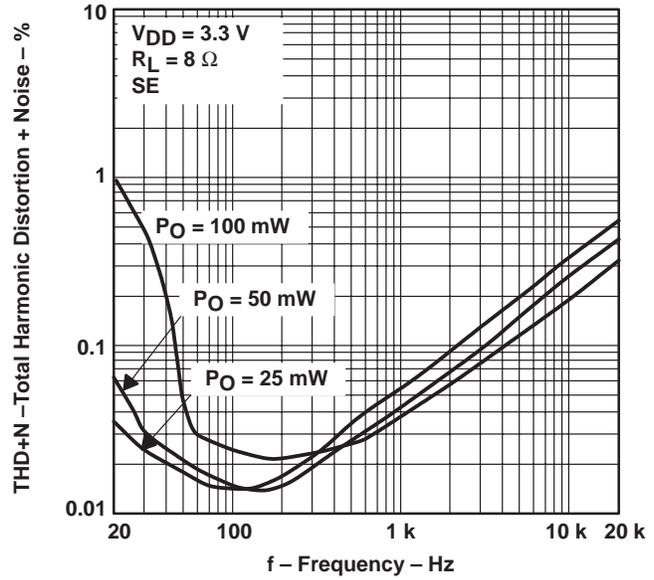
Figure 32

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER
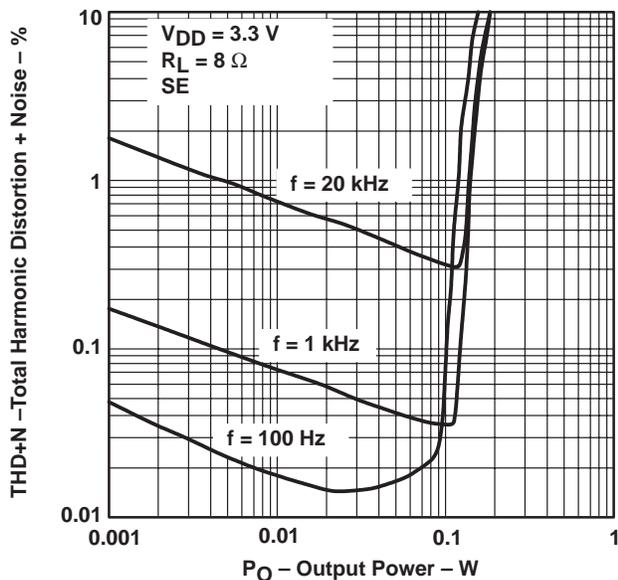
Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
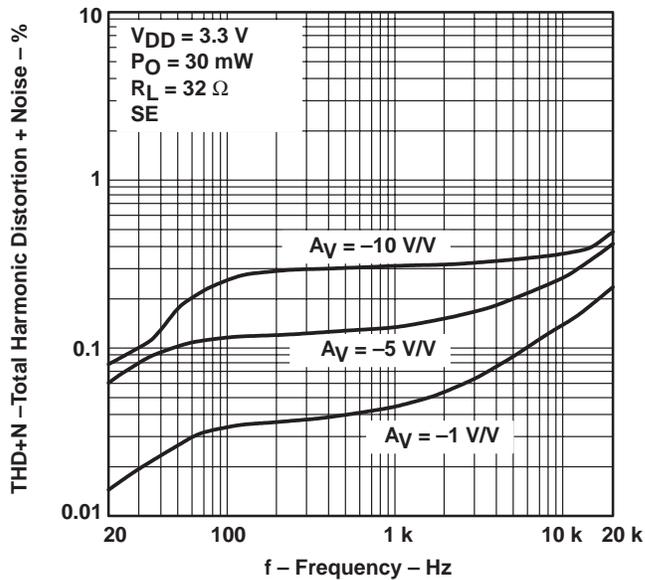
Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY
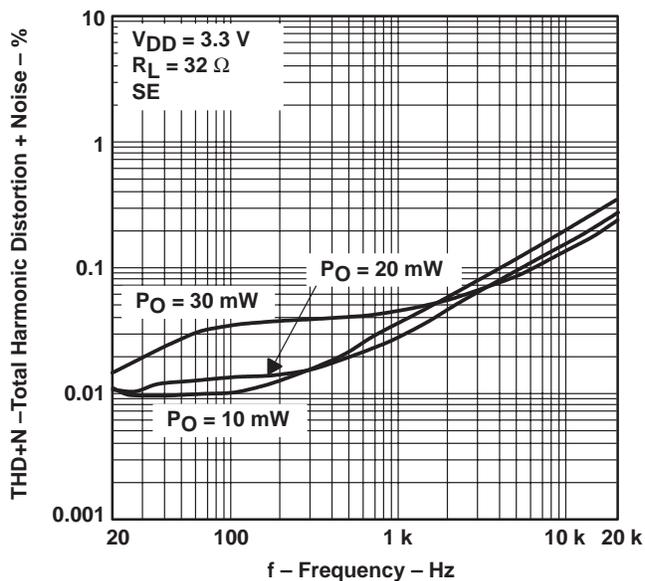
Figure 35

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER
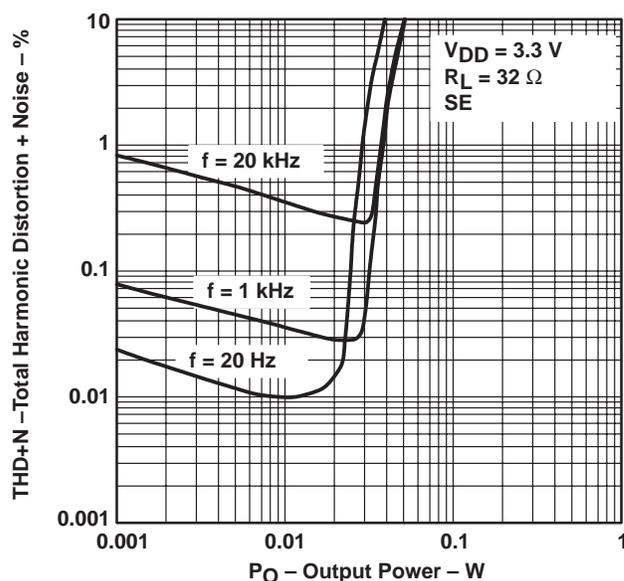
Figure 36

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 37

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 38

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

Figure 39

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY
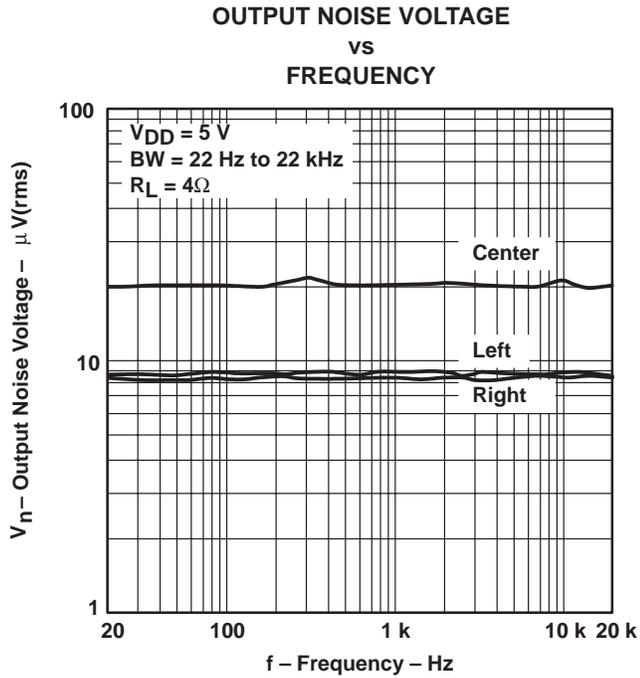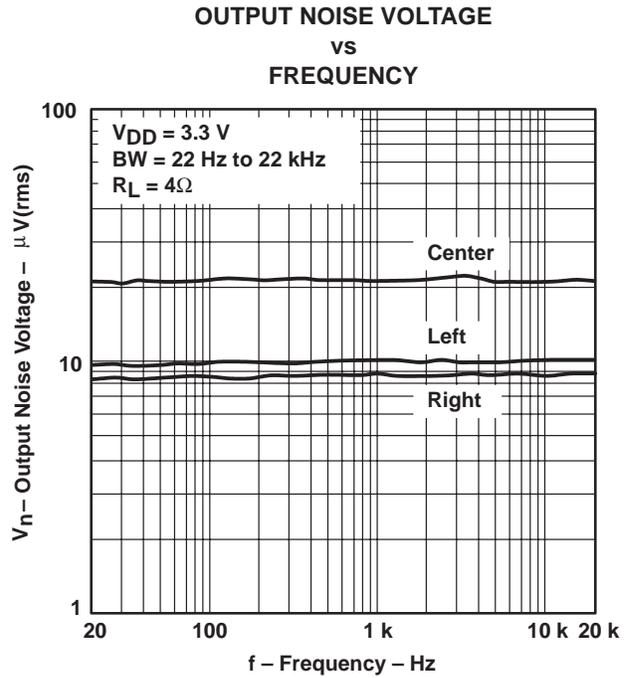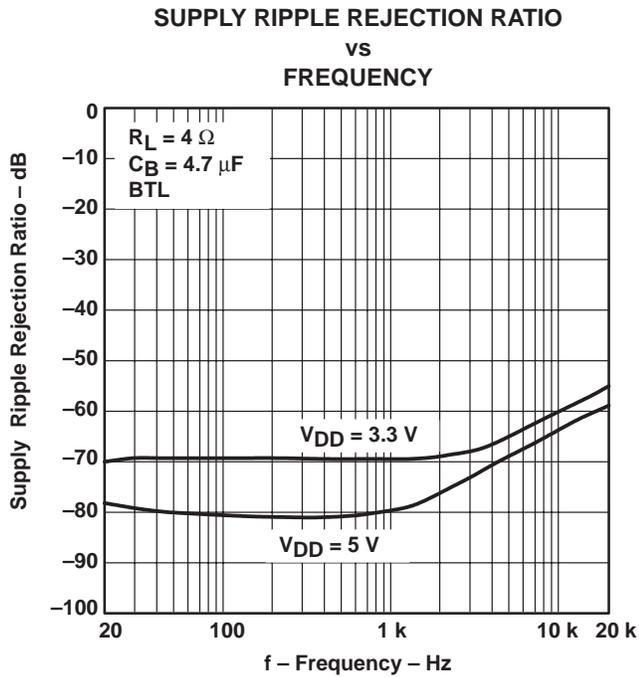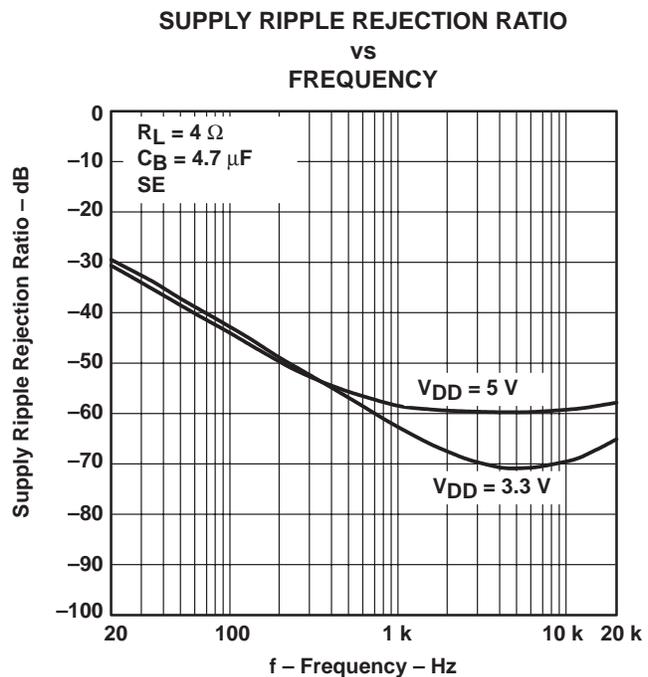
Figure 40

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

V_{DD} = 5 V
P_O = 75 mW
R_L = 32 Ω
SE

Left to Right

Right to Left

Crosstalk – dB

f – Frequency – Hz

Figure 41

CROSSTALK
vs
FREQUENCY

V_{DD} = 3.3 V
P_O = 35 mW
R_L = 32 Ω
SE

Left to Right

Right to Left

Crosstalk – dB

f – Frequency – Hz

Figure 42

OPEN LOOP RESPONSE

V_{DD} = 5 V
BTL

Phase

Gain

Gain – dB

Phase

f – Frequency – kHz

Figure 43

TYPICAL CHARACTERISTICS

OPEN LOOP RESPONSE

Figure 44

CLOSED LOOP RESPONSE

Figure 45

TYPICAL CHARACTERISTICS

CLOSED LOOP RESPONSE

V_{DD} = 3.3 V
A_V = −2 V/V
P_O = 0.75 W
BTL

Figure 46

CLOSED LOOP RESPONSE

V_{DD} = 5 V
A_V = −1 V/V
P_O = 0.5 W
SE

Figure 47

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

CLOSED LOOP RESPONSE

Figure 48

SUPPLY CURRENT vs SUPPLY VOLTAGE

Figure 49

OUTPUT POWER vs SUPPLY VOLTAGE

Figure 50

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

**OUTPUT POWER
vs
SUPPLY VOLTAGE**

THD+N = 1%
SE
Each L/R Channel

R_L = 4 Ω
R_L = 8 Ω
R_L = 32 Ω

P_O – Output Power – W
V_{DD} – Supply Voltage – V

Figure 51

**OUTPUT POWER
vs
LOAD RESISTANCE**

THD+N = 1%
BTL
Center Channel

V_{DD} = 5 V
V_{DD} = 3.3 V

P_O – Output Power – W
R_L – Load Resistance – Ω

Figure 52

**OUTPUT POWER
vs
LOAD RESISTANCE**

THD+N = 1%
SE
Each L/R Channel

V_{DD} = 5 V
V_{DD} = 3.3 V

P_O – Output Power – W
R_L – Load Resistance – Ω

Figure 53

**POWER DISSIPATION
vs
OUTPUT POWER**

R_L = 4 Ω
R_L = 8 Ω

V_{DD} = 5 V
BTL
Center Channel

P_D – Power Dissipation – W
P_O – Output Power – W

Figure 54

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
OUTPUT POWER

$R_L = 4 \, \Omega$

$R_L = 8 \, \Omega$

$R_L = 32\Omega$

$V_{DD} = 5 \, V$
SE
Each L/R Channel

P_D – Power Dissipation – W

P_O – Output Power – W

Figure 55

POWER DISSIPATION
vs
OUTPUT POWER

$R_L = 4 \, \Omega$

$R_L = 8 \, \Omega$

$V_{DD} = 3.3 \, V$
BTL
Center Channel

P_D – Power Dissipation – W

P_O – Output Power – W

Figure 56

POWER DISSIPATION
vs
OUTPUT POWER

$V_{DD} = 3.3V$
SE
Each L/R Channel

$R_L = 4 \, \Omega$

$R_L = 8 \, \Omega$

$R_L = 32\Omega$

P_D – Power Dissipation – W

P_O – Output Power – W

Figure 57

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 58) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultra-thin, fine-pitch, surface-mount package can be reliably achieved.

Side View (a)

End View (b)

Bottom View (c)
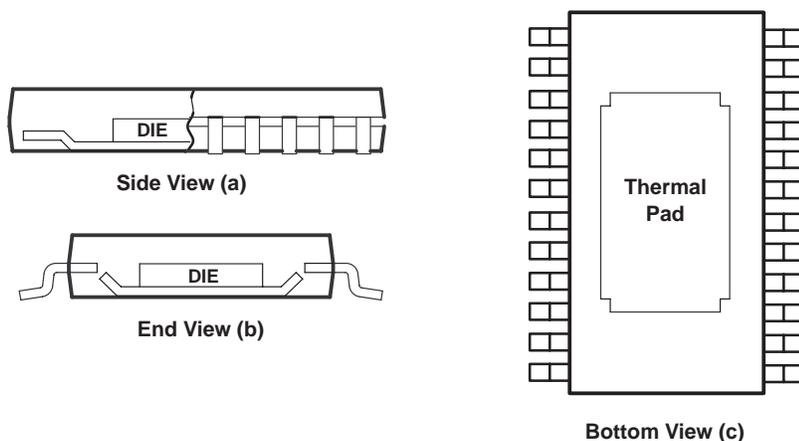
Figure 58. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

bridged-tied load versus single-ended mode

Figure 59 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA0103 center -channel BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$Power = \frac{V_{(rms)}^2}{R_L}$$

(1)
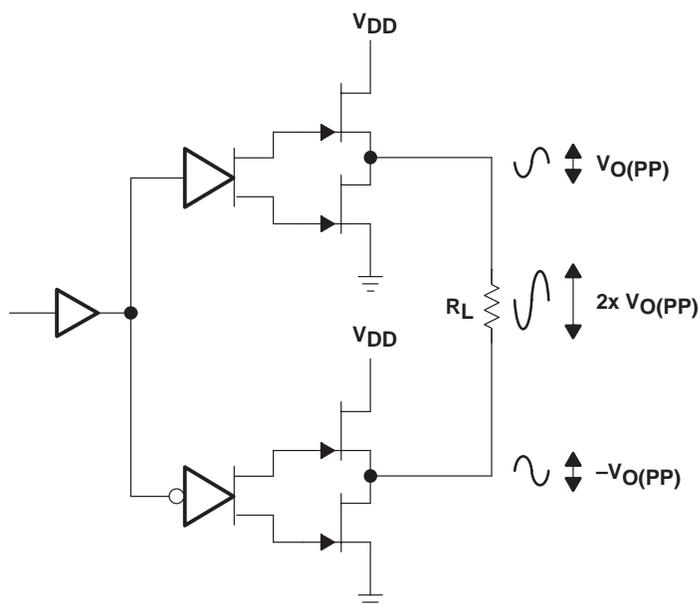
Figure 59. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power that is a 6-dB improvement — which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration of the L/R channels as shown in Figure 60. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

APPLICATION INFORMATION

$$f_C = \frac{1}{2\pi R_L C_C}$$ (2)

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.
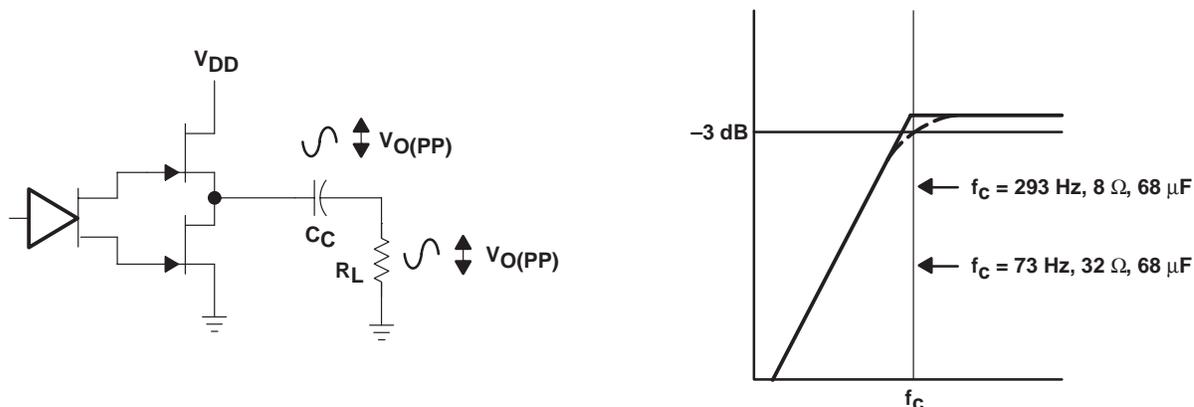
Figure 60. Single-Ended Configuration and Frequency Response

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 61).
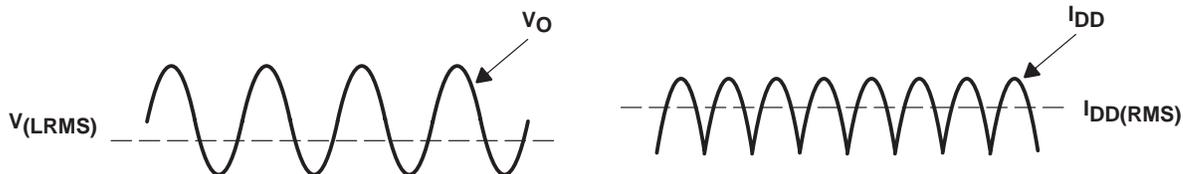
Figure 61. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \tag{3}$$

Where:

$$P_{L(BTL)} = \frac{V_L rms^2}{R_L} = \frac{V_{PP}^2}{2R_L}, \quad V_{PP} = \sqrt{P_L R_L 2}$$

$$V_L rms(BTL) = \frac{V_{PP}}{2\sqrt{2}} \times 2 = \frac{V_{PP}}{\sqrt{2}}$$

$$P_{SUP} = V_{DD} I_{DD} rms = \frac{V_{DD} V_{PP}}{\pi R_L}$$

$$I_{DD} rms = \frac{V_{PP}}{\pi R_L}$$

$V_{PP} = 2V_P$

$2V_{PP} = V_L$

$-V_{PP}$
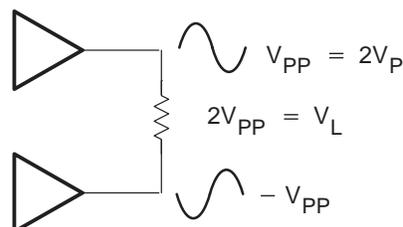
$$\text{Efficiency of a BTE Configuration} = \frac{P_L}{P_{SUP}} = \frac{V_{PP}^2}{2R_L} \times \frac{\pi R_L}{V_{DD}V_{PP}} = \frac{V_{PP}\pi}{2V_{DD}} = \frac{\pi\sqrt{2P_L R_L}}{2V_{DD}} \tag{4}$$

Equation 4 can also be used for SE operations.

Table 1 employs equation 4 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 1. Efficiency Vs Output Power in 5-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47[†]	0.53

[†] High peak voltages cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up. As the numerator values of R_L and P_L decrease, efficiency decreases.

TEXAS INSTRUMENTS

APPLICATION INFORMATION

For example, if the 5-V supply is replaced with a 3.3-V supply (TPA0103 has a maximum recommended V_{DD} of 5.5 V) in the calculations of Table 1 then efficiency at 0.5 W would rise from 44% to 67% and internal power dissipation would fall from 0.62 W to 0.25 W at 5 V. Then for a stereo 0.5-W system from a 3.3-V supply, the maximum draw would only be 1.5 W as compared to 2.24 W from 5 V. In other words, use the efficiency analysis to chose the correct supply voltage and speaker impedance for the application.

selection of components

Figure 62 and Figure 63 are a schematic diagrams of typical computer application circuits.
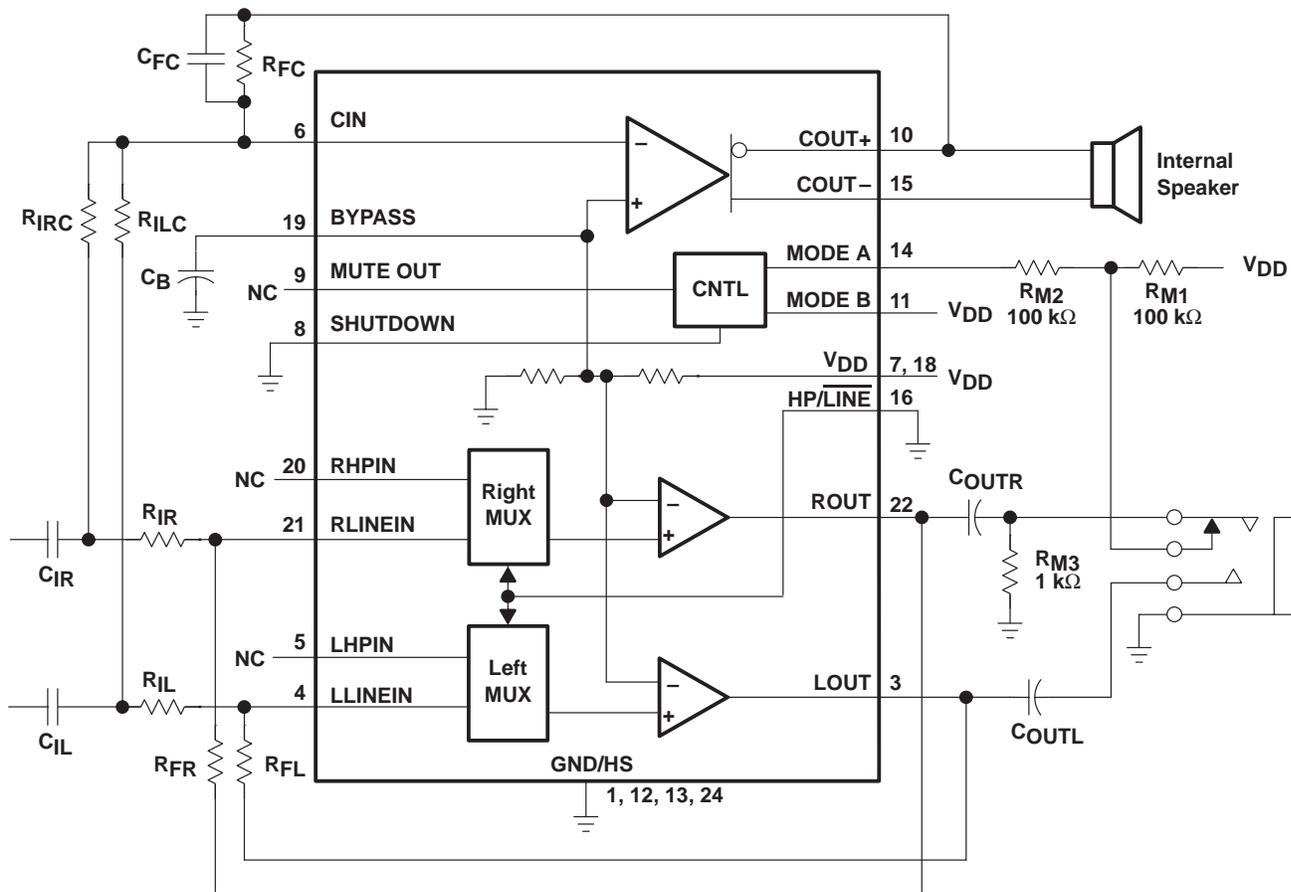
Figure 62. TPA0103 Minimum Configuration Application Circuit

APPLICATION INFORMATION

NOTE A: This connection is for ultralow current in shutdown mode.

Figure 63. TPA0103 Full Configuration Application Circuit

APPLICATION INFORMATION

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA0103 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 6. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = -\left(\frac{R_F}{R_I}\right) \tag{6}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA0103 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values are required for proper startup operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 7.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{7}$$

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 8.

$$f_{c(\text{lowpass})} = \frac{1}{2\pi R_F C_F} \tag{8}$$
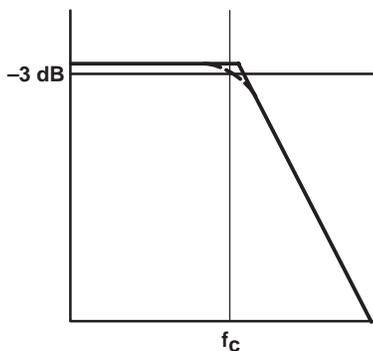
For example, if R_F is 100 kΩ and Cf is 5 pF then f_c is 318 kHz, which is well outside of the audio range.

APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 9.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I}$$
(9)
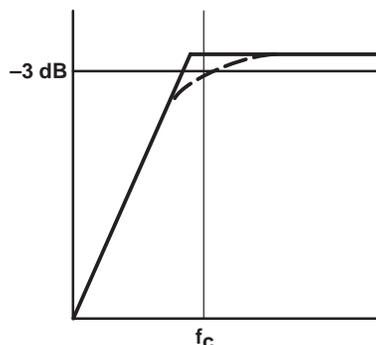
The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 10.

$$C_I = \frac{1}{2\pi R_I f_c}$$
(10)

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA0103 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

APPLICATION INFORMATION

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, serves several important functions. During startup or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 25-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 11 should be maintained.

$$\frac{1}{\left(C_B \times 25 \text{ k}\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \tag{11}$$

As an example, consider a circuit where C_B is 0.1 µF, C_I is 0.22 µF and R_I is 10 kΩ. Inserting these values into the equation 10 we get $400 \leq 454$ which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 12.

$$f_{c(high)} = \frac{1}{2\pi R_L C_C} \tag{12}$$
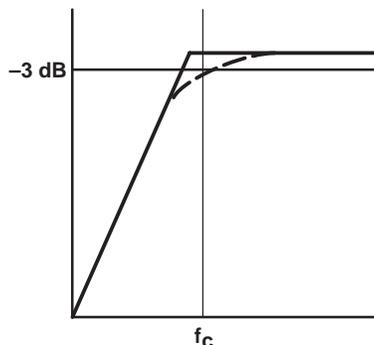
The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 4 Ω, 8 Ω, 32 Ω, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

APPLICATION INFORMATION

output coupling capacitor, C_C (continued)

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
4 Ω	330 μF	120 Hz
8 Ω	330 μF	60 Hz
32 Ω	330 μF	15 Hz
47,000 Ω	330 μF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the relationship shown in equation 13.

$$\frac{1}{\left(C_B \times 25 \ k\Omega\right)} \leq \frac{1}{\left(C_I R_I\right)} \ll \frac{1}{R_L C_C} \tag{13}$$

mode control resistor network, R_{M1}, R_{M2}, R_{M3}

Using a readily available 1/8-in. (3.5-mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider (see Figure 64) pulls the MODE A input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the MODE A input is pulled high. When the input goes high, the center BTL amplifier is shutdown causing the speaker to mute. The SE amplifiers then drive through the output capacitors (C_O) into the headphone jack.

Input MUX operation

The HP/$\overline{\text{LINE}}$ MUX feature gives the audio designer the flexibility of a multichip design in a single IC (see Figure 64). The primary function of the MUX is to allow different gain settings for different types of audio loads. Speakers typically require approximately a factor of 10 more gain for similar volume listening levels as compared to headphones. To achieve headphone and speaker listening parity, the resistor values would need to be set as follows:

$$\text{Gain}_{(HP)} \ = \ - \left(\frac{R_{F(HP)}}{R_{I(HP)}}\right) \tag{14}$$

If, for example $R_{I(HP)} = 20 \ k\Omega$ and $R_{F(HP)} = 20 \ k\Omega$ then SE Gain$_{(HP)} = -1$

$$\text{Gain}_{(LINE)} \ = \ - \left(\frac{R_{F(LINE)}}{R_{I(LINE)}}\right) \tag{15}$$

If, for example $R_{I(LINE)} = 10 \ k\Omega$ and $R_{F(LINE)} = 100 \ k\Omega$ then Gain$_{(LINE)} = -10$

![Texas Instruments logo]
TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

APPLICATION INFORMATION

Input MUX operation (continued)
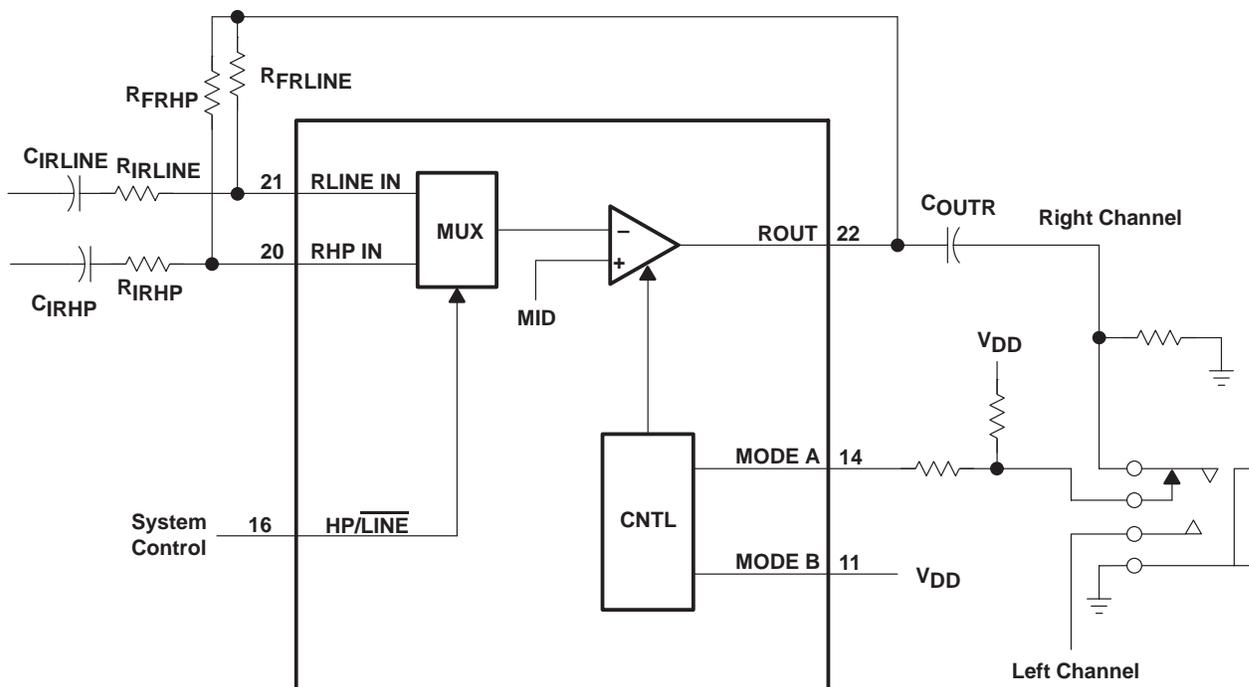
Figure 64. TPA0103 Example Input MUX Circuit

Another advantage of using the MUX feature is setting the gain of the headphone channel to –1. This provides the optimum distortion performance into the headphones where clear sound is more important.

mute and shutdown modes

The TPA0103 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The SHUTDOWN input terminal should be held low during normal operation when the amplifier is in use. Pulling SHUTDOWN high causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD} = 5 \, \mu A$. SHUTDOWN should never be left unconnected because amplifier operation would be unpredictable. Mute mode alone reduces $I_{DD} < 1 \, mA$.

APPLICATION INFORMATION

mute and shutdown modes (continued)

Table 3. Shutdown and Mute Mode Functions

INPUTS†				OUTPUT	AMPLIFIER STATE	
MODE A	HP/$\overline{\text{LINE}}$	MODE B	SHUTDOWN	MUTE OUT	INPUT	OUTPUT
Low	Low	Low	Low	Low	L/R Line	3 Channel
X	X	—	High	High	X	Mute
X	X	High	Low	High	X	Mute
Low	High	Low	Low	Low	L/R HP	3 Channel
High	Low	Low	Low	High	L/R Line	Mute
High	High	Low	Low	High	L/R HP	Mute
Low	Low	High	Low	Low	L/R Line	Center BTL
Low	High	High	Low	Low	L/R HP	Center BTL
High	Low	High	Low	Low	L/R Line	L/R SE
High	High	High	Low	Low	L/R HP	L/R SE

† Inputs should never be left unconnected.
X = do not care

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

5-V versus 3.3-V operation

The TPA0103 operates over a supply range of 3 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability goes. For 3.3-V operation, supply current is reduced from 19 mA (typical) to 13 mA (typical). The most important consideration is that of output power. Each amplifier in TPA0103 can produce a maximum voltage swing of $V_{DD} - 1$ V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)} = 2.3$ V as opposed to $V_{O(PP)} = 4$ V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies. When the application demands less than 500 mW, 3.3-V operation should be strongly considered, especially in battery-powered applications.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

APPLICATION INFORMATION

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA0103 data sheet, one can see that when the TPA0103 is operating from a 5-V supply into a 4-Ω speaker that 2 W RMS levels are available. Converting watts to dB:

$$P_{dB} = 10 Log \left(\frac{P_W}{P_{ref}}\right)$$
$$= 10 Log \left(\frac{2}{1}\right)$$
$$= 3 \ dB$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$3 \ dB - 15 \ dB = -12 \ dB \ (15 \ dB \ headroom)$$

Converting dB back into watts:

$$P_W = 10^{P_{dB}/10} \times P_{ref}$$
$$P_W = -12 \ dB = 63 \ mW \ (15 \ dB \ headroom)$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 1.5 W of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 4-Ω system, the internal dissipation in the TPA0103 and maximum ambient temperatures is shown in Table 4.

Table 4. TPA0103 Power Rating, 5-V, 4-Ω, Three Channel

CONFIGURATION	HEADROOM[†]	POWER DISSIPATION			T_A (MAX)[‡]	
		2 × L/R + CENTER = TOTAL			35°C/W	25°C/W
Center only, P_O = 2 W max	0 dB	0	1.25 W	1.25 W	81°C	93°C
	15 dB	0	0.6 W	0.6 W	104°C	110°C
L/R only, P_O = 500 mW max	0 dB	0.6 W	0	1.2 W	83°C	95°C
	15 dB	0.2 W	0	0.4 W	111°C	115°C
Center, P_O = 2 W max and L/R , P_O = 500 mW max	0 dB	0.6 W	1.25 W	2.45 W	39°C	63°C
	15 dB	0.2 W	0.6 W	1 W	90°C	100°C

† The 2 W max at 0 dB is a maximum level tone that is very loud. 15 dB is a typical headroom requirement for music.
‡ This parameter is based on a maximum junction temperature (T_J) of 125°C.

APPLICATION INFORMATION

headroom and thermal considerations (continued)

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP†	2.7 W	21.8 mW/°C	1.7 W	1.4 W
PWP‡	2.8 W	22.1 mW/°C	1.8 W	1.4 W

† This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 4 in² 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage.

‡ This parameter is measured with the recommended copper heat sink pattern on an 8-layer PCB, 6.9 in² 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²).

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 LFM and 300 LFM data from the dissipation rating table, the derating factor for the PWP package with 6.9 in² of copper area on a multilayer PCB is 22.1 mW/°C and 53.7 mW/°C respectively. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}}$$

For 0 LFM :

$$= \frac{1}{22.1 \text{ mW/°C}}$$

$$= 45°C/W$$

For 300 LFM :

$$= \frac{1}{53.7 \text{ mW/°C}}$$

$$= 18°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for the two SE channels and added to the center channel dissipation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0103 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D$$

$$= 125 - 45(0.2 \times 2 + 0.6) = 80°C \text{ (15 dB headroom, 0 LFM)}$$

$$= 125 - 18(0.2 \times 2 + 0.6) = 107°C \text{ (15 dB headroom, 300 LFM)}$$

NOTE:
Internal dissipation of 1 W is estimated for a 3-channel system with 15 dB headroom per channel (see Table 4 for more information).

Table 4 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA0103 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. However, sustained operation above 125°C is not recommended. Table 4 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

![Texas Instruments logo]

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA0103PWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-	TPA0103
TPA0103PWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPA0103PWP	TPA0103
TPA0103PWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-	TPA0103
TPA0103PWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	See TPA0103PWPR	TPA0103

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
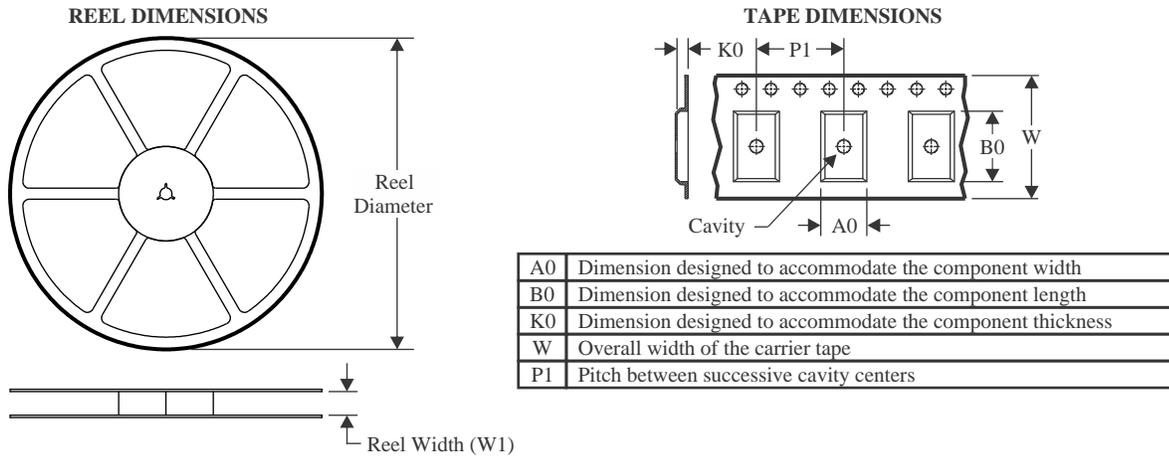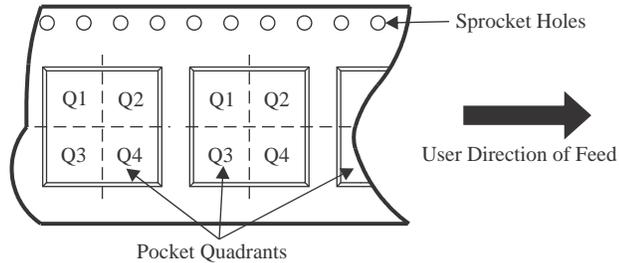
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0103PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0103PWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TUBE
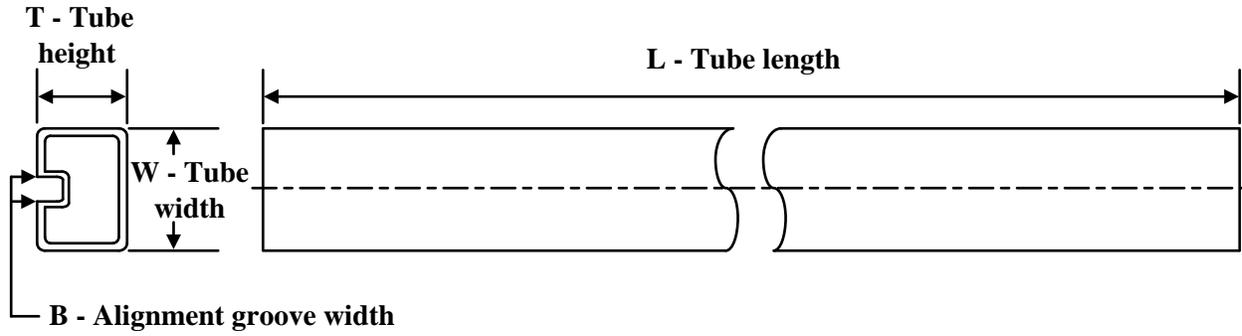
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA0103PWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
TPA0103PWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5

PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
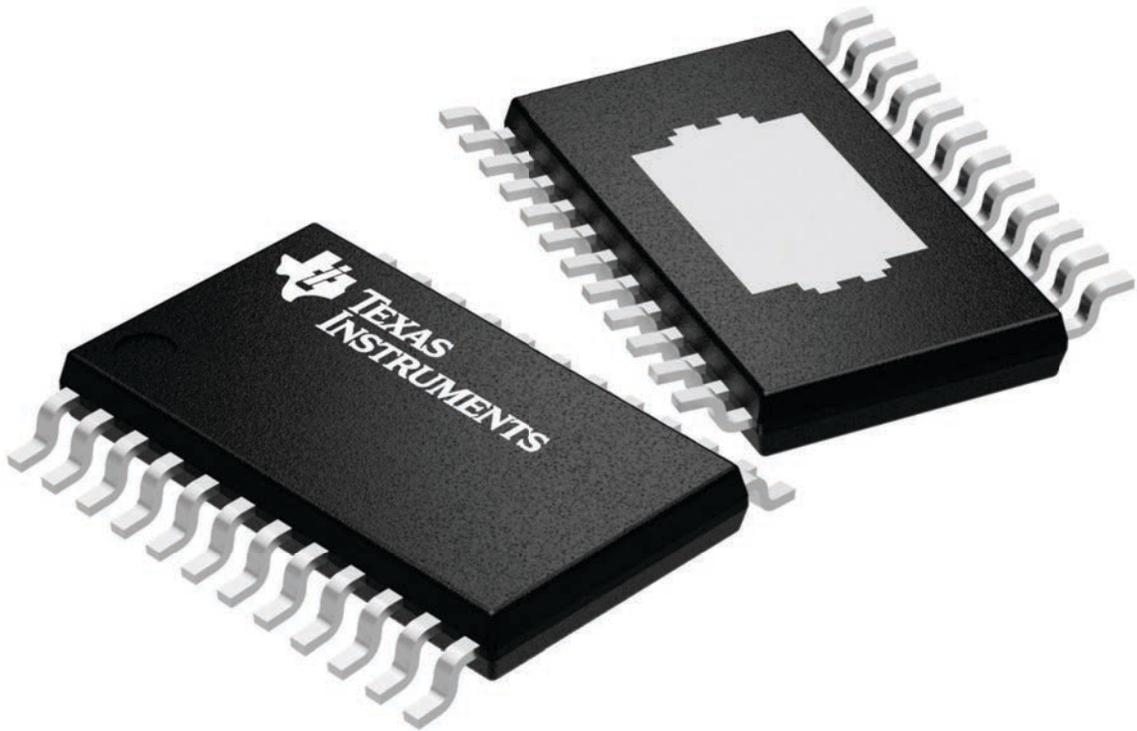
4224742/B

PWP (R−PDSO−G24)   PowerPAD™ PLASTIC SMALL OUTLINE
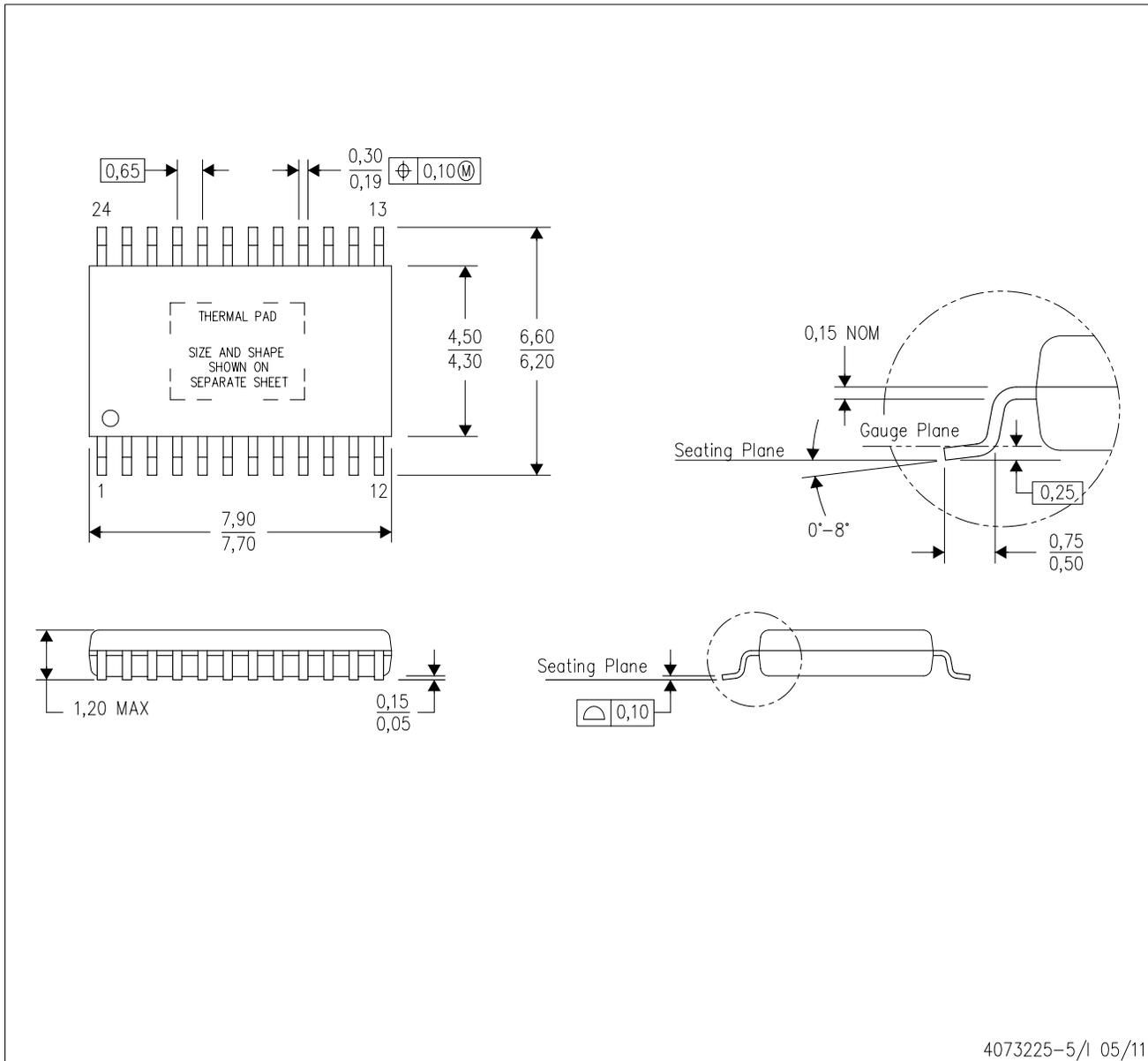
4073225−5/I 05/11

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad
            Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
            recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        E. Falls within JEDEC MO−153

PowerPAD is a trademark of Texas Instruments.

PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Top View

Exposed Thermal Pad Dimensions
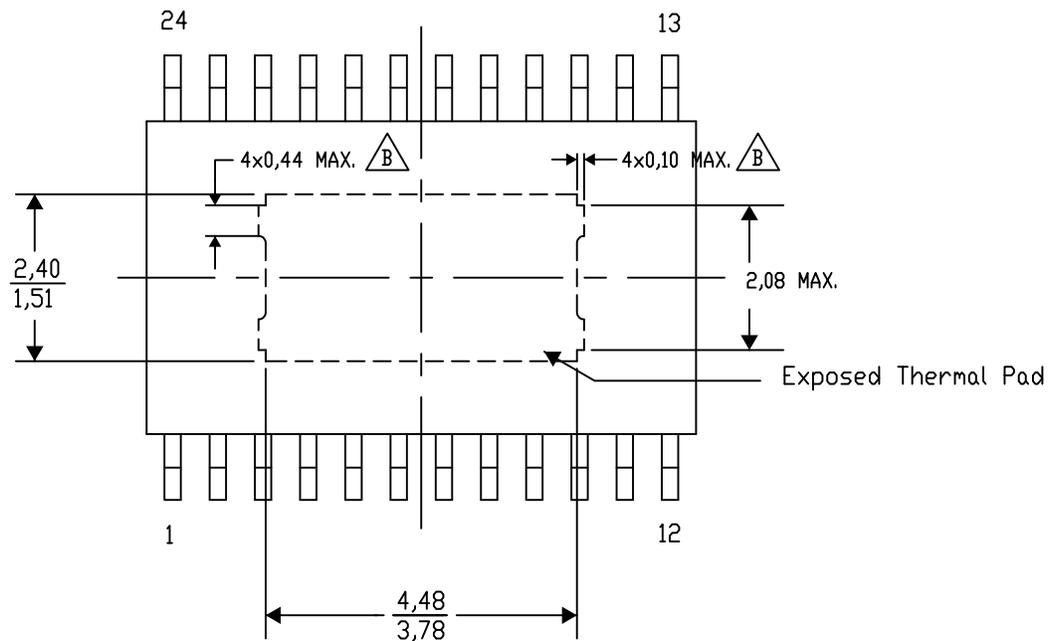
4206332–42/AO 01/16

NOTE: A. All linear dimensions are in millimeters

  B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

Texas
INSTRUMENTS
www.ti.com
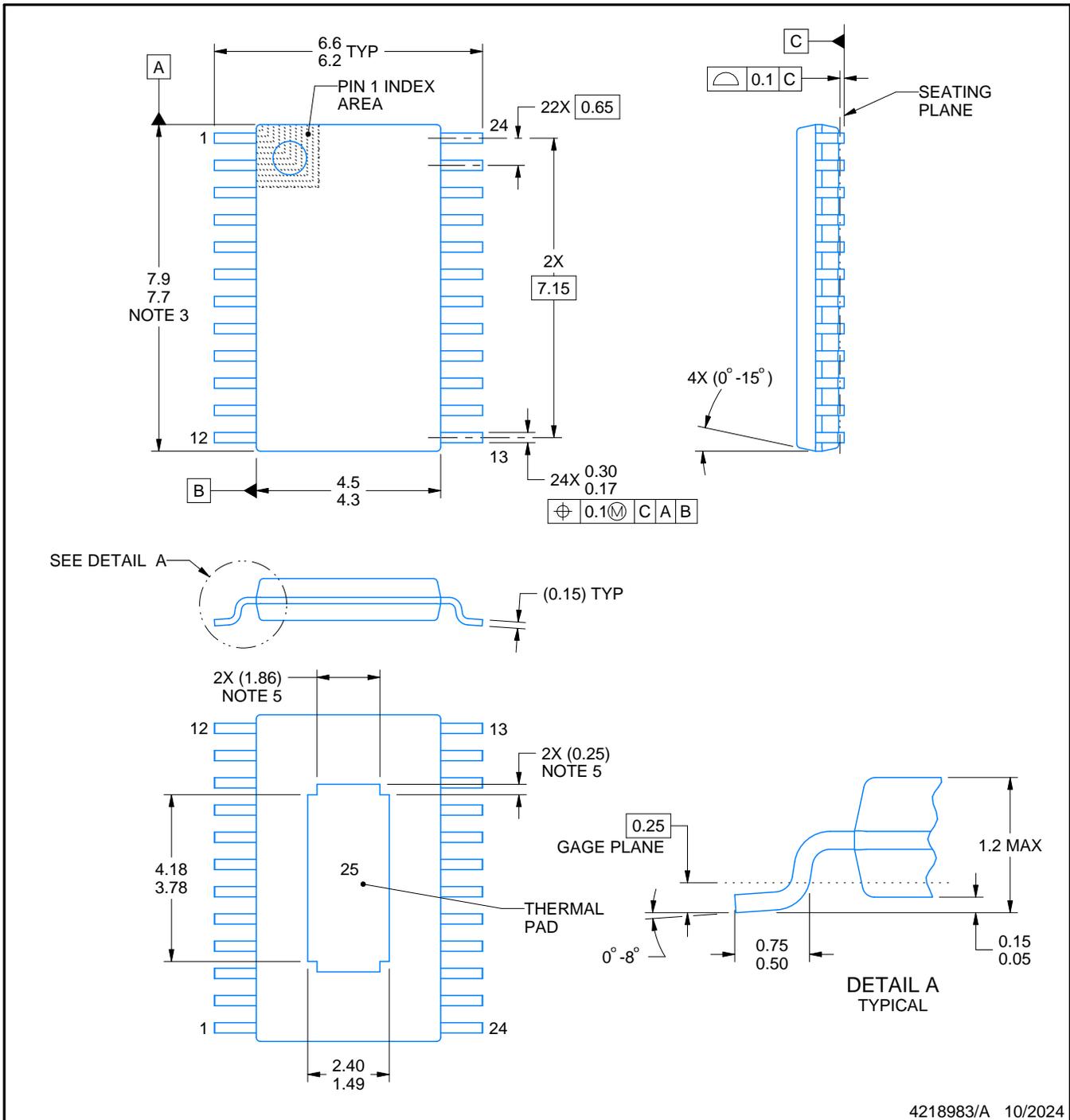
4218983/A   10/2024
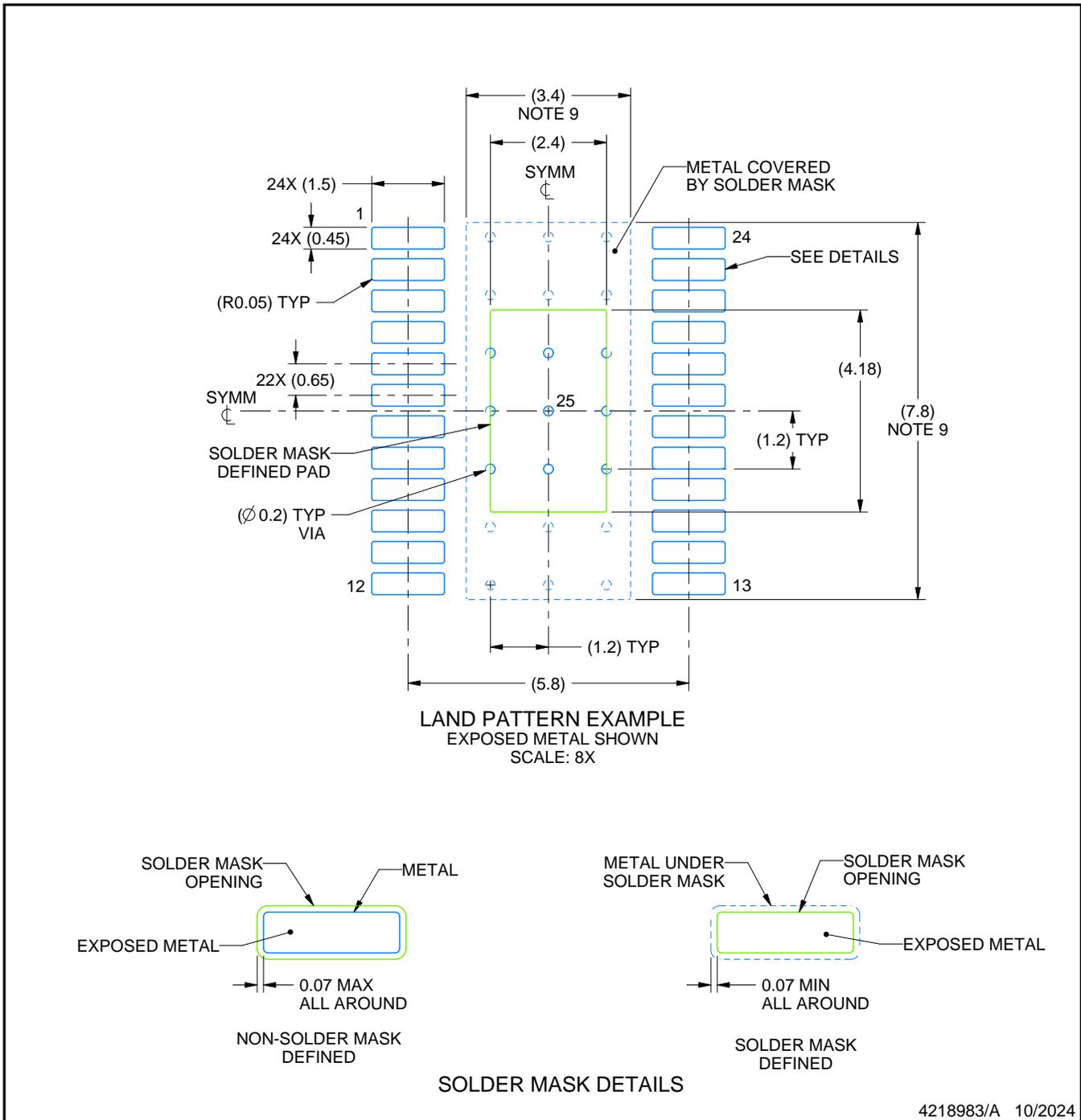
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

PWP0024A

(3.4)
NOTE 9

(2.4)
SYMM

24X (1.5)

1

24X (0.45)

(R0.05) TYP

METAL COVERED
BY SOLDER MASK

24

SEE DETAILS

22X (0.65)

SYMM

25

SOLDER MASK
DEFINED PAD

(Ø 0.2) TYP
VIA

(4.18)

(7.8)
NOTE 9

(1.2) TYP

12

13

(1.2) TYP

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

**NON-SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ALL AROUND

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS

4218983/A   10/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
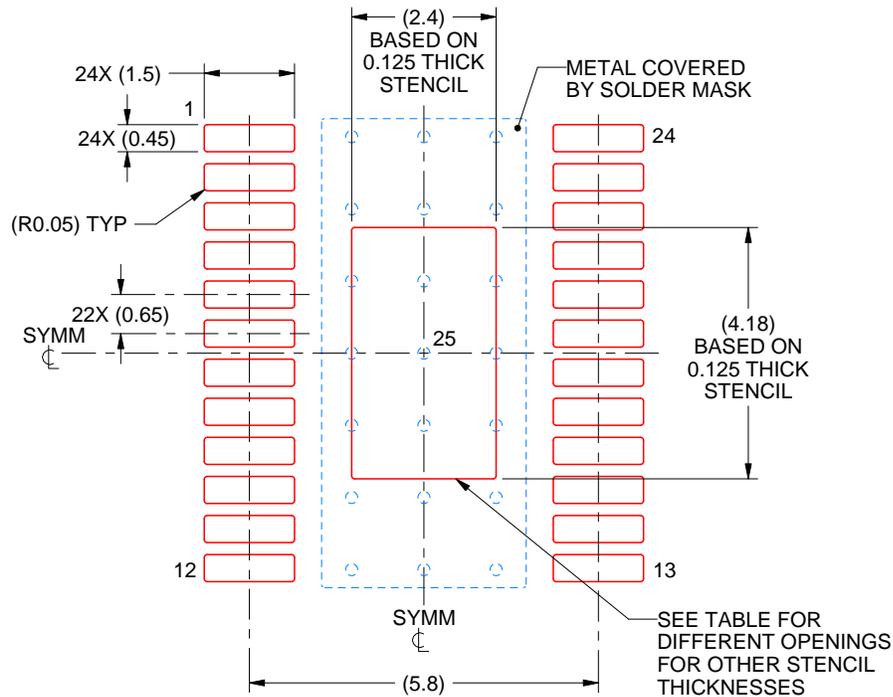
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 4.67
0.125	2.40 X 4.18 (SHOWN)
0.15	2.19 X 3.82
0.175	2.03 X 3.53

4218983/A   10/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER