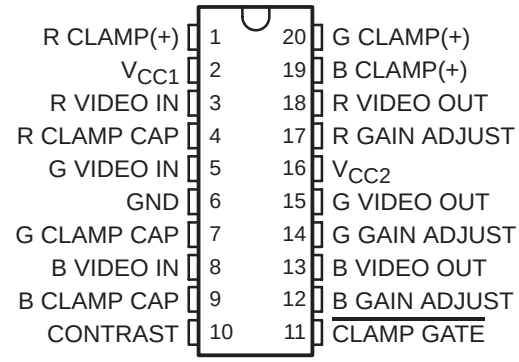
- **Wide Bandwidth . . . Typ 100 MHz at −3 dB**
- **Three Channels**
- **0 V to 4 V, Digital Level-Contrast Control**
- **0 V to 4 V, Digital Level-Gain Adjust Control**
- **20-Pin Plastic DIP for Small PCB Area Required**
- **Fewer Peripheral Components Required Than for LM1203 Applications**
- **Independent CLAMP(+) Adjustment to Each Channel**

N PACKAGE
(TOP VIEW)

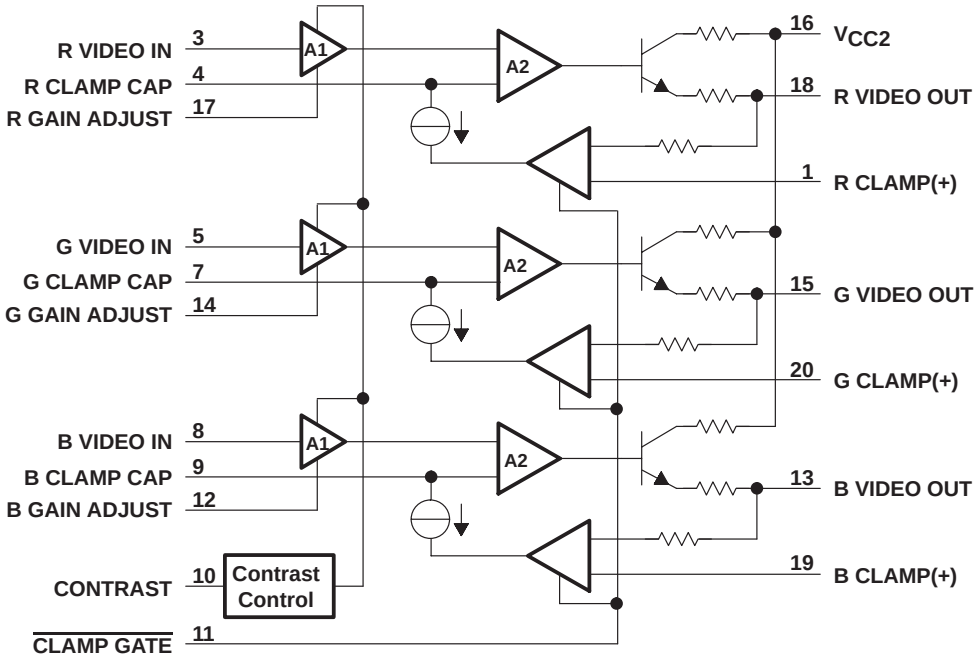


description

The TLS1233 is a 100-MHz wide-band video preamplifier system intended for mid-to-high-resolution RGB (red-green-blue) color monitors. Each video amplifier (R, G, and B) contains a gain set for adjusting maximum system gain (A_V = 7.8 V/V). The TLS1233 provides digital level-operated contrast, brightness, and gain adjustment control. All the control inputs offer high input impedance and an operation range from 0 V to 4 V for easy interface to the serial digital buses. Provided in a 20-pin plastic dual-in-line package (DIP), the TLS1233 integrates most of the external components required to accommodate the video system.

The TLS1233 operates from a 12-V supply and contains an internal input bias voltage. Also, the TLS1233 contains the feedback resistor required between output and CLAMP(−) for dc level holding. The device is characterized for operation from 0°C to 70°C.

functional block diagram

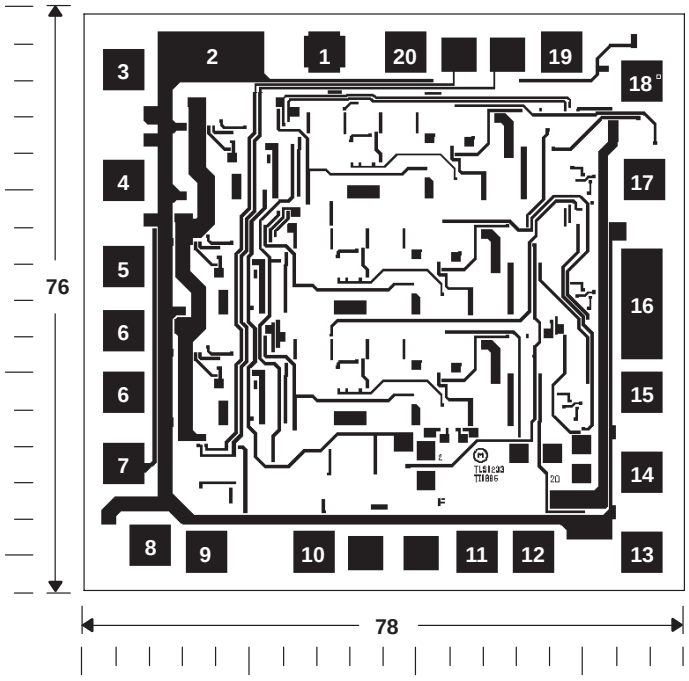


TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251−1443

TLS1233Y chip information

This chip, when properly assembled, displays characteristics similar to the TLS1233. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS



CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	13.5 V
Input voltage range, V_I (see Note 1)	0 V to V_{CC}
Video output current, I_O (per channel)	28 mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	1.87 W
Operating virtual junction temperature range, T_J	−55°C to 150°C
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All V_{CC} terminals must be externally wired together to prevent internal damage during V_{CC} power-on/-off cycles.

2. For operation above 25°C free-air temperature, derate linearly from 1.87 W (T_A = 25°C) to 1.2 W (T_A = 70°C). This equates to a derating factor of 15 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1} and V_{CC2}		11	12	13	V
High-level input voltage range, $\overline{\text{CLAMP GATE}}$, V_{IH}	Clamp comparators off	2.4		5	V
Low-level input voltage range, $\overline{\text{CLAMP GATE}}$, V_{IL}	Clamp comparators on	0		0.8	V
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at 25°C free-air temperature range, $\overline{\text{CLAMP GATE}}$ = 0 V, CLAMP(+) = 2 V, CONTRAST = R,G,B GAIN ADJUST = 4 V, V_{CC1} = V_{CC2} = 12 V (see Figure 2) (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current		$V_{CC1} + V_{CC2}$		84	94	mA
V_{ref}	Video input reference voltage		Measure R/G/B video input	2.1	2.3	2.5	V
I_I	Contrast and R,G,B GAIN ADJUST input current		Measure CONTRAST, R/G/B GAIN ADJUST		−0.5	-10	µA
I_{IL}	Clamp gate low input current		$\overline{\text{CLAMP GATE}}$ = 0 V		−0.5	−2.4	µA
I_{IH}	Clamp gate high input current		$\overline{\text{CLAMP GATE}}$ = 12 V		0.005	1	µA
	Clamp capacitor charge current	$I_{K(chg)}$	R,G,B CLAMP CAP = 0 V		1		mA
	Clamp capacitor discharge current	$I_{K(dschg)}$	R,G,B CLAMP CAP = 5 V		−1		mA
V_{OL}	Low-level output voltage		R,G,B CLAMP CAP = 0 V		0.3		V
V_{OH}	High-level output voltage		R,G,B CLAMP CAP = 5 V		7.8		V
$V_{O(diff)}$	Output voltage difference	$V_{O(diff)}$	Between any two channels		±0.5	±50	mV

operating characteristics at 25°C free-air temperature, $\overline{\text{CLAMP GATE}}$ = 0 V, CLAMP(+) = 4 V, CONTRAST = R,G,B GAIN ADJUST = 4 V, f_I = 10 kHz, V_{CC1} = V_{CC2} = 12 V (unless otherwise noted)

PARAMETER		ALTERNATE SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{V(max)}$	Maximum voltage amplification	A_{VMAX}	CONTRAST = 4 V, V_{IPP} = 700 mV		7.8		V/V
$A_{V(mid)}$	Midrange voltage amplification	A_{VMID}	CONTRAST = 2 V, V_{IPP} = 700 mV		2		V/V
	Contrast voltage for minimum amplification	$V_{CONT-LOW}$	$V_{I(PP)}$ = 1 V, See Note 3		1		V
	Amplification match at $A_{V(max)}$	$A_{Vmax(diff)}$	CONTRAST = 4 V, See Note 4		±0.2		dB
	Amplification match at $A_{V(mid)}$	$A_{Vmid(diff)}$	CONTRAST = 2 V, See Note 3		±0.2		dB
	Amplification match at $A_{V(low)}$	$A_{Vlow(diff)}$	CONTRAST = $V_{CONT-LOW}$, See Note 3 and 4		±0.2		dB
THD	Total harmonic distortion		CONTRAST = 1 V, V_{IPP} = 1 V		0.5		%
BW	Amplifier bandwidth	BW(−3 dB)	CONTRAST = 4 V, See Notes 5 And 7		100		MHz
	Crosstalk attenuation	a_X	CONTRAST = 4 V, f = 10 kHz, See Note 6		60		dB
			CONTRAST = 4 V, See Notes 6 or 7 f = 10 MHz,		40		dB
	Pulse test for rise time	t_r	CONTRAST = 4 V, CLAMP(+) = 2 V, $V_{O(PP)}$ = 4 V See Notes 5 and 7		3		ns
	Pulse test for fall time	t_f			4		ns

NOTES: 3. Determine $V_{CONT-LOW}$ for −40 dB attenuation of output. Reference to $A_{V(max)}$.
4. Measure gain difference between any two amplifiers, $V_{I(PP)}$ = 1 V.
5. Adjust input frequency from 10 kHz ($A_{V(max)}$ reference level) to the −3-dB corner frequency (f −3 dB). $V_{I(PP)}$ = 700 mV.
6. $V_{I(PP)}$ = 700 mV at f = 10 kHz to any amplifier. Measure output levels of the other two undriven amplifiers relative to driven amplifier.
7. A special text fixture without a socket and a double-sided full-ground-plane PC board are required.

PARAMETER MEASUREMENT INFORMATION

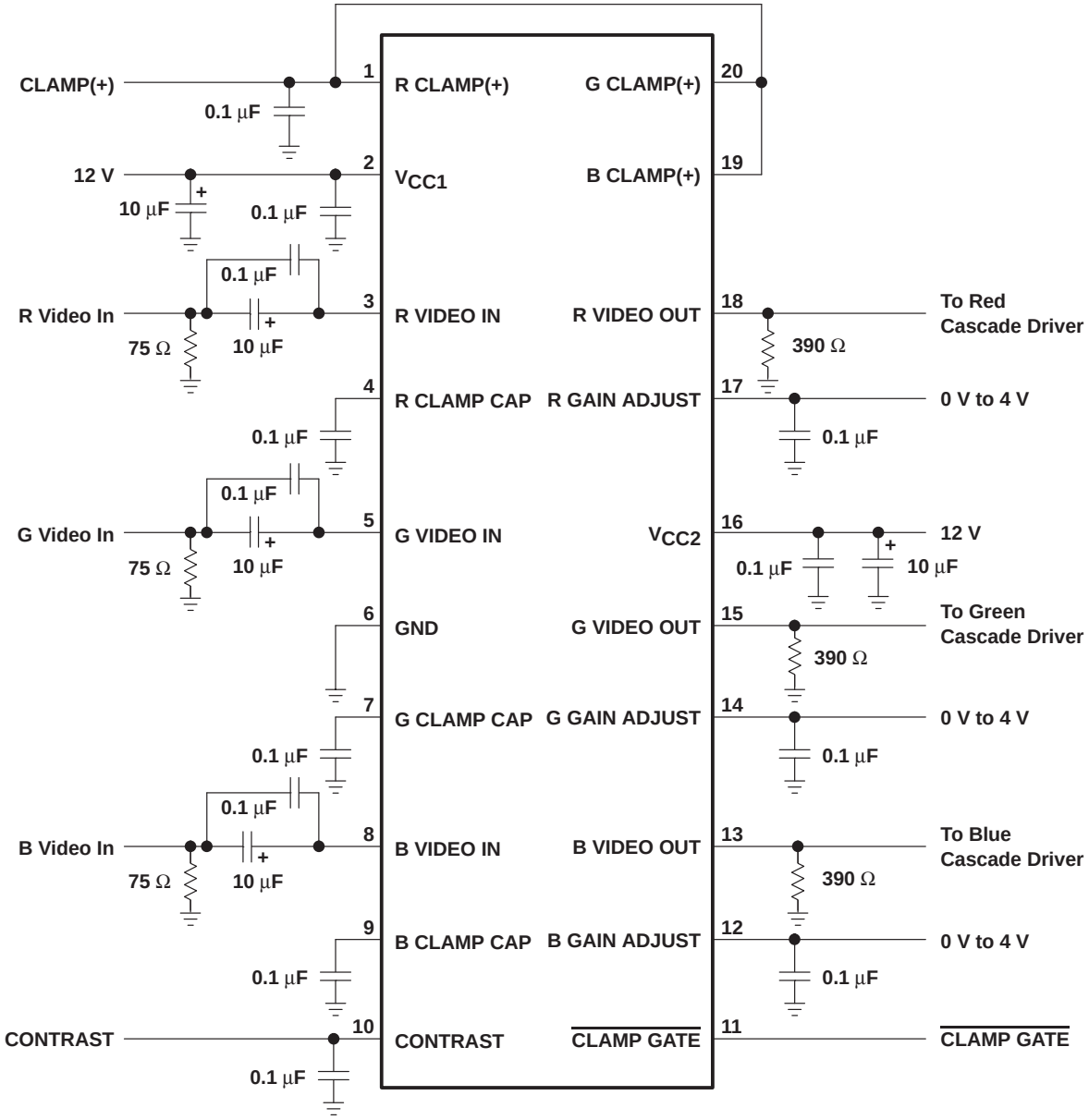
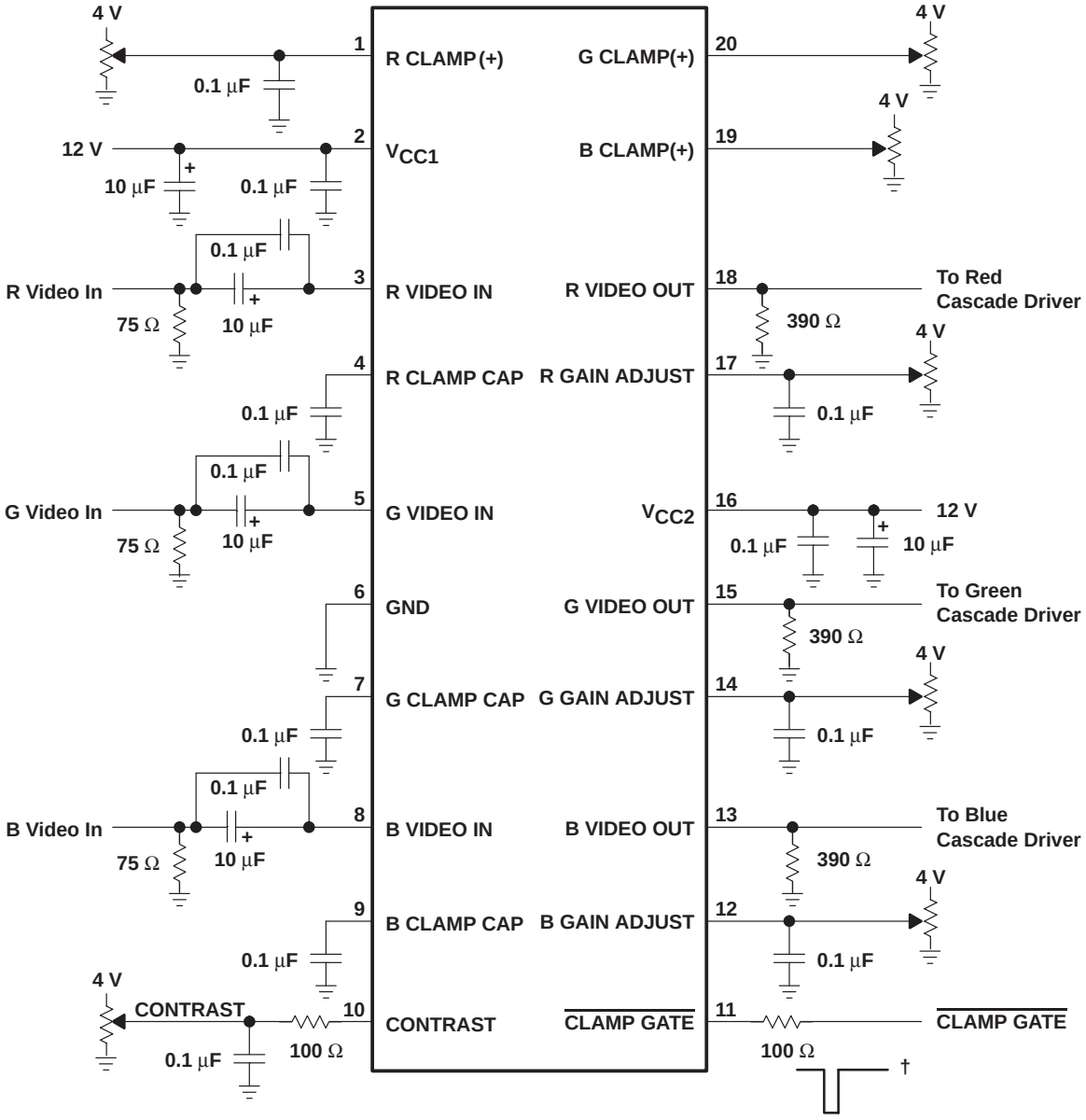


Figure 1. Test Circuit

APPLICATION INFORMATION



† Minimum pulse width: 300 ns

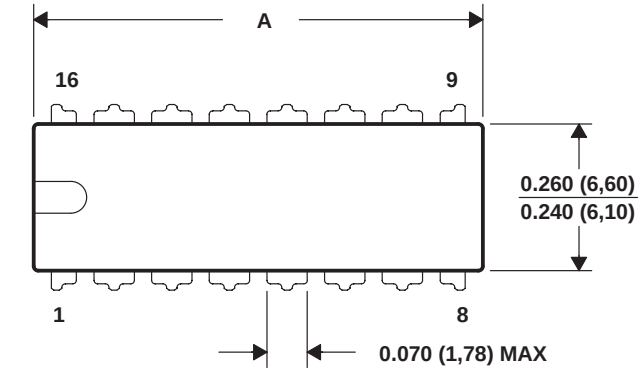
Figure 2. Application Circuit

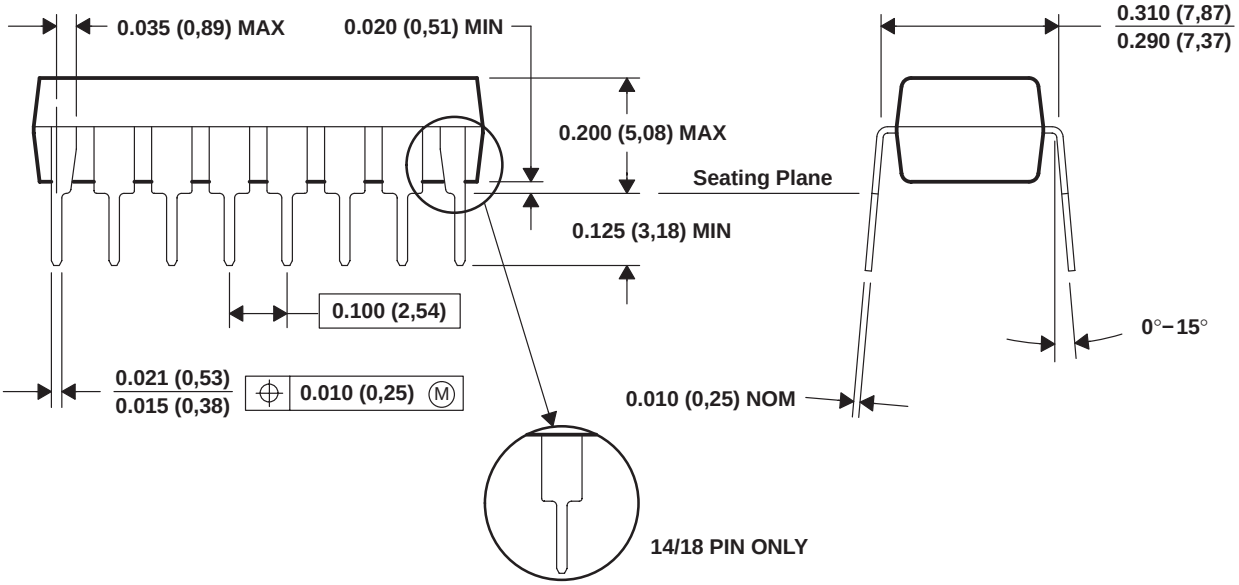
MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)





4040049/C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLS1233N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLS1233N
TLS1233N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLS1233N

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

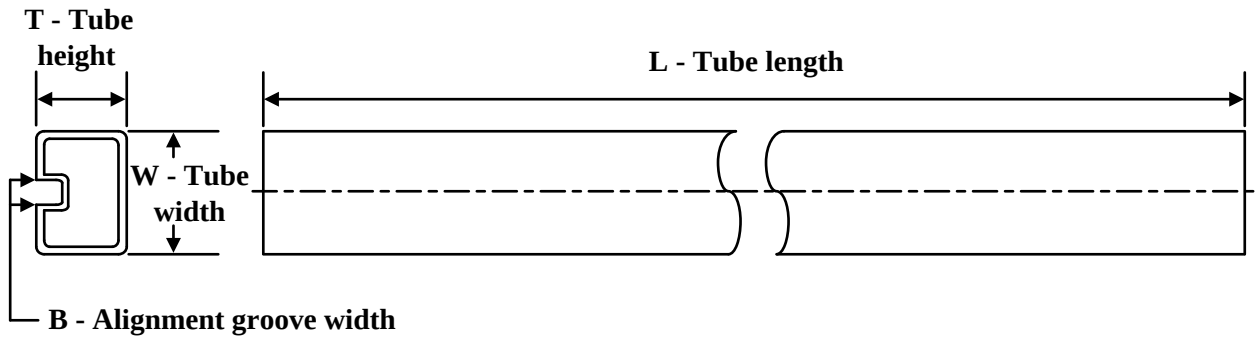
(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLS1233N	N	PDIP	20	20	506	13.97	11230	4.32
TLS1233N.A	N	PDIP	20	20	506	13.97	11230	4.32

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