Link Replicator for Fibre Channel, Gigabit Ethernet, and HDTV Data Rates

Check for Samples: SN65LVCP15

FEATURES

- **Replicates Serial Links Such as Fibre Channel, Gigabit Ethernet, and HDTV Links**
- **T11 Fibre Channel Compliant at 1.0634 Gb/s**
- **IEEE802.3-2005 Gigabit Ethernet Compliant at 1.25 Gb/s (1000Base-X)**
- **Support for SMPTE-292M Data Rate at 1.485 Gb/s**
- **Compatible With VSC7132-01**
- **No External Components Required**
- **0.455 W Maximum Power Dissipation**
- **3.3 V Power Supply**
- **28-Pin, 4,4 mm × 9,7 mm TSSOP Package**
- **Footprint Compatible with VSC7132**

APPLICATIONS

- **Test Equipment**
- **Gigabit Ethernet and Fibre Channel Switches/Repeaters**

DESCRIPTION

The SN65LVCP15 is a high performance serial link mux for use in Fibre Channel (1.0625 Gb/s), Gigabit Ethernet (1.25 Gb/s), and other high speed interface applications. A common application involves a serializer/deserializer (SerDes), such as the TLK2201B, which would normally be connected to the IN± and OUT± ports in order to provide duplicate set of links on the IN0/OUT0 and IN1/OUT1 ports. This type of application is often used to implement high speed test ports that can be monitored without affecting the serial data stream of the application. A popular application is in Line Cards, that use serial links from a SerDes like TLK2201B (SLLS585), where the SN65LVCP15 provides redundant, hot-swappable links to redundant Switch Fabric Cards.

During normal operation, IN is sent to both OUT0 and OUT1 whose buffers are enabled when OE0 and OE1 are HIGH. OUT0 can select between IN and IN1. OUT1 can select between IN and IN0. OUT can select between IN0 and IN1.

In Link Replicator applications, such as the Line Card to Switch Card links, IN is transmitted to both OUT0 and OUT1 which either IN0 or IN1 is selected at OUT. In host Adapter applications, IN goes to OUT0 (an internal connector) which returns data and IN0. IN0 is looped to OUT1 (an external connector) which returns data on IN1 and then back to the SerDes on OUT.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

ORDERABLE PART NUMBER	DESCRIPTION
SN65LVCP15PW(1)	28-Pin TSSOP, 4,4 mm × 9,7 mm Body

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
V_{DD}	Power supply voltage, TTL	0.5 to 4.0	V
$V_{IN(P)}$	DC input voltage, PECL	–0.5 to V_{DD} +0.5	V
$V_{IN(T)}$	DC input voltage, TTL	–0.5 to +5.5	V
$V_{IN(TTL)}$	DC voltage applied to outputs for high output state	–0.5 to V_{DD} +0.5	V
ESD	Electrostatic discharge voltage (human body model)	2	kV
T_{JA}	Junction to Ambient Thermal Resistance (Assumes High K Board)	61.7	°C/W

(1) Stresses listed under absolute maximum ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to theses values for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Power supply voltage	3.14	3.47	V
	Operating temperature range	–40	85	°C

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f	Operating frequency range		1		1.5	Gb/s
t_1	Flow-through propagation delay	Delay from any input to any output			1	ns
t_r, t_f	Serial data rise and fall time	20% to 80%			300	ps
t_{DJ}	Deterministic jitter added to serial input	1 Gb/s to 1.25 Gb/s. Measured on K28.5+, K28.5– pattern			35	ps pp
		1.25 Gb/s to 1.5 Gb/s. Measured on K28.5+, K28.5– pattern			45	

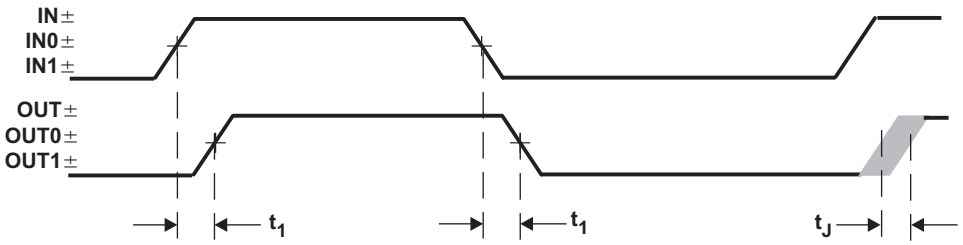


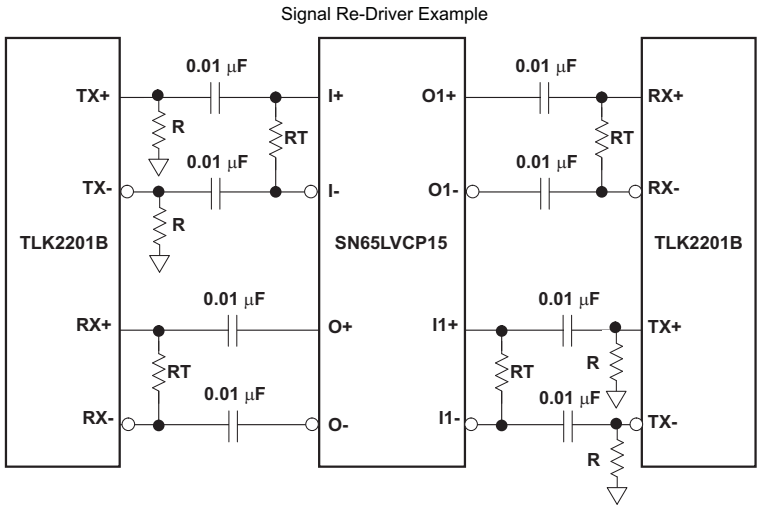
Figure 1. Timing Waveforms

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH(TTL)}$	Input HIGH voltage		2		5.5	V
$V_{IL(TTL)}$	Input LOWS voltage		0		0.8	V
$I_{IH(TTL)}$	Input HIGH current	V_{IN} = 2.4 V	-100		100	µA
$I_{IL(TTL)}$	Input HIGH current	V_{IN} = 0.5 V	–100		100	µA
V_{DD}	Supply voltage	V_{DD} = 3.30 V ±5%	3.14		3.47	V
I_{DD}	Supply current	Outputs open, V_{DD} = V_{DD} max			131	mA
P_D	Power dissipation	Outputs open, V_{DD} = V_{DD} max			455	mW
ΔV_{IN}	Receiver differential peak-to-peak input sensitivity (IN, IN0, IN1)	AC coupled, Internally biased at V_{DD}/2	300		2600	mV_{PP}
ΔV_{OUT50}	Output differential peak-to-peak voltage swing (OUT, OUT0, OUT1)	50 Ω to V_{DD} – 2 V	1000		2200	mV_{PP}
ΔV_{OUT75}		75 Ω to V_{DD} – 2 V	1200		2200	mV_{PP}

APPLICATION EXAMPLE



R is 150 Ω for both 100 Ω differential or 150 Ω differential traces.

RT matches the differential impedance of the link.

For optimal signal integrity performance, A/C coupling is recommended.

Figure 2. TLK2201B and SN65LVCP15 Interconnect

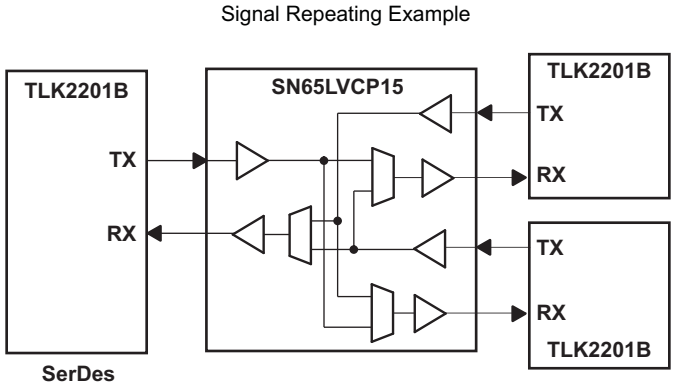
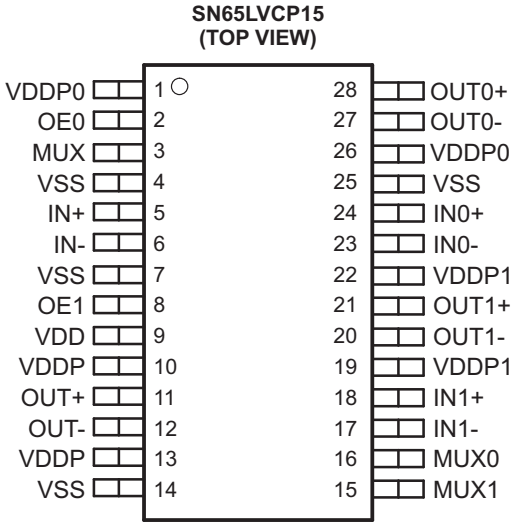


Figure 3.

PACKAGE INFORMATION – PIN DIAGRAM



PIN FUNCTIONS

PIN		TYPE	LEVEL	DESCRIPTION
NO.	NAME			
5, 6 24, 23 18, 17	IN+, IN– IN0+, IN0– IN1+, IN1–	I	PECL	Differential (biased to V_{DD}/2) High-speed serial inputs
11, 12 28, 27 21, 20	OUT+, OUT– OUT0+, OUT0– OUT1+, OUT1–	O	PECL	Differential high-speed serial outputs
2 8	OE0 OE1	I	TTL	OE0/OE1 enables OUT0/OUT1 when HIGH. When LOW, OUTx is powered down and both OUTx+ and OUTx– float HIGH.
3	MUX	I	TTL	Determines source of OUT. Selects either IN0 (LOW) or IN1 (HIGH).
15	MUX1	I	TTL	Determines source of OUT1. Selects either IN (HIGH) or IN0 (LOW).
16	MUX0	I	TTL	Determines source of OUT0. Selects either IN (LOW) or IN1 (HIGH).
9	VDD	Pwr		3.3 V power supply for digital logic
10, 13 1, 26 19, 22	VDDP VDDP0 VDDP1	Pwr		High-speed output power supply: 3.3 V supply for PECL drivers. VDDP0 is for OUT0, VDDP is for OUT, and VDDP1 is for OUT1.
4, 7 14, 25	VSS	Pwr		Ground

MOISTURE SENSITIVITY LEVEL

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standards.

REVISION HISTORY

Changes from Original (October 2008) to Revision A **Page**

- Deleted I_O - DC output HIGH current, PECL from the ABSOLUTE MAXIMUM RATINGS table 2

Changes from Revision A (November 2008) to Revision B **Page**

- Changed Case operating temperature To: Operating temperature range and the range From: 0 to 85°C To: –40 to 85°C 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVCP15PW	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCP15
SN65LVCP15PW.B	Active	Production	TSSOP (PW) | 28	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCP15
SN65LVCP15PWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCP15
SN65LVCP15PWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCP15

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

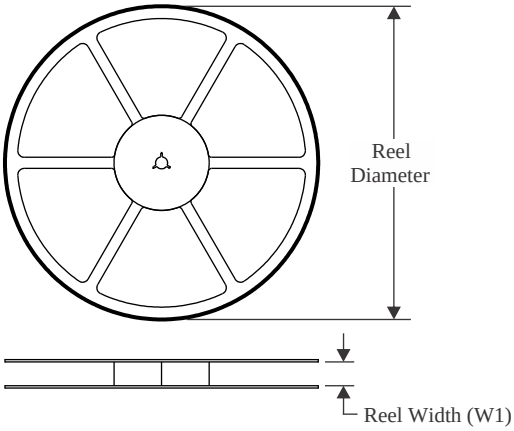
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

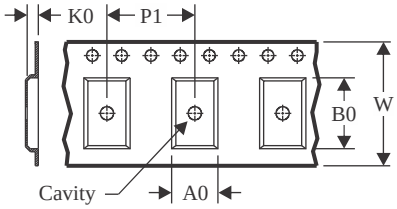
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

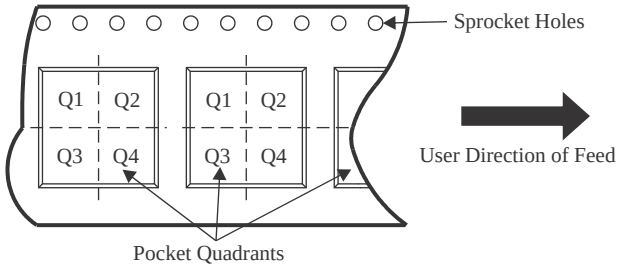


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

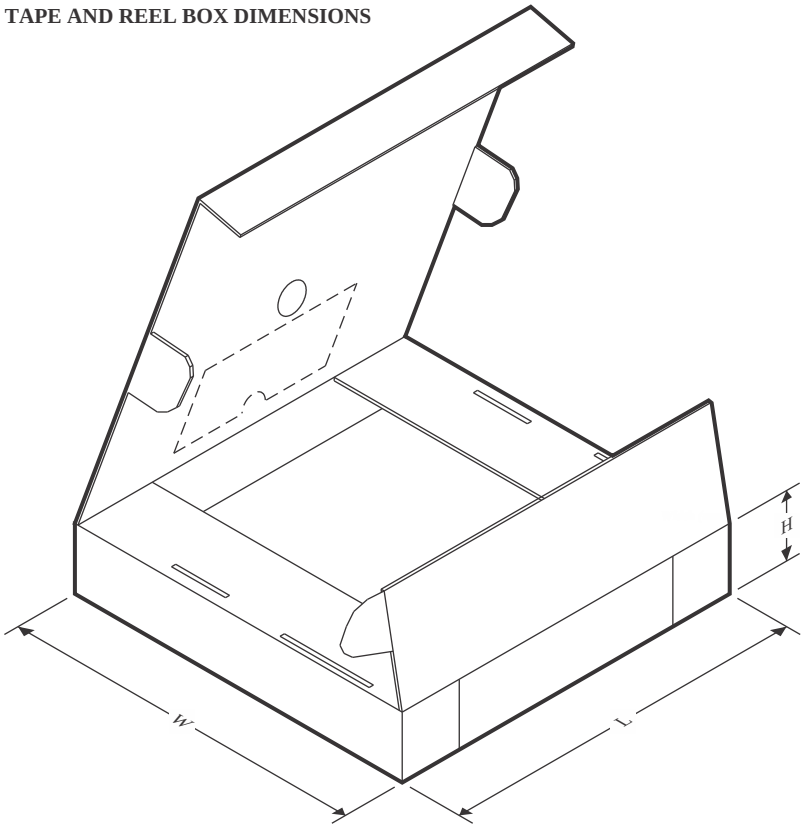
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP15PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

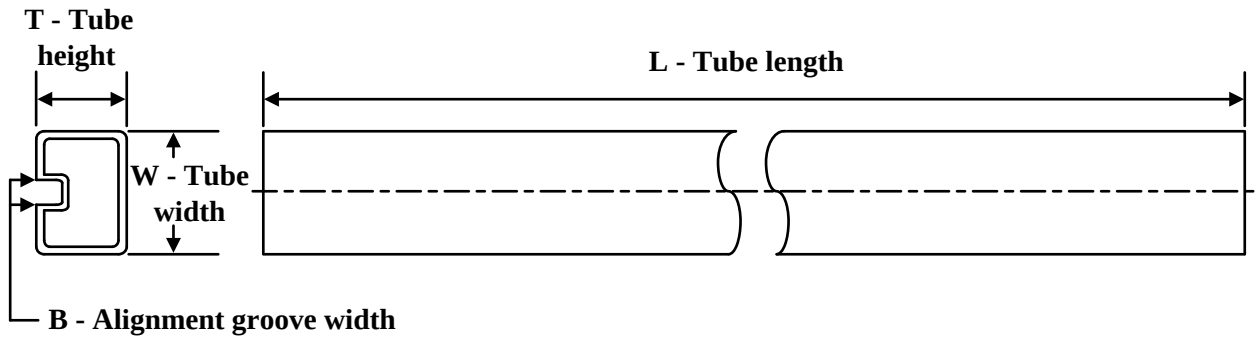
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP15PWR	TSSOP	PW	28	2000	353.0	353.0	32.0

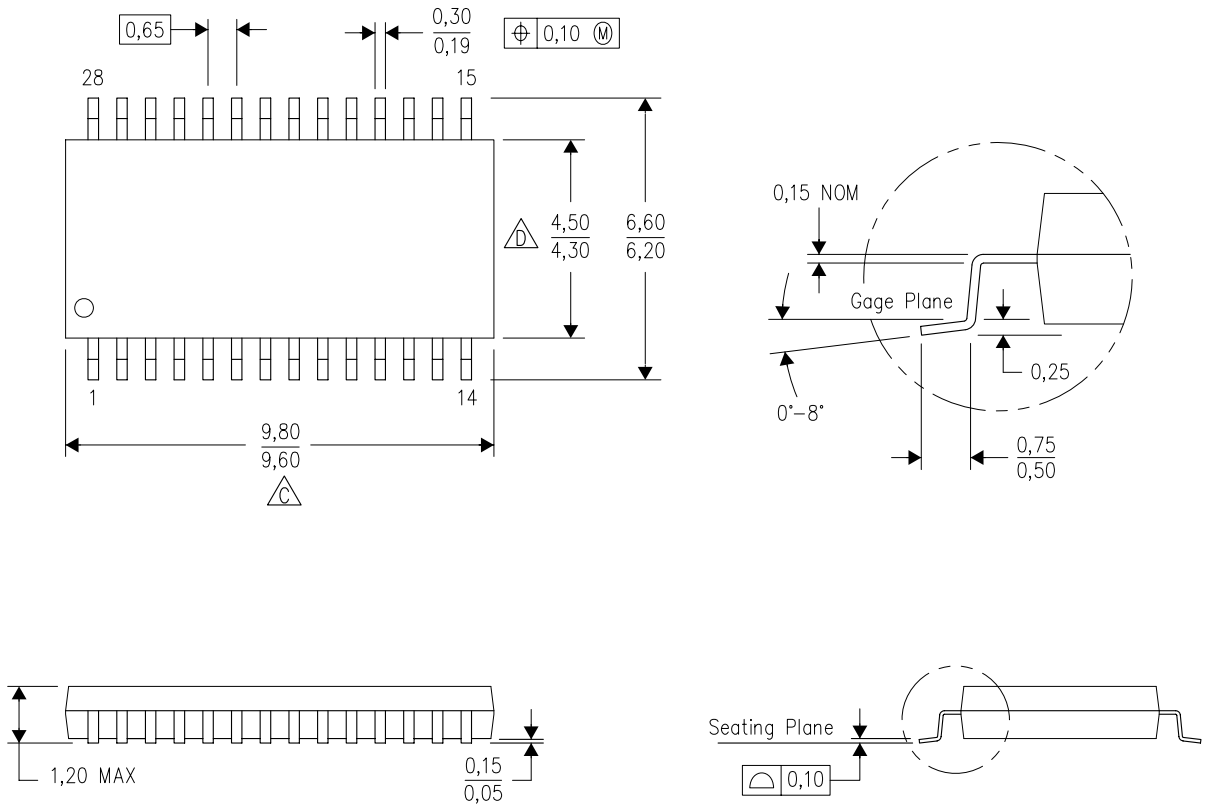
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVCP15PW	PW	TSSOP	28	50	530	10.2	3600	3.5
SN65LVCP15PW.B	PW	TSSOP	28	50	530	10.2	3600	3.5

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265