Current Mode PWM Controller

SG1844/SG1845/SG3845

Product Overview

Description

The SG1844/45 family of control ICs provides all the required features to implement off-line Fixed Frequency, Current-mode switching power supplies with a minimum number of external components. Current-mode architecture demonstrates improved line regulation, improved load regulation, pulse-by pulse current limiting and inherent protection of the power supply output switch.

The Bandgap reference is trimmed to ±1% over temperature. Oscillator discharge current is trimmed to less than ±10%. The SG1844/45 has under-voltage lockout, current-limiting circuitry, and start-up current of less than 1 mA. The totem-pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N-channel device. Both operate up to a maximum duty cycle range of zero to < 50% due to an internal toggle flip-flop which blanks the output off every other clock cycle. The SG1844/45 is specified for operation over the full military ambient temperature range of –55 °C to 125 °C. The SG3845 is designed for the commercial range of 0 °C to 70 °C.

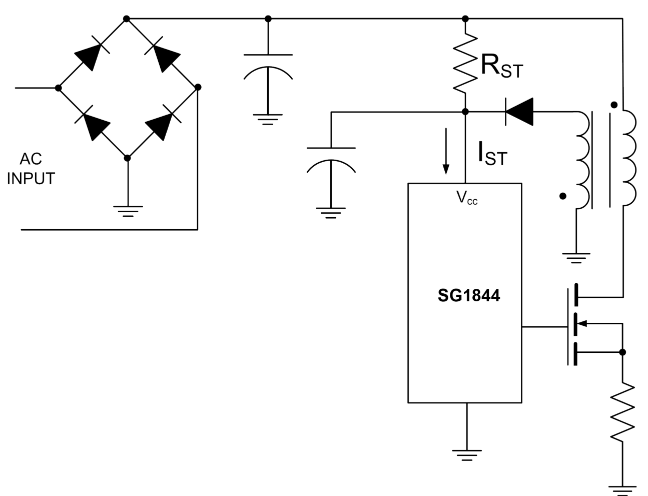
Features

- Optimized for off-line control
- Low start-up current (<1 mA)
- Automatic feed forward compensation
- Trimmed oscillator
- Discharge current
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Undervoltage lockout with 6V hysteresis (SG1844 only)
- Double pulse suppression
- High-current totem-pole output
- Internally trimmed bandgap reference
- 500 kHz operation
- Under-voltage lockout
  SG1844 – 16 volts
  SG1845 – 8.4 volts
- Low shoot-through current < 75 mA over temperature

Application

- Available to MIL-STD-883
- Available to DLA
  - Standard Microcircuit Drawing (SMD)

Figure 1. Product Highlight



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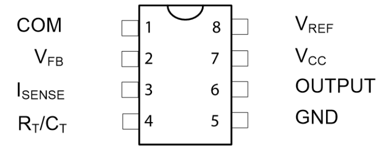
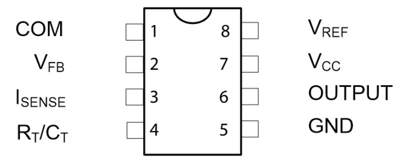
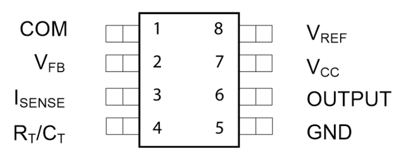
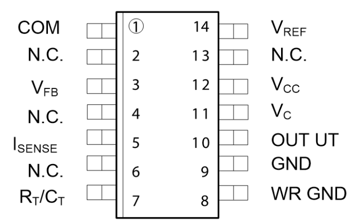
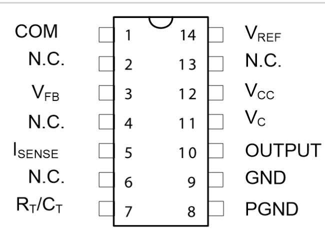
1. Connection Diagrams and Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
0 °C to 70 °C	M	8-Pin Plastic Dual Inline Package	SG3845M	PDIP	 **M PACKAGE** (Top View) **M Package**: RoHS / Pb-free 100% Matte Tin Lead Finish
-55 °C to 125 °C	Y	8-Pin Ceramic DUAL Inline Package	SG1844Y SG1845Y SG1844Y-883B SG1845Y-883B SG1844Y-DESC SG1845Y-DESC	CERDIP	 **Y PACKAGE** (Top View) PbSn Tin Lead Finish
0 °C to 70 °C	DM	8-Pin Small Outline Integrated Circuit	SG3845DM	SOIC	 **DM PACKAGE** (Top View) RoHS / Pb-free 100% Matte Tin Lead Finish
0 °C to 70 °C	D	14-Pin Small Outline Integrated Circuit	SG3845D	SOIC	 **D PACKAGE** (Top View) RoHS / Pb-free 100% Matte Tin Lead Finish
-55 °C to 125 °C	J	14-Pin Ceramic Dual Inline Package	SG1844J SG1845J SG1844J-883B SG1845J-883B SG1844J-DESC SG1845J-DESC	CERDIP	 **J PACKAGE** (Top View) **PbSn** Lead Finish

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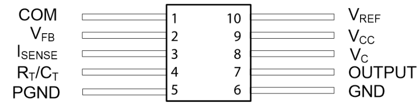
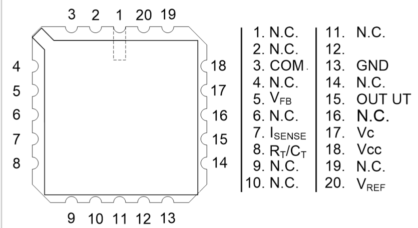
Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
-55 °C to 125 °C	F	10-Pin Ceramic Flat Pack Package	SG1844F-DESC	FLAT PACK	 **F PACKAGE** (Top View) PbSn Lead Finish
			SG1845F-DESC		
-55 °C to 125 °C	L	20-Pin Ceramic	SG1844L	Ceramic (LCC) Leadless Chip Carrier	 **L PACKAGE** (Top View) PbSn Lead Finish
			SG1845L		
			SG1844L-883B		
			SG1845L-883B		
			SG1844L-DESC		
			SG1845L-DESC		

Notes:
1. Contact factory for DESC part availability.
2. All parts are viewed from the top.
3. Available in tape and reel. Append the letters “TR” to the part number.
4. Hermetic packages J, F, L, and Y use Pb37/Sn63 hot solder lead finish. Contact factory for availability of RoHS versions.

2. Absolute Maximum Ratings[1-2]

Parameter	Value	Units
Supply voltage (low impedance source)	30	V
Output current (peak)	±1	A
Output current (continuous)	350	mA
Output energy (capacitive load)	5	μJ
Analog inputs (V_{FB}, I_{SENSE})	–0.3 to +6.3	V
Error amplifier output sink current	10	mA
Operating Junction Temperature		
Hermetic (J, Y, F, L packages)	150	°C
Plastic (M, D, DM packages)	150	°C
Storage temperature range	–65 to +150	°C
Lead temperature (soldering, 10 seconds)	300	°C
RoHS / Pb-free peak package solder reflow temp. (40 second max. exposure)	260 (+0, –5)	°C

Notes:

1. Exceeding these ratings could cause damage to the device.
2. All voltages are with respect to pin 5. All currents are positive into the specified terminal.

3. Thermal Data[1]

Parameter	Value	Units
M Package		
Thermal resistance-junction to ambient, θ_{JA}	95	°C/W
DM Package		
Thermal resistance-junction to ambient, θ_{JA}	165	°C/W
D Package		
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W
Y Package		
Thermal resistance-junction to case, θ_{JC}	30	°C/W
Thermal resistance-junction to ambient, θ_{JA}	130	°C/W
J Package		
Thermal resistance-junction to case, θ_{JC}	30	°C/W
Thermal resistance-junction to ambient, θ_{JA}	80	°C/W
F Package		
Thermal resistance-junction to case, θ_{JC}	80	°C/W
Thermal resistance-junction to ambient, θ_{JA}	145	°C/W
L Package		
Thermal resistance-junction to case, θ_{JC}	35	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W

Note:

1. Junction temperature calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
   The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

4. Recommended Operating Conditions

Symbol	Parameter	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
V_S	Supply voltage range	—	30	—	V
I_{PK}	Output current (peak)	—	±1	—	A
I_{OUT}	Output current (continuous)	—	200	—	mA
	Analog inputs (pin 2, pin 3)	0	—	2.6	V
EA_{ISNK}	Error amp output sink current	—	5	—	mA
OSC_{FR}	Oscillator frequency range	0.1	—	500	kHz
R_T	Oscillator timing resistor	0.52	—	150	kΩ
C_T	Oscillator timing capacitor	0.001	—	1.0	µF
Operating Ambient Temperature Range[1]					
	SG1844/45	–55	—	125	°C
	SG3845	0	—	70	°C
1. Range over which the device is functional.					

5. Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1844/SG1845 with -55 °C ≤ T_A ≤ 125 °C, SG3845 with 0 °C ≤ T_A ≤ 70 °C, VCC = 15V (Note 7), R_T = 10 kΩ, and C_T = 3.3 nF. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Symbol	Parameter	Test Conditions	SG1844/SG1845			SG3845			Units
			Min.	Typ.	Max	Min.	Typ.	Max	
Reference Section									
V_{REF}	Output voltage	T_J = 25 °C, I_O = 1 mA	4.95	5.00	5.05	4.90	5.00	5.10	V
V_{REG}	Line regulation	12V ≤ V_{IN} ≤ 25V	—	6	20	—	6	20	mV
I_{REG}	Load regulation	1 ≤ I_O ≤ 20 mA	—	6	25	—	6	25	mV
	Temperature stability[4]		—	0.2	0.4	—	0.2	0.4	mV/°C
	Total output variation[4]	Line, load, temperature	4.90	—	5.10	4.82	—	5.18	V
V_N	Output noise voltage[4]	10 Hz ≤ f ≤ 10 kHz, T_J = 25 °C	—	50	—	—	50	—	µV
	Long term stability[4]	T_A = 125 °C, 1000 hrs	—	5	25	—	5	25	mV
V_{REFISC}	Output short circuit		–30	–100	–180	–30	–100	–180	mA
Oscillator Section									
f	Initial accuracy[8]	T_J = 25 °C	47	52	57	47	52	57	kHz
f_{REG}	Voltage stability	12V ≤ V_{CC} ≤ 25V	—	0.2	1	—	0.2	1	%
	Temperature stability[4]	T_{MIN} ≤ T_A ≤ T_{MAX}	—	5	—	—	5	—	%
OSC_{PP}	Amplitude	$V_{RT/CT}$ (peak to peak)	—	1.7	—	—	1.7	—	V
I_{DSG}	Discharge current	T_J = 25 °C	7.8	8.3	9.1	7.5	8.4	9.3	mA
		T_{MIN} ≤ T_A ≤ T_{MAX}	6.8	—	9.3	7.2	—	9.5	mA
Error Amplifier Section									
EA_{IH}	Input voltage	V_{COMP} = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
EA_{IIB}	Input bias current		—	–0.3	–1	—	–0.3	-2	µA
A_{VOL}	Open loop gain	2V ≤ V_O ≤ 4V	65	90	—	65	90	—	dB
EA_{BW}	Unity gain bandwidth[4]	T_J = 25 °C	0.7	1	—	0.7	1	—	MHz
PSRR	Power supply rejection ratio	12V ≤ V_{CC} ≤ 25V	60	70	—	60	70	—	dB
EA_{SNK}	Output sink current	V_{VFB} = 2.7V, V_{COMP} = 1.1V	2	6	—	2	6	—	mA
EA_{SRC}	Output source current	V_{VFB} = 2.3V, V_{COMP} = 5V	–0.5	–0.8	—	–0.5	–0.8	—	mA
EA_{VOH}	V_{OUT} High	V_{VFB} = 2.3V, R_L = 15k to GND	5	6	—	5	6	—	V
EA_{VOL}	V_{OUT} Low	V_{VFB} = 2.7V, R_L = 15k to V_{REF}	—	0.7	1.1	—	0.7	1.1	V
Current Sense Section									
CS_{AVOL}	Gain[5, 6]		2.85	3	3.15	2.85	3	3.15	V/V
	Maximum input signal[5]	V_{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	V
PSRR	Power supply rejection ratio	12V ≤ V_{CC} ≤ 25V	—	70	—	—	70	—	dB

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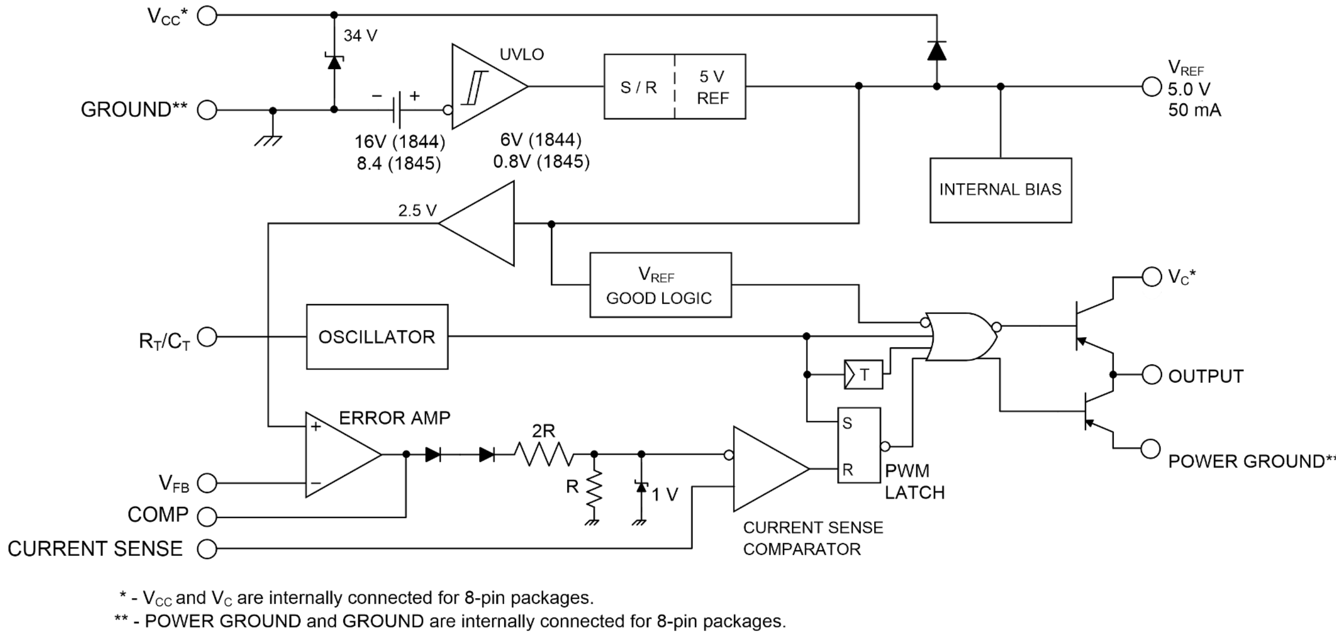
Symbol	Parameter	Test Conditions	SG1844/SG1845			SG3845			Units
			Min.	Typ.	Max	Min.	Typ.	Max	
CS_{IIB}	Input bias current		—	–2	–10	—	–2	–10	μA
CS_{DELAY}	Delay to output[4]		—	150	300	—	150	300	ns
Output Section									
VOL	Output low level	I_{SINK} = 20 mA	—	0.1	0.4	—	0.1	0.4	V
		I_{SINK} = 200 mA	—	1.5	2.2	—	1.5	2.2	V
VOH	Output high level	I_{SOURCE} = 20 mA	13	13.5	—	13	13.5	—	V
		I_{SOURCE} = 200 mA	12	13.5	—	12	13.5	—	V
RS	Rise time[4]	T_J = 25 °C, C_L = 1 nF	—	50	150	—	50	150	ns
FT	Fall time[4]	T_J = 25 °C, C_L = 1 nF	—	50	150	—	50	150	ns
Under-Voltage Lockout Section									
UVLO	Start threshold	1844	15	16	17	14.5	16	17.5	V
		1845	7.8	8.4	9.0	7.8	8.4	9.0	V
V_{SMIN}	Min. operation voltage after turn-on	1844	9	10	11	8.5	10	11.5	V
		1845	7.0	7.6	8.3	7.0	7.6	8.2	V
PWM Section									
DC_{MAX}	Maximum duty cycle		46	48	50	46	48	50	%
DC_{MIN}	Minimum duty cycle		—	—	0	—	—	0	%
Power Consumption Section									
I_S	Start-up current		—	0.5	1	—	0.5	1	mA
I	Operating supply current	V_{FB} = V_{ISENSE} = 0V	—	11	17	—	11	17	mA
Z	V_{CC} Zener voltage	I_{CC} = 25 mA	—	34	—	—	34	—	V

Notes:

1. These parameters, although guaranteed, are not 100% tested in production.
2. Parameter measured at trip point of latch with V_{VFB} = 0.
3. Gain defined as: $A = \Delta V_{COMP} / \Delta V_{ISENSE}$; $0 \le V_{ISENSE} \le 0.8V$
4. Adjust V_{CC} above the start threshold before setting at 15V.
5. Output frequency equals one half of oscillator frequency.

6. Block Diagram

Figure 6-1. Block Diagram



7. Characteristic Curves

Figure 7-1. Dropout Voltage Vs. Temperature

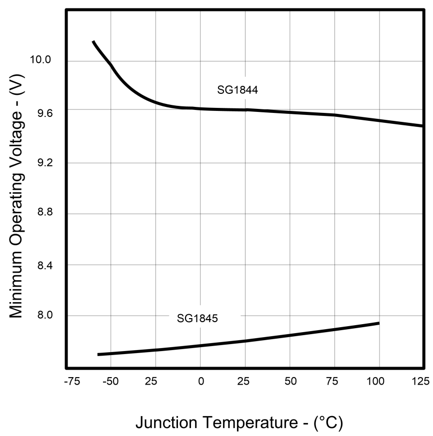


Figure 7-2. Oscillator Temperature Stability

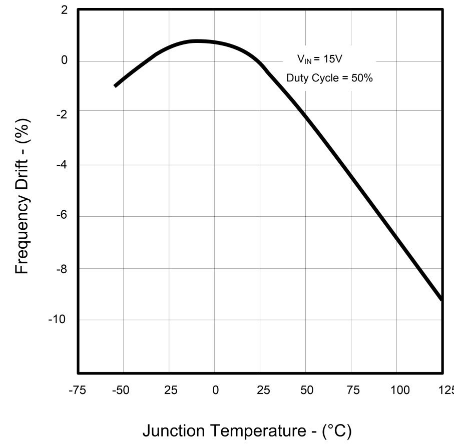


Figure 7-3. Current Sense to Output Delay Vs. Temperature

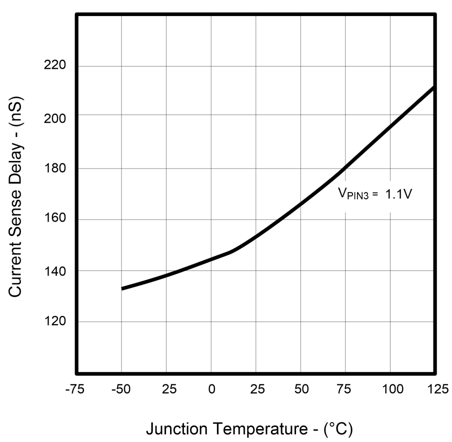


Figure 7-4. Start-Up Current Vs. Temperature

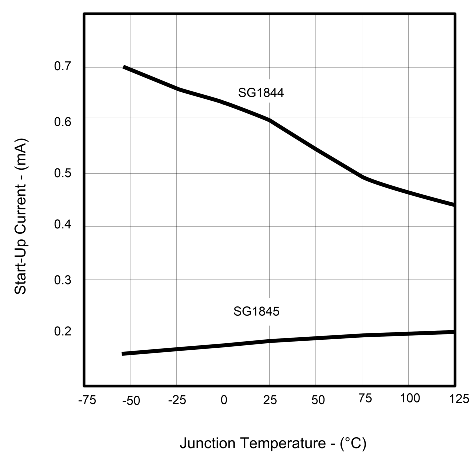


Figure 7-5. Reference Voltage Vs. Temperature

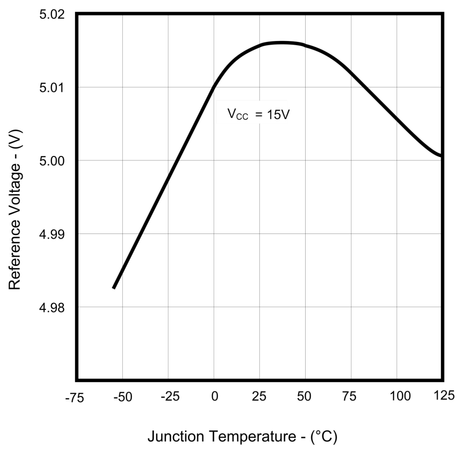


Figure 7-6. Start-Up Voltage Threshold Vs. Temperature

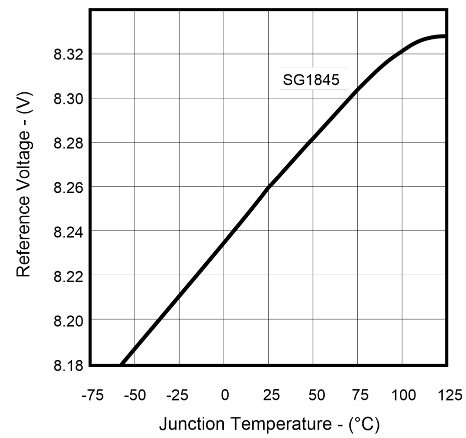


Figure 7-7. Start-Up Voltage Threshold Vs. Temperature

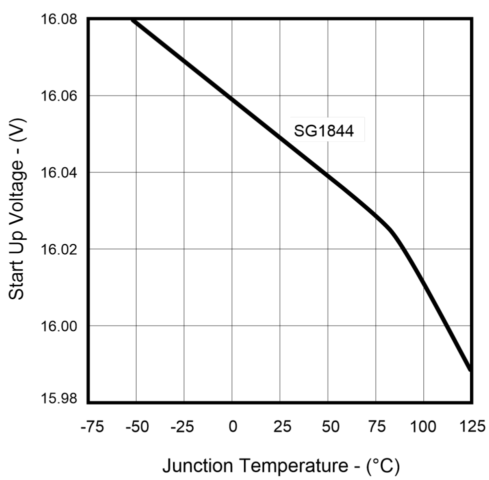


Figure 7-8. Oscillator Discharge Current Vs. Temperature

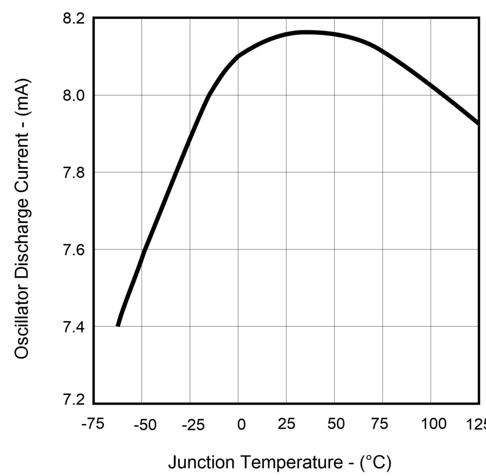


Figure 7-9. Output Saturation Voltage Vs. Output Current and Temperature (Sink Transistor)

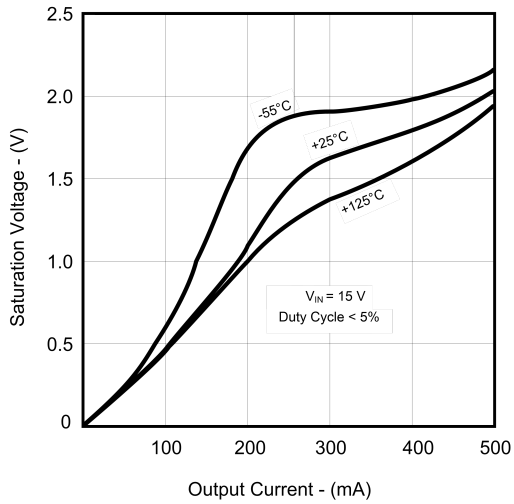


Figure 7-10. Current Sense Threshold Vs. Error Amplifier Output

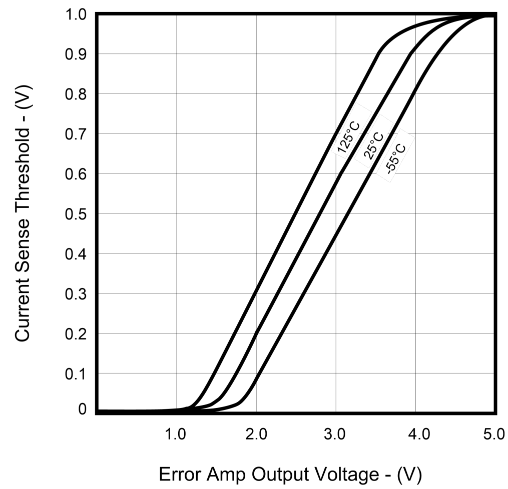
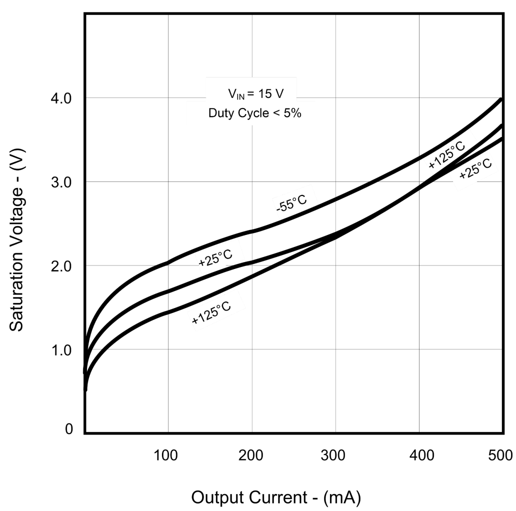


Figure 7-11. Output Saturation Voltage Vs. Output Current and Temperature (Source Transistor)



8. Application Information

The oscillator of the 1844/45 family of PWM's is programmed by the external timing components (R_T, C_T) as shown in Figure 8-1.

Figure 8-1. Oscillator Timing Circuit

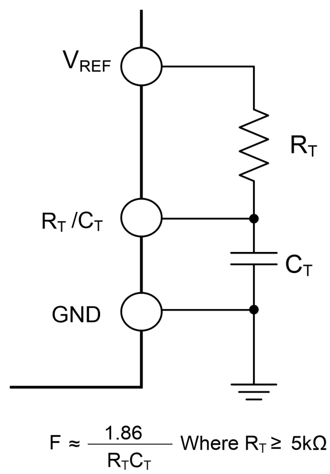
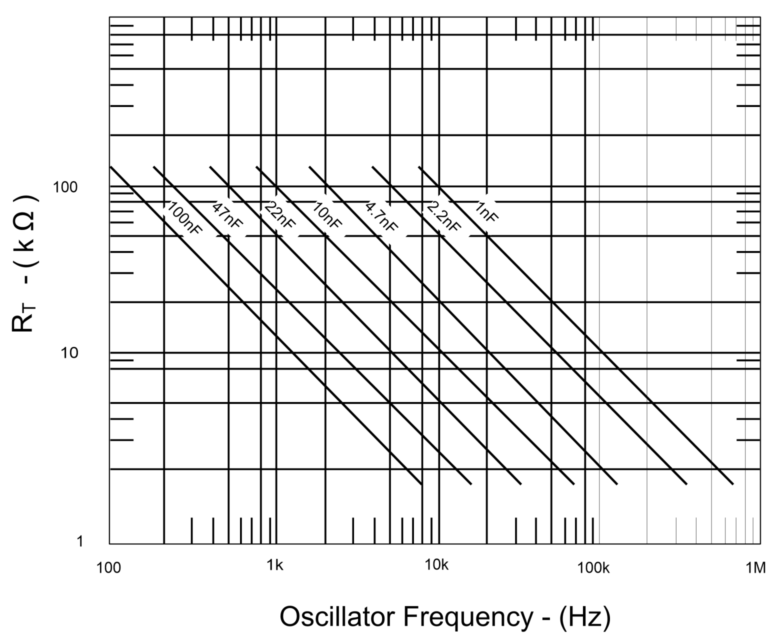


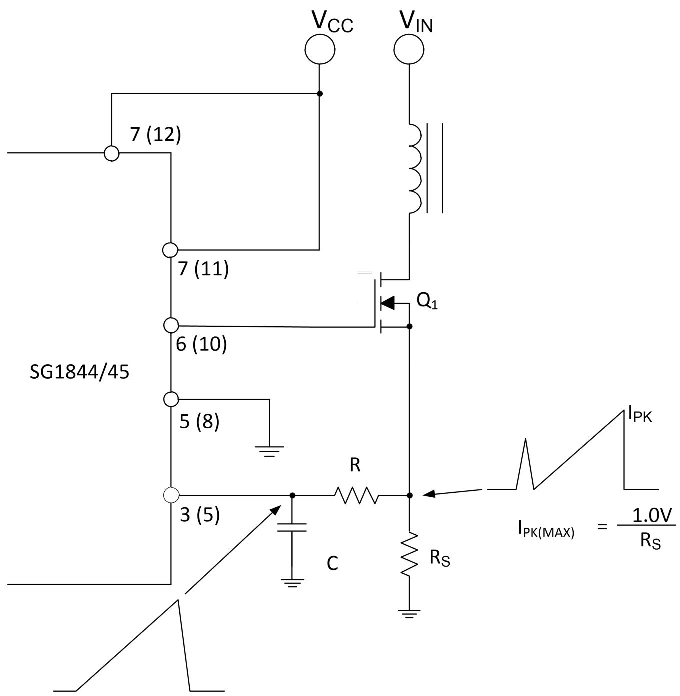
Figure 8-2. Oscillator Frequency Vs. R_T for Various C_T



9. Typical Application Circuits

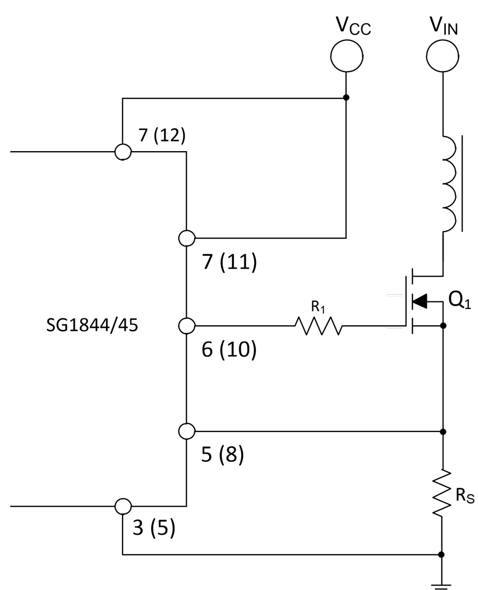
Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.

Figure 9-1. Current Sense Spike Suppression



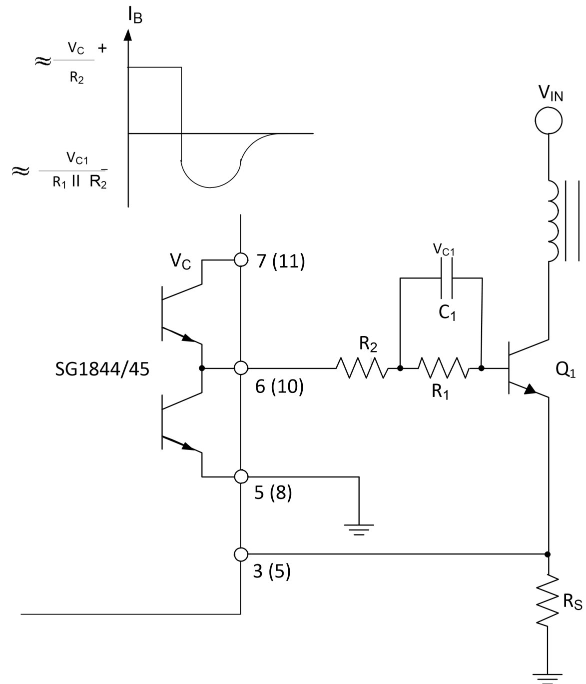
The RC low-pass filter will eliminate the leading edge current spike caused by parasitic of Power MOSFET.

Figure 9-2. MOSFET Parasitic Oscillations



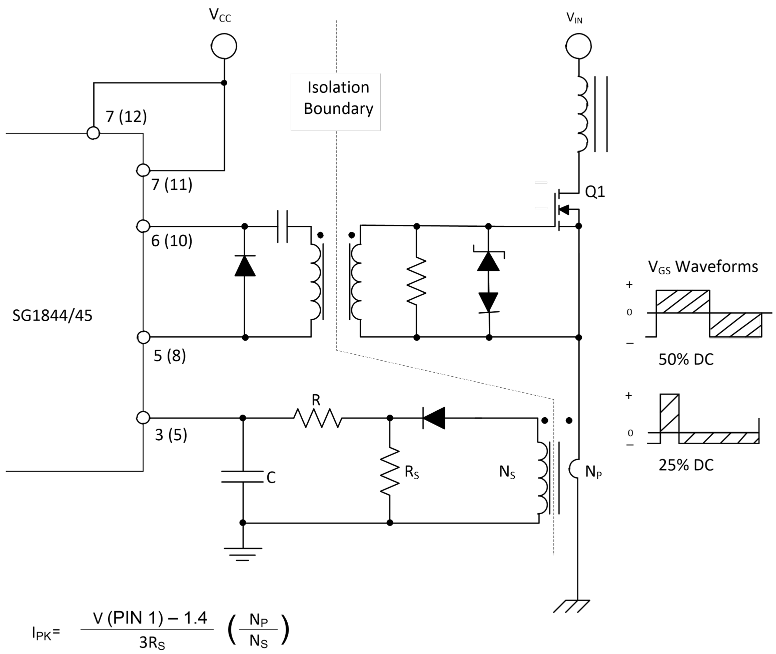
A resistor (R1) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

Figure 9-3. Bipolar Transistor Drive



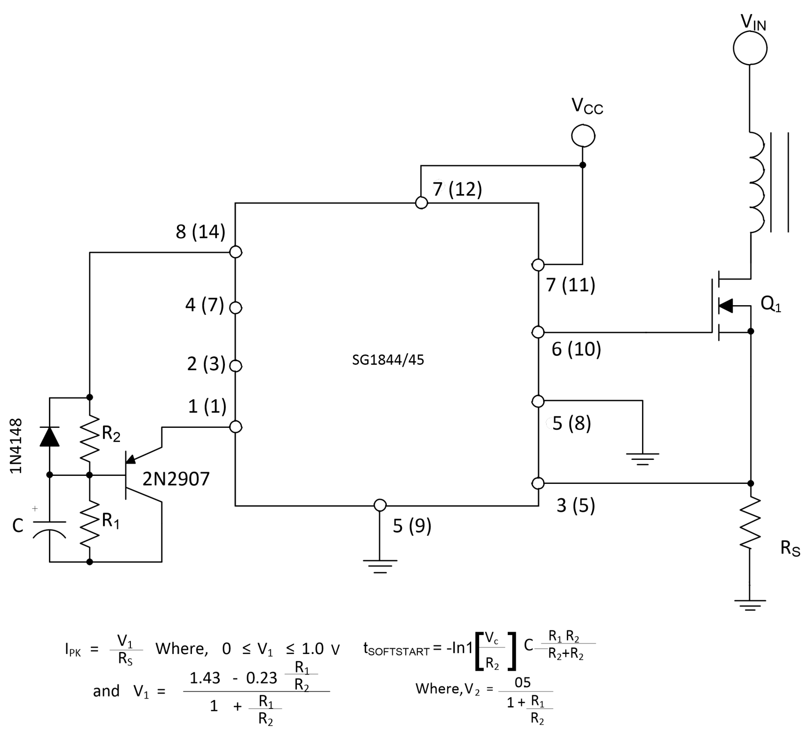
The 1844/45 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

Figure 9-4. Isolated MOSFET Drive



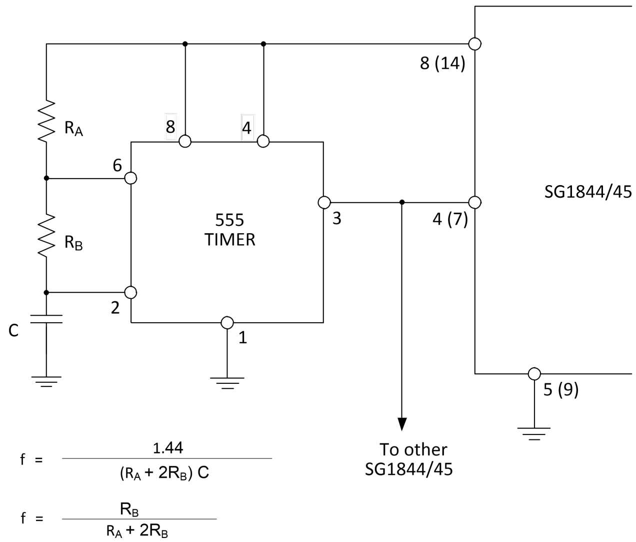
Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

Figure 9-5. Adjustable Buffered Reduction of Clamp Level with Softstart



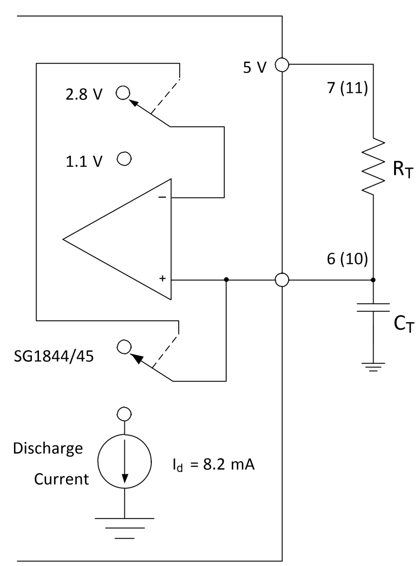
Softstart and adjustable peak current can be done with the external circuitry shown in Figure 9-5.

Figure 9-6. External Duty Cycle Clamp and Multi-Unit Synchronization



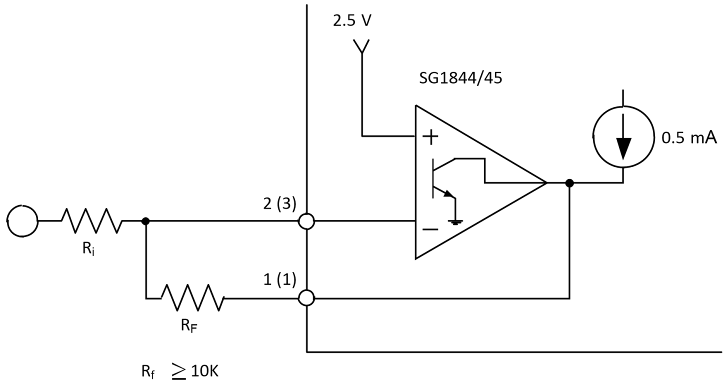
Precision duty cycle limiting for a duty cycle of < 50%, as well as synchronizing several 1844/45's is possible with the circuitry shown in Figure 9-6.

Figure 9-7. Oscillator Connection



The oscillator is programmed by the values selected for the timing components RT and CT. Refer to application information for calculation of the component values.

Figure 9-8. Error Amplifier Connection

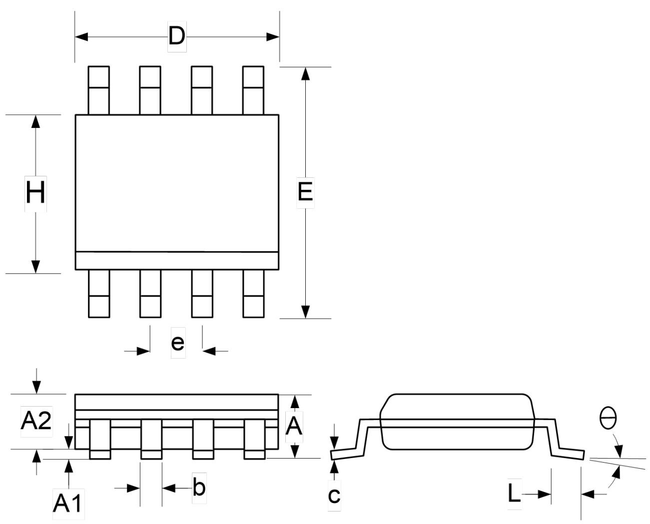


Error amplifier is capable of sourcing and sinking current up to 0.5 mA.

10. Package Outline Dimensions

Controlling dimensions are in inches. Metric equivalents are shown for general information.

Figure 10-1. DM 8-Pin SOIC Package Dimensions

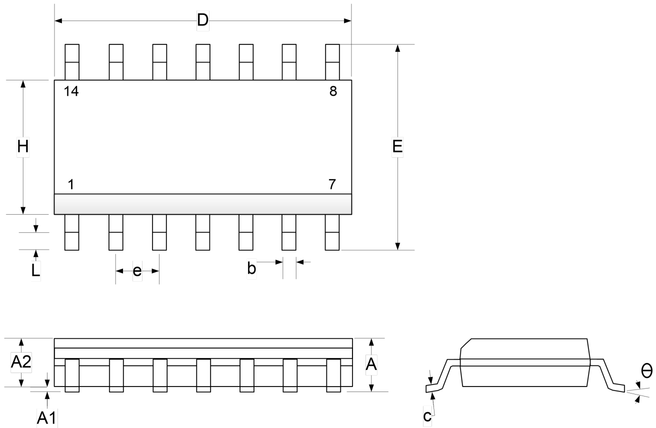


Dim[1]	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	4.83	5.21	0.189	0.205
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0	8	0	8
LC[2]	—	.010	—	0.004

Notes:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Lead coplanarity.

Figure 10-2. D 14-Pin SOIC Package Dimensions

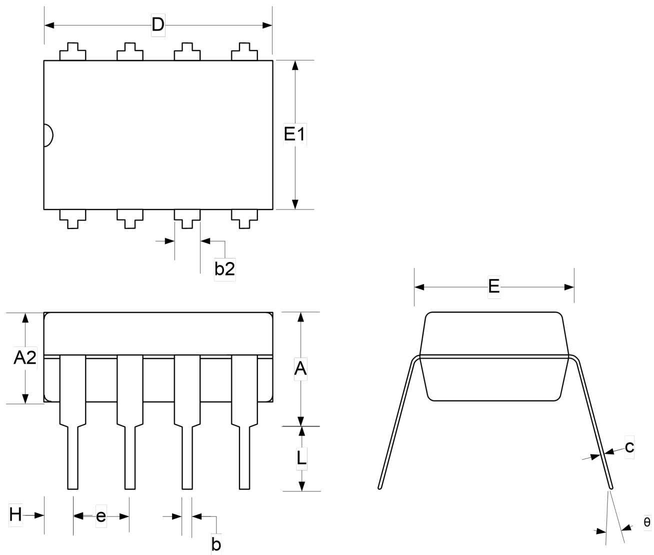


Dim[1]	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	8.54	8.74	0.336	0.344
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0	8	0	8
LC[2]	—	.010	—	0.004

Notes:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.
2. Lead coplanarity.

Figure 10-3. M 8-Pin PDIP Package Dimensions

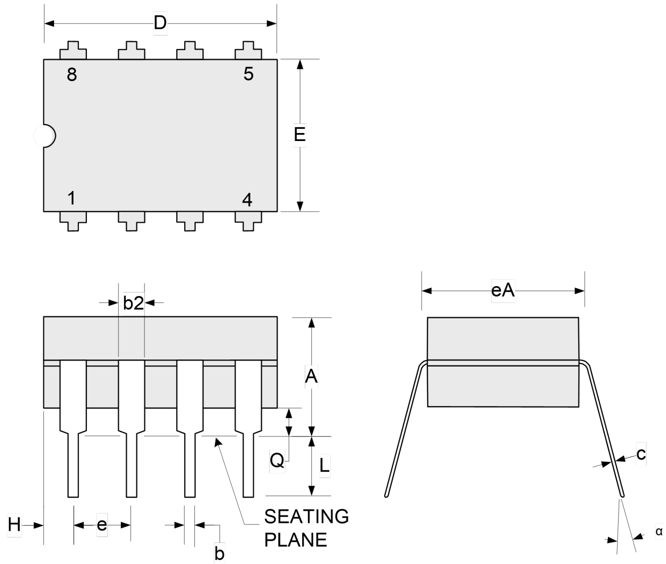


Dim[1]	Millimeters		Inches	
	Min	Max	Min	Max
A	—	5.08	—	0.200
A2	3.30 Typ.		1.30 Typ.	
b	0.38	0.51	0.145	0.020
b2	0.76	1.65	0.030	0.065
c	0.20	0.38	0.008	0.015
D	—	10.16	—	0.400
E	7.62 BSC		0.300 BSC	
e	2.54 BSC		0.100 BSC	
E1	6.10	6.86	0.240	0.270
L	3.05	—	0.120	—
θ	0	15	0	15

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 10-4. Y 8-Pin CERDIP Package Dimensions

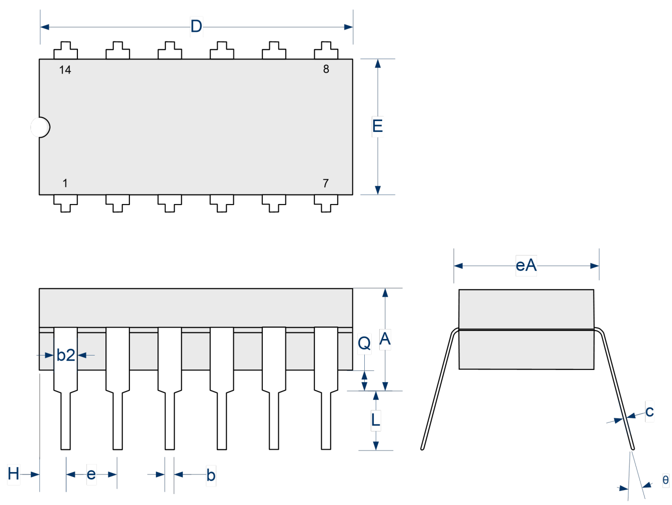


Dim[1]	Millimeters		Inches	
	Min	Max	Min	Max
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	9.52	10.29	0.375	0.405
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	—	15°	—	15°
Q	0.51	1.02	0.020	0.040

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 10-5. J 14-Pin CERDIP Package Dimensions

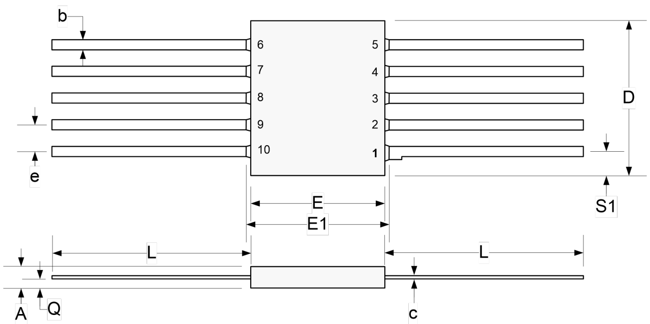


Dim[1]	Millimeters		Inches	
	Min	Max	Min	Max
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	19.30	19.94	0.760	0.785
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	—	15°	—	15°
Q	0.51	1.02	0.020	0.040

Note:

1. Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006”) on any side. Lead dimension shall not include solder coverage.

Figure 10-6. F 10-Pin Ceramic Flatpack Package Dimensions

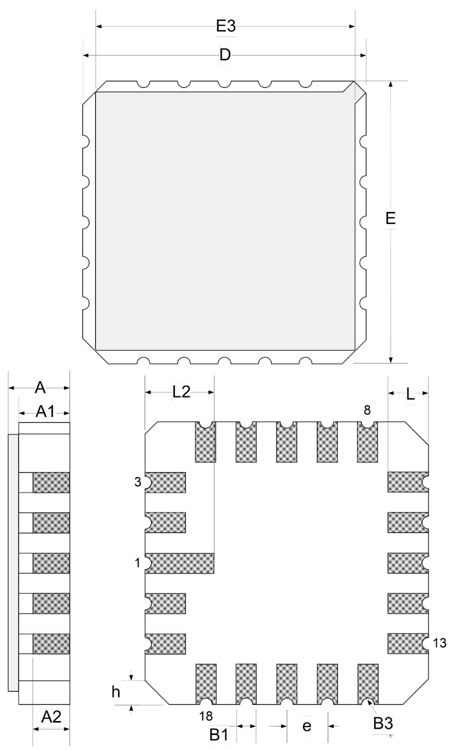


Dim	Millimeter		Inches	
	Min	Max	Min	Max
A	1.45	1.90	0.057	0.075
b	0.25	0.483	0.010	0.019
c	0.102	0.152	0.004	0.006
D	—	7.37	—	0.290
E	6.04	6.40	0.238	0.252
E1	—	6.91	—	0.272
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.51	1.02	0.020	0.040
S1	0.20	0.38	0.008	0.015

Notes:

1. Lead No. 1 is identified by tab on lead or dot on cover.
2. Leads are within 0.13 mm (.0005”) radius of the true position (TP) at maximum material condition.
3. Dimension “e” determines a zone within which all body and lead irregularities lie.

Figure 10-7. L 20-Pin Leadless Chip Carrier Package Dimensions



Dim[1]	Millimeters		Inches	
	Min	Max	Min	Max
D/E	8.64	9.14	0.340	0.360
E3	—	8.128	—	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	—	1.168	—	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

1. All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

11. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	09/2023	Initial revision.

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ISBN: 978-1-6683-3102-6

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