

# 60 V, 4.0 A, Low $V_{CE(sat)}$ NPN Transistor NSS60201LT1G

onsemi e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are miniature surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	Vdc
Collector-Base Voltage	$V_{CBO}$	140	Vdc
Emitter-Base Voltage	$V_{EBO}$	8.0	Vdc
Collector Current – Continuous	$I_C$	2.0	A
Collector Current – Peak	$I_{CM}$	4.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

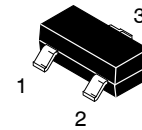
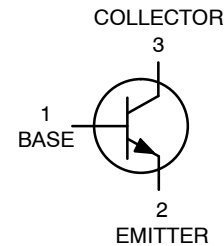
### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25\text{ }^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	$P_D$ (Note 1)	460 3.7	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	270	$^\circ\text{C/W}$
Total Device Dissipation $T_A = 25\text{ }^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	$P_D$ (Note 2)	540 4.3	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	230	$^\circ\text{C/W}$
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{Dsingle}$ (Note 3)	710	mW
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

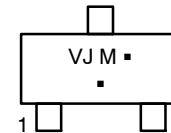
1. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces.
2. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces.
3. Thermal response.

## 60 VOLTS, 4.0 AMPS NPN LOW $V_{CE(sat)}$ TRANSISTOR EQUIVALENT $R_{DS(on)}$ 70 m $\Omega$



SOT-23 (TO-236)  
CASE 318  
STYLE 6

### MARKING DIAGRAM



- VJ = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\* Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NSS60201LT1G	SOT-23 (Pb-Free)	3000/Tape & Reel
NSV60201LT1G	SOT-23 (Pb-Free)	3000/Tape & Reel

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# NSS60201LT1G

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector - Emitter Breakdown Voltage (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	60	–	–	Vdc
Collector - Base Breakdown Voltage (I <sub>C</sub> = 0.1 mA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	140	–	–	Vdc
Emitter - Base Breakdown Voltage (I <sub>E</sub> = 0.1 mA, I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	8.0	–	–	Vdc
Collector Cutoff Current (V <sub>CB</sub> = 60 Vdc, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	0.1	μA <sub>dc</sub>
Emitter Cutoff Current (V <sub>EB</sub> = 6.0 Vdc)	I <sub>EBO</sub>	–	–	0.1	μA <sub>dc</sub>

## ON CHARACTERISTICS

DC Current Gain (Note 4) (I <sub>C</sub> = 10 mA, V <sub>CE</sub> = 2.0 V) (I <sub>C</sub> = 500 mA, V <sub>CE</sub> = 2.0 V) (I <sub>C</sub> = 1.0 A, V <sub>CE</sub> = 2.0 V) (I <sub>C</sub> = 2.0 A, V <sub>CE</sub> = 2.0 V)	h <sub>FE</sub>	160 160 150 100	– – – –	– – 350 –	
Collector - Emitter Saturation Voltage (Note 4) (I <sub>C</sub> = 0.1 A, I <sub>B</sub> = 0.010 A) (I <sub>C</sub> = 1.0 A, I <sub>B</sub> = 0.100 A) (I <sub>C</sub> = 2.0 A, I <sub>B</sub> = 0.200 A)	V <sub>CE(sat)</sub>	– – –	– – –	0.020 0.075 0.140	V
Base - Emitter Saturation Voltage (Note 4) (I <sub>C</sub> = 1.0 A, I <sub>B</sub> = 10 mA)	V <sub>BE(sat)</sub>	–	0.790	0.900	V
Base - Emitter Turn-on Voltage (Note 4) (I <sub>C</sub> = 1.0 A, V <sub>CE</sub> = 2.0 V)	V <sub>BE(on)</sub>	–	0.760	0.900	V
Cutoff Frequency (I <sub>C</sub> = 100 mA, V <sub>CE</sub> = 5.0 V, f = 100 MHz)	f <sub>T</sub>	100	–	–	MHz
Input Capacitance (V <sub>EB</sub> = 0.5 V, f = 1.0 MHz)	C <sub>ibo</sub>	–	–	380	pF
Output Capacitance (V <sub>CB</sub> = 3.0 V, f = 1.0 MHz)	C <sub>obo</sub>	–	–	45	pF

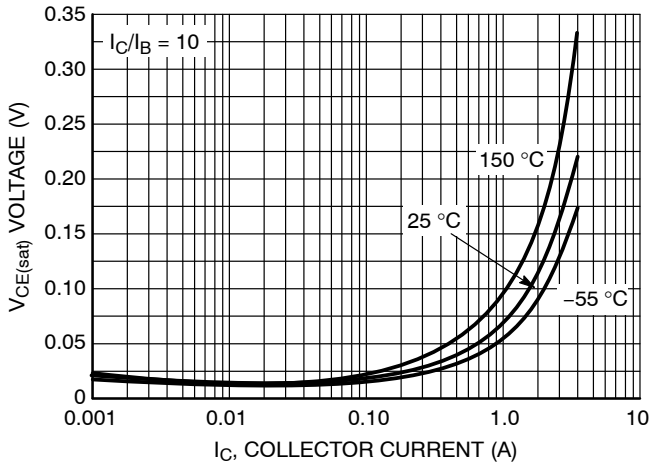
## SWITCHING CHARACTERISTICS

Delay (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>d</sub>	–	–	55	ns
Rise (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>r</sub>	–	–	100	ns
Storage (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>s</sub>	–	–	1100	ns
Fall (V <sub>CC</sub> = 30 V, I <sub>C</sub> = 750 mA, I <sub>B1</sub> = 15 mA)	t <sub>f</sub>	–	–	120	ns

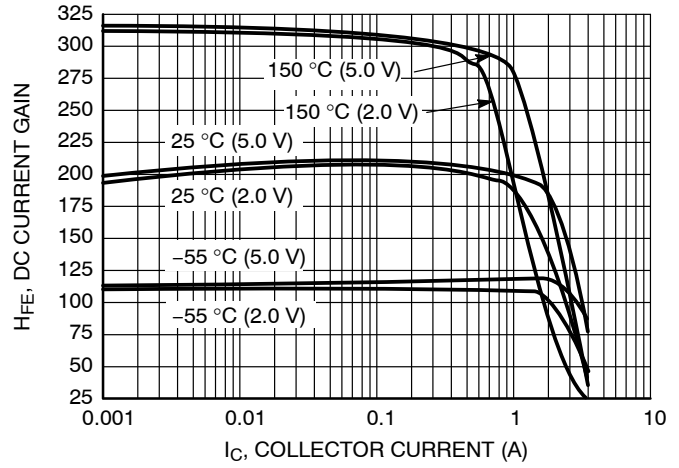
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

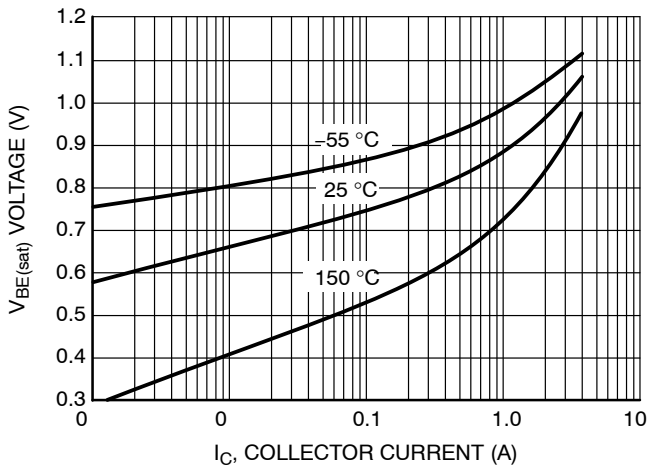
# NSS60201LT1G



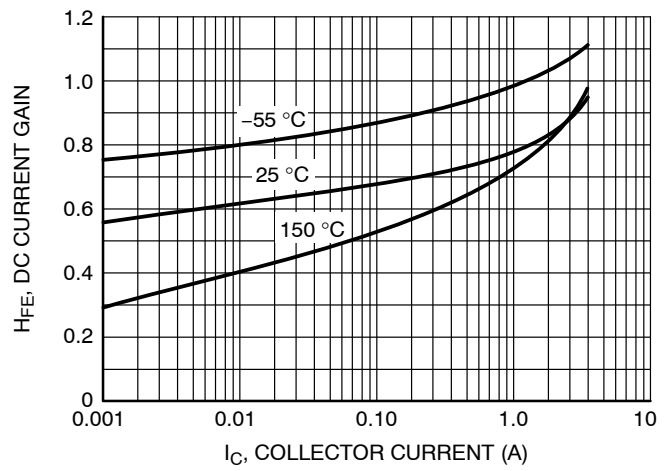
**Figure 1. Collector-Emitter Saturation Voltage**



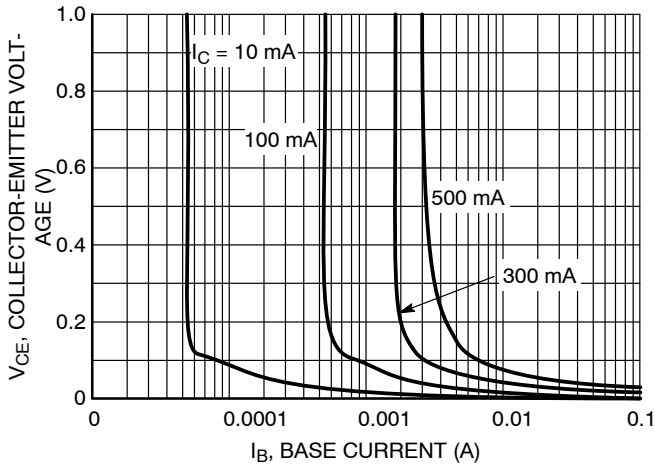
**Figure 2. DC Current versus Collector Current**



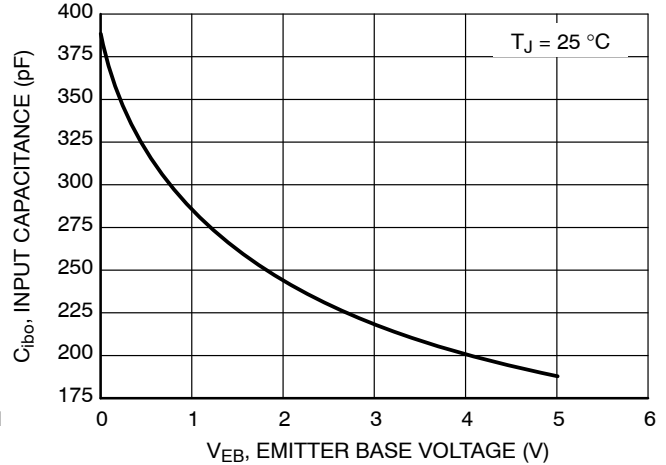
**Figure 3.  $V_{BE(sat)}$**



**Figure 4.  $V_{BE(on)}$**

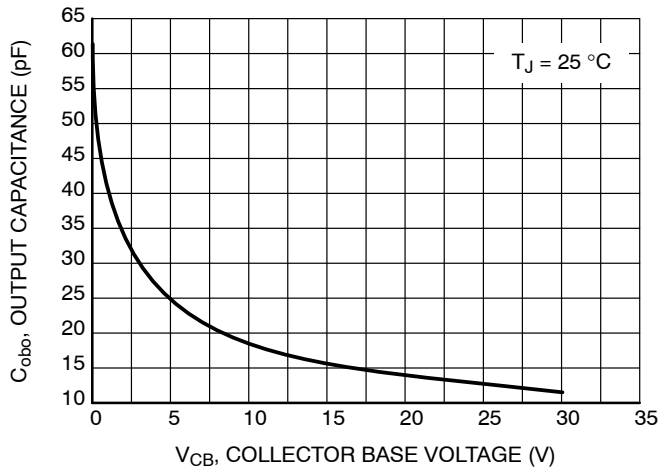


**Figure 5. Saturation Region**

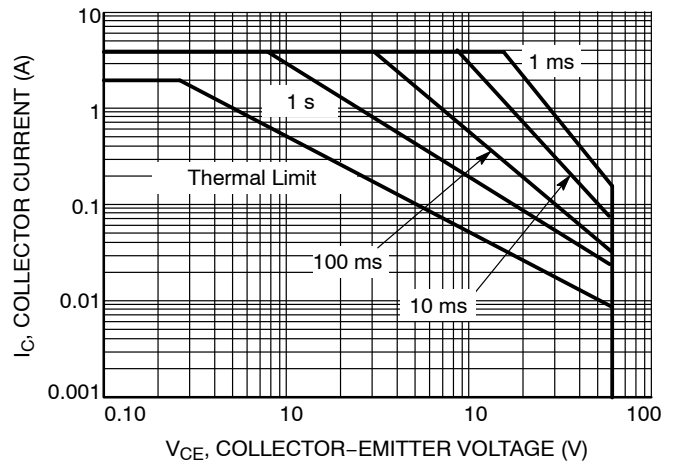


**Figure 6. Input Capacitance**

# NSS60201LT1G



**Figure 7. Output Capacitance**



**Figure 8. Safe Operating Area  
Single Pulse Test @  $T_{amb} = 25\text{ }^\circ\text{C}$**

# NSS60201LT1G

## REVISION HISTORY

Revision	Description of Changes	Date
5	Rebranded the Data Sheet to <b>onsemi</b> format.	10/14/2025

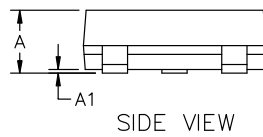
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



SCALE 4:1

**SOT-23 (TO-236) 2.90x1.30x1.00 1.90P**  
CASE 318  
ISSUE AU

DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

**GENERIC MARKING DIAGRAM\***



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**SOT-23 (TO-236) 2.90x1.30x1.00 1.90P**  
**CASE 318**  
**ISSUE AU**

DATE 14 AUG 2024

STYLE 1 THRU 5:  
CANCELLED

STYLE 6:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 7:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 8:  
PIN 1. ANODE  
2. NO CONNECTION  
3. CATHODE

STYLE 9:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 10:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE

STYLE 11:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 12:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 13:  
PIN 1. SOURCE  
2. DRAIN  
3. GATE

STYLE 14:  
PIN 1. CATHODE  
2. GATE  
3. ANODE

STYLE 15:  
PIN 1. GATE  
2. CATHODE  
3. ANODE

STYLE 16:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE

STYLE 17:  
PIN 1. NO CONNECTION  
2. ANODE  
3. CATHODE

STYLE 18:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. ANODE

STYLE 19:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE-ANODE

STYLE 20:  
PIN 1. CATHODE  
2. ANODE  
3. GATE

STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

STYLE 22:  
PIN 1. RETURN  
2. OUTPUT  
3. INPUT

STYLE 23:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 24:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE

STYLE 25:  
PIN 1. ANODE  
2. CATHODE  
3. GATE

STYLE 26:  
PIN 1. CATHODE  
2. ANODE  
3. NO CONNECTION

STYLE 27:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE

STYLE 28:  
PIN 1. ANODE  
2. ANODE  
3. ANODE

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