MP8801

6.5V, 150mA, Low-Noise, Low-Dropout Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP8801 is a low-noise, low-dropout linear regulator. It operates from a 2.7V to 6.5V input voltage (V_{IN}) and regulates the output voltage (V_{OUT}) with 2% accuracy at 2.5V, 2.85V or 3.3V. The internally set V_{OUT} can be overridden via an external resistor divider from 1.25V to 5V.

The MP8801 can supply up to 150mA of load current. It also features thermal shutdown, and is available in a TSOT23-5 package.

FIXED VOLTAGE PART NUMBERS

Part Number	Output Voltage
MP8801DJ-2.5	2.5V
MP8801DJ-2.85	2.85V
MP8801DJ-3.3	3.3V

EVALUATION BOARD REFERENCE

Board Number	Output (1)	Dimensions
EV8801DJ-00A	2.85V	2.0"Xx2.0"Yx0.4"Z

Note:

1) The default V_{OUT} can be set between 1.25V and 5V via an external resistor divider.

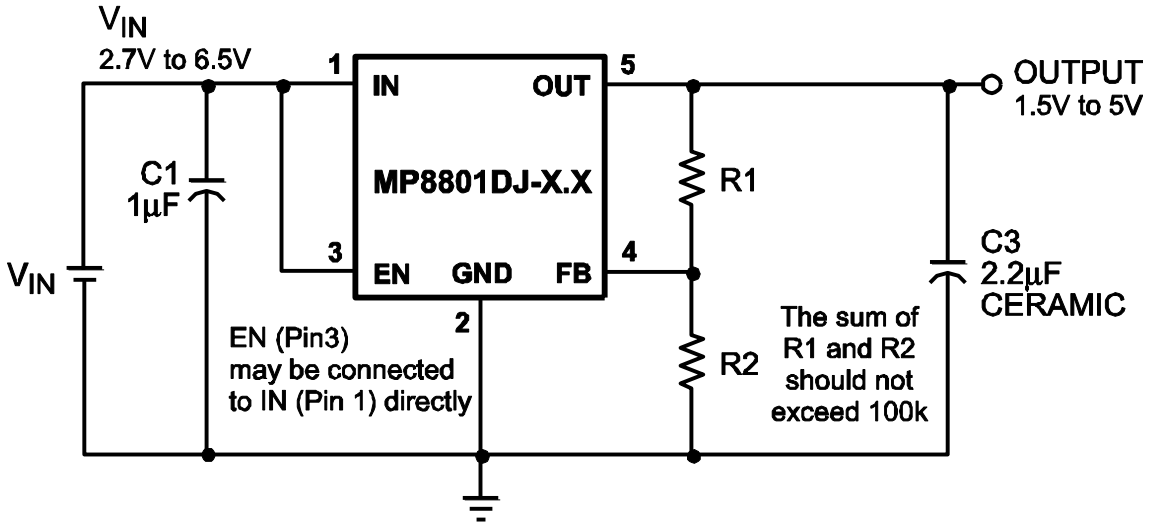
FEATURES

- Low 100mV Dropout at 100mA Output
- 2% Accurate Output Voltage (V_{OUT})
- Fixed V_{OUT} Options of 2.5V, 2.85V, or 3.3V
- Adjustable V_{OUT} from 1.25V to 5V via an External Resistor Divider
- Up to 6.5V Input Voltage (V_{IN})
- High PSRR: 70dB at 1kHz and 30dB at 1MHz
- More than 0.001%/mA Load Regulation
- Stable with Low-ESR Output Capacitor
- Low 125µA Ground Current
- Thermal Shutdown

APPLICATIONS

- 802.11 PC Cards
- Mobile Handset PLL Power
- Audio Codec Power

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP8801DJ-2.5	TSOT23-5	*See Below*	-40°C to +85°C
MP8801DJ-2.85		*See Below*	
MP8801DJ-3.3		*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MP8801DJ-2.85-Z).
For RoHS-compliant packaging, add suffix -LF (e.g. MP8801DJ-2.85-LF-Z).

TOP MARKING

|D2YW

D2: Product code for MP8801DJ-2.5
Y: Year code
W: Week code

TOP MARKING

|C1YW

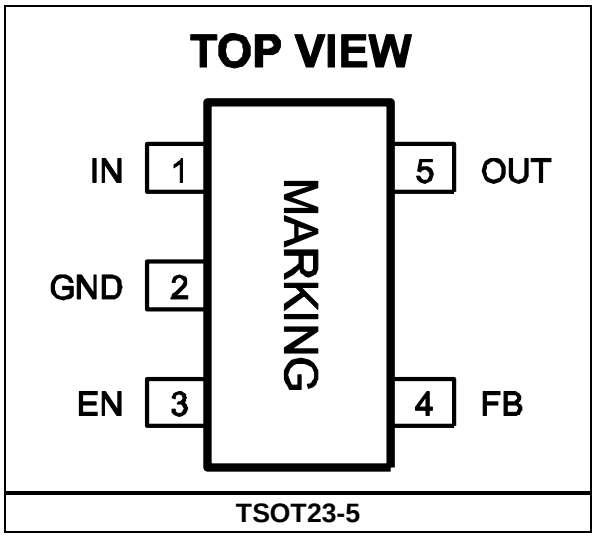
C1: Product code for MP8801DJ-2.85
Y: Year code
W: Week code

TOP MARKING

|D3YW

D3: Product code for MP8801DJ-3.3
Y: Year code
W: Week code

PACKAGE REFERENCE



TSOT23-5

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Power source input.** The IN pin supplies the internal power to the linear regulator. In is also the source for the pass transistor. Bypass IN to GND via a 1µF or greater capacitor.
2	GND	**Ground.**
3	EN	**Enable (EN) input.** Pull the EN pin high to turn the regulator on; pull EN low to turn it off. For automatic start-up, connect the EN and IN pins.
4	FB	**Feedback input.** Connect a resistive voltage divider between the OUT and FB pins to set the output voltage (V_{OUT}). The V_{OUT} feedback threshold is 1.222V.
5	OUT	**Regulator output.** The OUT pin is the output of the linear regulator. Bypass OUT to GND via a 1µF or greater capacitor.

ABSOLUTE MAXIMUM RATINGS (2)

IN supply voltage ..... -0.3V to +7V
FB voltage (V_{FB}) ..... -0.3V to V_{OUT} + 0.3V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (3)
……..0.56W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Input voltage ..... 2.7V to 6.5V
Output voltage ..... 1.25V to 5V
Load current ..... 150mA Maximum
Maximum junction temp (T_J) ..... 125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSOT23-5	220	110 ..°C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions
5) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given is only valid for comparison with other packages and cannot be used for design purposes. Values were calculated in accordance with JESD51-7, and were simulated on a specified JEDEC board. They do not represent the performance obtained in actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ (6)	Max	Units
Operating voltage		I_{OUT} = 1mA		2.7		6.5	V
Ground pin current		I_{OUT} = 1mA to 150mA			125	150	µA
Shutdown current		V_{EN} = 0V, V_{IN} = 5V			0.1	1	µA
FB regulation		Adjustable		1.197	1.222	1.246	V
			-40°C ≤ T_A ≤ 85°C	1.194	1.222	1.249	
Output voltage accuracy		2.5V		2.45	2.5	2.55	V
			-40°C ≤ T_A ≤ 85°C	2.448	2.5	2.562	
		2.85V		2.793	2.85	2.907	V
			-40°C ≤ T_A ≤ 85°C	2.779	2.85	2.921	
		3.3V		3.234	3.3	3.366	V
			-40°C ≤ T_A ≤ 85°C	3.218	3.3	3.382	
Dropout voltage (7)		I_{OUT} = 150mA	V_{OUT} = 3V		150		mV
			V_{OUT} = 4V		125		
Line regulation		I_{OUT} = 1mA, V_{IN} = (V_{OUT} + 0.5V) to 6.5V (8)			0.005		%/V
Load regulation		I_{OUT} = 1mA to 150mA, V_{IN} = V_{OUT} + 0.5V (8)			0.001		%/mA
PSRR		V_{IN} > V_{OUT} + 0.5V, C3 = 2.2µF, V_{IN} (AC) = 100mV, f = 1kHz (6)			70		dB
		V_{IN} > V_{OUT} +0.5V, C3 = 2.2µF, V_{IN} (AC) = 100mV, f = 1MHz (6)			30		dB
Output voltage noise		f = 1kHz, C2 > 0.1µF, I_{OUT} = 1mA (6)			300		nV/√Hz
EN input high voltage				1.5			V
EN input low voltage						0.4	V
EN input bias current		V_{EN} = 0V, 5V			0.01	1	µA
Thermal shutdown threshold (6)					155		°C
Thermal shutdown hysteresis (6)					30		°C

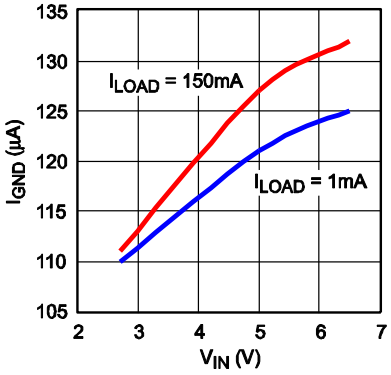
Notes:

6) Derived from bench characterization. Not tested in production.
7) The dropout voltage is defined as the input to output differential once V_{OUT} drops below 1% of its normal value.
8) V_{IN} = 2.7V for V_{OUT} = 1.25V to 2.2V.

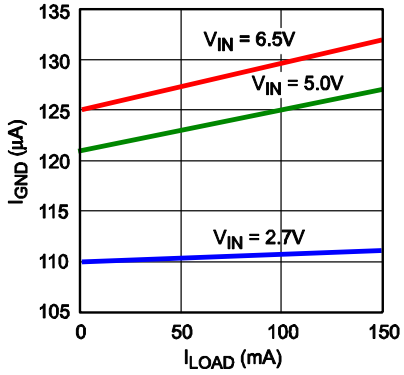
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 4.5V, V_{OUT} = 2.85V, C1 = 1µF, C2 = 0.1µF, C3 = 2.2µF, T_A = 25°C, unless otherwise noted.

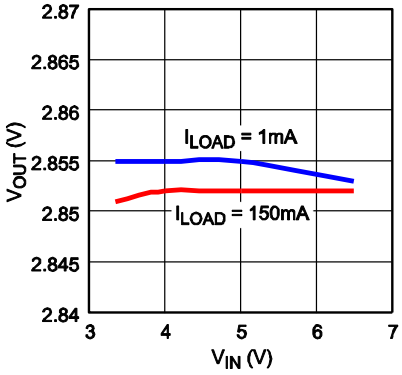
I_{GND} vs V_{IN}



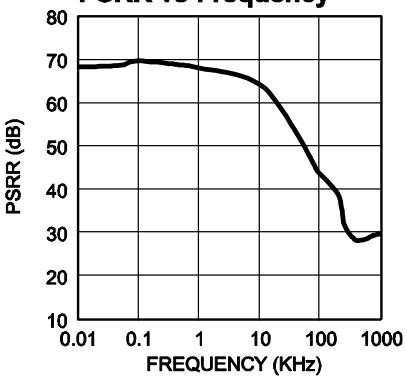
I_{GND} vs I_{LOAD}



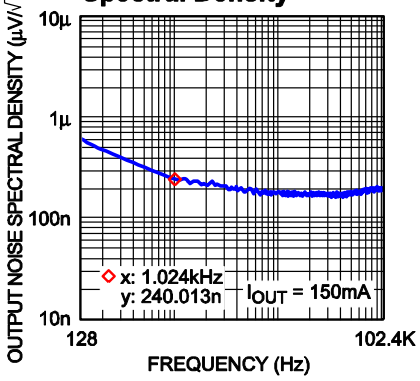
V_{OUT} vs. V_{IN}



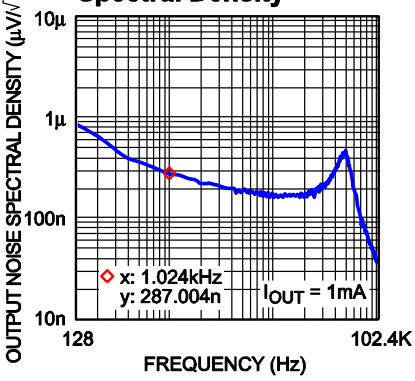
PSRR vs Frequency



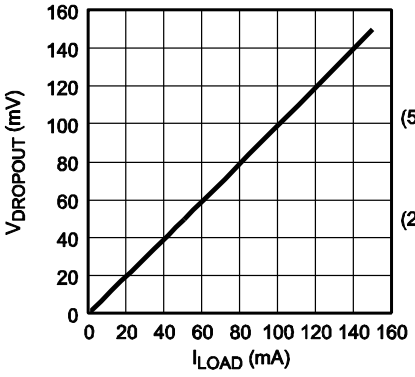
Output Noise Spectral Density



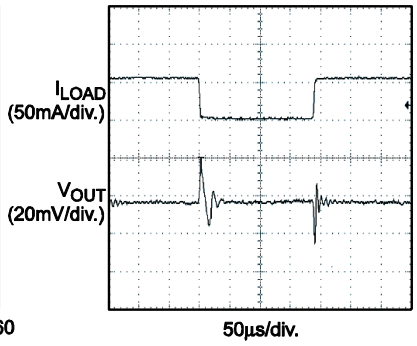
Output Noise Spectral Density



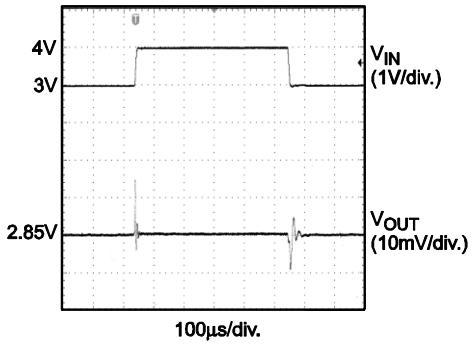
$V_{DROPOUT}$ vs I_{LOAD}



Load-Transient Response
(Circuit in Figure 3)



Line-Transient Response
(Circuit in Figure 3)



OPERATION

The MP8801 is a low-current, low-noise, high-PSRR, low-dropout linear regulator. It is designed for use in devices that require low-noise power supplies and high-PSRR applications, such as PLL VCO supplies for mobile handsets, 802.11 PC Cards, as well as audio codecs and microphones. It also uses a PMOS pass element and features internal thermal shutdown. The MP8801's typically fixed output can be set to 2.5V, 2.85V, or 3.3V, depending on the internal resistor divider (see Figure 1). The fixed output can be converted to an adjustable output via a resistor divider (R1 + R2) (see Figure 2). For improved transient response, add a feed-forward capacitor (C_{BYP}) to the resistor divider.

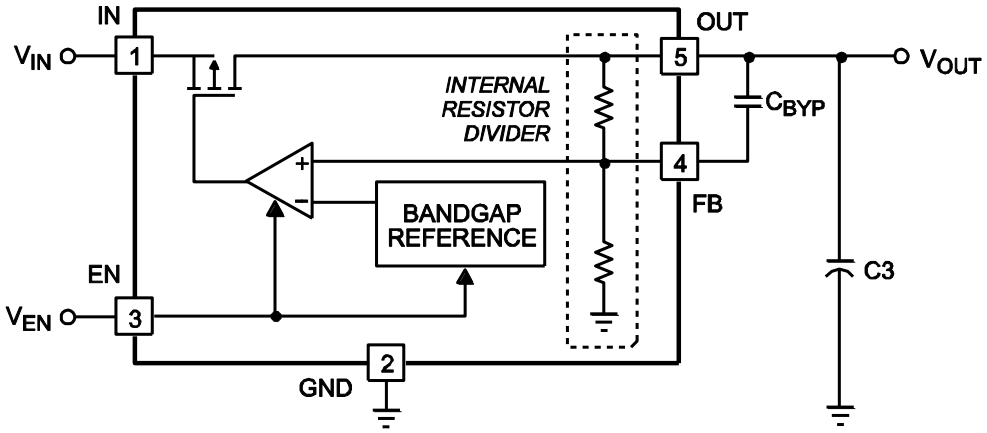


Figure 1: Low-Noise, Fixed Output, Linear Regulator

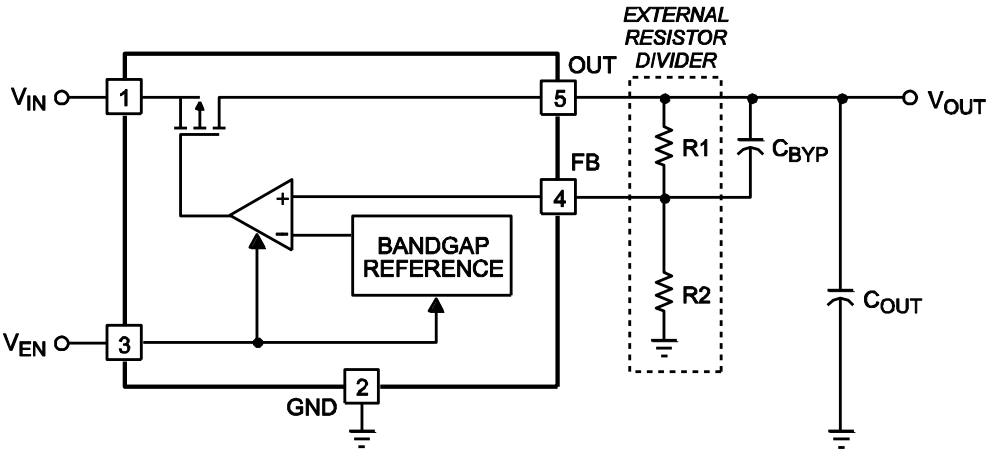


Figure 2: Low-Noise, Adjustable Output, Linear Regulator (V_{OUT} = V_{FB} x 1 + [R1 / R2])

APPLICATION INFORMATION

Setting the Output Voltage

The MP8801's fixed output voltage (V_{OUT}) can be set to 2.5V, 2.85V, or 3.3V, depending on the internal resistor divider. The fixed output can be converted to an adjustable output via an external resistor divider (R1 + R2). To minimize the impact of the internal resistor divider, the sum of R1 and R2 should be below 100kΩ. For an accurate V_{OUT} setting, use a 10kΩ (±1%) resistor for the low-side resistor (R2). Then the high-side resistor (R1) can be calculated with Equation (1):

$$R1 = R2 \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right) \quad (1)$$

Where V_{FB} is the output feedback voltage threshold (1.222V).

For example, if V_{OUT} is 2.5V, then R1 can be calculated with Equation (2):

$$R1 = \frac{2.5V - 1.222V}{\left(\frac{1.222V}{10k\Omega} \right)} = 10.41k\Omega \quad (2)$$

Select a standard 10.5kΩ (±1%) resistor for R1.

Table 1 lists the selected R1 values for typical output voltages.

Table 1: R1 Values for Adjustable V_{OUT}

V_{OUT} (V)	R1 (Ω)	R2 (Ω)
1.25	232Ω	10kΩ
1.5	2.26kΩ	
1.8	4.75kΩ	
2	6.34kΩ	
2.5	10.5kΩ	
2.8	13kΩ	
3	14.7kΩ	
3.3	16.9kΩ	
4	22.6kΩ	
5	30.9kΩ	

A capacitor (C2) can be added for improved transient response (see Figure 3 and Figure 4 on page 9).

Selecting the Input Capacitor

For stable operation, choose a 1µF to 10µF ceramic capacitor (C1) with X5R or X7R dielectrics. Place C1 between the IN pin and ground. A larger-value capacitor improves line transient response; however, a larger-value capacitor also has a larger physical size.

Selecting the Output Capacitor

For stable operation, choose a 1µF to 10µF ceramic capacitor (C3) with X5R or X7R dielectrics. A larger-value capacitor improves load transient response and reduces noise; however, a larger-value capacitor also has a larger physical size. Output capacitors with other dielectric types may be used, but are not recommended as their capacitance can deviate from the rated value over temperature.

To improve load transient response, add a small ceramic (X5R, X7R, or Y5V dielectric) 100nF feed-forward capacitor in parallel with R1. This capacitor is not required for stable operation.

TYPICAL APPLICATION CIRCUITS

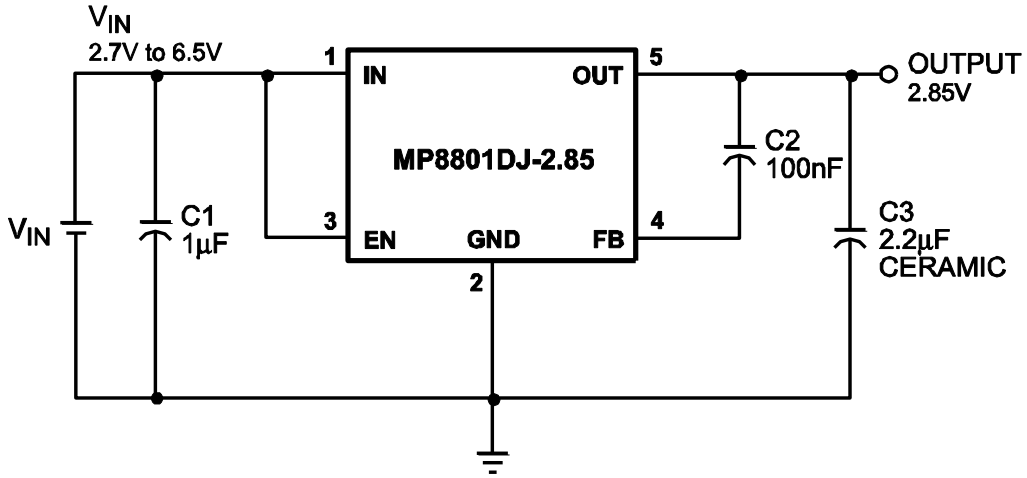


Figure 3: Typical Application Circuit (Fixed Output)

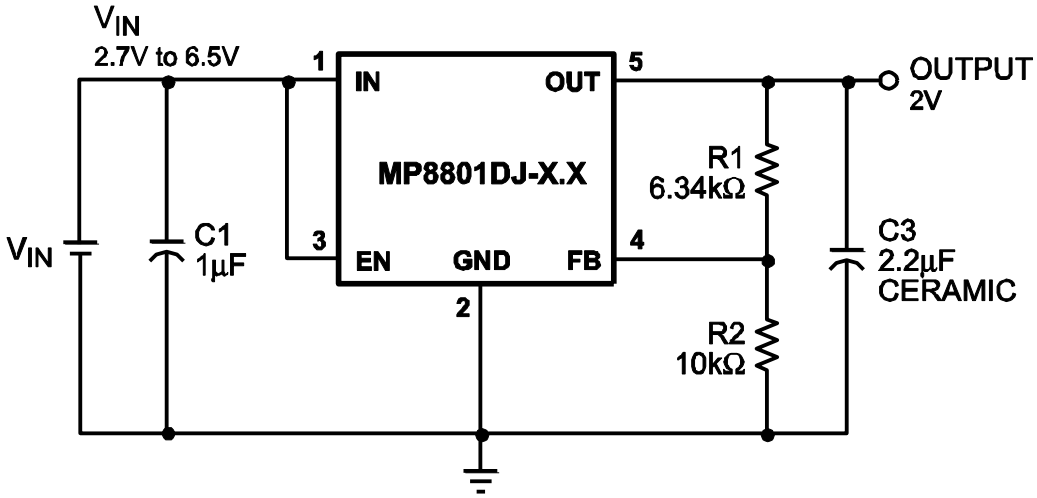


Figure 4: Typical Application Circuit (Adjustable Output)

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the input and output bypass capacitors close to the IN and OUT pins.
2. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the IC as possible.
3. For improved thermal performance, connect the IN, OUT, and GND pins to a large copper area to cool the IC.

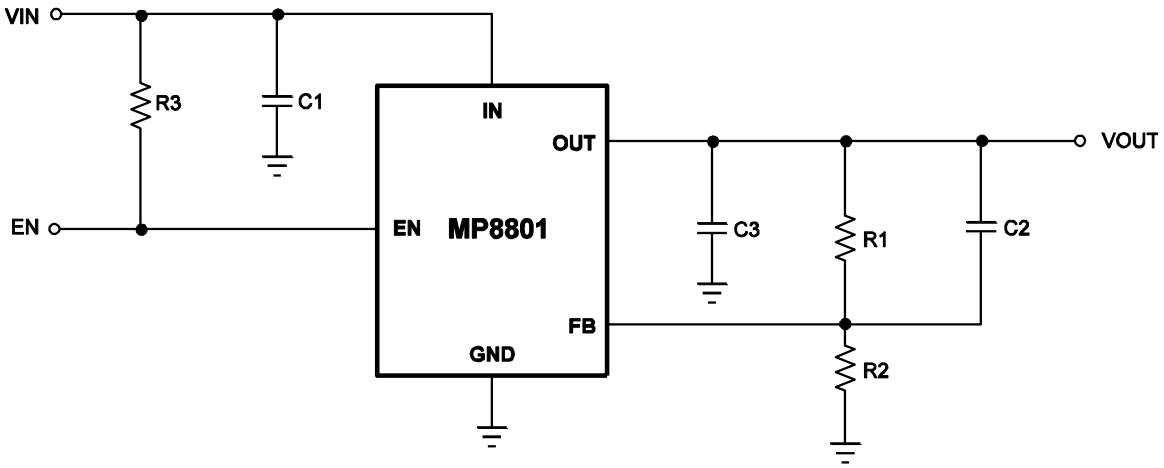


Figure 5: Typical Application Circuit

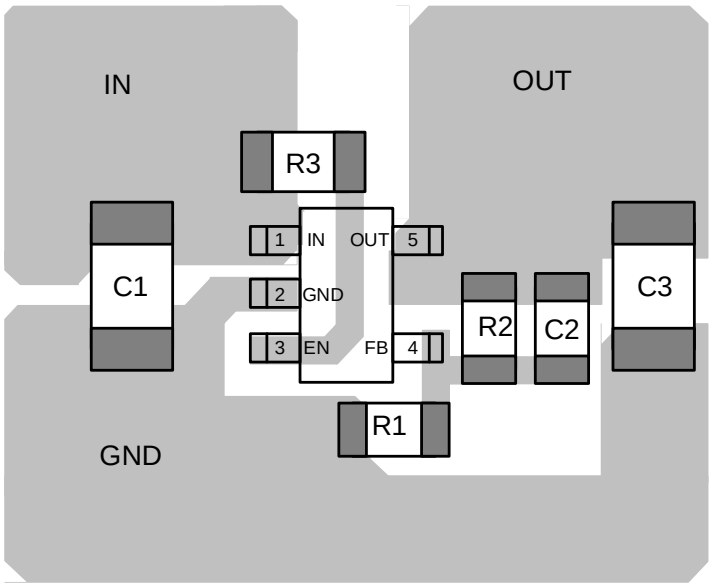
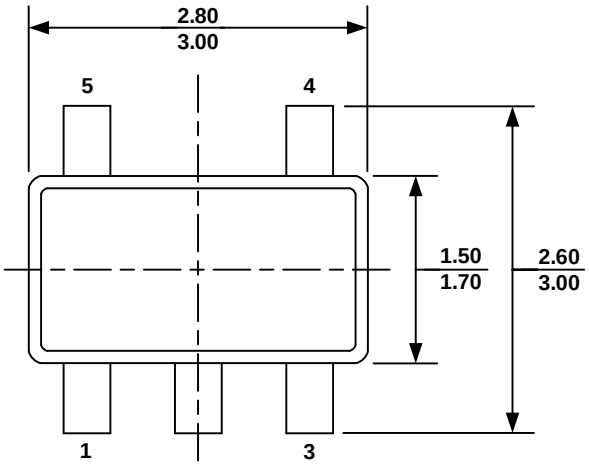


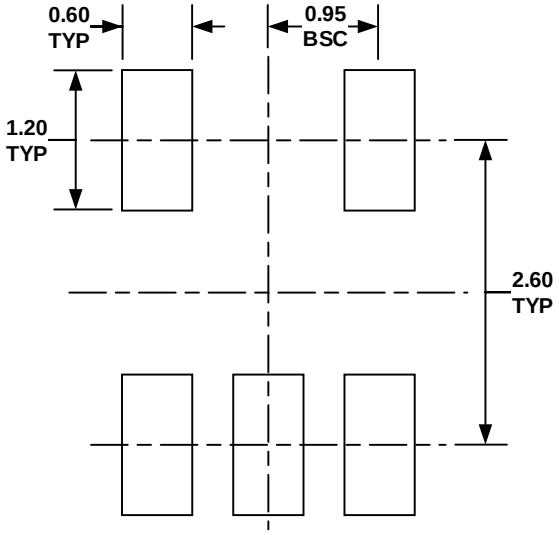
Figure 6: Recommended PCB Layout

PACKAGE INFORMATION

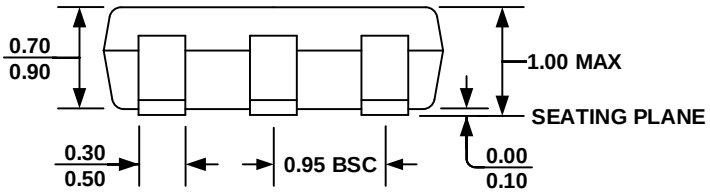
TSOT23-5



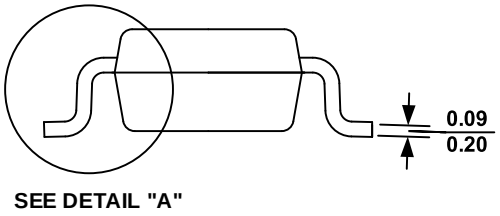
TOP VIEW



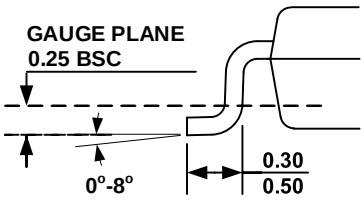
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/6/2004	Initial Release	-
1.1	5/2/2005	Added the 2.5V and 3.3V fixed output voltage options; added Fixed Voltage Part Numbers table; updated “150mV” to “125mV” in the Features section	1
		Formatting updates	All
1.2	6/7/2005	Updated nomenclature	All
1.3	9/21/2005	Updated nomenclature	All
1.4	10/7/2005	Updated page header	11
		Removed watermark	All
1.5	2/21/2006	Added “C2 = 0.1µF” to the conditions in the Typical Performance Characteristics section	6
1.6	3/6/2006	Removed “C2” from Figure 3 (fixed output voltage schematic)	9
1.7	6/27/2008	Updated the Electrical Characteristics section	5
1.8	6/11/2009	Updated the Electrical Characteristics section	5
1.9	10/10/2011	Removed “Output Voltage Accuracy” from the Electrical Characteristics section	5
2.0	7/2/2021	Updated the footnote below the Applications section	1
		Added top marking information	2
		Added equation numbers	8
		Updated the PCB Layout Guidelines section	10
		Grammatical, formatting, and clerical updates; updated headers and footers; updated figure titles; updated footnote numbers; updated pagination	All