

# 8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

High-Performance Silicon-Gate CMOS

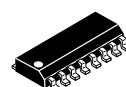
## MC74HC595A, MC74HCT595A

The MC74HC595A/MC74HCT595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

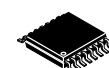
The device directly interfaces with the SPI serial data port on CMOS MPUs and MCUs. The MC74HC595A device inputs are compatible Standard CMOS outputs; with pullup resistors, they are compatible with TTL outputs. The MC74HCT595A device inputs are compatible Standard CMOS or TTL outputs.

### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595/HCT595
  - ◆ Improved Propagation Delays
  - ◆ 50% Lower Quiescent Power
  - ◆ Improved Input Noise and Latchup Immunity
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



SOIC-16  
D SUFFIX  
CASE 751B

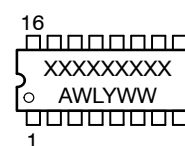


TSSOP-16  
DT SUFFIX  
CASE 948F

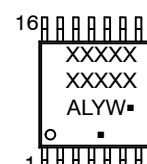


QFN16  
MN SUFFIX  
CASE 485AW

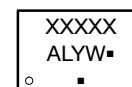
### MARKING DIAGRAMS



SOIC-16



TSSOP-16



QFN16

|       |                     |
|-------|---------------------|
| A     | = Assembly Location |
| WL, L | = Wafer Lot         |
| YY, Y | = Year              |
| WW, W | = Work Week         |
| G, ■  | = Pb-Free Package   |

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

# MC74HC595A, MC74HCT595A

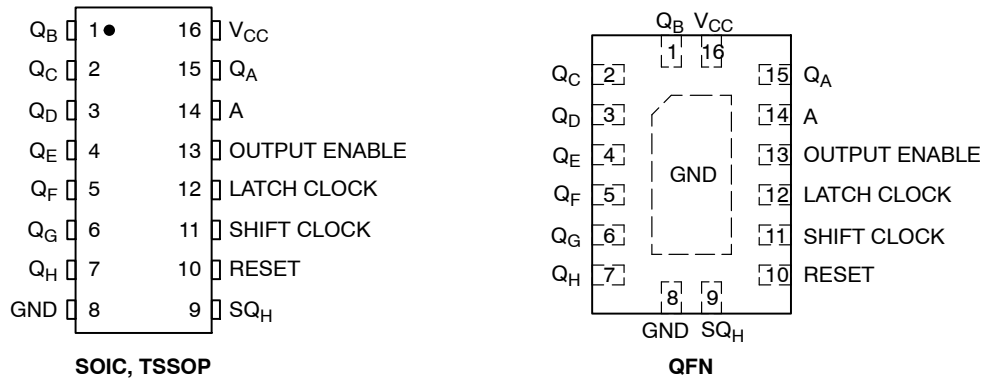
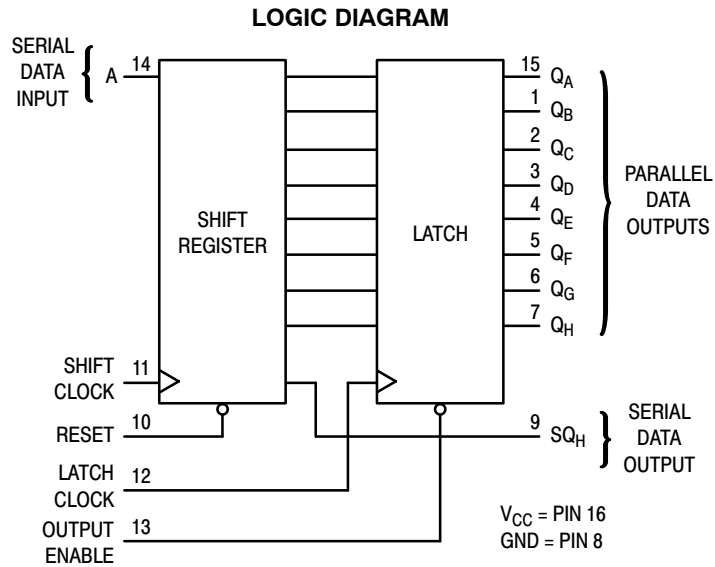


Figure 1. Pin Assignments



# MC74HC595A, MC74HCT595A

## MAXIMUM RATINGS

| Symbol           | Parameter                                                                          | Value                                    | Unit                    |      |
|------------------|------------------------------------------------------------------------------------|------------------------------------------|-------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage                                                                  | −0.5 to +6.5                             | V                       |      |
| V <sub>IN</sub>  | DC Input Voltage                                                                   | −0.5 to V <sub>CC</sub> + 0.5            | V                       |      |
| V <sub>OUT</sub> | DC Output Voltage                                                                  | −0.5 to V <sub>CC</sub> + 0.5            | V                       |      |
| I <sub>IN</sub>  | DC Input Current, per Pin                                                          | ±20                                      | mA                      |      |
| I <sub>OUT</sub> | DC Output Current, per Pin                                                         | ±35                                      | mA                      |      |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                    | ±75                                      | mA                      |      |
| I <sub>IK</sub>  | Input Clamp Current (V <sub>IN</sub> < 0 or V <sub>IN</sub> > V <sub>CC</sub> )    | ±20                                      | mA                      |      |
| I <sub>OK</sub>  | Output Clamp Current (V <sub>OUT</sub> < 0 or V <sub>OUT</sub> > V <sub>CC</sub> ) | ±20                                      | mA                      |      |
| T <sub>STG</sub> | Storage Temperature                                                                | −65 to +150                              | °C                      |      |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 Seconds                                    | 260                                      | °C                      |      |
| T <sub>J</sub>   | Junction Temperature Under Bias                                                    | ±150                                     | °C                      |      |
| θ <sub>JA</sub>  | Thermal Resistance (Note 1)                                                        | SOIC−16<br>QFN16<br>TSSOP−16             | 126<br>118<br>159       | °C/W |
| P <sub>D</sub>   | Power Dissipation in Still Air at 25°C                                             | SOIC−16<br>QFN16<br>TSSOP−16             | 995<br>1062<br>787      | mW   |
| MSL              | Moisture Sensitivity                                                               | Level 1                                  | –                       |      |
| F <sub>R</sub>   | Flammability Rating                                                                | Oxygen Index: 28 to 34                   | UL 94 V−0 @<br>0.125 in | –    |
| V <sub>ESD</sub> | ESD Withstand Voltage (Note 2)                                                     | Human Body Model<br>Charged Device Model | >3000<br>>1000          | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

| Symbol                             | Parameter                                    | Min                                                                           | Max                     | Unit |
|------------------------------------|----------------------------------------------|-------------------------------------------------------------------------------|-------------------------|------|
| <b>MC74HC</b>                      |                                              |                                                                               |                         |      |
| V <sub>CC</sub>                    | DC Supply Voltage                            | 2.0                                                                           | 6.0                     | V    |
| V <sub>IN</sub> , V <sub>OUT</sub> | DC Input Voltage, Output Voltage (Note 3)    | 0                                                                             | V <sub>CC</sub>         | V    |
| T <sub>A</sub>                     | Operating Free-Air Temperature               | −55                                                                           | +125                    | °C   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise or Fall Time                      | V <sub>CC</sub> = 2.0 V<br>V <sub>CC</sub> = 4.5 V<br>V <sub>CC</sub> = 6.0 V | 0<br>1000<br>500<br>400 | ns   |
| <b>MC74HCT</b>                     |                                              |                                                                               |                         |      |
| V <sub>CC</sub>                    | DC Supply Voltage                            | 4.5                                                                           | 5.5                     | V    |
| V <sub>IN</sub> , V <sub>OUT</sub> | DC Input Voltage, DC Output Voltage (Note 3) | 0                                                                             | V <sub>CC</sub>         | V    |
| T <sub>A</sub>                     | Operating Free-Air Temperature               | −55                                                                           | +125                    | °C   |
| t <sub>r</sub> , t <sub>f</sub>    | Input Rise or Fall Time                      | 0                                                                             | 500                     | ns   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

# MC74HC595A, MC74HCT595A

## DC ELECTRICAL CHARACTERISTICS (MC74HC595A)

| Symbol          | Parameter                                                          | Test Conditions                                                                                                                     | V <sub>CC</sub><br>V     | Guaranteed Limit          |                           |                           | Unit |
|-----------------|--------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|--------------------------|---------------------------|---------------------------|---------------------------|------|
|                 |                                                                    |                                                                                                                                     |                          | -55 to<br>25°C            | ≤ 85°C                    | ≤ 125°C                   |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage                                   | V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>OUT</sub>   ≤ 20 μA                                                  | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                                    | V <sub>OUT</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>OUT</sub>   ≤ 20 μA                                                  | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V    |
| V <sub>OH</sub> | Minimum High-Level Output Voltage, Q <sub>A</sub> - Q <sub>H</sub> | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                                                                |                          |                           |                           |                           | V    |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 20 μA                                                                                                          | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 2.4 mA                                                                                                         | 3.0                      | 2.48                      | 2.34                      | 2.2                       |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 6.0 mA                                                                                                         | 4.5                      | 3.98                      | 3.84                      | 3.7                       |      |
| V <sub>OL</sub> | Minimum Low-Level Output Voltage, Q <sub>A</sub> - Q <sub>H</sub>  | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                                                                |                          |                           |                           |                           | V    |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 20 μA                                                                                                          | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 2.4 mA                                                                                                         | 3.0                      | 0.26                      | 0.33                      | 0.4                       |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 6.0 mA                                                                                                         | 4.5                      | 0.26                      | 0.33                      | 0.4                       |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage, SQ <sub>H</sub>                 | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                                                                |                          |                           |                           |                           | V    |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 20 μA                                                                                                          | 2.0<br>4.5<br>6.0        | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         | 1.9<br>4.4<br>5.9         |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 2.4 mA                                                                                                         | 3.0                      | 2.48                      | 2.34                      | 2.2                       |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 4.0 mA                                                                                                         | 4.5                      | 3.98                      | 3.84                      | 3.7                       |      |
| V <sub>OL</sub> | Minimum Low-Level Output Voltage, SQ <sub>H</sub>                  | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                                                                |                          |                           |                           |                           | V    |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 20 μA                                                                                                          | 2.0<br>4.5<br>6.0        | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         | 0.1<br>0.1<br>0.1         |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 2.4 mA                                                                                                         | 3.0                      | 0.26                      | 0.33                      | 0.4                       |      |
|                 |                                                                    | I <sub>OUT</sub>   ≤ 4.0 mA                                                                                                         | 4.5                      | 0.26                      | 0.33                      | 0.4                       |      |
| I <sub>IN</sub> | Maximum Input Leakage Current                                      | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                                            | 6.0                      | ±0.1                      | ±1.0                      | ±1.0                      | μA   |
| I <sub>OZ</sub> | Maximum Three-State Leakage Current                                | Output in High-Impedance State<br>V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>OUT</sub> = V <sub>CC</sub> or GND | 6.0                      | ±0.5                      | ±5.0                      | ±10                       | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package)                     | V <sub>IN</sub> = V <sub>CC</sub> or GND                                                                                            | 6.0                      | 4.0                       | 40                        | 160                       | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74HC595A, MC74HCT595A

## AC ELECTRICAL CHARACTERISTICS (MC74HC595A)

| Symbol                                 | Parameter                                                                                                | V <sub>CC</sub><br>V     | Guaranteed Limit       |                        |                        | Unit |
|----------------------------------------|----------------------------------------------------------------------------------------------------------|--------------------------|------------------------|------------------------|------------------------|------|
|                                        |                                                                                                          |                          | –55 to 25°C            | ≤ 85°C                 | ≤ 125°C                |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 7)                                            | 2.0<br>3.0<br>4.5<br>6.0 | 6.0<br>15<br>30<br>35  | 4.8<br>10<br>24<br>28  | 4.0<br>8.0<br>20<br>24 | MHz  |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Shift Clock to SQ <sub>H</sub><br>(Figures 1 and 7)                           | 2.0<br>3.0<br>4.5<br>6.0 | 140<br>100<br>28<br>24 | 175<br>125<br>35<br>30 | 210<br>150<br>42<br>36 | ns   |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to SQ <sub>H</sub><br>(Figures 2 and 7)                                 | 2.0<br>3.0<br>4.5<br>6.0 | 145<br>100<br>29<br>25 | 180<br>125<br>36<br>31 | 220<br>150<br>44<br>38 | ns   |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Latch Clock to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 3 and 7)           | 2.0<br>3.0<br>4.5<br>6.0 | 140<br>100<br>28<br>24 | 175<br>125<br>35<br>30 | 210<br>150<br>42<br>36 | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 4 and 8)         | 2.0<br>3.0<br>4.5<br>6.0 | 150<br>100<br>30<br>26 | 190<br>125<br>38<br>33 | 225<br>150<br>45<br>38 | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 4 and 8)         | 2.0<br>3.0<br>4.5<br>6.0 | 135<br>90<br>27<br>23  | 170<br>110<br>34<br>29 | 205<br>130<br>41<br>35 | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 3 and 7)                     | 2.0<br>3.0<br>4.5<br>6.0 | 60<br>23<br>12<br>10   | 75<br>27<br>15<br>13   | 90<br>31<br>18<br>15   | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, SQ <sub>H</sub><br>(Figures 1 and 7)                                     | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>27<br>15<br>13   | 95<br>32<br>19<br>16   | 110<br>36<br>22<br>19  | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                                                | –                        | 10                     | 10                     | 10                     | pF   |
| C <sub>out</sub>                       | Maximum Three–State Output Capacitance (Output in High–Impedance State), Q <sub>A</sub> – Q <sub>H</sub> | –                        | 15                     | 15                     | 15                     | pF   |

|                 |                                              |                                         |    |
|-----------------|----------------------------------------------|-----------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|                 |                                              | 300                                     |    |

# MC74HC595A, MC74HCT595A

## TIMING REQUIREMENTS (MC74HC595A)

| Symbol                          | Parameter                                                            | V <sub>CC</sub><br>V | Guaranteed Limit |         |          | Unit |
|---------------------------------|----------------------------------------------------------------------|----------------------|------------------|---------|----------|------|
|                                 |                                                                      |                      | 25 °C to –55 °C  | ≤ 85 °C | ≤ 125 °C |      |
| t <sub>su</sub>                 | Minimum Setup Time, Serial Data Input A to Shift Clock<br>(Figure 5) | 2.0                  | 50               | 65      | 75       | ns   |
|                                 |                                                                      | 3.0                  | 40               | 50      | 60       |      |
|                                 |                                                                      | 4.5                  | 10               | 13      | 15       |      |
|                                 |                                                                      | 6.0                  | 9.0              | 11      | 13       |      |
| t <sub>su</sub>                 | Minimum Setup Time, Shift Clock to Latch Clock<br>(Figure 6)         | 2.0                  | 75               | 95      | 110      | ns   |
|                                 |                                                                      | 3.0                  | 60               | 70      | 80       |      |
|                                 |                                                                      | 4.5                  | 15               | 19      | 22       |      |
|                                 |                                                                      | 6.0                  | 13               | 16      | 19       |      |
| t <sub>h</sub>                  | Minimum Hold Time, Shift Clock to Serial Data Input A<br>(Figure 5)  | 2.0                  | 5.0              | 5.0     | 5.0      | ns   |
|                                 |                                                                      | 3.0                  | 5.0              | 5.0     | 5.0      |      |
|                                 |                                                                      | 4.5                  | 5.0              | 5.0     | 5.0      |      |
|                                 |                                                                      | 6.0                  | 5.0              | 5.0     | 5.0      |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Shift Clock<br>(Figure 2)   | 2.0                  | 50               | 65      | 75       | ns   |
|                                 |                                                                      | 3.0                  | 40               | 50      | 60       |      |
|                                 |                                                                      | 4.5                  | 10               | 13      | 15       |      |
|                                 |                                                                      | 6.0                  | 9.0              | 11      | 13       |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 2)                             | 2.0                  | 60               | 75      | 90       | ns   |
|                                 |                                                                      | 3.0                  | 45               | 60      | 70       |      |
|                                 |                                                                      | 4.5                  | 12               | 15      | 18       |      |
|                                 |                                                                      | 6.0                  | 10               | 13      | 15       |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Shift Clock<br>(Figure 1)                       | 2.0                  | 50               | 65      | 75       | ns   |
|                                 |                                                                      | 3.0                  | 40               | 50      | 60       |      |
|                                 |                                                                      | 4.5                  | 10               | 13      | 15       |      |
|                                 |                                                                      | 6.0                  | 9.0              | 11      | 13       |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Latch Clock<br>(Figure 6)                       | 2.0                  | 50               | 65      | 75       | ns   |
|                                 |                                                                      | 3.0                  | 40               | 50      | 60       |      |
|                                 |                                                                      | 4.5                  | 10               | 13      | 15       |      |
|                                 |                                                                      | 6.0                  | 9.0              | 11      | 13       |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)                      | 2.0                  | 1000             | 1000    | 1000     | ns   |
|                                 |                                                                      | 3.0                  | 800              | 800     | 800      |      |
|                                 |                                                                      | 4.5                  | 500              | 500     | 500      |      |
|                                 |                                                                      | 6.0                  | 400              | 400     | 400      |      |

# MC74HC595A, MC74HCT595A

## DC ELECTRICAL CHARACTERISTICS (MC74HCT595A)

| Symbol           | Parameter                                                            | Test Conditions                                                                                                                     | V <sub>CC</sub><br>V | Guaranteed Limit |             |         | Unit |
|------------------|----------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------------|------------------|-------------|---------|------|
|                  |                                                                      |                                                                                                                                     |                      | – 55 to 25°C     | ≤ 85°C      | ≤ 125°C |      |
| V <sub>IH</sub>  | Minimum High–Level Input Voltage                                     | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                  | 4.5 to 5.5           | 2.0              | 2.0         | 2.0     | V    |
| V <sub>IL</sub>  | Maximum Low–Level Input Voltage                                      | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> – 0.1 V<br> I <sub>out</sub>   ≤ 20 μA                                                  | 4.5 to 5.5           | 0.8              | 0.8         | 0.8     | V    |
| V <sub>OH</sub>  | Minimum High–Level Output Voltage, Q <sub>A</sub> – Q <sub>H</sub>   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                 | 4.5                  | 4.4              | 4.4         | 4.4     | V    |
|                  |                                                                      | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA                                                   | 4.5                  | 3.98             | 3.84        | 3.7     |      |
| V <sub>OL</sub>  | Maximum Low–Level Output Voltage, Q <sub>A</sub> – Q <sub>H</sub>    | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                 | 4.5                  | 0.1              | 0.1         | 0.1     | V    |
|                  |                                                                      | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA                                                   | 4.5                  | 0.26             | 0.33        | 0.4     |      |
| V <sub>OH</sub>  | Minimum High–Level Output Voltage, SQ <sub>H</sub>                   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                 | 4.5                  | 4.4              | 4.4         | 4.4     | V    |
|                  |                                                                      | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA                                                   | 4.5                  | 3.98             | 3.84        | 3.7     |      |
| V <sub>OL</sub>  | Maximum Low–Level Output Voltage, SQ <sub>H</sub>                    | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                 | 4.5                  | 0.1              | 0.1         | 0.1     | V    |
|                  |                                                                      | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA                                                   | 4.5                  | 0.26             | 0.33        | 0.4     |      |
| I <sub>in</sub>  | Maximum Input Leakage Current                                        | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                            | 5.5                  | ± 0.1            | ± 1.0       | ± 1.0   | μA   |
| I <sub>OZ</sub>  | Maximum Three–State Leakage Current, Q <sub>A</sub> – Q <sub>H</sub> | Output in High–Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 5.5                  | ± 0.5            | ± 5.0       | ± 10    | μA   |
| I <sub>CC</sub>  | Maximum Quiescent Supply Current (per Package)                       | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                                                 | 5.5                  | 4.0              | 40          | 160     | μA   |
| ΔI <sub>CC</sub> | Additional Quiescent Supply Current                                  | V <sub>in</sub> = 2.4V, Any One Input<br>V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs<br>I <sub>out</sub> = 0μA           | 5.5                  | ≥ –55°C          | 25 to 125°C |         | mA   |
|                  |                                                                      |                                                                                                                                     |                      | 2.9              | 2.4         |         |      |

# MC74HC595A, MC74HCT595A

## AC ELECTRICAL CHARACTERISTICS (MC74HCT595A)

| Symbol                                 | Parameter                                                                                                | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|----------------------------------------|----------------------------------------------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                                        |                                                                                                          |                      | – 55 to 25°C     | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 7)                                            | 4.5 to 5.5           | 30               | 24     | 20      | MHz  |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Shift Clock to SQ <sub>H</sub><br>(Figures 1 and 7)                           | 4.5 to 5.5           | 28               | 35     | 42      | ns   |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to SQ <sub>H</sub><br>(Figures 2 and 7)                                 | 4.5 to 5.5           | 29               | 36     | 44      | ns   |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Latch Clock to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 3 and 7)           | 4.5 to 5.5           | 28               | 35     | 42      | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 4 and 8)         | 4.5 to 5.5           | 30               | 38     | 45      | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 4 and 8)         | 4.5 to 5.5           | 27               | 34     | 41      | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 3 and 7)                     | 4.5 to 5.5           | 12               | 15     | 18      | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, SQ <sub>H</sub><br>(Figures 1 and 7)                                     | 4.5 to 5.5           | 15               | 19     | 22      | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                                                | —                    | 10               | 10     | 10      | pF   |
| C <sub>out</sub>                       | Maximum Three-State Output Capacitance (Output in High-Impedance State), Q <sub>A</sub> – Q <sub>H</sub> | —                    | 15               | 15     | 15      | pF   |

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|-----------------|----------------------------------------------|-----------------------------------------|----|
|                 |                                              | 300                                     |    |

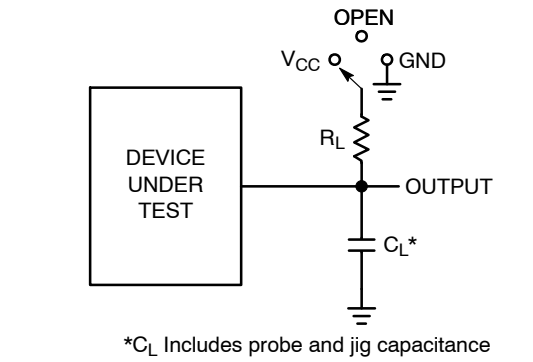
\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## TIMING REQUIREMENTS (MC74HCT595A)

| Symbol                          | Parameter                                                            | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|----------------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                                 |                                                                      |                      | 25°C to –55°C    | ≤ 85°C | ≤ 125°C |      |
| t <sub>su</sub>                 | Minimum Setup Time, Serial Data Input A to Shift Clock<br>(Figure 5) | 4.5 to 5.5           | 10               | 13     | 15      | ns   |
| t <sub>su</sub>                 | Minimum Setup Time, Shift Clock to Latch Clock<br>(Figure 6)         | 4.5 to 5.5           | 15               | 19     | 22      | ns   |
| t <sub>h</sub>                  | Minimum Hold Time, Shift Clock to Serial Data Input A<br>(Figure 5)  | 4.5 to 5.5           | 5.0              | 5.0    | 5.0     | ns   |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Shift Clock<br>(Figure 2)   | 4.5 to 5.5           | 10               | 13     | 15      | ns   |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 2)                             | 4.5 to 5.5           | 12               | 15     | 18      | ns   |
| t <sub>w</sub>                  | Minimum Pulse Width, Shift Clock<br>(Figure 1)                       | 4.5 to 5.5           | 10               | 13     | 15      | ns   |
| t <sub>w</sub>                  | Minimum Pulse Width, Latch Clock<br>(Figure 6)                       | 4.5 to 5.5           | 10               | 13     | 15      | ns   |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)                      | 4.5 to 5.5           | 500              | 500    | 500     | ns   |

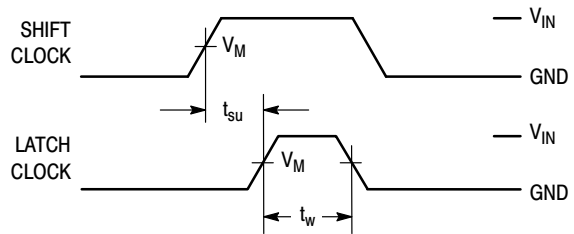
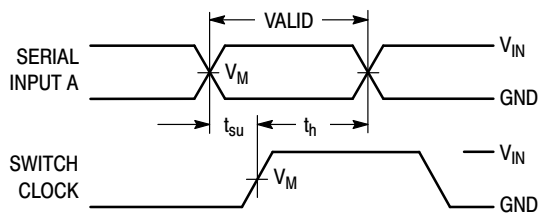
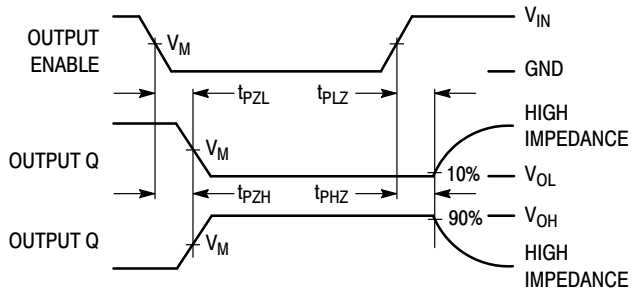
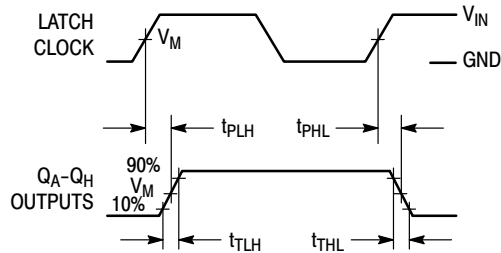
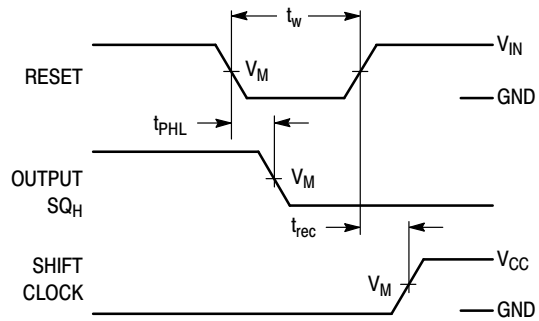
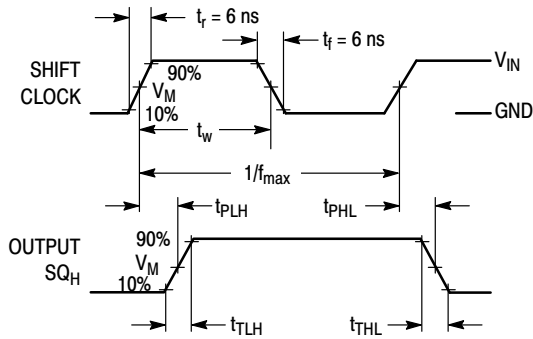


# MC74HC595A, MC74HCT595A



| Test                                | Switch Position | C <sub>L</sub> | R <sub>L</sub> |
|-------------------------------------|-----------------|----------------|----------------|
| t <sub>PLH</sub> / t <sub>PHL</sub> | Open            | 50 pF          | 1 kΩ           |
| t <sub>PLZ</sub> / t <sub>PZL</sub> | V <sub>CC</sub> |                |                |
| t <sub>PHZ</sub> / t <sub>PZH</sub> | GND             |                |                |

Figure 1. Test Circuit



| Device      | V <sub>IN</sub> , V | V <sub>m</sub> , V    |
|-------------|---------------------|-----------------------|
| MC74HC595A  | V <sub>CC</sub>     | 50% x V <sub>CC</sub> |
| MC74HCT595A | 3 V                 | 1.3 V                 |

Figure 2. Switching Waveforms

# MC74HC595A, MC74HCT595A

FUNCTION TABLE

| Operation                                          | Inputs |                |             |             |               | Resulting Function                                           |                                   |                                   |                                                  |
|----------------------------------------------------|--------|----------------|-------------|-------------|---------------|--------------------------------------------------------------|-----------------------------------|-----------------------------------|--------------------------------------------------|
|                                                    | Reset  | Serial Input A | Shift Clock | Latch Clock | Output Enable | Shift Register Contents                                      | Latch Register Contents           | Serial Output SQ <sub>H</sub>     | Parallel Outputs Q <sub>A</sub> – Q <sub>H</sub> |
| Reset shift register                               | L      | X              | X           | L, H, ↓     | L             | L                                                            | U                                 | L                                 | U                                                |
| Shift data into shift register                     | H      | D              | ↑           | L, H, ↓     | L             | D → SR <sub>A</sub> ;<br>SR <sub>N</sub> → SR <sub>N+1</sub> | U                                 | SR <sub>G</sub> → SR <sub>H</sub> | U                                                |
| Shift register remains unchanged                   | H      | X              | L, H, ↓     | L, H, ↓     | L             | U                                                            | U                                 | U                                 | U                                                |
| Transfer shift register contents to latch register | H      | X              | L, H, ↓     | ↑           | L             | U                                                            | SR <sub>N</sub> → LR <sub>N</sub> | U                                 | SR <sub>N</sub>                                  |
| Latch register remains unchanged                   | X      | X              | X           | L, H, ↓     | L             | *                                                            | U                                 | *                                 | U                                                |
| Enable parallel outputs                            | X      | X              | X           | X           | L             | *                                                            | **                                | *                                 | Enabled                                          |
| Force outputs into high impedance state            | X      | X              | X           | X           | H             | *                                                            | **                                | *                                 | Z                                                |

SR = shift register contents  
LR = latch register contents

D = data (L, H) logic level  
U = remains unchanged

↑ = Low-to-High  
↓ = High-to-Low

\* = depends on Reset and Shift Clock inputs  
\*\* = depends on Latch Clock input

## PIN DESCRIPTIONS

### INPUTS

#### A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

### CONTROL INPUTS

#### Shift Clock (Pin 11)

Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

#### Reset (Pin 10)

Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

#### Latch Clock (Pin 12)

Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

#### Output Enable (Pin 13)

Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q<sub>A</sub>–Q<sub>H</sub>) into the high-impedance state. The serial output is not affected by this control unit.

### OUTPUTS

#### Q<sub>A</sub> – Q<sub>H</sub> (Pins 15, 1, 2, 3, 4, 5, 6, 7)

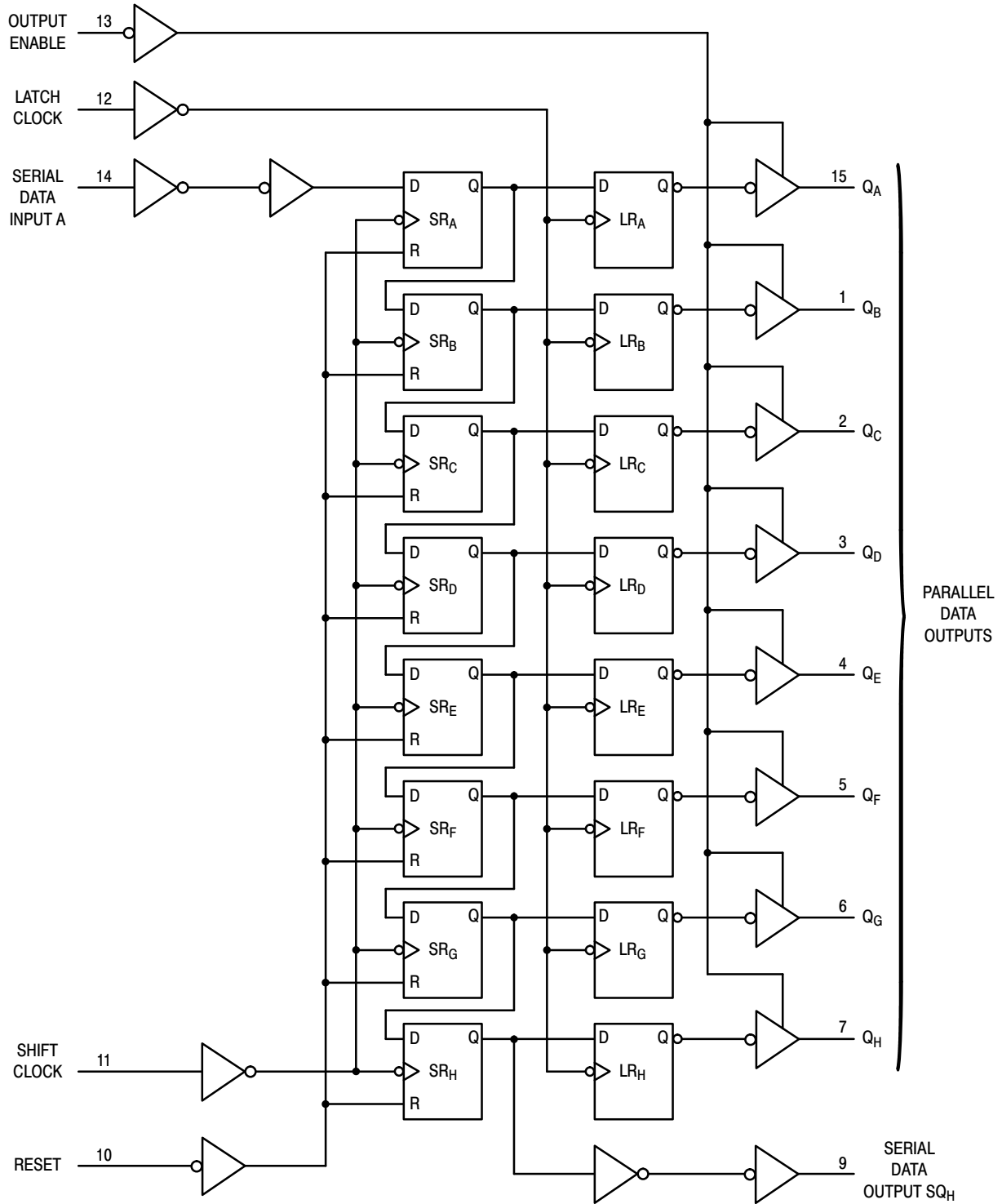
Noninverted, 3-state, latch outputs.

#### SQ<sub>H</sub> (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

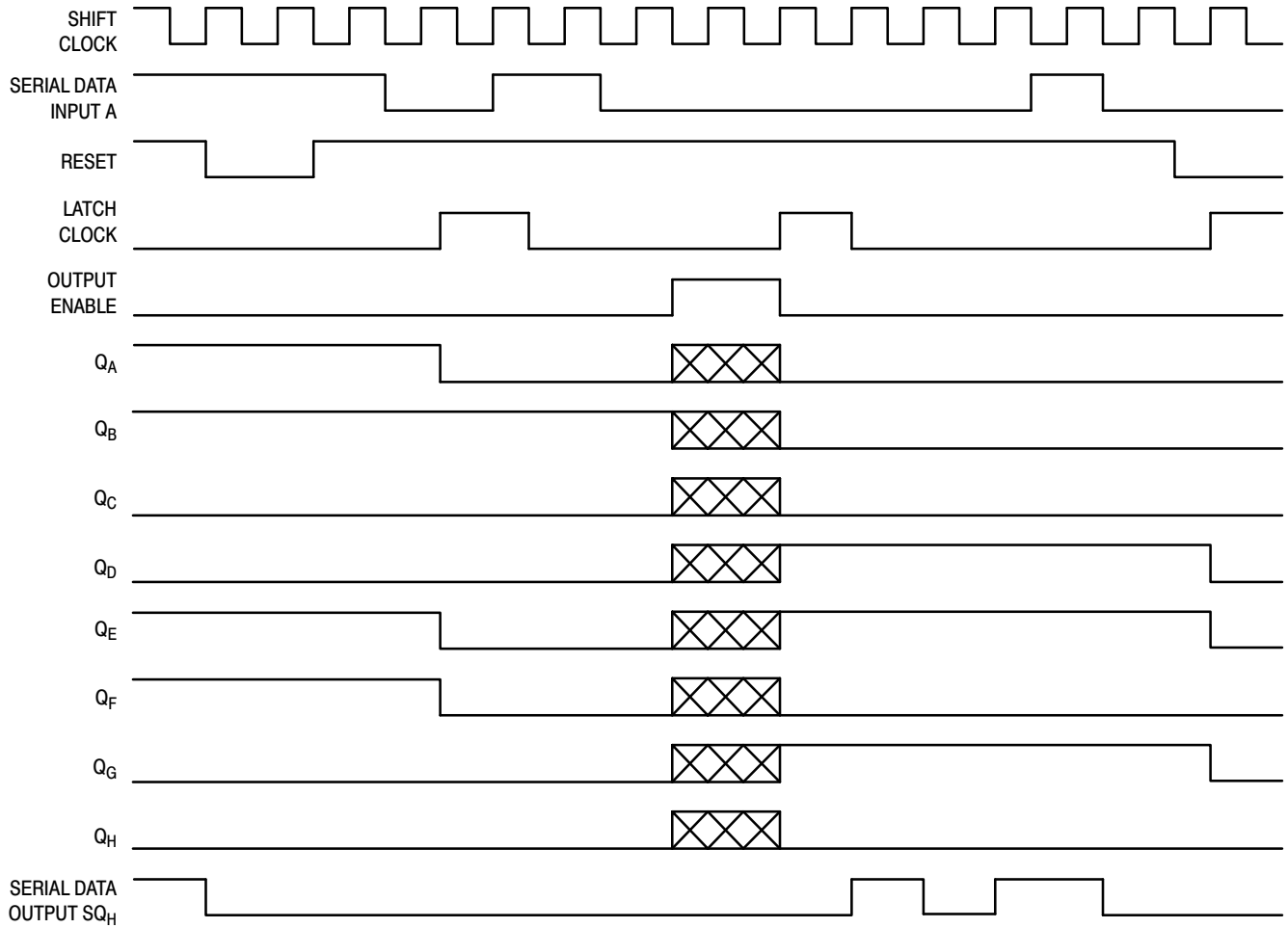
# MC74HC595A, MC74HCT595A

## EXPANDED LOGIC DIAGRAM



# MC74HC595A, MC74HCT595A

## TIMING DIAGRAM



NOTE: **XXX** implies that the output is in a high-impedance state.

## MC74HC595A, MC74HCT595A

### ORDERING INFORMATION

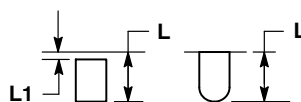
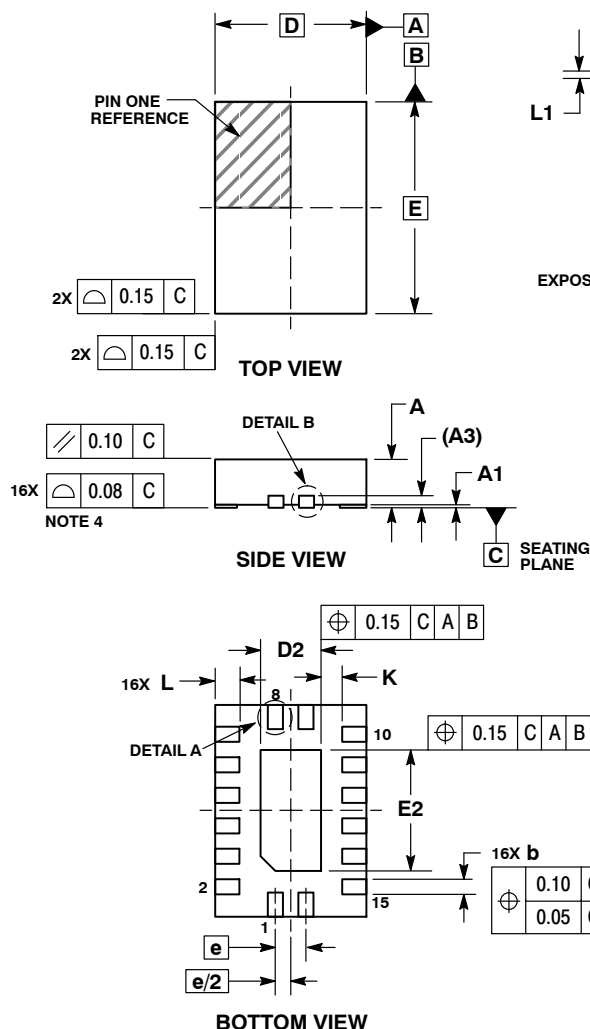
| Device              | Package  | Marking     | Shipping <sup>†</sup>                          |
|---------------------|----------|-------------|------------------------------------------------|
| MC74HC595ADG        | SOIC-16  | HC595A      | 48 Units / Rail                                |
| MC74HC595ADR2G      | SOIC-16  | HC595A      | 2500 / Tape & Reel                             |
| MC74HC595ADR2G-Q*   | SOIC-16  | HC595A      | 2500 / Tape & Reel                             |
| MC74HC595ADTG       | TSSOP-16 | HC<br>595A  | 96 Units / Rail                                |
| MC74HC595ADTR2G     | TSSOP-16 | HC<br>595A  | 2500 / Tape & Reel                             |
| MC74HC595ADTR2G-Q*  | TSSOP-16 | HC<br>595A  | 2500 / Tape & Reel                             |
| MC74HC595AMN1TWG-Q* | QFN16    | V595A       | 3000 / Tape & Reel<br>(8mm pitch carrier tape) |
| MC74HCT595ADG       | SOIC-16  | HCT595A     | 48 Units / Rail                                |
| MC74HCT595ADR2G     | SOIC-16  | HCT595A     | 2500 / Tape & Reel                             |
| MC74HCT595ADTG      | TSSOP-16 | HCT<br>595A | 96 Units / Rail                                |
| MC74HCT595ADTR2G    | TSSOP-16 | HCT<br>595A | 2500 / Tape & Reel                             |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

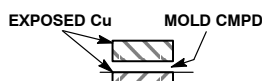
\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable



DATE 11 DEC 2008



**DETAIL A**  
**ALTERNATE TERMINAL**  
**CONSTRUCTIONS**

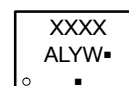


**DETAIL B**  
**ALTERNATE**  
**CONSTRUCTIONS**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.20        | 0.30 |
| D   | 2.50 BSC    |      |
| D2  | 0.85        | 1.15 |
| E   | 3.50 BSC    |      |
| E2  | 1.85        | 2.15 |
| e   | 0.50 BSC    |      |
| L   | 0.20        | ---  |
| L   | 0.35        | 0.45 |
| L1  | ---         | 0.15 |

### GENERIC MARKING DIAGRAM\*

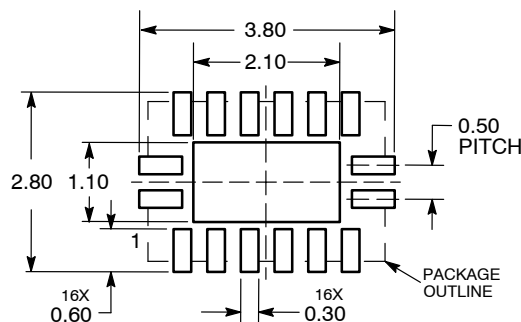


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED SOLDERING FOOTPRINT\*

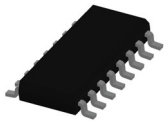


DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                             |                                                                                                                                                                                     |
|-------------------------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98AON36347E</b>          | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>QFN16, 2.5X3.5, 0.5P</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                                  |

**onsemi** and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

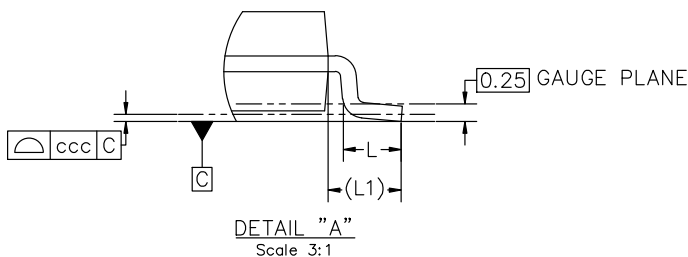
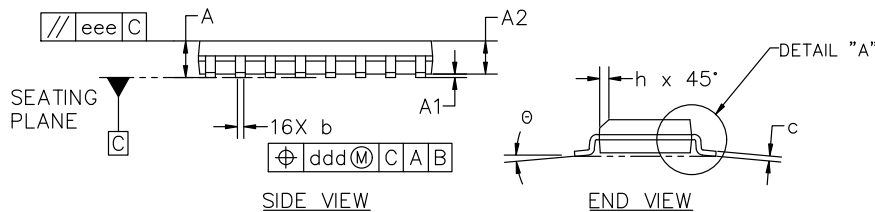
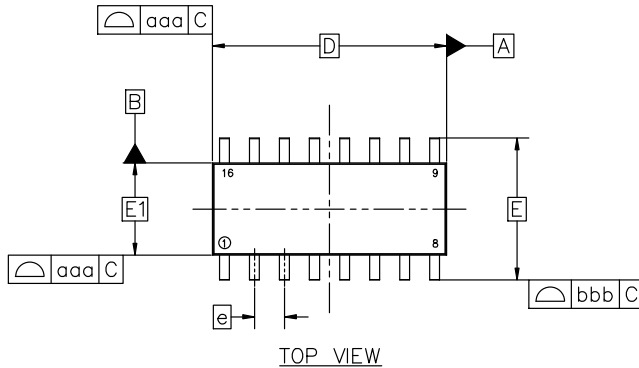


SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

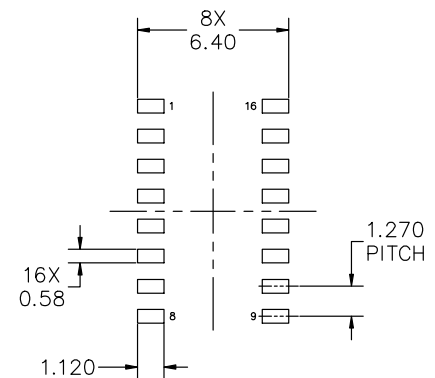
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS                    |          |      |      |
|--------------------------------|----------|------|------|
| DIM                            | MIN      | NOM  | MAX  |
| A                              | 1.35     | 1.55 | 1.75 |
| A1                             | 0.10     | 0.18 | 0.25 |
| A2                             | 1.25     | 1.37 | 1.50 |
| b                              | 0.35     | 0.42 | 0.49 |
| c                              | 0.19     | 0.22 | 0.25 |
| D                              | 9.90 BSC |      |      |
| E                              | 6.00 BSC |      |      |
| E1                             | 3.90 BSC |      |      |
| e                              | 1.27 BSC |      |      |
| h                              | 0.25     | ---  | 0.50 |
| L                              | 0.40     | 0.83 | 1.25 |
| L1                             | 1.05 REF |      |      |
| θ                              | 0°       | ---  | 7°   |
| TOLERANCE OF FORM AND POSITION |          |      |      |
| aaa                            | 0.10     |      |      |
| bbb                            | 0.20     |      |      |
| ccc                            | 0.10     |      |      |
| ddd                            | 0.25     |      |      |
| eee                            | 0.10     |      |      |



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

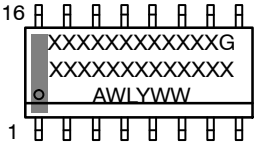
|                  |                              |                                                                                                                                                                                  |
|------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42566B                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-16 9.90X3.90X1.37 1.27P | PAGE 1 OF 2                                                                                                                                                                      |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

DATE 18 OCT 2024

GENERIC  
MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

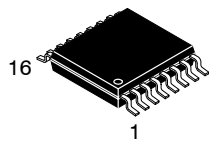
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. COLLECTOR<br>2. BASE<br>3. EMITTER<br>4. NO CONNECTION<br>5. EMITTER<br>6. BASE<br>7. COLLECTOR<br>8. COLLECTOR<br>9. BASE<br>10. EMITTER<br>11. NO CONNECTION<br>12. EMITTER<br>13. BASE<br>14. COLLECTOR<br>15. EMITTER<br>16. COLLECTOR                           | STYLE 2:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION<br>4. CATHODE<br>5. CATHODE<br>6. NO CONNECTION<br>7. ANODE<br>8. CATHODE<br>9. CATHODE<br>10. ANODE<br>11. NO CONNECTION<br>12. CATHODE<br>13. CATHODE<br>14. NO CONNECTION<br>15. ANODE<br>16. CATHODE | STYLE 3:<br>PIN 1. COLLECTOR, DYE #1<br>2. BASE, #1<br>3. EMITTER, #1<br>4. COLLECTOR, #1<br>5. COLLECTOR, #2<br>6. BASE, #2<br>7. EMITTER, #2<br>8. COLLECTOR, #2<br>9. COLLECTOR, #3<br>10. BASE, #3<br>11. EMITTER, #3<br>12. COLLECTOR, #3<br>13. COLLECTOR, #4<br>14. BASE, #4<br>15. EMITTER, #4<br>16. COLLECTOR, #4                                                                                         | STYLE 4:<br>PIN 1. COLLECTOR, DYE #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #3<br>6. COLLECTOR, #3<br>7. COLLECTOR, #4<br>8. COLLECTOR, #4<br>9. BASE, #4<br>10. EMITTER, #4<br>11. BASE, #3<br>12. EMITTER, #3<br>13. BASE, #2<br>14. EMITTER, #2<br>15. BASE, #1<br>16. EMITTER, #1 |
| STYLE 5:<br>PIN 1. DRAIN, DYE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. DRAIN, #3<br>6. DRAIN, #3<br>7. DRAIN, #4<br>8. DRAIN, #4<br>9. GATE, #4<br>10. SOURCE, #4<br>11. GATE, #3<br>12. SOURCE, #3<br>13. GATE, #2<br>14. SOURCE, #2<br>15. GATE, #1<br>16. SOURCE, #1 | STYLE 6:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE<br>4. CATHODE<br>5. CATHODE<br>6. CATHODE<br>7. CATHODE<br>8. CATHODE<br>9. ANODE<br>10. ANODE<br>11. ANODE<br>12. ANODE<br>13. ANODE<br>14. ANODE<br>15. ANODE<br>16. ANODE                                 | STYLE 7:<br>PIN 1. SOURCE N-CH<br>2. COMMON DRAIN (OUTPUT)<br>3. COMMON DRAIN (OUTPUT)<br>4. GATE P-CH<br>5. COMMON DRAIN (OUTPUT)<br>6. COMMON DRAIN (OUTPUT)<br>7. COMMON DRAIN (OUTPUT)<br>8. SOURCE P-CH<br>9. SOURCE P-CH<br>10. COMMON DRAIN (OUTPUT)<br>11. COMMON DRAIN (OUTPUT)<br>12. COMMON DRAIN (OUTPUT)<br>13. GATE N-CH<br>14. COMMON DRAIN (OUTPUT)<br>15. COMMON DRAIN (OUTPUT)<br>16. SOURCE N-CH |                                                                                                                                                                                                                                                                                                                             |

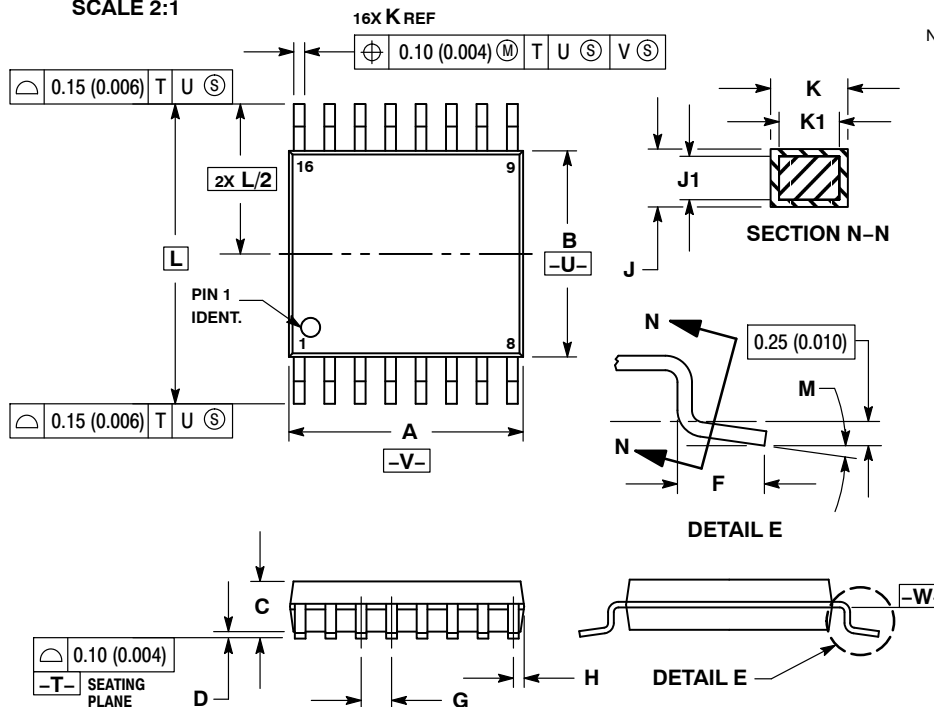
|                  |                              |                                                                                                                                                                                     |
|------------------|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DOCUMENT NUMBER: | 98ASB42566B                  | Electronic versions are uncontrolled except when accessed directly from the Document Repository.<br>Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION:     | SOIC-16 9.90X3.90X1.37 1.27P | PAGE 2 OF 2                                                                                                                                                                         |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



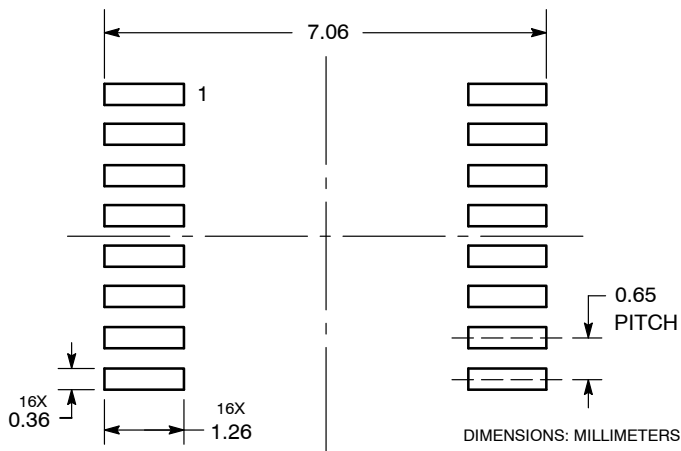
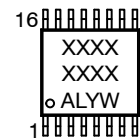

**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                    |                                                                                                                                                                                  |
|-------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>DOCUMENT NUMBER:</b> | <b>98ASH70247A</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>TSSOP-16</b>    | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)