

INA105 Precision Unity Gain Differential Amplifier

1 Features

- Unity-gain difference amplifier configuration
- High common-mode rejection (CMRR): 72dB (minimum)
- Low gain error: 0.025% (maximum)
- Low gain drift: 5ppm/°C (maximum)
- Low nonlinearity: 0.001% (maximum)
- Bandwidth: 1MHz (typical)
- Low offset voltage: 500μV (maximum)
- Low offset voltage drift: 20μV/°C (maximum)

2 Applications

- [Battery cell formation & test equipment](#)
- [Sensor tag & data logger](#)
- [Servo drive position feedback](#)
- [Level transmitter](#)
- [String inverter](#)

3 Description

The INA105 is a monolithic Gain = 1 differential amplifier consisting of a precision operational amplifier (op amp) and on-chip metal film resistor network. The resistors are laser trimmed for accurate gain and high common-mode rejection. Excellent tracking of resistors (TCR) maintains gain accuracy and common-mode rejection over temperature. The input common-mode range extends beyond the positive and negative supply rails.

The differential amplifier is the foundation of many commonly used circuits. The INA105 provides precision circuit function without using an expensive precision resistor network. The INA105 is available in 8-pin plastic DIP, SOIC surface-mount and TO-99 metal packages.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
INA105	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.90mm × 6.00mm
	LMC (TO-CAN, 8)	8.96mm × 8.96mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

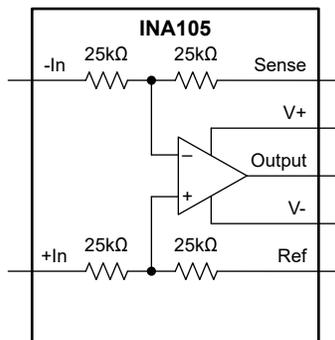


Figure 3-1. Precision Unity Gain Differential Amplifier



Table of Contents

1 Features	1	7.1 Application Information.....	11
2 Applications	1	7.2 Typical Application.....	12
3 Description	1	7.3 Additional Applications.....	12
4 Pin Configuration and Functions	3	7.4 Power Supply Recommendations.....	24
5 Specifications	4	7.5 Layout.....	24
5.1 Absolute Maximum Ratings.....	4	8 Device and Documentation Support	26
5.2 Recommended Operating Conditions.....	4	8.1 Device Support.....	26
5.3 Thermal Information.....	4	8.2 Receiving Notification of Documentation Updates.....	26
5.4 Electrical Characteristics.....	5	8.3 Support Resources.....	26
5.5 Typical Characteristics.....	7	8.4 Trademarks.....	26
6 Detailed Description	9	8.5 Electrostatic Discharge Caution.....	27
6.1 Overview.....	9	8.6 Glossary.....	27
6.2 Functional Block Diagram.....	9	9 Revision History	27
6.3 Feature Description.....	9	10 Mechanical, Packaging, and Orderable Information	28
6.4 Device Functional Modes.....	10		
7 Application and Implementation	11		

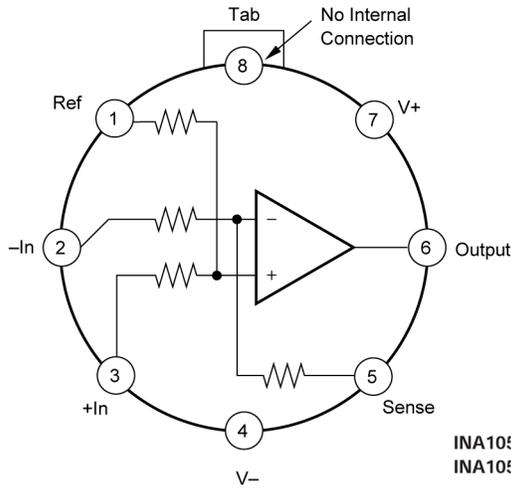
4 Pin Configuration and Functions

Top View

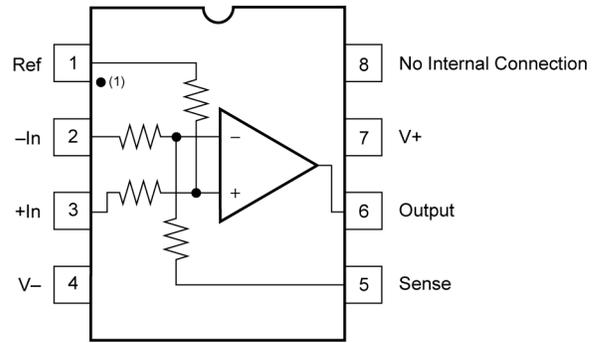
TO-99

Top View

DIP/SOIC



Case internally connected to V-. Make no connection.



NOTE: Performance grade identifier box for small outline surface mount. Blank indicates K grade. Part is marked INA105U.

Table 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
+In	3	Input	Positive (noninverting) input 25kΩ resistor to noninverting terminal of op amp
-In	2	Input	Negative (inverting) input 25kΩ resistor to inverting terminal of op amp
Output	6	Output	Output
Ref	1	Input	Reference input 25kΩ resistor to noninverting terminal of op amp
V+	7	-	Positive (highest) power supply
V-	4	-	Negative (lowest) power supply
Sense	5	Input	Sense input 25kΩ resistor to inverting terminal of op amp
NC	8	-	No internal connection (can be left floating)

5 Specifications

Note

TI has qualified multiple fabrication flows for this device. Differences in performance are labeled by chip site origin (CSO). For system robustness, designing for all flows is highly recommended. For more information, please see [Section 8.1.1](#).

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	36	V
Signal input pins	Single Supply, +In, -In, Sense, and REF	0	V_S	V
Output short-circuit ⁽²⁾		Continuous		
Temperature	Operating, T_A (INA105KP, KU)	-40	85	°C
	Operating, T_A (INA105AM, BM)	-55	125	
	Junction, T_J		150	
	Storage, T_{stg} (INA105KP, KU)	-40	125	
	Storage, T_{stg} (INA105AM, BM)	-65	150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to $V_S / 2$.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single supply	10	30	36	V
	Dual supply	±5	±15	±18	
Specified temperature		-40		85	°C

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		INA105		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.9	74.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	38.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	18.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.7	37.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.4 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, $V_{\text{REF}} = 0\text{V}$, $G = 1$, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OS}	Offset voltage	RTO ^{(1) (2)}	INA105AM, INA105BM		50	250	μV
			INA105KP, KU		50	500	
	Offset voltage drift	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, RTO ^{(1) (2)}	INA105AM		5	20	$\mu\text{V}/^\circ\text{C}$
		INA105BM		5	10		
			INA105KP, KU		5	20	
PSRR	Power-supply rejection ratio	RTO ^{(1) (2)} , $V_S = \pm 6\text{V}$ to $\pm 18\text{V}$	INA105AM		1	25	$\mu\text{V}/\text{V}$
			INA105BM		1	15	
			INA105KP, KU		1	25	
	Long-term stability	RTO ^{(1) (2)}			20		$\mu\text{V}/\text{mo}$
ZIN-DM	Differential impedance ⁽³⁾				50		$\text{k}\Omega$
ZIN-CM	Common-mode impedance ⁽³⁾				50		$\text{k}\Omega$
V_{CM}	Operating common-mode input voltage ⁽⁴⁾			-20		20	V
V_{DM}	Operating differential-mode input voltage ⁽⁴⁾			-10		10	V
CMRR	Common-mode rejection ratio ⁽⁵⁾	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	INA105AM		80	90	dB
			INA105BM		86	100	
			INA105KP, KU		72	90	
NOISE VOLTAGE							
e_N	Voltage noise	RTO ^{(1) (6)}	$f_O = 10\text{kHz}$	CSO: SHE		60	$\text{nV}/\sqrt{\text{Hz}}$
				CSO: RFB		50	
			$f_B = 0.01\text{Hz}$ to 10Hz			2.4	μV_{PP}
GAIN							
GE	Gain error	INA105AM, INA105BM		± 0.005	± 0.01	%	
		INA105KP, KU		± 0.01	± 0.025		
	Gain drift			1	5	$\text{ppm}/^\circ\text{C}$	
	Gain nonlinearity			± 0.0002	± 0.001	% of FSR	
OUTPUT							
	Output voltage	$I_O = -5\text{mA}$, 20mA		10	12		V
	Load capacitance stability				1000		pF
I_{SC}	Short circuit current	Continuous to $V_S / 2$	Sourcing	CSO: SHE		40	mA
				CSO: RFB		70	
			Sinking	CSO: SHE		10	
				CSO: RFB		70	
Z_O	Output Impedance				0.01	Ω	

5.4 Electrical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$, $V_{\text{REF}} = 0\text{V}$, $G = 1$, and all chip site origins (CSO), unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE						
BW	Bandwidth, -3dB			1		MHz
FPBW	Full Power Bandwidth, -3dB	$V_O = 20\text{Vpp}$	30	50		kHz
SR	Slew rate	CSO: SHE	2	3		$\text{V}/\mu\text{s}$
		CSO: RFB		22		
t_s	Settling time	0.1% , $V_{\text{STEP}} = 10\text{V}$		4		μs
		0.01% , $V_{\text{STEP}} = 10\text{V}$		5		
		0.01% , $V_{\text{CM-STEP}} = 10\text{V}$, $V_{\text{DIFF}} = 0\text{V}$		1.5		
POWER SUPPLY						
I_Q	Quiescent current	$V_O = 0\text{V}$		± 1.5	± 2	mA

- (1) Referred to output in unity-gain difference configuration. Note that this circuit has a gain of 2 for the operational amplifier's offset voltage and noise voltage.
- (2) Includes effects of input bias and offset currents of the amplifier.
- (3) $25\text{k}\Omega$ resistors are ratio matched but have $\pm 20\%$ absolute value.
- (4) Maximum input voltage without protection is 10V more than either $\pm 15\text{V}$ supply ($\pm 25\text{V}$). Limit I_{IN} to 1mA.
- (5) With zero source impedance.
- (6) Includes effects of the input current noise of the amplifier and thermal noise contribution of resistor network.

5.5 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and all chip site origins (CSO), unless otherwise noted

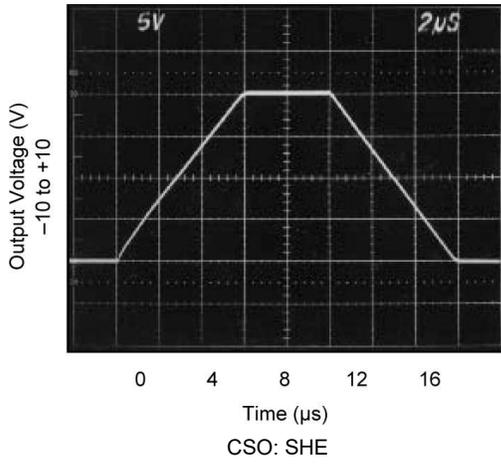


Figure 5-1. Step Response

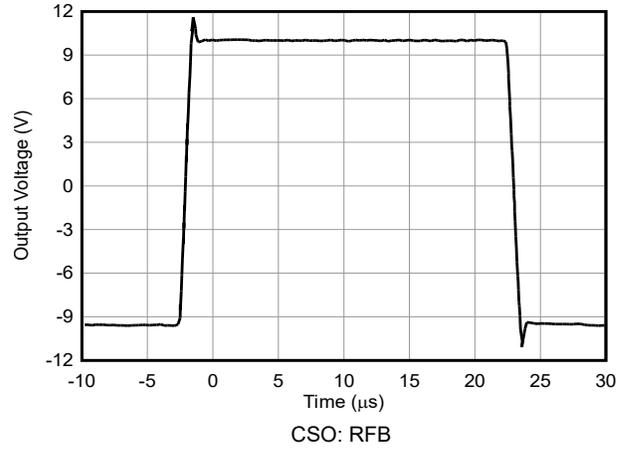


Figure 5-2. Step Response

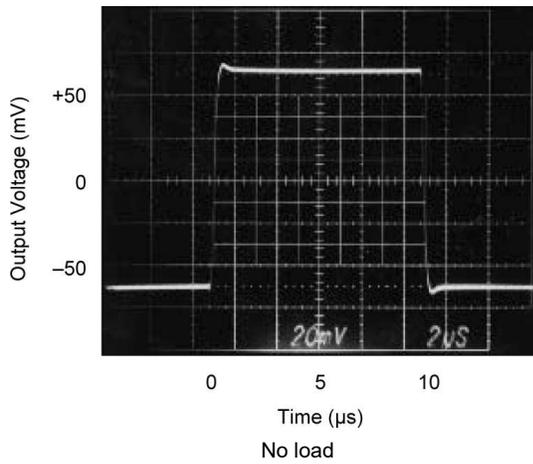


Figure 5-3. Small Signal Response (No Load)

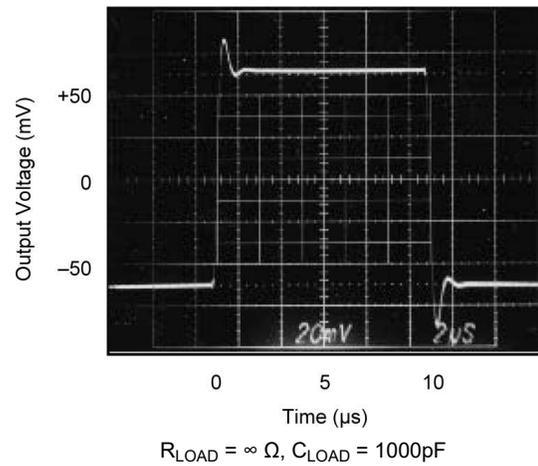


Figure 5-4. Small Signal Response

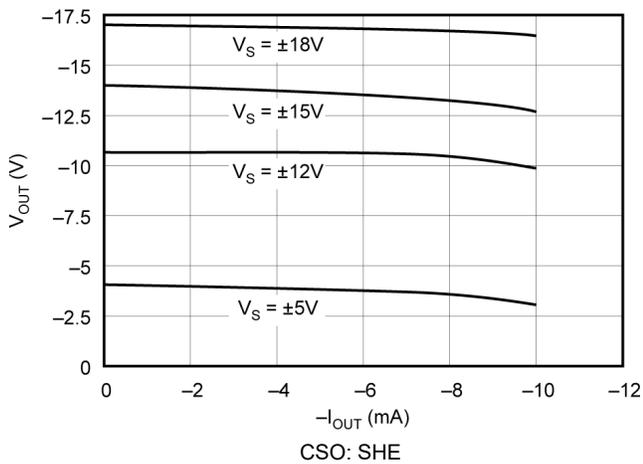


Figure 5-5. Maximum V_{OUT} vs I_{OUT} (Negative Swing)

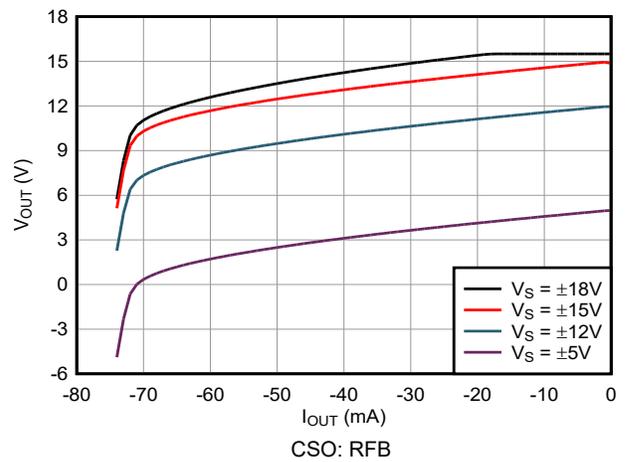


Figure 5-6. Maximum V_{OUT} vs I_{OUT} (Negative Swing)

5.5 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and all chip site origins (CSO), unless otherwise noted

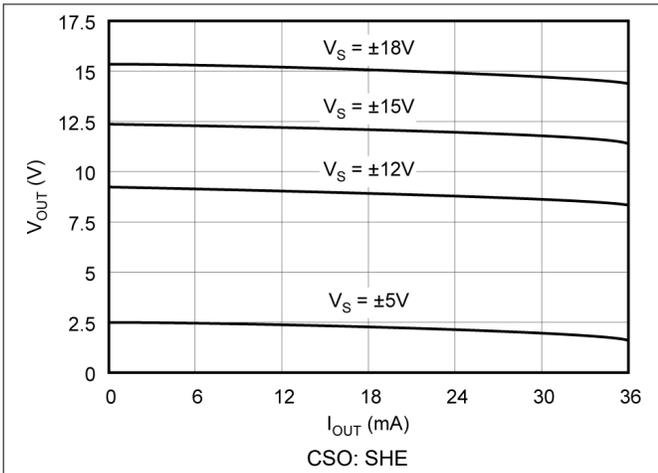


Figure 5-7. Maximum V_{OUT} vs I_{OUT} (Positive Swing)

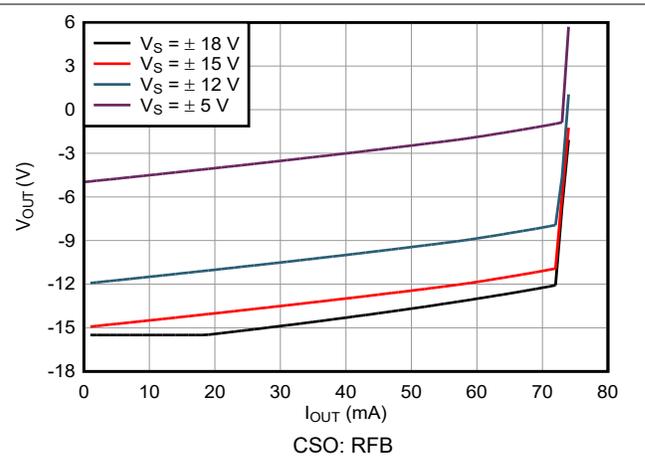


Figure 5-8. Maximum V_{OUT} vs I_{OUT} (Positive Swing)

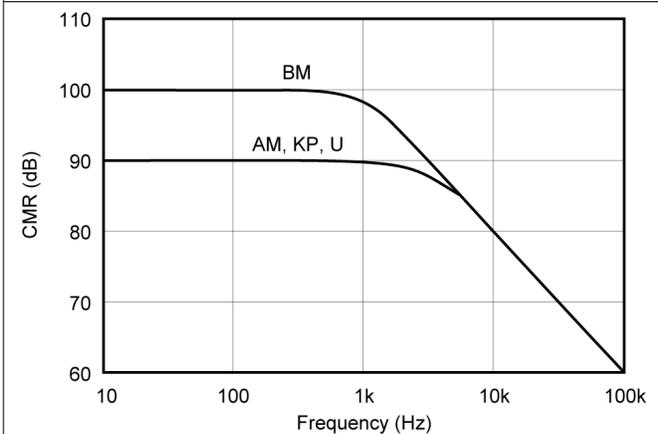


Figure 5-9. CMR vs Frequency

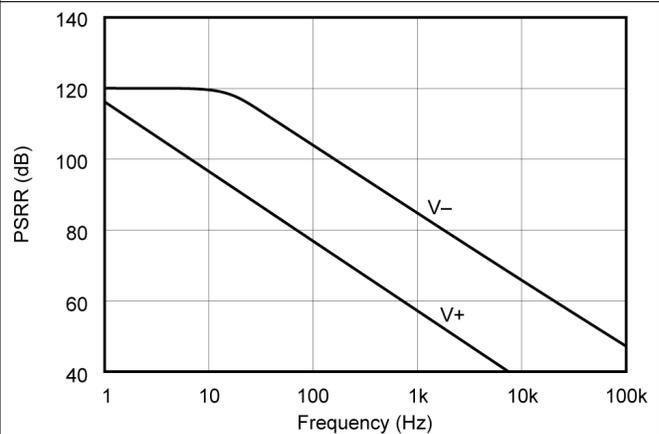


Figure 5-10. Power Supply Rejection vs Frequency

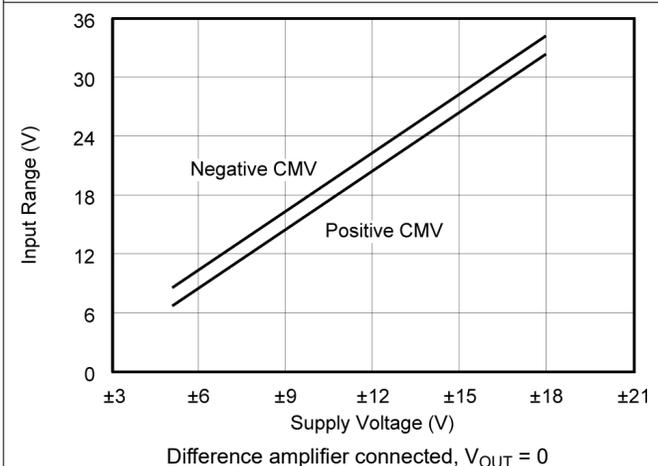


Figure 5-11. Common-Mode Input Range vs Supply

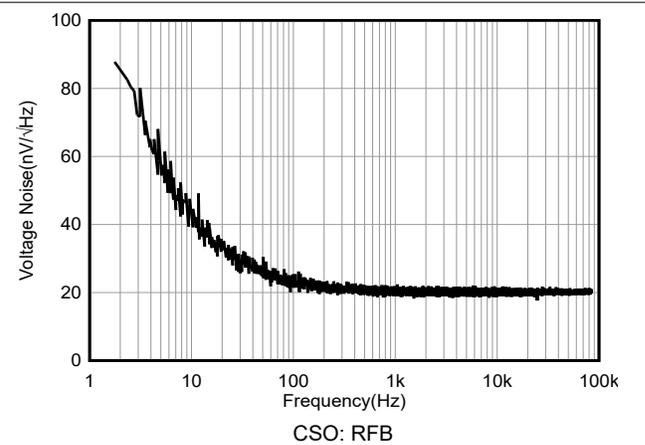


Figure 5-12. Voltage Noise

6 Detailed Description

6.1 Overview

The INA105 consists of a high-precision operational amplifier and four trimmed, on-chip resistors. The device can be configured to make a wide variety of amplifier configurations, including difference, non-inverting, and inverting configurations. The integrated, matched resistors provide an advantage over discrete implementation.

Much of the DC performance of op amp circuits depends on the accuracy of the surrounding resistors. The resistors on the INA105 are laid out to be tightly matched. The resistors of each part are matched on-chip and tested for matching accuracy. As a result, the INA105 provides high accuracy for specifications such as gain drift, common-mode rejection ratio, and gain error.

6.2 Functional Block Diagram

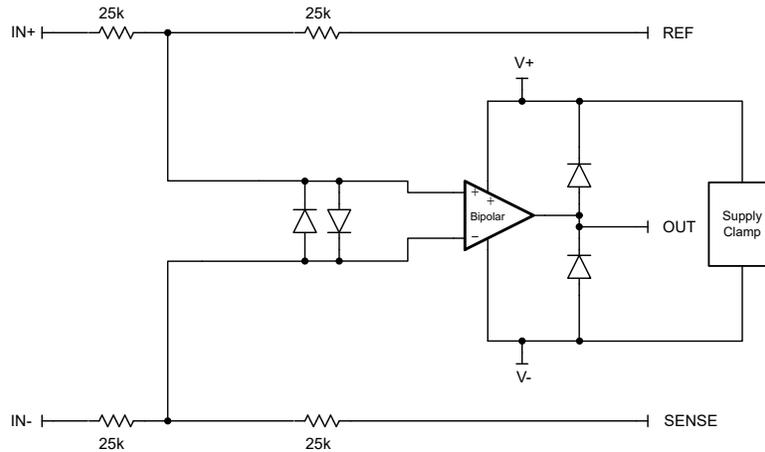


Figure 6-1. INA105 Internal Schematic for CSO:SHE

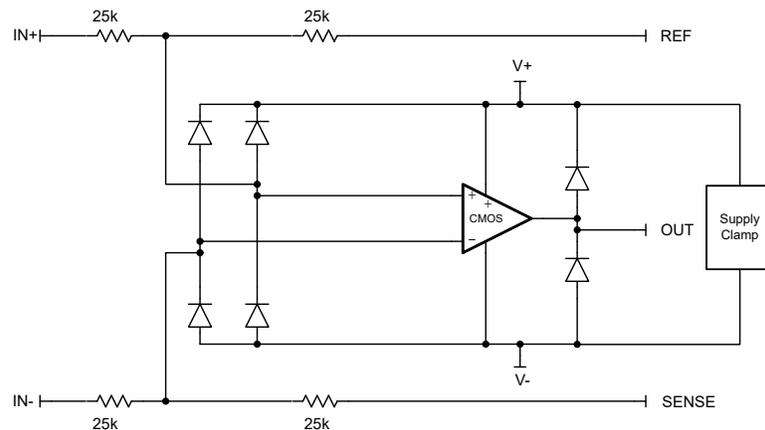


Figure 6-2. INA105 Internal Schematic for CSO:RFB

6.3 Feature Description

6.3.1 Gain Error and Drift

Gain error in the INA105 is limited by the mismatch of the integrated precision resistors. Gain drift is limited by the slight mismatch of the temperature coefficient of integrated resistors. The integrated resistors are precision-matched with low temperature coefficient resistors to improve overall gain drift compared to the discrete implementation of differences amplifiers build when using external resistors.

6.3.2 Input Voltage Range

The INA105 difference amplifier is able to achieve a wide input common-mode voltage range by dividing down the input signal with high-precision resistor divider. The internal resistors divide down the voltage before the voltage reaches the internal op amp and provide protection to the op amp inputs. Figure 6-3 shows an example of how the voltage division works in a difference-amplifier configuration. For the INA105 with a supply voltage of $\pm 15\text{V}$, the input common-mode voltage range is $\pm 20\text{V}$.

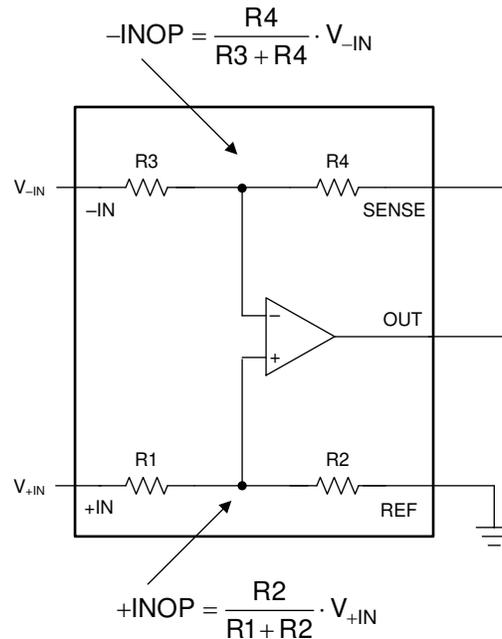


Figure 6-3. Voltage Division in the Difference Amplifier Configuration

6.4 Device Functional Modes

The INA105 has one functional mode. The device is specified on a power supply of $\pm 15\text{V}$ and can operate on a power supply from $\pm 5\text{V}$ to $\pm 18\text{V}$ with derated performance. See [Typical Characteristics](#).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Figure 7-1 shows the basic connections required for operation of the INA105. Connect power-supply bypass capacitors close to the device pins.

The differential input signal is connected to pins 2 and 3, as shown. The source impedances connected to the inputs must be nearly equal for good common-mode rejection. A 5Ω mismatch in source impedance can degrade the common-mode rejection of a typical device to approximately 80dB. If the source has a known mismatch in source impedance, an additional resistor in series with one input can be used to preserve good common-mode rejection.

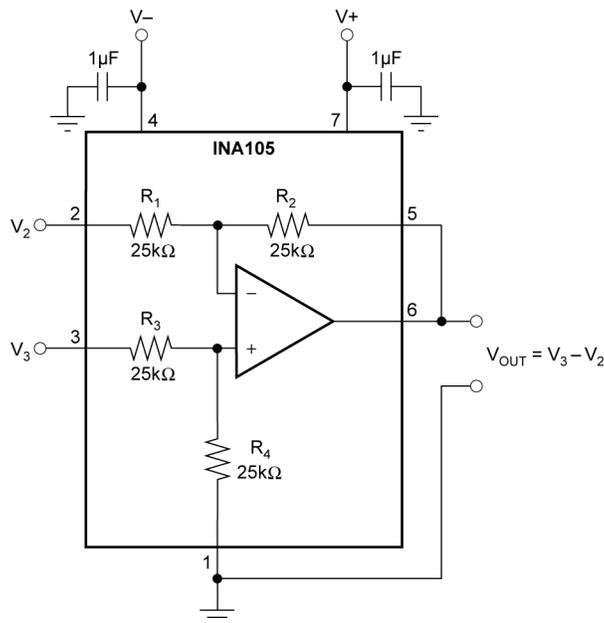


Figure 7-1. Basic Power-Supply and Signal Connections

The output is referred to the output reference terminal (pin 1) which is normally grounded. A voltage applied to the Ref terminal is summed with the output signal. This can be used to null offset voltage as shown in Figure 7-2. To maintain good common-mode rejection, keep the source impedance of a signal applied to the Ref terminal less than 10Ω.

Do not interchange pins 1 and 3 or pins 2 and 5, even though nominal resistor values are equal. These resistors are laser trimmed for precise resistor ratios to achieve accurate gain and highest CMR.

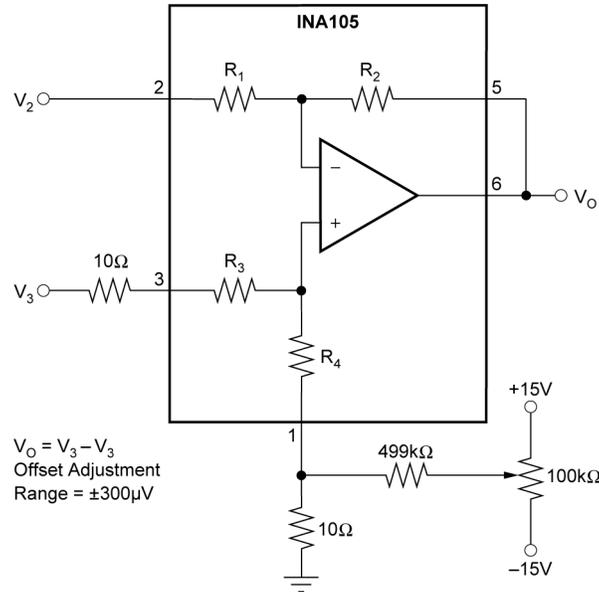


Figure 7-2. Offset Adjustment

7.2 Typical Application

The INA105 can be used in a variety of applications. [Figure 7-3](#) shows one example.

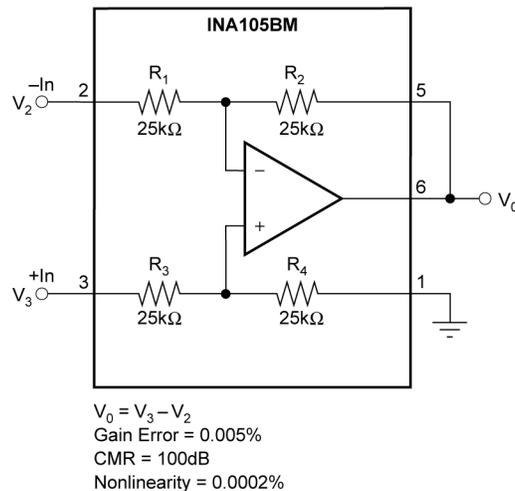


Figure 7-3. Precision Difference Amplifier

7.3 Additional Applications

The difference amplifier is a highly versatile building block that is useful in a wide variety of applications. The following section shows additional application circuit ideas.

7.3.1 Operational Amplifier Circuits

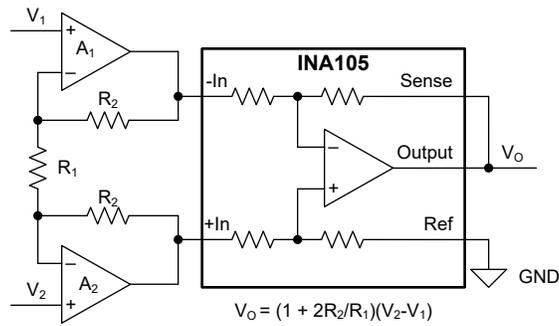


Figure 7-4. Precision Instrumentation Amplifier

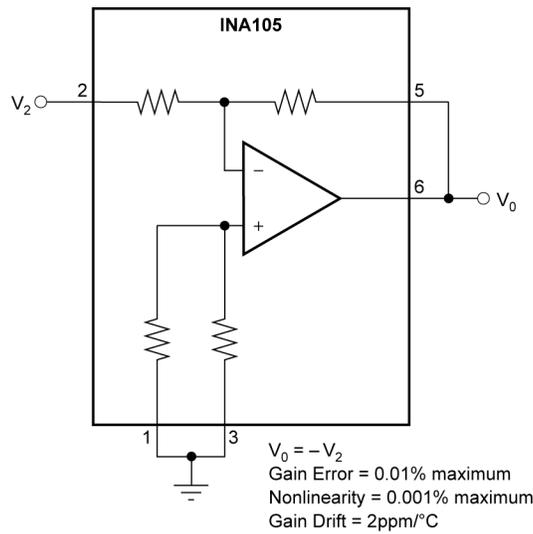


Figure 7-5. Precision Unity-Gain Inverting Amplifier

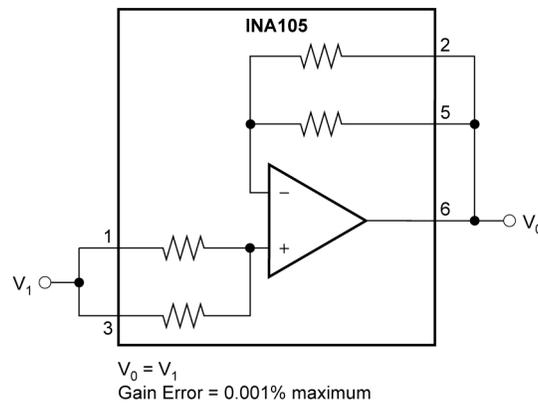


Figure 7-6. Precision Unity-Gain Buffer

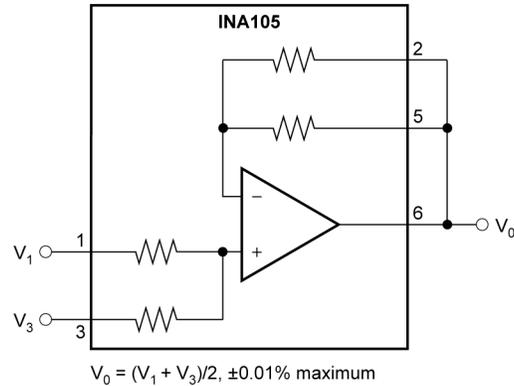


Figure 7-7. Precision Average-Value Amplifier

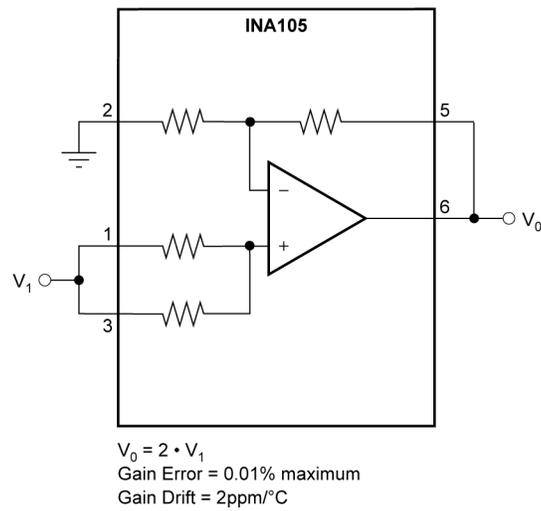


Figure 7-8. Precision Gain = 2 Amplifier

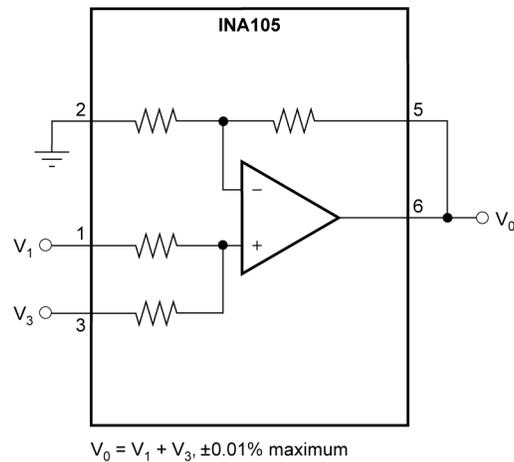


Figure 7-9. Precision Summing Amplifier

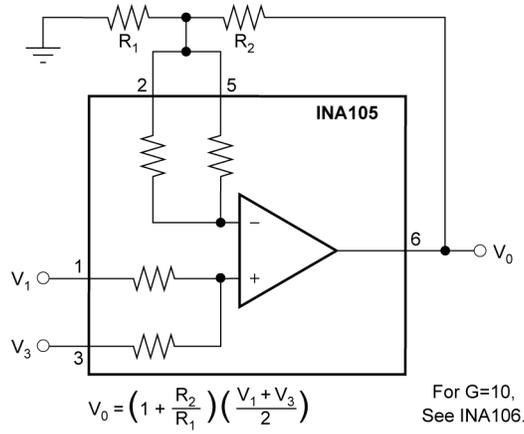


Figure 7-10. Precision Summing Amplifier With Gain

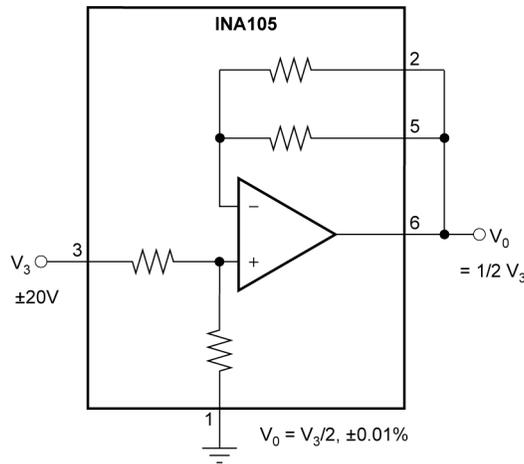


Figure 7-11. Precision Gain = 1/2 Amplifier

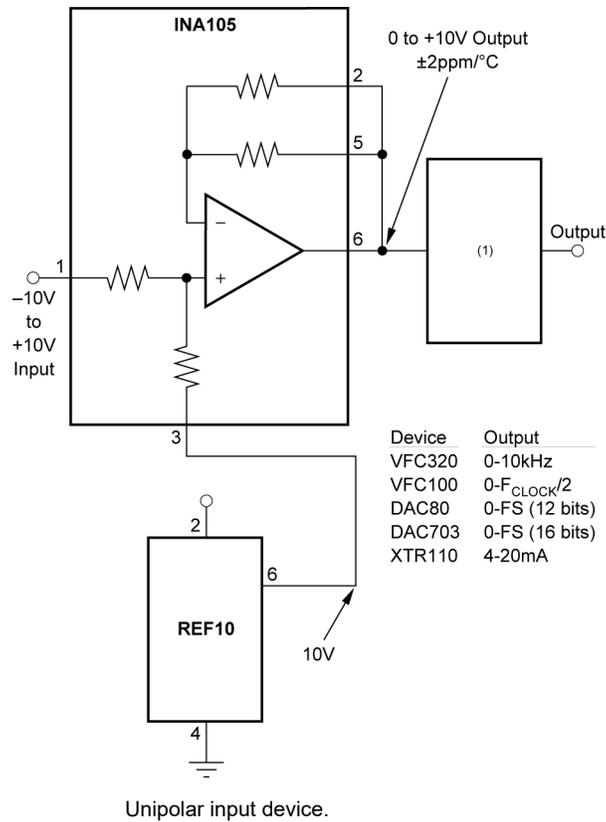


Figure 7-12. Precision Bipolar Offsetting

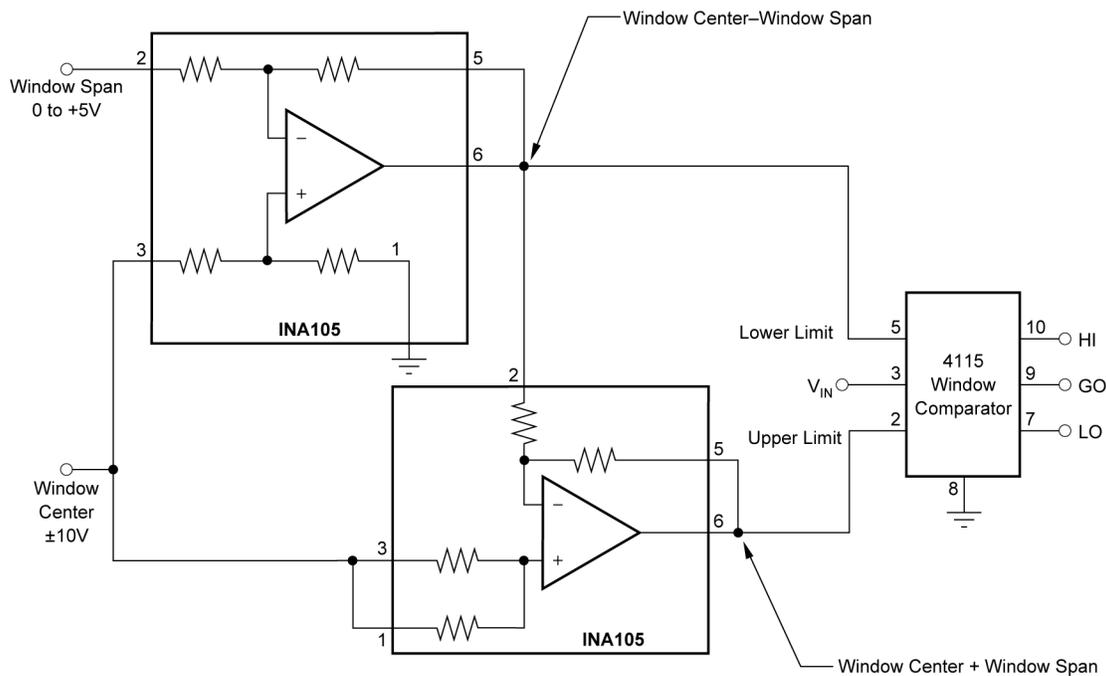


Figure 7-13. Window Comparator With Window-Span and Window-Center Inputs

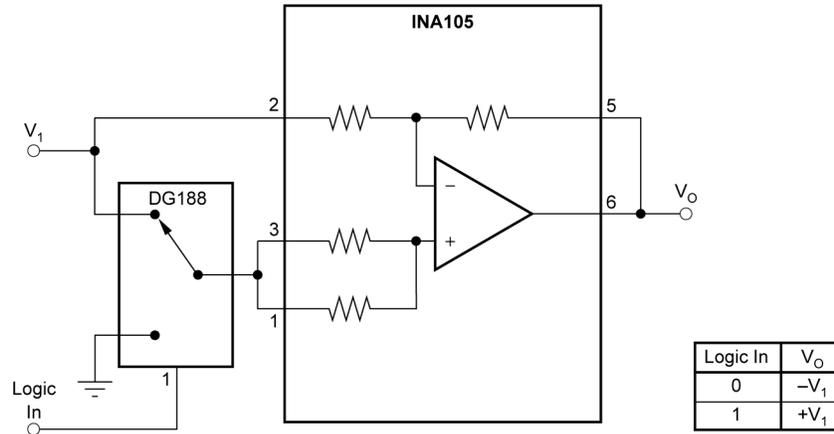


Figure 7-14. Digitally Controlled Gain of ± 1 Amplifier

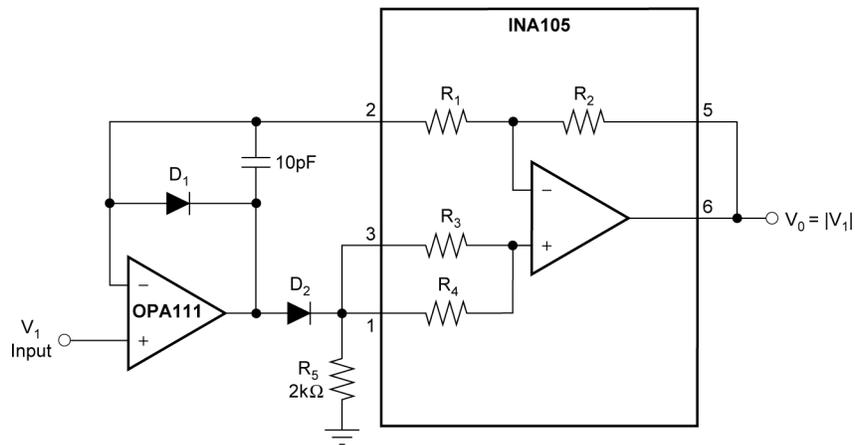


Figure 7-15. Precision Absolute-Value Buffer

7.3.2 Instrumentation Amplifier Circuits

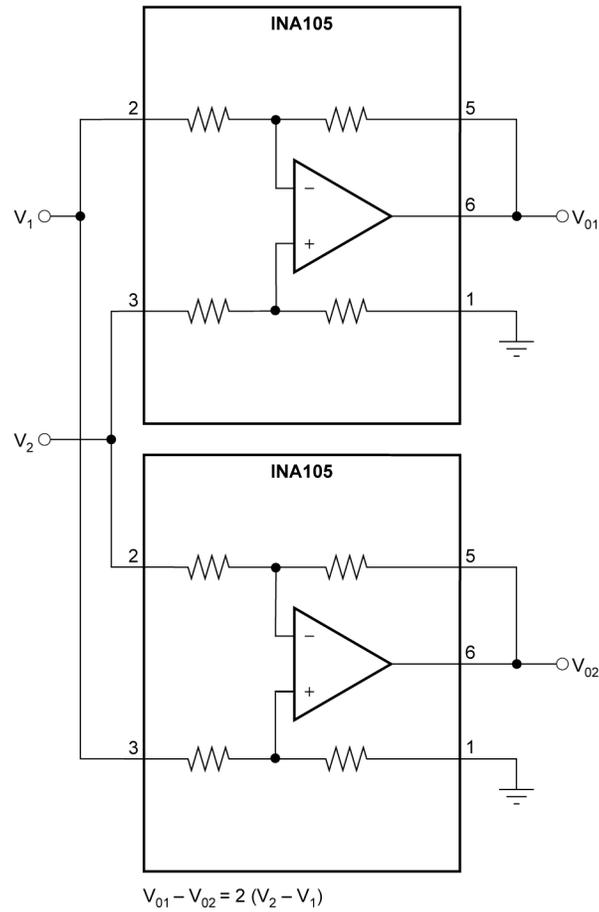


Figure 7-16. Differential Output Difference Amplifier

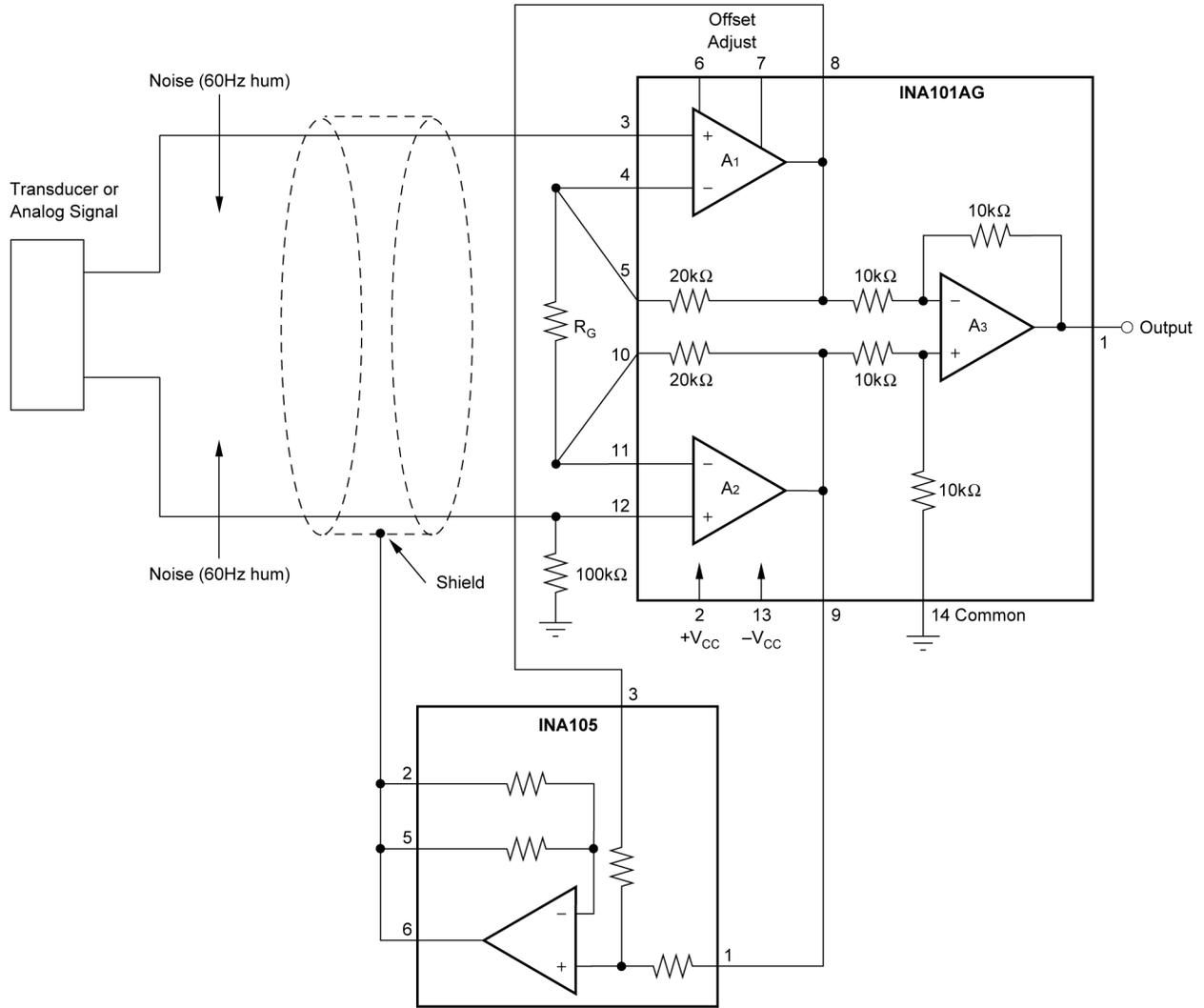


Figure 7-17. Instrumentation Amplifier Guard Drive Generator

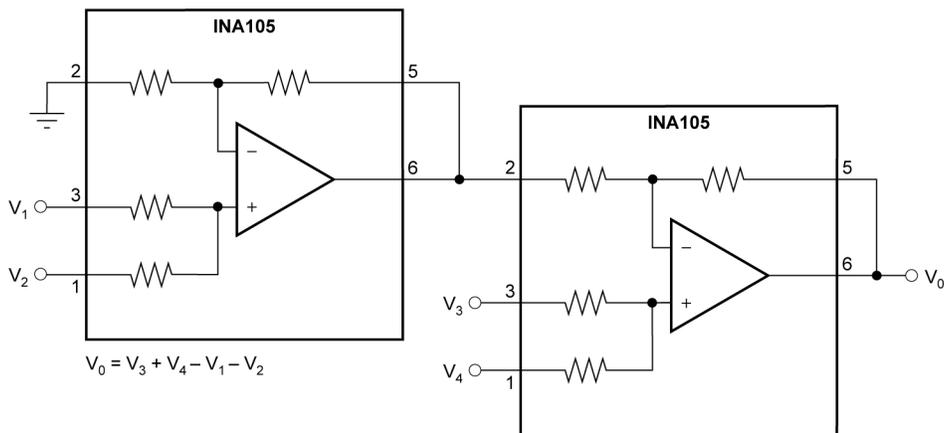


Figure 7-18. Precision Summing Instrumentation Amplifier

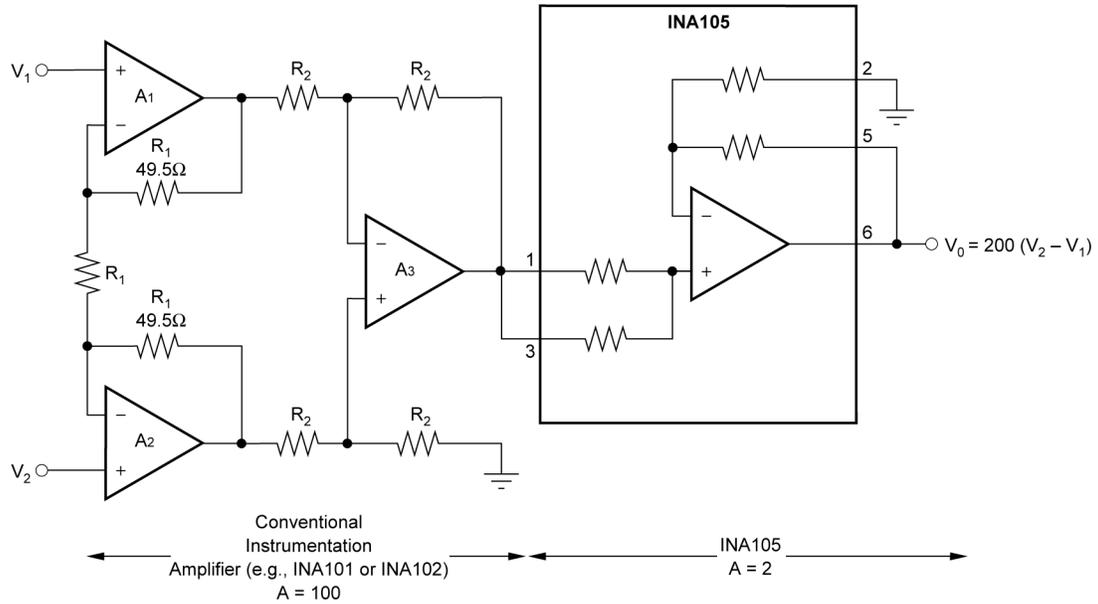


Figure 7-19. Boosting Instrumentation Amplifier Common-Mode Range From ±5V to ±7.5V With 10V Full-Scale Output

7.3.3 Voltage Reference Circuits

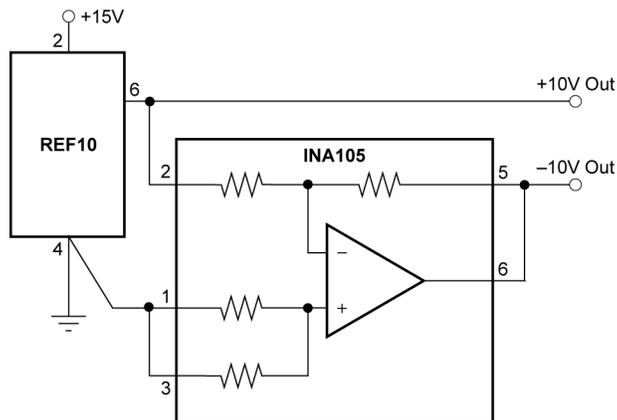


Figure 7-20. ±10V Precision Voltage Reference

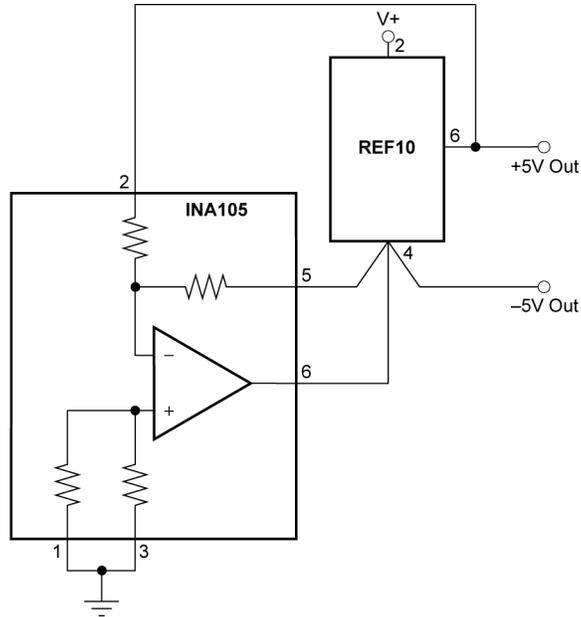


Figure 7-21. ±5V Precision Voltage Reference

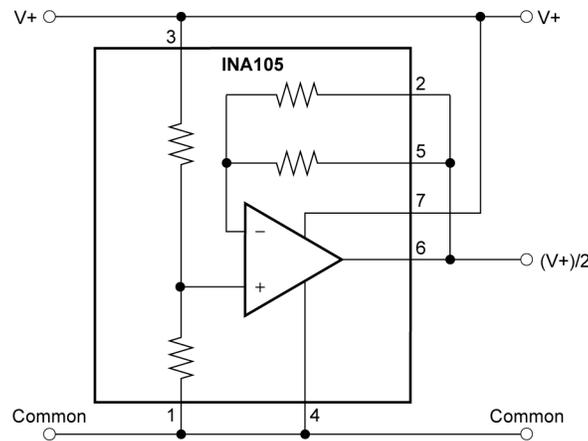


Figure 7-22. Pseudo-ground Generator

7.3.4 Special Function Circuits

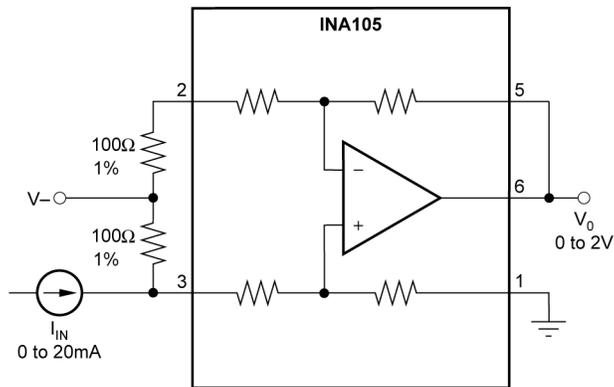


Figure 7-23. Current Receiver With Compliance to Rails

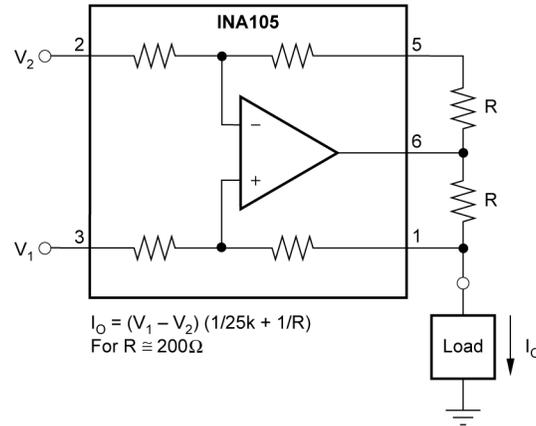


Figure 7-24. Precision Voltage-to-Current Converter With Differential Inputs

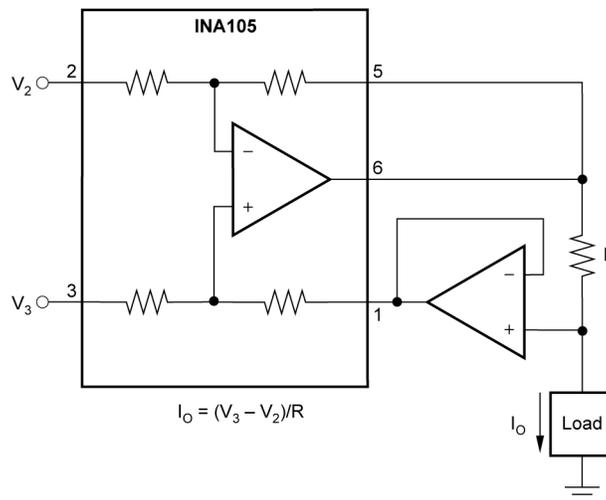


Figure 7-25. Differential Input Voltage-to-Current Converter for Low I_{OUT}

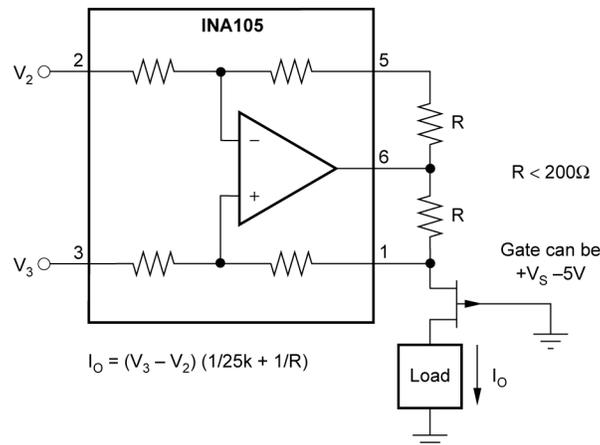


Figure 7-26. Isolating Current Source

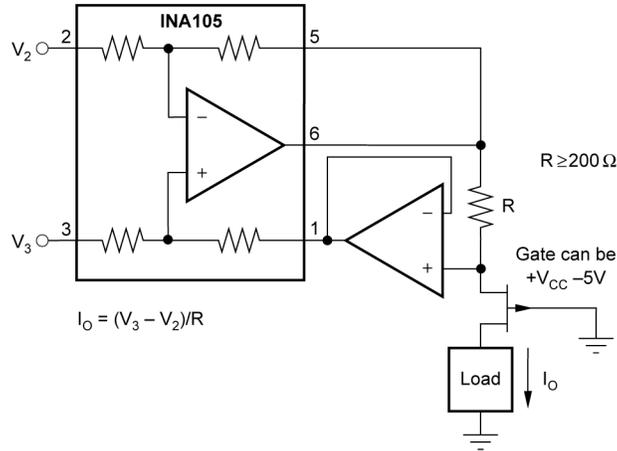


Figure 7-27. Isolating Current Source With Buffering Amplifier for Greater Accuracy

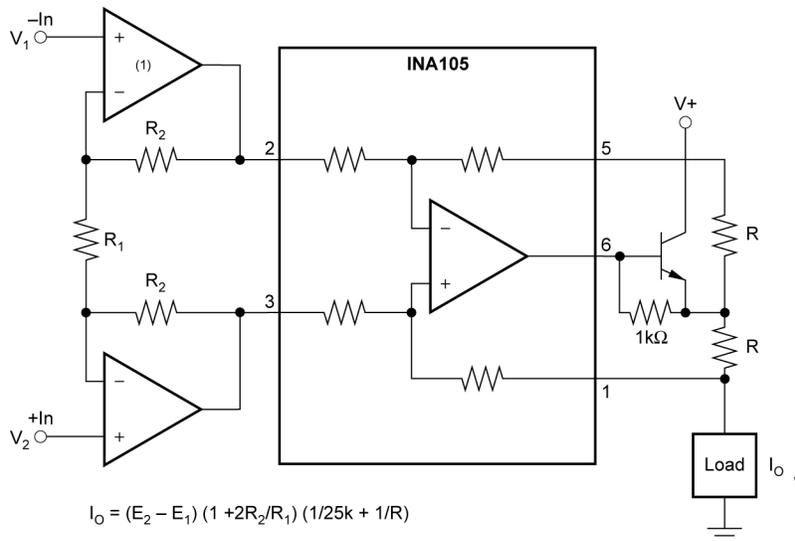


Figure 7-28. Precision Voltage-Controlled Current Source With Buffered Differential Inputs and Gain.

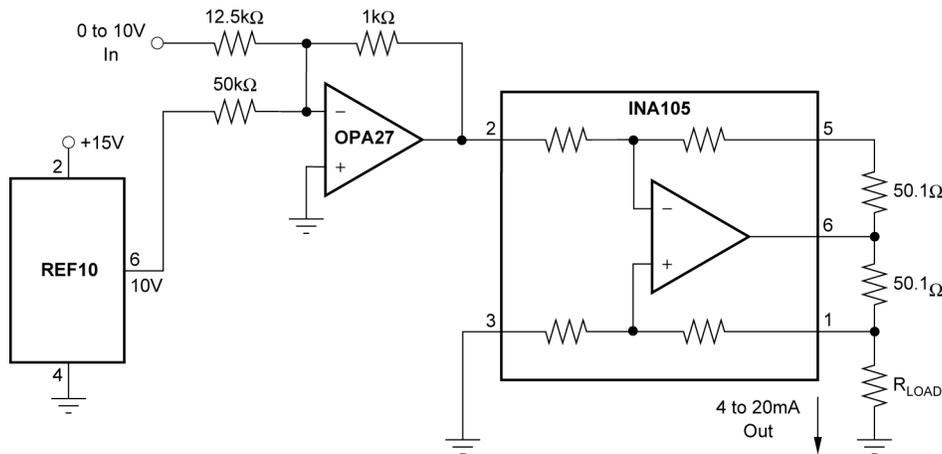


Figure 7-29. Precision 4mA to 20mA Current Transmitter

7.4 Power Supply Recommendations

The nominal performance of the INA105 is specified with a supply voltage of $\pm 15\text{V}$. The device operates using power supplies from $\pm 5\text{V}$ to $\pm 18\text{V}$ with varying performance. Parameters varying across the operating voltage and reference voltage range can be referenced in the [Typical Characteristics](#).

TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Place the C_{BYP} as close to the device as possible to reduce coupling errors from noisy or high-impedance power supplies. Route the power supply trace through C_{BYP} before reaching the device power supply terminals. For more information, see [Layout Guidelines](#).

7.5 Layout

7.5.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- Make sure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals.
- Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, $0.1\ \mu\text{F}$ ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from $V+$ to ground is applicable for single-supply applications.
- To reduce parasitic coupling, route the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is preferred over crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the traces as short as possible.

7.5.2 Layout Examples

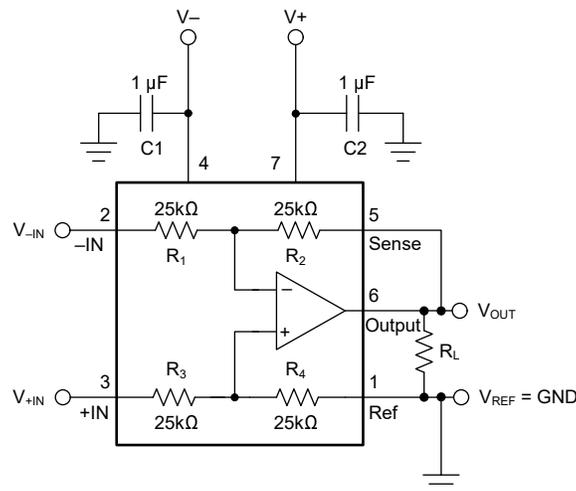


Figure 7-30. Example Schematic

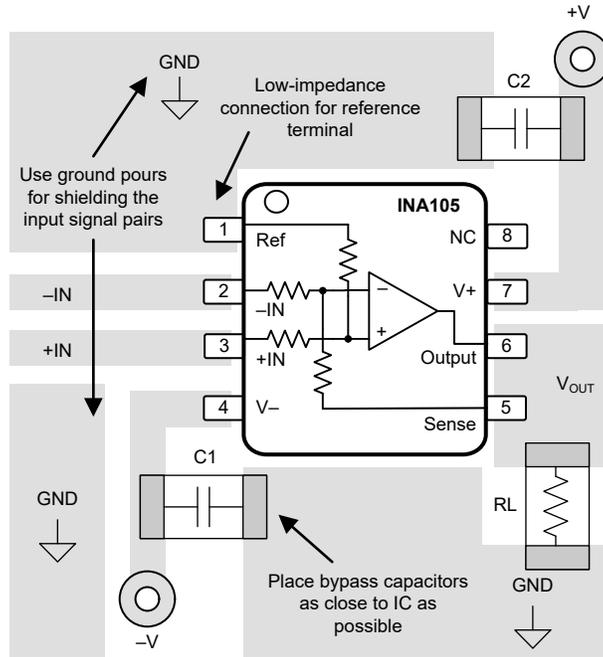


Figure 7-31. Associated PCB Layout for SOIC and PDIP Packages

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

Part Number	Definition
INA105KP INA105KU/2K5	The die is manufactured in CSO: SHE or CSO: RFB.
INA105AM INA105BM	The die is manufactured in CSO: SHE.

8.1.2 Development Support

For development support on this product, see the following:

8.1.2.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

8.1.2.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.

TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.

PSpice® is a registered trademark of Cadence Design Systems, Inc.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2025) to Revision B (December 2025)	Page
• Added description of device flow information in <i>Specifications</i>	4
• Added nominal value to Supply voltage in the <i>Recommended Operating Conditions</i>	4
• Added all chip site origins (CSO) condition to the typical test conditions in the <i>Electrical Characteristics</i>	5
• Merged INA105AM and INA105BM for Offset Voltage in <i>Electrical Characteristics</i>	5
• Added gain clarification in footnote (1) in the <i>Electrical Characteristics</i>	5
• Added different fabrication process specifications for voltage noise in the <i>Electrical Characteristics</i>	5
• Merged INA105AM and INA105BM for Gain Error in <i>Electrical Characteristics</i>	5
• Added different fabrication process specifications for short circuit current, sinking and sourcing, in the <i>Electrical Characteristics</i>	5
• Added different fabrication process specifications for slew rate in the <i>Electrical Characteristics</i>	5
• Added all chip site origins (CSO) condition to the typical test conditions in the <i>Typical Characteristics</i>	7
• Added "CSO: SHE" to Step Response, Maximum V_{OUT} vs. I_{OUT} (Negative Swing), and Maximum V_{OUT} vs. I_{OUT} (Positive Swing) curves in the <i>Typical Characteristics</i>	7
• Added Step Response, Maximum V_{OUT} vs. I_{OUT} (Negative Swing), and Maximum V_{OUT} vs. I_{OUT} (Positive Swing) curves for CSO: RFB in the <i>Typical Characteristics</i>	7
• Changed and added INA105 Internal Schematic for each fabrication process in the <i>Functional Block Diagram</i>	9
• Added Part Number flow information table to the <i>Device Nomenclature</i>	26

Changes from Revision * (August 1993) to Revision A (March 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the <i>Pin Configuration and Functions, Specifications, Recommended Operating Conditions, Thermal Information, Detailed Description, Overview, Functional Block Diagram, Feature Description, Device Functional Modes, Application and Implementation, , Power Supply Recommendations, Layout, Layout Guidelines, Layout Example, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections.....	1
• Added test conditions throughout <i>Electrical Characteristics</i> table.....	5
• Changed <i>Offset Voltage vs Time</i> to <i>Long-term stability</i> in <i>Electrical Characteristics</i>	5
• Changed <i>Current limit</i> to <i>Short-circuit current</i> for sinking and sourcing scenario.....	5
• Moved <i>Power Supply Voltage Range</i> and <i>Temperature Range</i> from <i>Electrical Characteristics</i> to <i>Recommended Operating Conditions</i> and <i>Absolute Maximum Ratings</i> table.....	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025