

MOSFET – Single, P-Channel, POWERTRENCH[®], Logic Level

FDN340P

General Description

This P-Channel Logic Level MOSFET is produced using onsemi advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging circuits, and dc–dc conversion.

Features

- 2 A, 20 V
 - $R_{DS(ON)} = 70 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
 - $R_{DS(ON)} = 110 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
- Low Gate Charge (7.2 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power Version of Industry Standard SOT–23 Package. Identical Pin–Out to SOT–23 with 30% Higher Power Handling Capability
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS

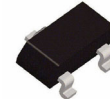
($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain–Source Voltage	–20	V
V_{GSS}	Gate–Source Voltage	± 8	V
I_D	Drain Current Continuous (Note 1a) Pulsed	–2 –10	A
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5 0.46	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

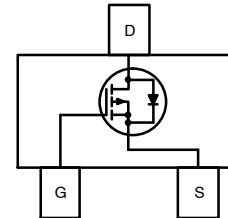
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

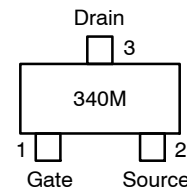
Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1a)	250	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case (Note 1)	75	$^\circ\text{C}/\text{W}$



SOT–23
CASE 527AG



MARKING DIAGRAM



M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDN340P

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = –250 μA	–20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C	–	–12	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = –16 V, V _{GS} = 0 V	–	–	–1	μA
		V _{DS} = –16 V, V _{GS} = 0 V, T _J = 55°C	–	–	–10	
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 8 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –8 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = –250 μA	–0.4	–0.8	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C	–	3	–	mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = –4.5 V, I _D = –2 A	–	60	70	mΩ
		V _{GS} = –4.5 V, I _D = –2 A, T _J = 125°C	–	77	120	
		V _{GS} = –2.5 V, I _D = –1.7 A	–	82	110	
I _{D(on)}	On–State Drain Current	V _{GS} = –4.5 V, V _{DS} = –5 V	–5	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = –4.5 V, I _D = –2 A	–	9	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = –10 V, V _{GS} = 0 V, f = 1.0 MHz	–	779	–	pF
C _{oss}	Output Capacitance		–	121	–	pF
C _{rss}	Reverse Transfer Capacitance		–	56	–	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = –10 V, I _D = –1 A, V _{GS} = –4.5 V, R _{GEN} = 6 Ω	–	10	20	ns
t _r	Turn–On Rise Time		–	9	10	ns
t _{d(off)}	Turn–Off Delay Time		–	27	43	ns
t _f	Turn–Off Fall Time		–	11	20	ns
Q _g	Total Gate Charge	V _{DS} = –10 V, I _D = –3.5 A, V _{GS} = –4.5 V	–	7.2	10	nC
Q _{gs}	Gate–Source Charge		–	1.7	–	nC
Q _{gd}	Gate–Drain Charge		–	1.5	–	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–0.42	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –0.42 A (Note 2)	–	–0.7	–1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 250°C/W when mounted on
a 0.02 in² pad of 2 oz copper



b) 270°C/W when mounted on
a 0.01 in² pad of 2 oz copper

Scale 1:1 on letter size paper

- Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDN340P	340	SOT–23 (Pb–Free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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TYPICAL CHARACTERISTICS

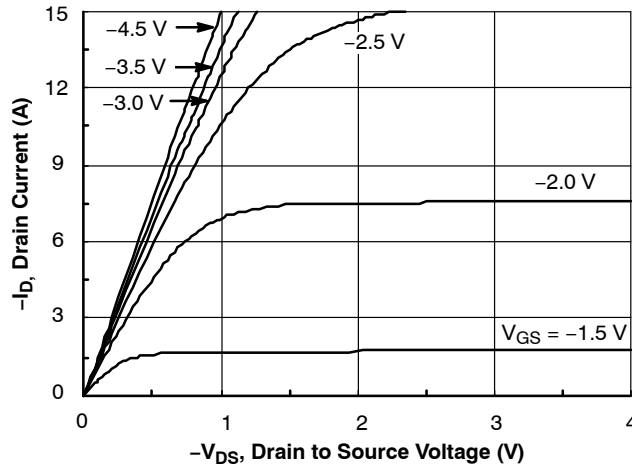


Figure 1. On-Region Characteristics

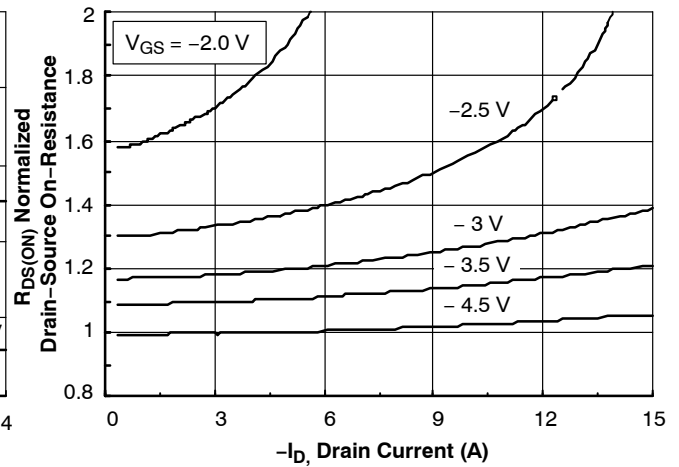


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

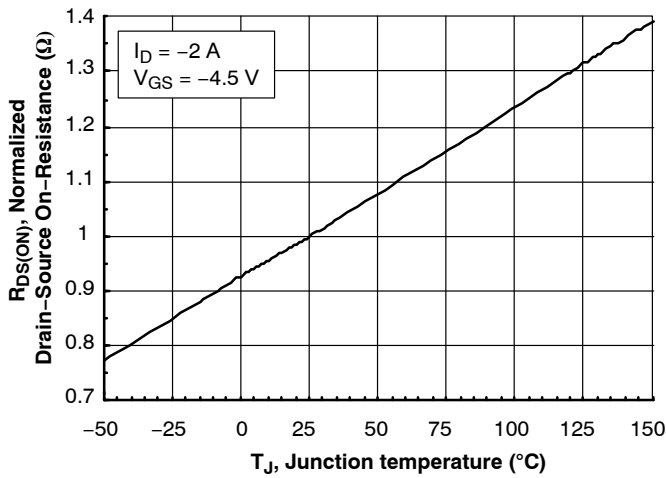


Figure 3. On-Resistance Variation with Temperature

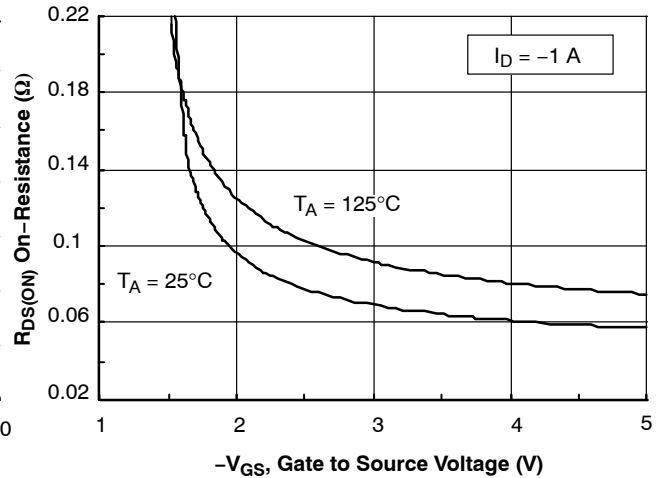


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

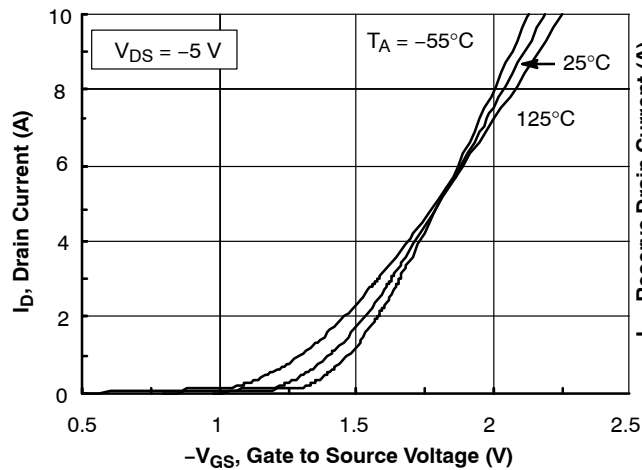


Figure 5. Transfer Characteristics

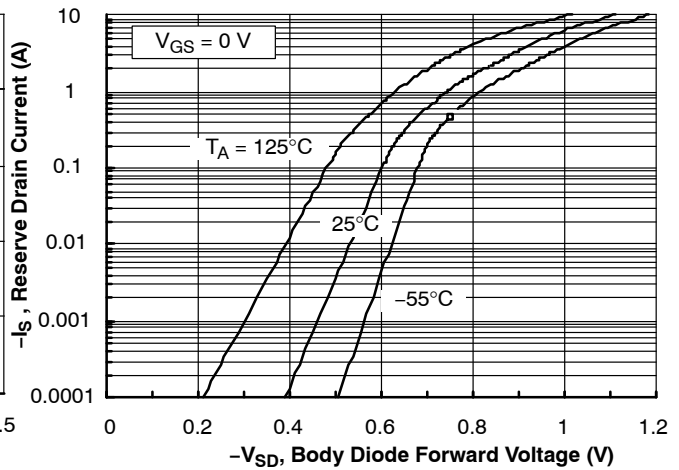


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Continued)

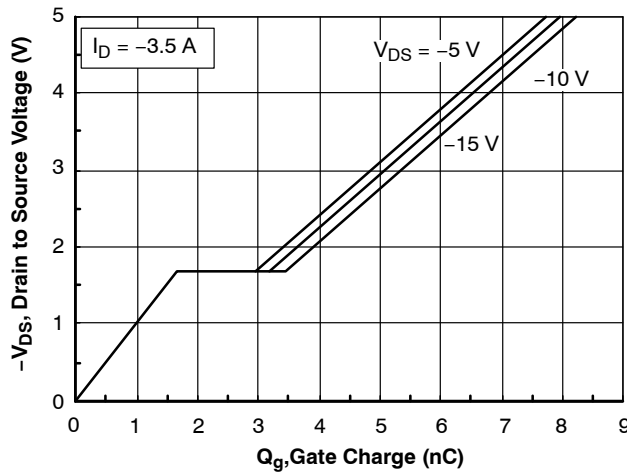


Figure 7. Gate Charge Characteristics

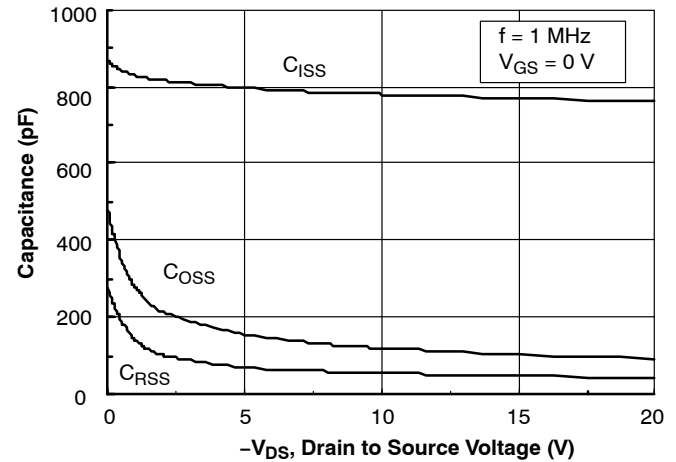


Figure 8. Capacitance Characteristics

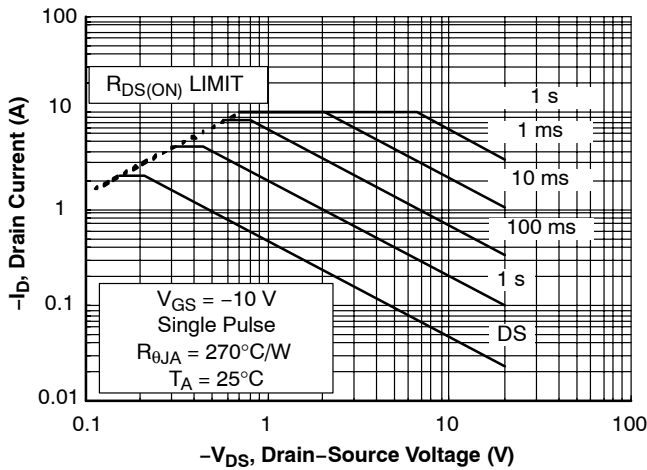


Figure 9. Maximum Safe Operating Area

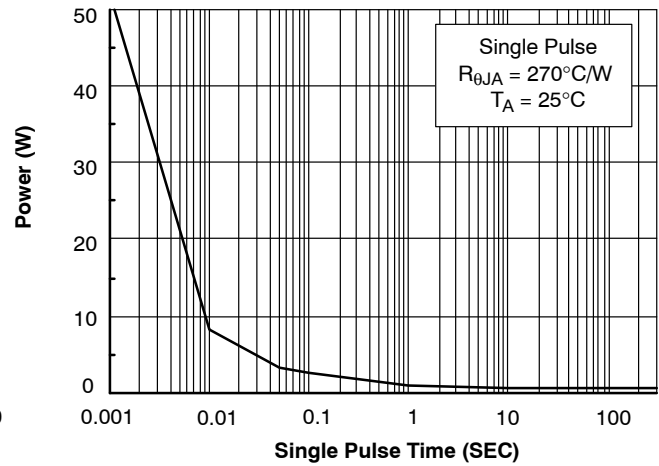


Figure 10. Single Pulse Maximum Power Dissipation

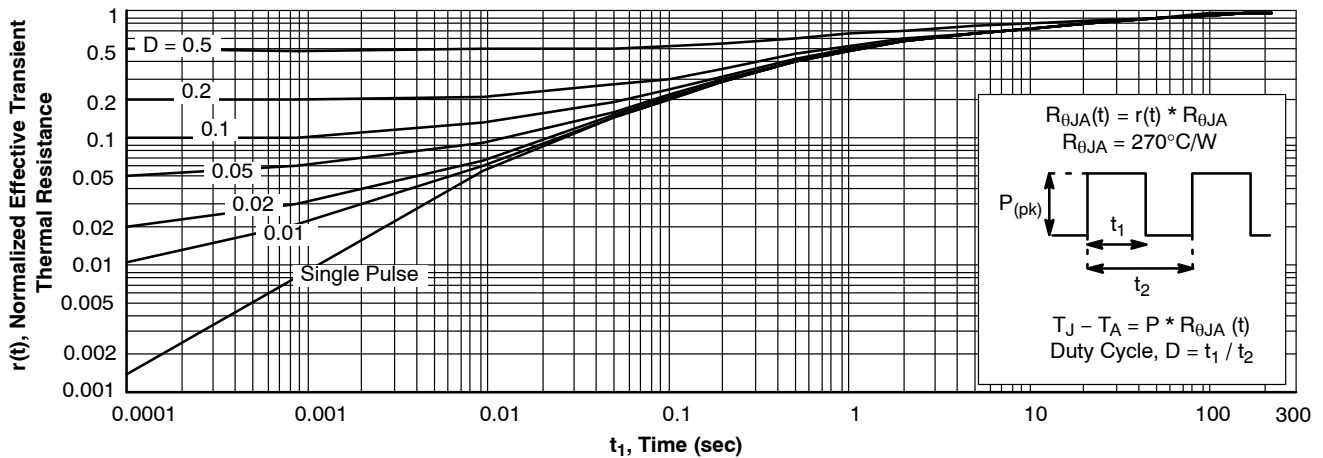
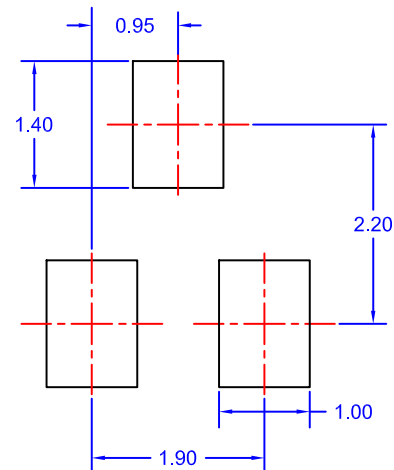
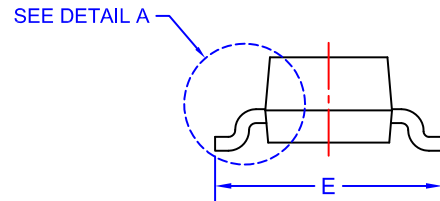


Figure 11. Transient Thermal Response Curve

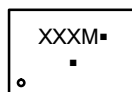
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.


SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019


LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*


XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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