10-A, 4.75-V to 14-V INPUT, NON-ISOLATED, WIDE-OUTPUT, DIGITAL POWERTRAIN™ MODULE

Check for Samples: PTD08A010W

FEATURES

- **Up to 10-A Output Current**
- **4.75-V to 14-V Input Voltage**
- **Programmable Wide-Output Voltage (0.7 V to 3.6 V)**
- **Efficiencies up to 96%**
- **Digital I/O**
  - **PWM signal**
  - **INHIBIT**
  - **Current limit flag (FAULT)**
  - **Sychronous Rectifier Enable (SRE)**
- **Analog I/O**
  - **Temperature**
  - **Output currrent**
- **Safety Agency Approvals: (Pending)**
  - **UL/IEC/CSA-C22.2 60950-1**
- **Operating Temperature: –40°C to 85°C**

APPLICATIONS

- **Digital Power Systems using UCD9XXX Digital Controllers**
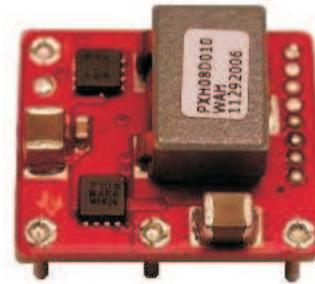
DESCRIPTION

The PTD08A010W is a high-performance 10-A rated, non-isolated digital PowerTrain module. This module is the power conversion section of a digital power system which incorporates TI's UCD7230 MOSFET driver IC. The PTD08A010W must be used in conjunction with a digital power controller such as the UCD9240 or UCD9110 family. The PTD08A010W receives control signals from the digital controller and provides parametric and status information back to the digital controller. Together, PowerTrain modules and a digital power controller form a sophisticated, robust, and easily configured power management solution.

Operating from an input voltage range of 4.75 V to 14 V, the PTD08A010W provides step-down power conversion to a wide range of output voltages from, 0.7 V to 3.6 V. The wide input voltage range makes the PTD08A010W particularly suitable for advanced computing and server applications that utilize a loosely regulated 8-V, 9.6-V or 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V or 12-V intermediate bus architectures.

The module incorporates output over-current and temperature monitoring which protects against most load faults. Output current and module temperature signals are provided for the digital controller to permit user defined over-current and over-temperature warning and fault scerarios.

The module uses double-sided surface mount construction to provide a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) - free and RoHS compatible.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

POWERTRAIN is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Standard PTD08A010W Application
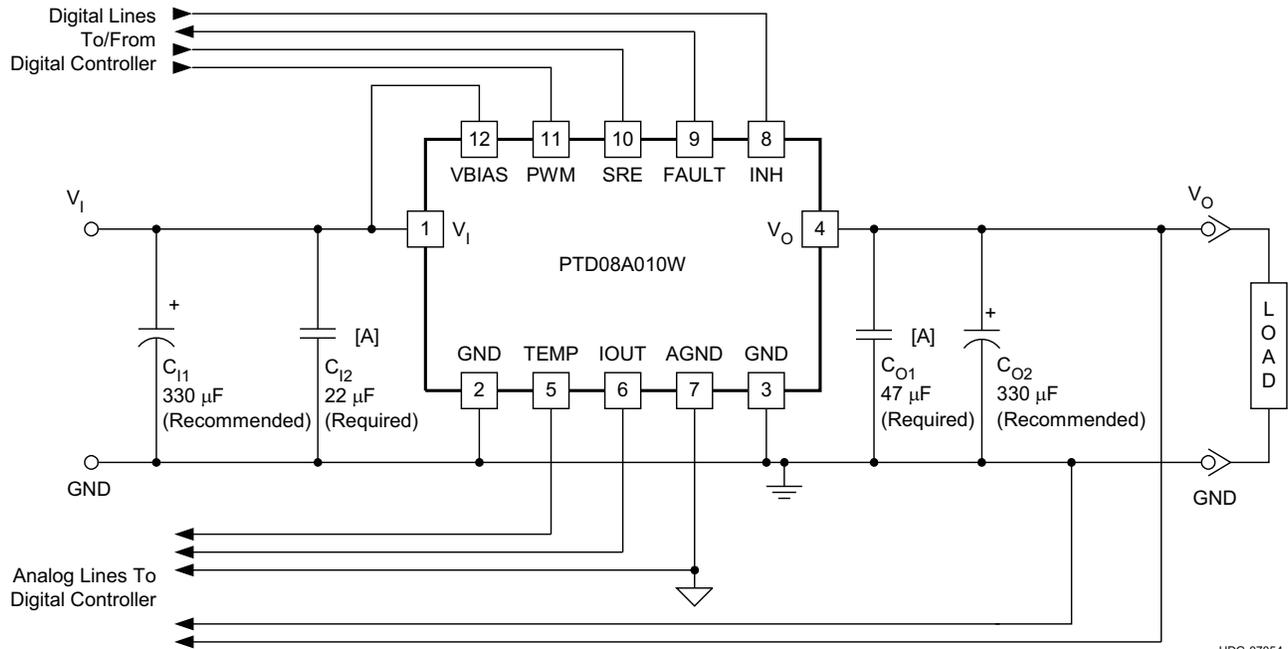
UDG-07054

A. C_{I2} and C_{O1} are optional when the operating frequency is greater than 500 kHz.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

DATASHEET TABLE OF CONTENTS

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

					UNIT
V_I	Input voltage			16	V
V_B	Bias voltage			16	V
T_A	Operating temperature range	Over V_I range		−40 to 85	°C
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins for 5 seconds maximum	suffix AD	260	
T_{stg}	Storage temperature			−55 to 125[(1)]	
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted	suffix AD	200	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz		15	
	Weight			3.9	grams
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign		9.4	10^6 Hr
	Flammability	Meets UL94V-O			

(1)   The shipping tray or tape and reel cannot be used to bake parts at temperatures higher than 65°C.

ELECTRICAL CHARACTERISTICS

PTD08A010W

T_A= 25°C, F_{SW}= 350kHz, V_I= 12 V, V_O= 3.3 V, V_B= V_I, C_{I1}= 330 µF, C_{I2}= 22 µF ceramic, C_{O1}= 47 µF ceramic, C_{O2}= 330 µF, and I_O= $I_{O(max)}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS		PTD08A010W			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection	0		10	A
V_I	Input voltage range	Over I_O range		4.75		14[1]	V
V_{OADJ}	Output voltage adjust range	Over I_O range		0.7[1]		3.6	V
η	Efficiency	$V_I = V_B = 5$ V $I_O = 10$ A, $fs = 350$ kHz	$V_O = 3.3$ V		95%		
			$V_O = 2.5$ V		92%		
			$V_O = 1.8$ V		89%		
			$V_O = 1.5$ V		88%		
			$V_O = 1.2$ V		86%		
			$V_O = 1.0$ V		84%		
V_{OPP}	V_O Ripple (peak-to-peak)	20-MHz bandwidth			20		mV_{PP}
V_B	Bias voltage			4.75		14	V
V_B UVLO	Bias voltage under voltage lockout	V_B increasing		4.25	4.5	4.75	V
		V_B decreasing		4.0	4.25	4.5	
I_B	Bias current	Inhibit (pin 8) to AGND	Standby		4		mA
			Switching		34		
V_{IH}	High-level input voltage	SRE, INH, & PWM input levels		2.0		5.5	V
V_{IL}	Low-level input voltage					0.8	
	PWM input	Frequency range		300		1000	kHz
		Pulse width limits		130			ns
	TEMP output	Range		-40		125	°C
		Accuracy, -40°C ≤ T_A ≤ 85°C		-4		6	°C
		Slope			10		mV/°C
		Offset, $T_A = 0$°C			500		mV
V_{OH}	FAULT output	High-level output voltage, $I_{FAULT} = 4mA$		2.7	3.3		V
V_{OL}		Low-level output voltage, $I_{FAULT} = 4mA$			0	0.6	
I_{LIM}		Overcurrent threshold; Reset, followed by auto-recovery			20		A
	IOUT output	Range		0.15		3.5	V
		Gain		70	100	130	mV/A
		Offset, $I_O = 0A$, $V_O = 1.2V$		0.44	0.6	0.76	V
		Output Impedance		10	15	21	kΩ
C_I	External input capacitance	Nonceramic			330 [2]		µF
		Ceramic		22 [2]			
C_O	External output capacitance	Capacitance Value	Nonceramic		330 [3]	5000[4]	µF
			Ceramic	47 [3]		[3]	
		Equivalent series resistance (non-ceramic)		1[5]			mΩ

(1) The maximum input voltage is duty cycle limited to (V_O/(130ns × F_{SW})) or 14 V, whichever is less. The maximum allowable input voltage is a function of switching frequency.
(2) A 22 µF ceramic input capacitor is required for proper operation. An additional 330 µF bulk capacitor rated for a minimum of 500mA rms of ripple current is recommended. When operating at frequencies > 500kHz the 22 µF ceramic capacitor is only recommended. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(3) A 47 µF ceramic output capacitor is required for basic operation. An additional 330 µF bulk capacitor is recommended for improved transient response. When operating at frequencies > 500kHz the 47 µF ceramic capacitor is only recommended. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(4) 5,000 µF is the calculated maximum output capacitance given a 1V/msec output voltage rise time. Additional capacitance or increasing the output voltage rise rate may trigger the overcurrent threshold at start-up. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.
(5) This is the minimum ESR for all non-ceramic output capacitance. Refer to the UCD9240 controller datasheet and user interface for application specific capacitor specifications.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	1	The positive input voltage power node to the module, which is referenced to common GND.
GND	2	This is the common ground connection for the V_I and V_O power connections.
	3	
V_O	4	The regulated positive power output with respect to GND.
TEMP	5	Temperature sense output. The voltage level on this pin represents the temperature of the module.
IOUT	6	Current sense output. The voltage level on this pin represents the average output current of the module.
AGND	7	Analog ground return. It is the 0 V_{dc} reference for the control inputs.
INH[1]	8	The inhibit pin is a negative logic input that is referenced to AGND. Applying a low-level signal to this pin disables the module and turns off the output voltage. A 10 kΩ pull-up to 3.3 V or 5 V is required if the INH signal is not used.
FAULT	9	Current limit flag. The Fault signal is a 3.3 V digital output which is latched high after an over-current condition. The Fault is reset after two complete PWM cycles without an over-current condition (third rising edge of the PWM).
SRE	10	Synchronous Rectifier Enable. This pin is a high impedance digital input. A 3.3 V or 5 V logic level signals is used to enable the synchronous rectifier switch. When this signal is high, the module will source and sink output current. When this signal is low, the module will only source current.
PWM	11	This is the PWM input pin. It is a high impedance digital input that accepts 3.3 V or 5 V logic level signals up to 1 MHz.
VBIAS	12	Bias voltage supply required to power internal circuitry. For optimal performance connect VBIAS to V_I.

(1)   Denotes negative logic: High = Normal operation, Low = Function active
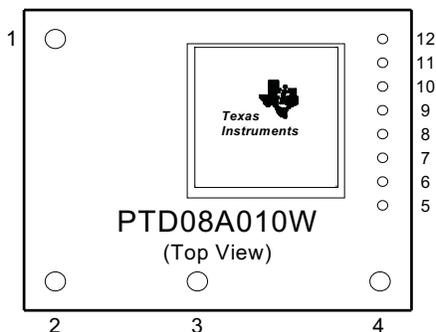
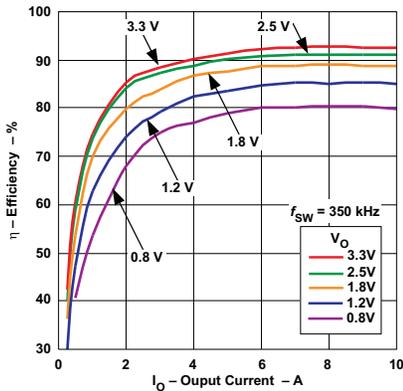## TYPICAL CHARACTERISTICS $(V_I = 12\ V)$ [1]

EFFICIENCY vs LOAD CURRENT
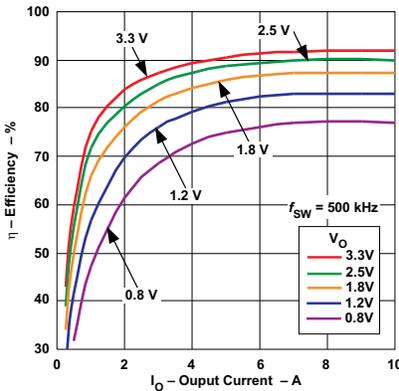

Figure 1.

EFFICIENCY vs LOAD CURRENT

Figure 2.

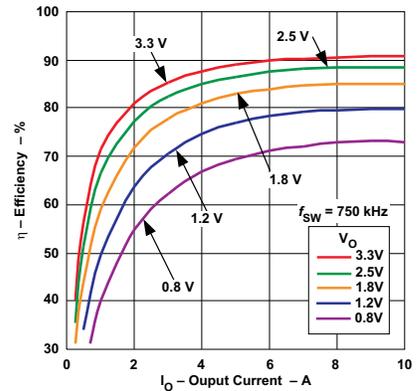**EFFICIENCY vs LOAD CURRENT**

Figure 3.

EFFICIENCY vs LOAD CURRENT
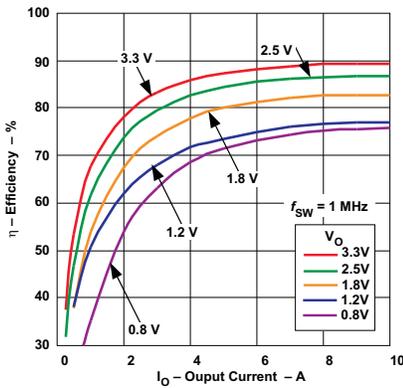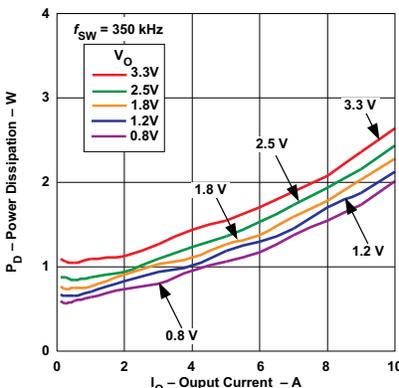

Figure 4.

POWER DISSIPATION vs LOAD CURRENT

Figure 5.

POWER DISSIPATION vs LOAD CURRENT
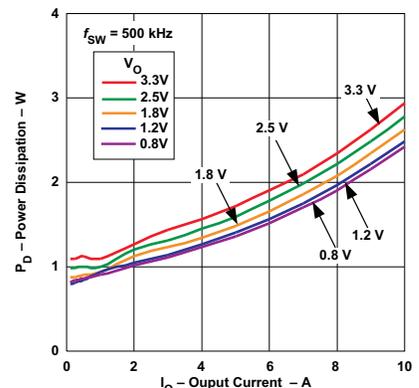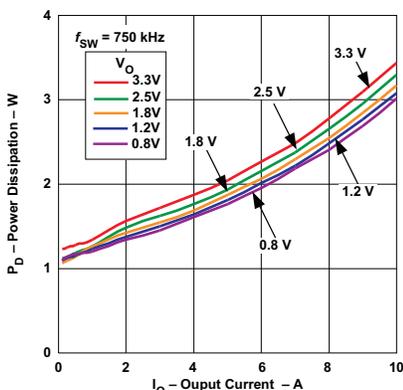

Figure 6.

POWER DISSIPATION vs LOAD CURRENT

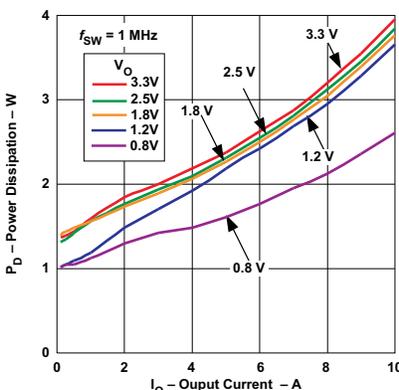

Figure 7.

POWER DISSIPATION vs LOAD CURRENT

Figure 8.

INPUT BIAS CURRENT vs SWITCHING FREQUENCY
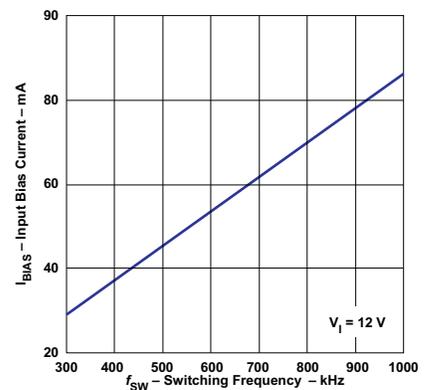
Figure 9.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter.

Product Folder Link(s): *PTD08A010W*

TYPICAL CHARACTERISTICS *(V$_I$ = 12 V)*
Safe Operating Area [(1)]

AMBIENT TEMPERATURE vs LOAD CURRENT

f_{SW} = 350 kHz
V_O = 3.3 V

400LFM
200LFM
100LFM
Nat conv
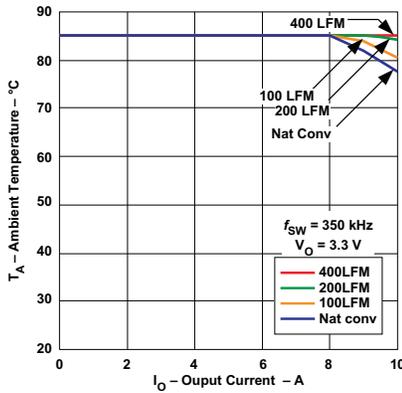
Figure 10.

AMBIENT TEMPERATURE vs LOAD CURRENT

f_{SW} = 500 kHz
V_O = 3.3 V

400LFM
200LFM
100LFM
Nat conv
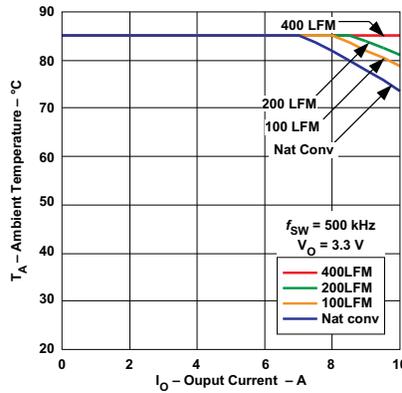
Figure 11.

AMBIENT TEMPERATURE vs LOAD CURRENT

f_{SW} = 350 kHz
V_O = 1.2 V

Nat conv
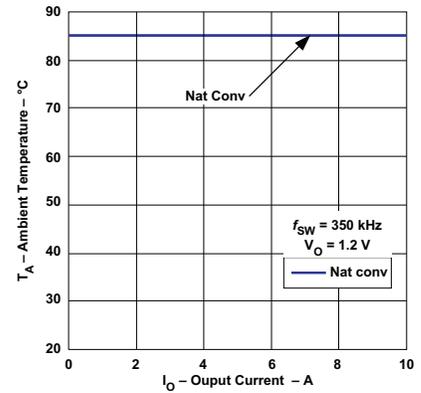
Figure 12.

AMBIENT TEMPERATURE vs LOAD CURRENT

f_{SW} = 500 kHz
V_O = 1.2 V

200LFM
100LFM
Nat conv
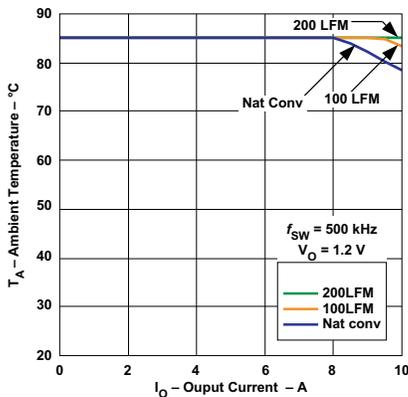
Figure 13.

AMBIENT TEMPERATURE vs LOAD CURRENT

f_{SW} = 750 kHz
V_O = 1.2 V

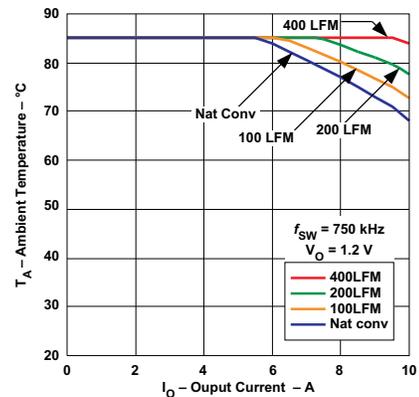400LFM
200LFM
100LFM
Nat conv

Figure 14.

(1)   The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Please refer to the mechanical specification for more information.
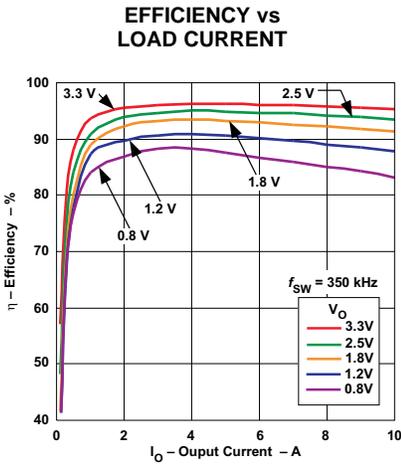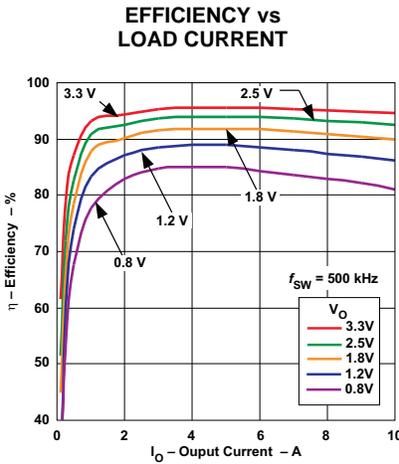
TYPICAL CHARACTERISTICS $(V_I = 5 \text{ V})$ [1]

EFFICIENCY vs LOAD CURRENT
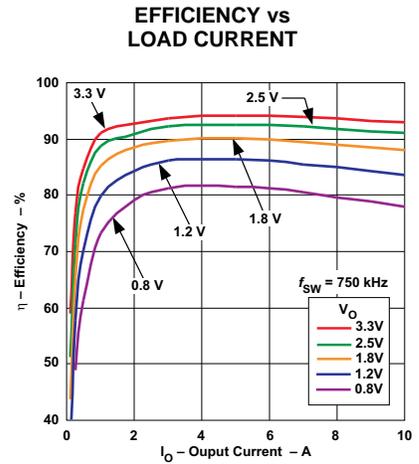

Figure 15.

EFFICIENCY vs LOAD CURRENT

Figure 16.

EFFICIENCY vs LOAD CURRENT

Figure 17.

EFFICIENCY vs LOAD CURRENT

Figure 18.

POWER DISSIPATION vs LOAD CURRENT

Figure 19.

POWER DISSIPATION vs LOAD CURRENT

Figure 20.

POWER DISSIPATION vs LOAD CURRENT

Figure 21.

POWER DISSIPATION vs LOAD CURRENT

Figure 22.

INPUT BIAS CURRENT vs SWITCHING FREQUENCY
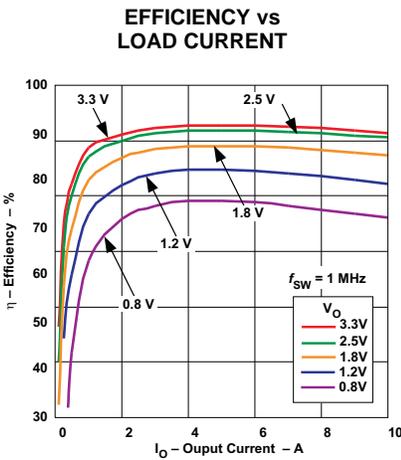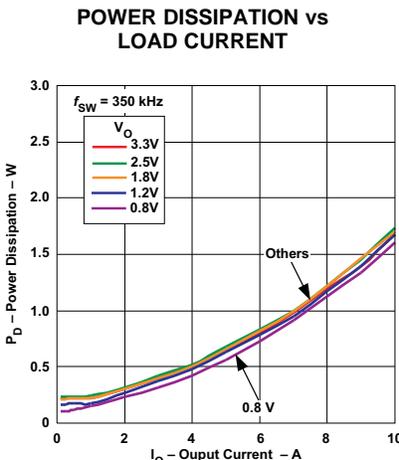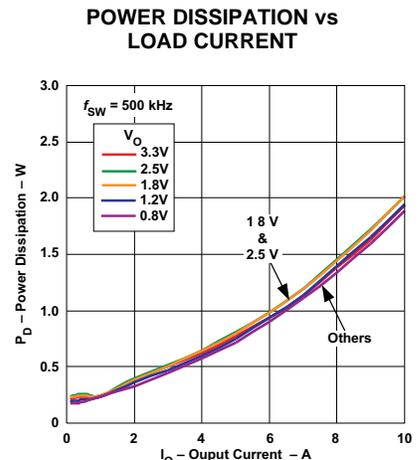
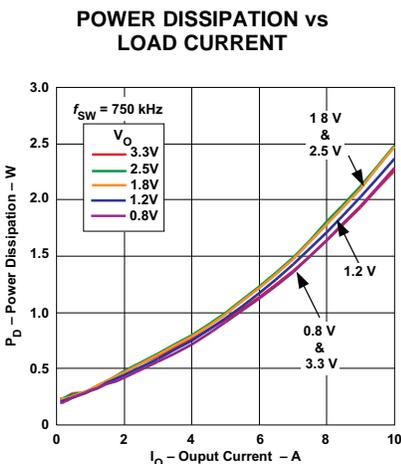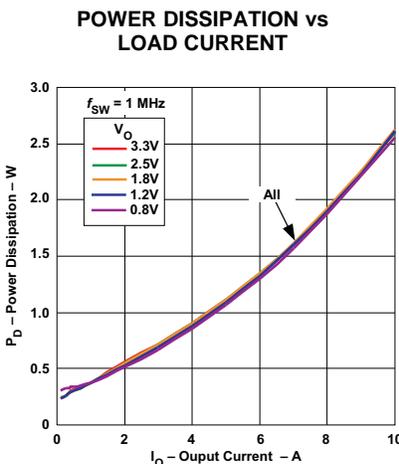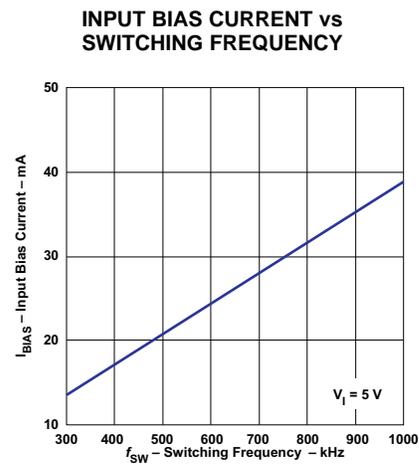**Figure 23.**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter.

Product Folder Link(s): *PTD08A010W*

TYPICAL CHARACTERISTICS *(V_I = 5 V)*
Safe Operating Area [(1)]

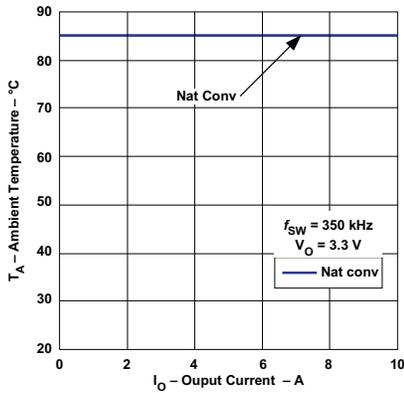**AMBIENT TEMPERATURE vs LOAD CURRENT**

Figure 24.

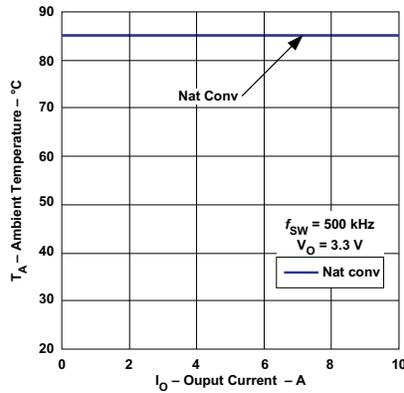**AMBIENT TEMPERATURE vs LOAD CURRENT**

Figure 25.

AMBIENT TEMPERATURE vs LOAD CURRENT

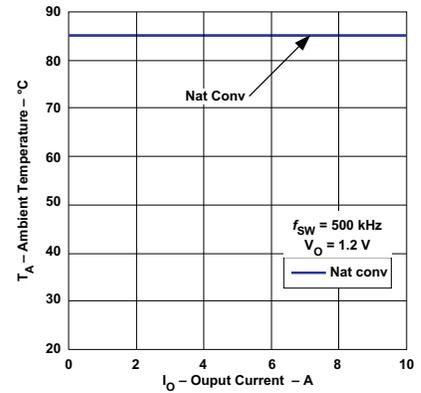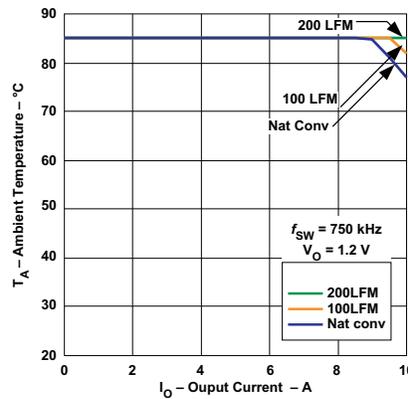Figure 26.

AMBIENT TEMPERATURE vs LOAD CURRENT

Figure 27.

(1) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Please refer to the mechanical specification for more information.

APPLICATION INFORMATION

DIgital Power
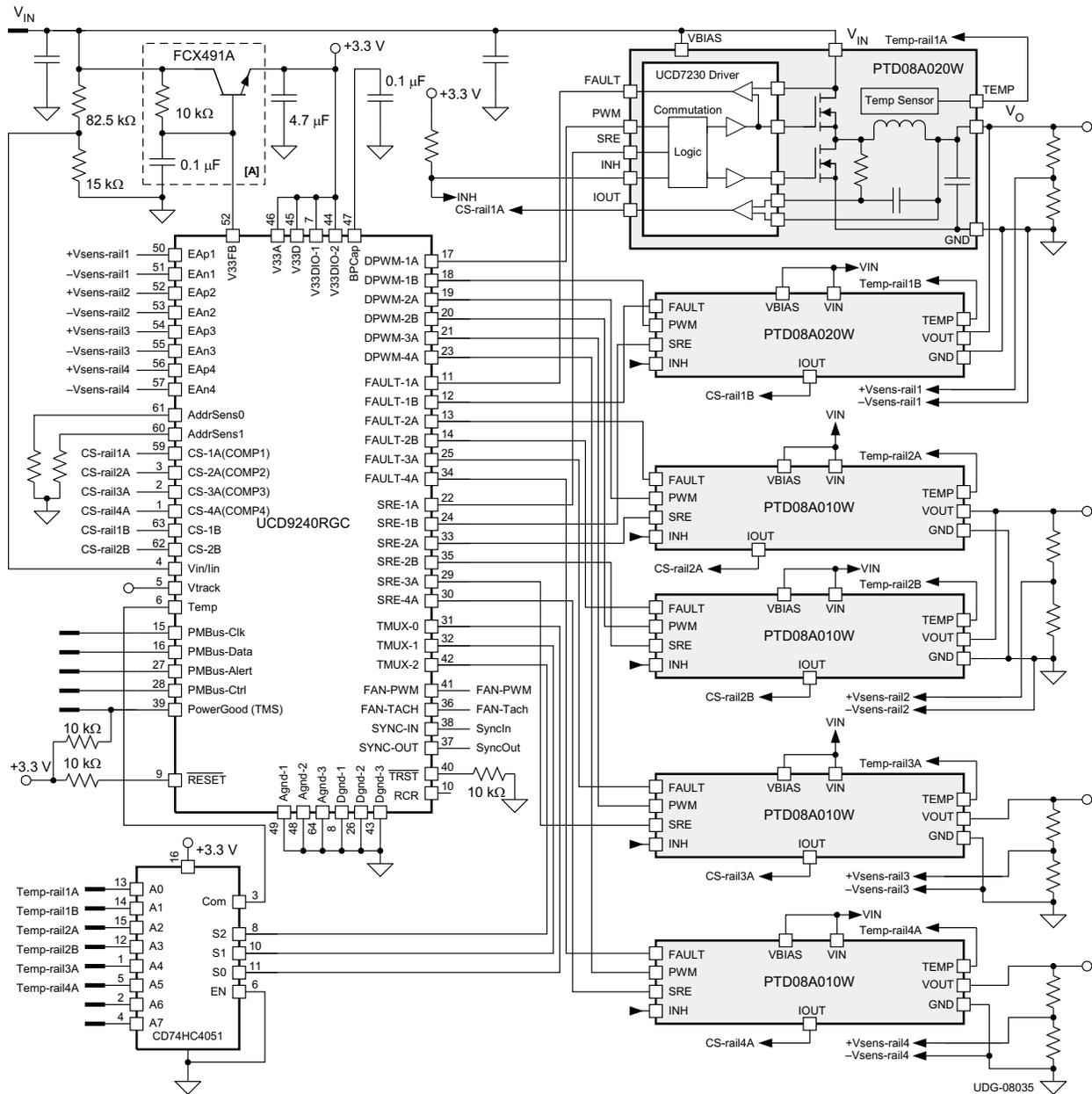
Figure 28. Typical Application Schematic

B.   This discrete bias power circuit may be substituted with a low dropout regulator (LDO). For example, TPS715A33 can provide bias power to the UCD9240.

Figure 28 shows the UCD9240 power supply controller working in a system which requires the regulation of four independent power supplies. The loop for each power supply is created by the respective voltage outputs feeding into the Error ADC differential inputs, and completed by DPWM outputs feeding into the UCD7230 drivers which are shown on the PTD08A0x0W modules.

UCD9240 Graphical User Interface (GUI)

When using the UCD9240 digital controller along with digital PowerTrain modules to design a digital power system, several internal parameters of the modules are required to run the Fusion Digital Power Designer GUI. See the plant parameters below for the PTD08A010W and PTD08A020W digital PowerTrain modules.

Table 1. PTD08A010W Plant Parameters

PTD08A010W Plant Parameters			
L (µH)	DCR (mΩ)	Rds-on-hi (mΩ)	Rds-on-lo (mΩ)
0.90	2.2	3.6	3.6

Table 2. PTD08A020W Plant Parameters

PTD08A020W Plant Parameters			
L (µH)	DCR (mΩ)	Rds-on-hi (mΩ)	Rds-on-lo (mΩ)
1.0	1.5	5.0	2.5

Internal output capacitance is present on the digital PowerTrain modules themselves. When using the GUI interface this capacitance information must be included along with any additional external capacitance. See the capacitor parameters below for the PTD08A010W and PTD08A020W digital PowerTrain modules.

Table 3. PTD08A010W Capacitor Parameters

PTD08A010W Capacitor Parameters			
C (µF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	1

Table 4. PTD08A020W Capacitor Parameters

PTD08A020W Capacitor Parameters			
C (µF)	ESR (mΩ)	ESL (nH)	Quantity
47	1.5	2.5	2

Product Folder Link(s): *PTD08A010W*

TRAY

NOTE: THE INDUCTOR IS USED TO PICK AND PLACE THE MODULE. IT'S LOCATION MAY VARY FROM PACKAGE STYLE. SEE PRODUCT TABLE

| DEVICES/TRAY | 36 |

PTDXXXXXX	"A"	"B"	"X"	"Y"
PTD08A010	28.61	28.63	40.00	30.70

ALL DIMENSIONS ARE IN MILLIMETER.

Product Folder Link(s): *PTD08A010W*

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTD08A010WAD	Active	Production	Through-Hole Module (EGS) | 12	36 | TIW TRAY	In-Work	SN	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTD08A010WAD.B	Active	Production	Through-Hole Module (EGS) | 12	36 | TIW TRAY	In-Work	SN	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.
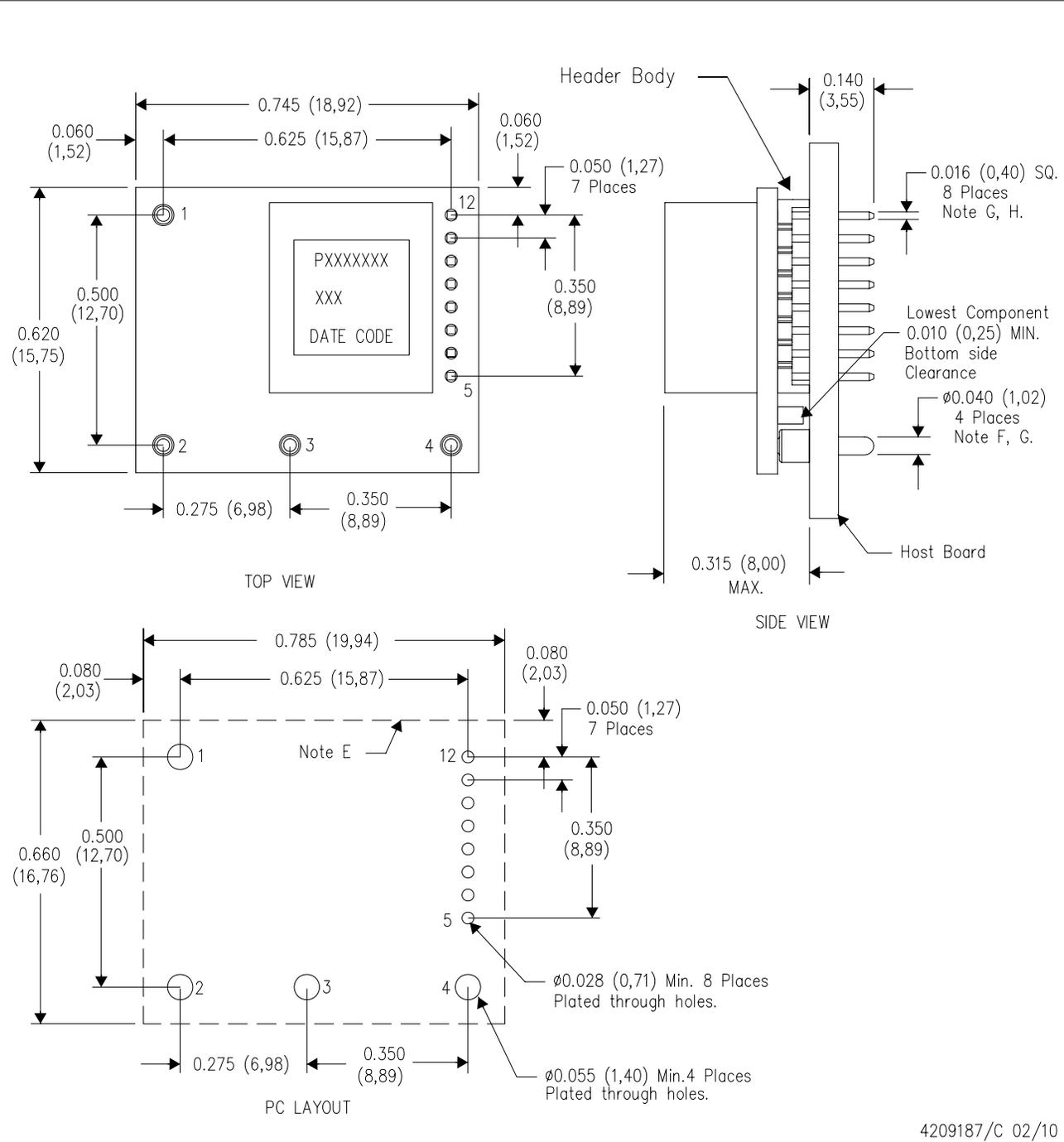
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EGS (R−PDSS−T12)   DOUBLE SIDED MODULE

0.745 (18,92)

0.625 (15,87)

0.060 (1,52)

0.060 (1,52)

0.050 (1,27) 7 Places

PXXXXXXX
XXX
DATE CODE

12

0.500 (12,70)

0.620 (15,75)

0.350 (8,89)

5

2   3   4

0.275 (6,98)   0.350 (8,89)

TOP VIEW

Header Body

0.140 (3,55)

0.016 (0,40) SQ. 8 Places Note G, H.

Lowest Component 0.010 (0,25) MIN. Bottom side Clearance

⌀0.040 (1,02) 4 Places Note F, G.

Host Board

0.315 (8,00) MAX.

SIDE VIEW

0.785 (19,94)

0.625 (15,87)

0.080 (2,03)

0.080 (2,03)

0.050 (1,27) 7 Places

Note E

12

0.500 (12,70)

0.660 (16,76)

0.350 (8,89)

5

1

2   3   4

0.275 (6,98)   0.350 (8,89)

⌀0.028 (0,71) Min. 8 Places Plated through holes.

⌀0.055 (1,40) Min.4 Places Plated through holes.

PC LAYOUT

4209187/C 02/10

NOTES: A.   All linear dimensions are in inches (mm).
         B.   This drawing is subject to change without notice.
         C.   2 place decimals are ±0.030 (±0,76mm).
         D.   3 place decimals are ±0.010 (±0,25mm).
         E.   Recommended keep out area for user components.

         F.   Pins are 0.040" (1,02) diameter with
              0.070" (1,78) diameter standoff shoulder.
         G.   Header pins are 0.016 (0,40) SQ.
         H.   All pins: Material − Copper Alloy
                        Finish − Tin (100%) over Nickel plate

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