MPM81204

16V, Quad-Output, Step-Down Power Module with Dual 5A and Dual 12A Outputs

DESCRIPTION

The MPM81204 is a quad-output, step-down power module with dual 12A and dual 5A outputs. It can achieve high efficiency across a wide output current (I_{OUT}) range, and has a wide 4V to 16V input voltage (V_{IN}) range.

Constant-on-time (COT) control provides fast transient response and easy loop stabilization.

The configurable switching frequency (f_{SW}) can be set at 600kHz, 800kHz, or 1000kHz via a resistor. This allows the device to maintain a constant f_{SW}, regardless of the input and output voltages.

Four open-drain power good (PG) signals indicate the whether the outputs are within the normal voltage range. If the input supply fails to power the device, then an external pull-up voltage clamps the PGx pin's voltage (V_{PG}) at about 0.7V.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage lockout (UVLO) protection, and thermal shutdown.

The MPM81204 requires a minimal number of readily available, standard external components, and is available in a BGA (9.5mmx16mmx4.98mm) package.

FEATURES

- Wide 4V to 16V Input Supply Range
- Dual 12A DC Outputs from 0.6V to 3.3V (Channel 0 and Channel 3)
- Dual 5A DC Outputs from 0.6V to 5.5V (Channel 1 and Channel 2)
- Constant-On-Time (COT) Control for Fast Transient Response
- Stable with Zero-ESR Output Capacitors
- Forced Continuous Conduction Mode (FCCM)
- Excellent Load Regulation
- Output Voltage (V_{OUT}) Tracking and Discharge
- PG Clamped Low Voltage during Power Failure
- Configurable Soft-Start Time (t_{SS})
- Pre-Biased Start-Up
- 600kHz, 800kHz, or 1000kHz Selectable Switching Frequency (f_{SW})
- Non-Latch Over-Current Protection (OCP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO) Protection, and Thermal Shutdown
- Available in a BGA (9.5mmx16mmx4.98mm) Package

APPLICATIONS

- Telecommunication Systems
- Networking Systems
- Servers
- Base Stations

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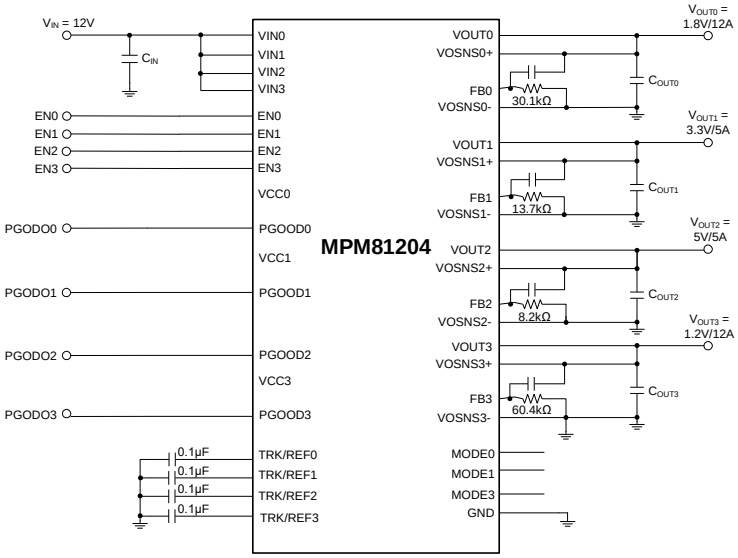
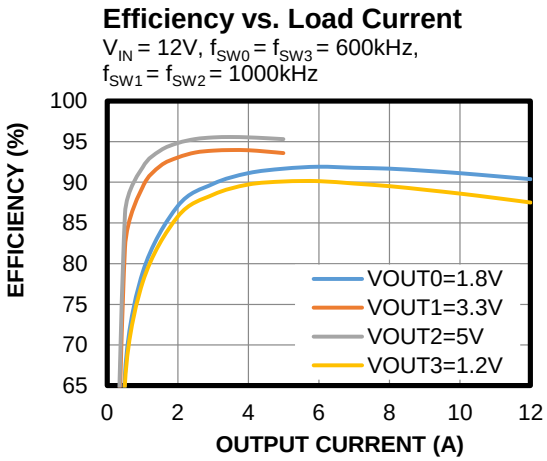
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM81204GBC	BGA (9.5mmx16mmx4.98mm)	*See Below*	3

* For Tray, add suffix -T (e.g. MPM81204GBC-T).

TOP MARKING

MPSYYWW
MP81204
LLLLLLLLL
M

MPS: MPS prefix
YY: Year code
WW: Week code
MP81204: Part number
LLLLLLLLL: Lot number
M: Module

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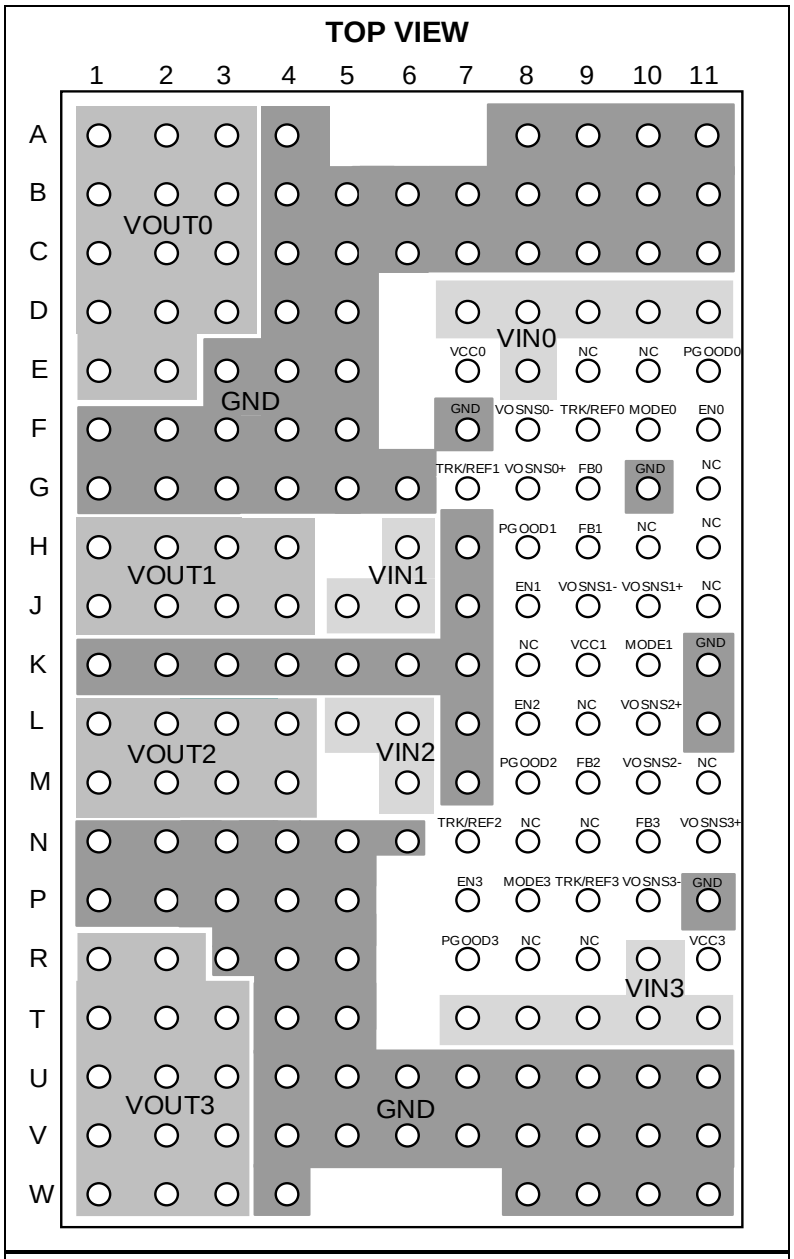
PACKAGE REFERENCE



BGA (9.5mmx16mmx4.98mm)

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PIN FUNCTIONS

Pin #	Name	Description
F10, K10, P8	MODE0, MODE1, MODE3	**Channels 0, 1, and 3 switching frequency selection.** The MODEx pin sets the switching frequency (f_{SW}) via a resistor connected between MODEx and GND (see Table 1 on page 21).
F9, G7, N7, P9	TRK/REF0, TRK/REF1, TRK/REF2, TRK/REF3	**Channels 0, 1, and 3 external tracking voltage.** The output voltage (V_{OUT}) tracks the TRK/REF input signal. Decouple the TRK/REFx pin with a ceramic capacitor placed as close to TRK/REFx as possible. X7R or X5R dielectric capacitors are recommended for their stable temperature characteristics. This capacitance also determines the soft-start time (t_{SS}) (see Equation 3 on page 21).
G8, J10, L10, N11	VOSNS0+, VOSNS1+, VOSNS2+, VOSNS3+	**Channels 0, 1, 2, and 3 differential remote-sense positive input.** There is an integrated 60.4kΩ resistor connected between the VOSNSx+ and FBx pins. Connect the VOSNSx+ pin directly to the positive side of the voltage sense point.
F8, J9, M10, P10	VOSNS0-, VOSNS1-, VOSNS2-, VOSNS3-	**Channels 0, 1, 2, and 3 differential remote-sense negative input.** Connect the VOSNSx- pin directly to the negative side of the voltage sense point. If remote sense is not being used, then short VOSNSx- to GND.
G9, H9, M9, N10	FB0, FB1, FB2, FB3	**Channels 0, 1, 2, and 3 feedback channel.** V_{OUT} is set via an external resistor divider connected between the output and VOSNSx- or GND (tapped to FB). Place this resistor divider as close to FB as possible.
F11, J8, L8, P7	EN0, EN1, EN2, EN3	**Channels 0, 1, 2, and 3 enable (EN).** The ENx pin enables and disables the regulator. Pull ENx high to turn the regulator on; pull ENx low to turn the regulator off. For automatic start-up, place a pull-up resistor or a voltage resistor divider between ENx and VINx. Do not float ENx.
E11, H8, M8, R7	PG0, PG1, PG2, PG3	**Channels 0, 1, 2, and 3 power good (PG).** The PGx pin is an open-drain signal. A pull-up resistor connected to a DC voltage is required, and indicates whether V_{OUT} is within its regulation range. There is a delay (about 0.9ms) from when FBx exceeds 92.5% of the reference voltage (V_{REF}) to when PGx pulls high.
D7, D8, D9, D10, D11, E8, H6, J5, J6, L5, L6, M6, R10, T7, T8, T9, T10, T11	VIN0, VIN1 VIN2, VIN3	**Channels 0, 1, 2, and 3 input voltage (V_{IN}).** The VINx pin supplies power to the internal MOSFET and regulator. Input capacitors are required to decouple the input rail. Use wide PCB traces to make this connection.
A4, A8, A9, A10, A11, B4, B5, B6, B7, B8, B9, B10, B11, C4, C5, C6, C7, C8, C9, C10, C11, D4, D5, E3, E4, E5, F1, F2, F3, F4, F5, F7, G1, G2, G3, G4, G5, G6, G10, H7, J7, K1, K2, K3, K4, K5, K6, K7, K11, L7, L11, M7, N1, N2, N3, N4, N5, N6, P1, P2, P3, P4, P5, P11, R3, R4, R5, T4, T5, U4, U5, U6, U7, U8, U9, U10, U11, V4, V5, V6, V7, V8, V9, V10, V11, W4, W8, W9, W10, W11	GND	**System ground.** The GND pin is the regulated V_{OUT}'s reference ground. Connect wide copper PCB traces to GND.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
E7, K9, R11	VCC0, VCC1, VCC3	**Channels 0, 1, and 3 internal 3V LDO output.** The VCCx pin powers the driver and the control circuits.
A1, A2, A3, B1, B2, B3, C1, C2, C3, D1, D2, D3, E1, E2, H1, H2, H3, H4, J1, J2, J3, J4, L1, L2, L3, L4, M1, M2, M3, M4, R1, R2, T1, T2, T3, U1, U2, U3, V1, V2, V3, W1, W2, W3	VOUT0, VOUT1, VOUT2, VOUT3	**Channels 0, 1, 2, and 3 power output.** Place a low-ESR capacitor as close to the chip as possible, with a short return path to the ground plane.

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PIN MAP

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
A1	VOUT0	B4	GND	C4	GND	D4	GND	E5	GND	F7	GND
A2	VOUT0	B5	GND	C5	GND	D5	GND	E7	VCC0	F8	VOSNS0-
A3	VOUT0	B6	GND	C6	GND	D7	VIN0	E8	VIN0	F9	TRK/REF0
A4	GND	B7	GND	C7	GND	D8	VIN0	E9	NC	F10	MODE0
A8	GND	B8	GND	C8	GND	D9	VIN0	E10	NC	F11	EN0
A9	GND	B9	GND	C9	GND	D10	VIN0	E11	PG0	G1	GND
A10	GND	B10	GND	C10	GND	D11	VIN0	F1	GND	G2	GND
A11	GND	B11	GND	C11	GND	E1	VOUT0	F2	GND	G3	GND
B1	VOUT0	C1	VOUT0	D1	VOUT0	E2	VOUT0	F3	GND	G4	GND
B2	VOUT0	C2	VOUT0	D2	VOUT0	E3	GND	F4	GND	G5	GND
B3	VOUT0	C3	VOUT0	D3	VOUT0	E4	GND	F5	GND	G6	GND

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
G7	TRK/REF1	H8	PG1	J8	EN1	K8	NC	L8	EN2	M9	FB2
G8	VOSNS0+	H9	FB1	J9	VOSNS1-	K9	VCC1	L9	NC	M10	VOSNS2-
G9	FB0	H10	NC	J10	VOSNS1+	K10	MODE1	L10	VOSNS2+	M11	NC
G10	GND	H11	NC	J11	NC	K11	GND	L11	GND	N1	GND
G11	NC	J1	VOUT1	K1	GND	L1	VOUT2	M1	VOUT2	N2	GND
H1	VOUT1	J2	VOUT1	K2	GND	L2	VOUT2	M2	VOUT2	N3	GND
H2	VOUT1	J3	VOUT1	K3	GND	L3	VOUT2	M3	VOUT2	N4	GND
H3	VOUT1	J4	VOUT1	K4	GND	L4	VOUT2	M4	VOUT2	N5	GND
H4	VOUT1	J5	VIN1	K5	GND	L5	VIN2	M6	VIN2	N6	GND
H6	VIN1	J6	VIN1	K6	GND	L6	VIN2	M7	GND	N7	TRK/REF2
H7	GND	J7	GND	K7	GND	L7	GND	M8	PG2	N8	NC

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
N9	NC	P10	VOSNS3-	R11	VCC3	U1	VOUT3	V1	VOUT3	W1	VOUT3
N10	FB3	P11	GND	T1	VOUT3	U2	VOUT3	V2	VOUT3	W2	VOUT3
N11	VOSNS3+	R1	VOUT3	T2	VOUT3	U3	VOUT3	V3	VOUT3	W3	VOUT3
P1	GND	R2	VOUT3	T3	VOUT3	U4	GND	V4	GND	W4	GND
P2	GND	R3	GND	T4	GND	U5	GND	V5	GND	W8	GND
P3	GND	R4	GND	T5	GND	U6	GND	V6	GND	W9	GND
P4	GND	R5	GND	T7	VIN3	U7	GND	V7	GND	W10	GND
P5	GND	R7	PG3	T8	VIN3	U8	GND	V8	GND	W11	GND
P7	EN3	R8	NC	T9	VIN3	U9	GND	V9	GND		
P8	MODE3	R9	NC	T10	VIN3	U10	GND	V10	GND		
P9	TRK/REF3	R10	VIN3	T11	VIN3	U11	GND	V11	GND		

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
Output voltage (V_{OUT1}, V_{OUT2}) 6V
VCCx voltage (V_{CC}), ENx voltage (V_{EN}).....4.5V
All other pins..... -0.3V to +4.3V
Continuous power dissipation (T_A = 25°C) (2) (4)
.....10.42W
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +170°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
Output voltage (V_{OUT1}, V_{OUT2}) ..... 0.6V to 5.5V
Output voltage (V_{OUT0}, V_{OUT3}) ..... 0.6V to 3.3V
Max VOUTx current (I_{OUT_MAX1}, I_{OUT_MAX2}).....5A
Max VOUTx current (I_{OUT_MAX0}, I_{OUT_MAX3}).....12A
EN voltage (V_{EN}) 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC_TOP}

EVM81204-BC-00A ..... 9.6.... 2.25...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JA}: Thermal resistance from junction to ambient.
θ_{JC_TOP}: Thermal resistance from junction to top of package.
Measured on EVM81204-BC-00A, 12cmx11cm, 6-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [5], typical values are tested at 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Shutdown current	I_{SD}	V_{EN} = 0V, all channels		0	12	μA
Quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.62V, all channels		2.6	3.4	mA
Current Limit						
Current-sense (CS) current to output current ratio	I_{CS} / I_{OUT}	I_{OUT} ≥ 2A	18	20	22	μA/A
Low-side (LS) negative current limit	$I_{LIM\_NEG\_LS}$			-7.5		A
Negative current limit timer [6]	t_{LIM_NEG}			200		ns
Switching Frequency (f_{SW})						
Switching frequency	f_{SW}	MODEx = GND, I_{OUT} = 0A, V_{OUT} = 1V	480	600	720	kHz
		MODEx = 60.4kΩ, I_{OUT} = 0A, V_{OUT} = 1V	680	800	920	kHz
		I_{OUT} = 0A, V_{OUT} = 1V	850	1000	1150	kHz
Minimum on time [6]	t_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time [6]	t_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage Protection (OVP)						
OVP threshold	V_{OVP}	% of V_{REF}	113%	116%	119%	V_{REF}
Feedback (FB) Voltage (V_{FB}) and Soft-Start (SS)						
FBx voltage	V_{FB}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to 70°C	597	600	603	mV
TRK/REFx source current	I_{TRK/REF_SOURCE}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REFx sink current	I_{TRK/REF_SINK}	$V_{TRK/REF}$ = 1V		12		μA
Error Amplifier (EA)						
EA offset	V_{EA_OFFSET}		-3	0	+3	mV
FBx current	I_{FB}	V_{FB} = V_{REF}		50	100	nA
Enable (EN) and Under-Voltage Lockout (UVLO) Protection						
ENx input rising threshold	V_{EN_RISING}		1.19	1.22	1.25	V
ENx hysteresis	V_{EN_HYS}		160	220	280	mV
ENx input current	I_{EN}	V_{EN} = 2V		0		μA
Shutdown discharge FET	R_{ON_DISCH}			80	150	Ω
V_{IN} UVLO Protection						
V_{IN} UVLO rising threshold	$V_{IN\_UVLO\_RISING}$	V_{CC} = 3.3V	2.1	2.4	2.7	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$	V_{CC} = 3.3V	1.55	1.85	2.15	V
VCC Regulator						
V_{CC} UVLO rising threshold	V_{CC_RISING}		2.65	2.8	2.95	V
V_{CC} UVLO falling threshold	$V_{CC\_FALLING}$		2.35	2.5	2.65	V
VCCx regulator	V_{CC}		2.88	3	3.12	V
VCCx load regulation		I_{CC} = 25mA		0.5		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (5), typical values are tested at 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good (PG)						
PGx high rising threshold	$V_{PG\_RISING\_HIGH}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
PGx high falling threshold	$V_{PG\_FALLING\_HIGH}$	FB from high to low	102%	105%	108%	V_{REF}
PGx low rising threshold	$V_{PG\_RISING\_LOW}$	FB from low to high	113%	116%	119%	V_{REF}
PGx low falling threshold	$V_{PG\_FALLING\_LOW}$	FB from high to low	77%	80%	83%	V_{REF}
PGx low-to-high delay	t_{DELAY_PG}	T_J = 25°C	0.63	0.9	1.17	ms
PGx sink current	V_{PG}	I_{PG} = 10mA			0.4	V
PGx leakage current	I_{PG_LEAK}	V_{PG} = 3.3 V			3	µA
PGx low-level output voltage	V_{OUT_LOW}	V_{IN} = 0V, use a 100kΩ resistor to pull PGx up to 3.3V		650	850	mV
		V_{IN} = 0V, use a 10kΩ resistor to pull PGx up to 3.3V		800	1000	mV
Thermal Protection						
Thermal shutdown (6)	T_{SD}			160		°C
Thermal shutdown hysteresis (6)				30		°C

Notes:

5) Guaranteed by over-temperature (OT) correlation. Not tested in production.
6) Guaranteed by engineering sample characterization.

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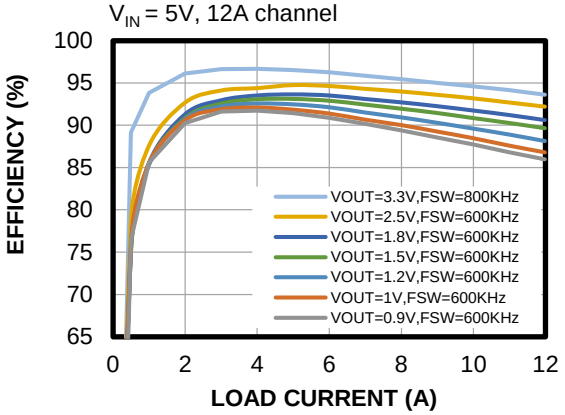
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT0} = 1.8V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{OUT3} = 1.2V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, FCCM, T_A = 25°C, unless otherwise noted.

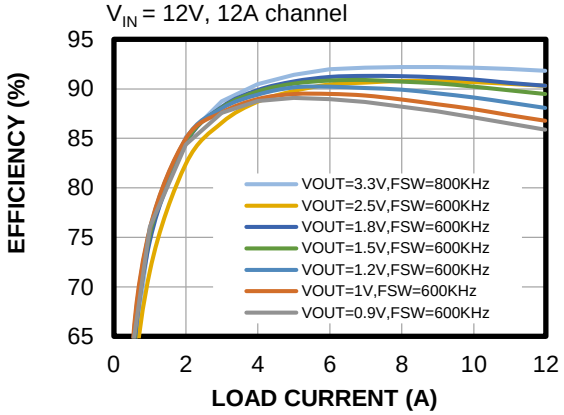
Efficiency vs. Load Current

V_{IN} = 5V, 12A channel



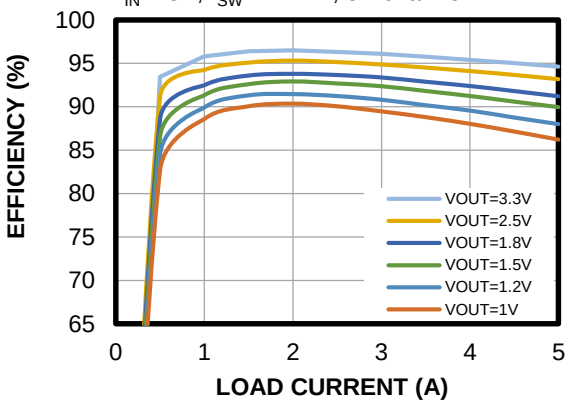
Efficiency vs. Load Current

V_{IN} = 12V, 12A channel



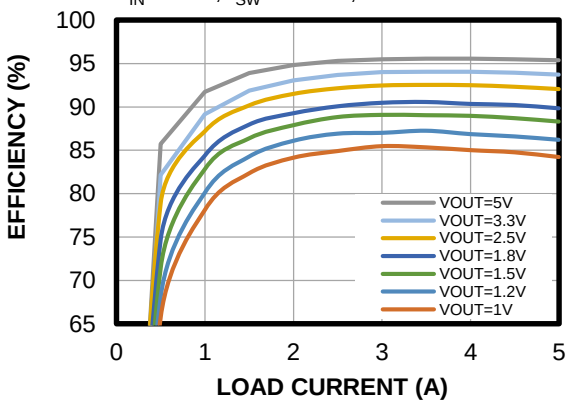
Efficiency vs. Load Current

V_{IN} = 5V, f_{SW} = 1MHz, 5A channel



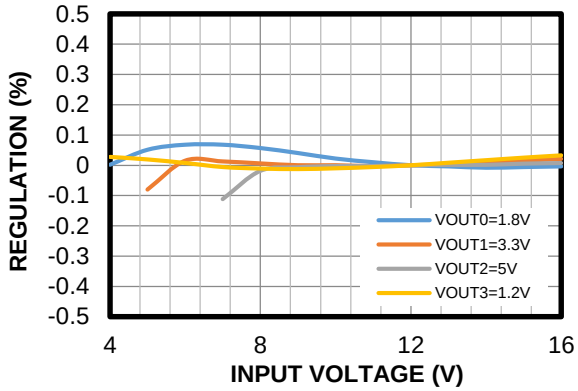
Efficiency vs. Load Current

V_{IN} = 12V, f_{SW} = 1MHz, 5A channel



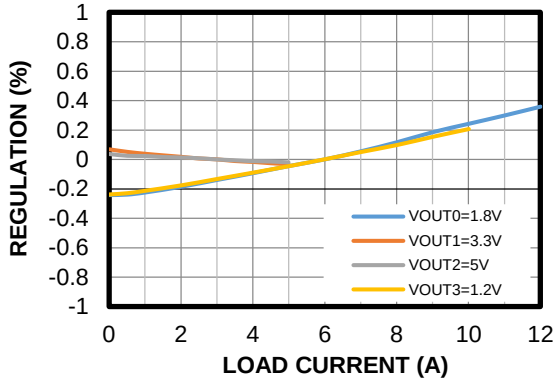
Line Regulation

f_{SW0} = f_{SW3} = 600kHz,
f_{SW1} = f_{SW2} = 1MHz, full load



Load Regulation

V_{IN} = 12V, f_{SW0} = f_{SW3} = 600kHz,
f_{SW1} = f_{SW2} = 1MHz



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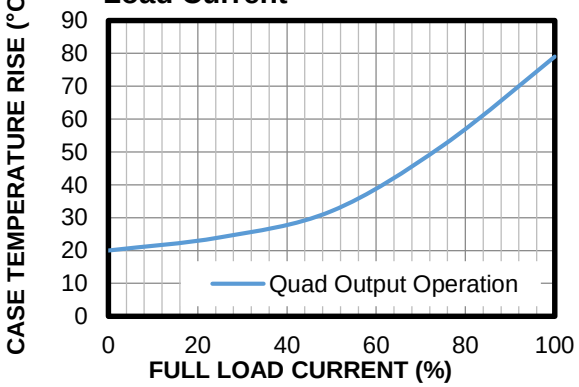
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

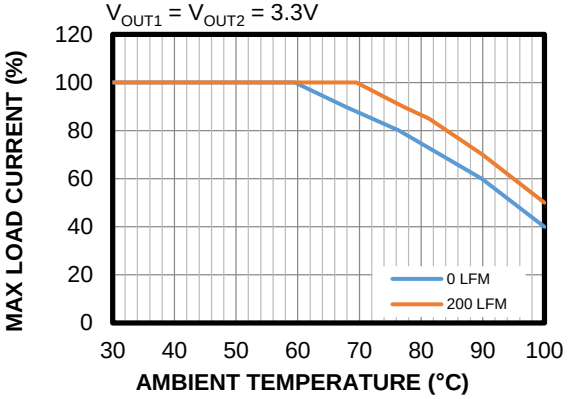
V_{IN} = 12V, V_{OUT0} = 1.8V, V_{OUT1} = 3.3V, V_{OUT2} = 5V, V_{OUT3} = 1.2V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, FCCM, T_A = 25°C, unless otherwise noted.

Case Temperature Rise vs. Full Load Current



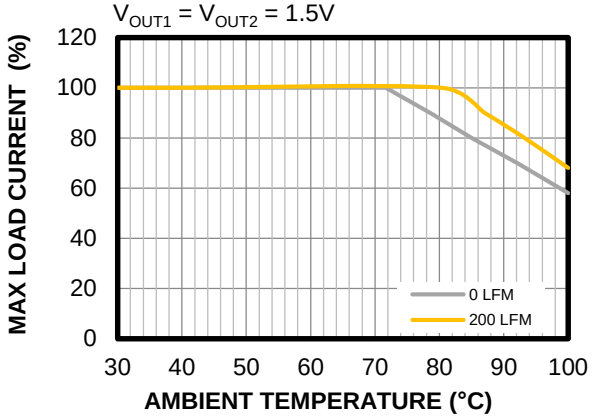
Thermal Derating

V_{IN} = 12V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, V_{OUT0} = V_{OUT3} = 1.8V, V_{OUT1} = V_{OUT2} = 3.3V



Thermal Derating

V_{IN} = 12V, f_{SW0} = f_{SW3} = 600kHz, f_{SW1} = f_{SW2} = 1MHz, V_{OUT0} = V_{OUT3} = 1V, V_{OUT1} = V_{OUT2} = 1.5V



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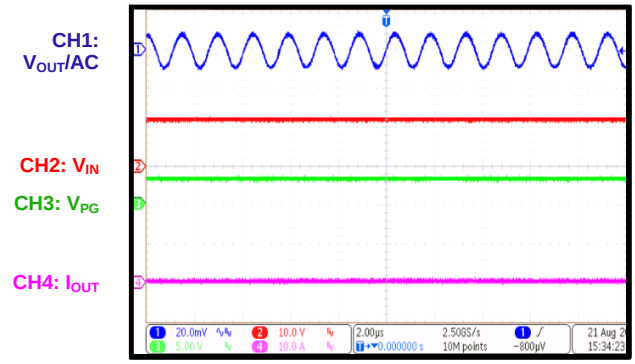
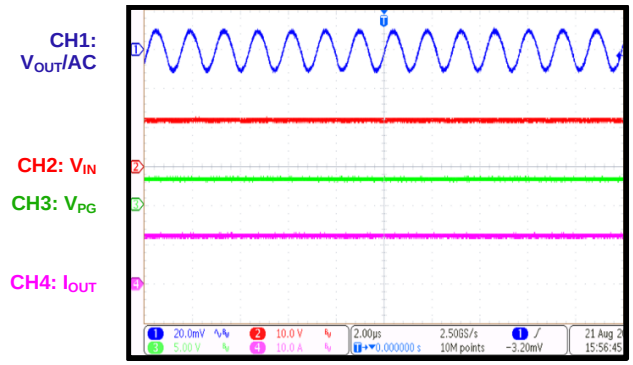
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

12A channel, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz, C_{OUT} = 3 x 47µF ceramic capacitor + 220µF aluminum electrolytic SP capacitor, T_A = 25°C, unless otherwise noted.

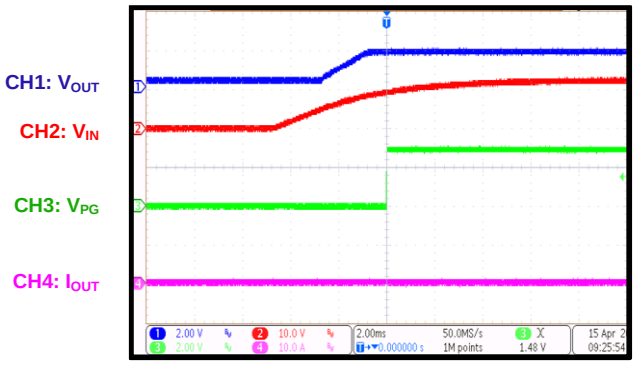
Steady State
I_{OUT} = 0A



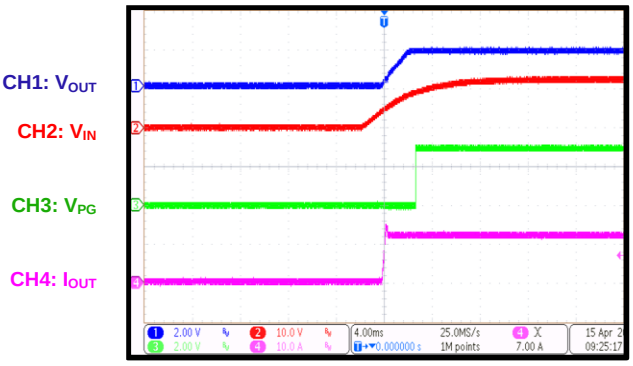
Steady State
I_{OUT} = 12A



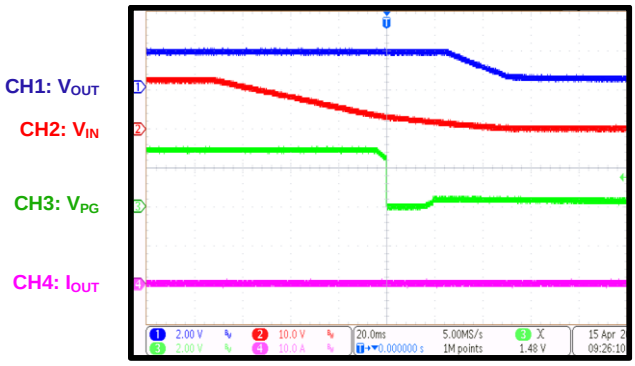
Start-Up through VINx
I_{OUT} = 0A



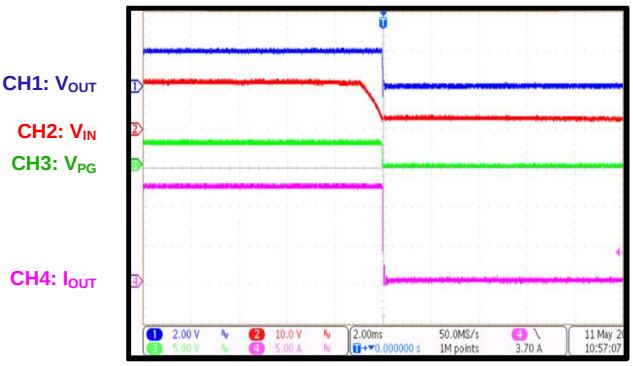
Start-Up through VINx
I_{OUT} = 12A



Shutdown through VINx
I_{OUT} = 0A



Shutdown through VINx
I_{OUT} = 12A



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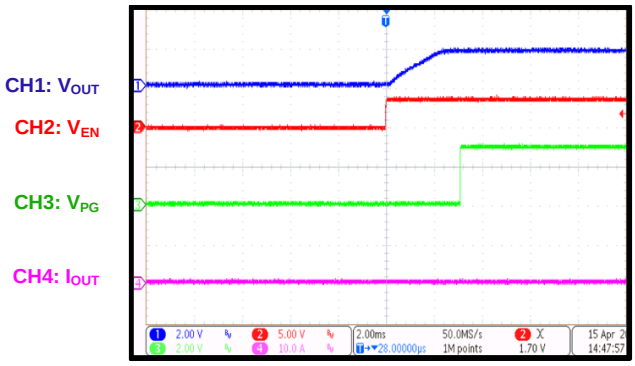
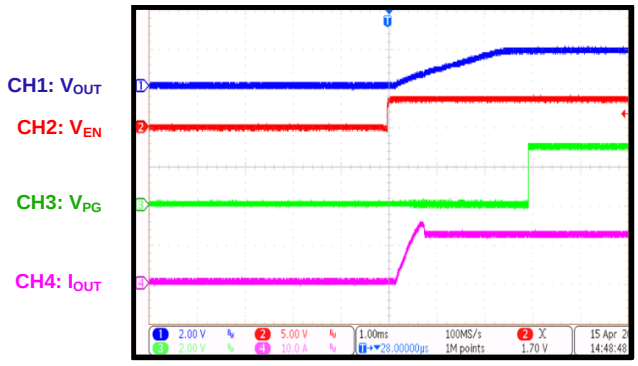
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

12A channel, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz, C_{OUT} = 3 x 47µF ceramic capacitor + 220µF aluminum electrolytic SP capacitor, T_A = 25°C, unless otherwise noted.

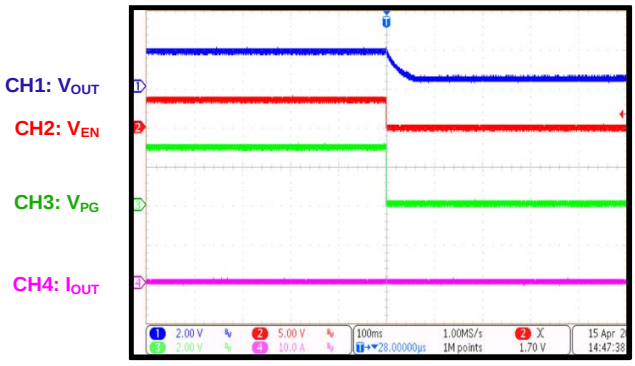
Start-Up through ENx
I_{OUT} = 0A



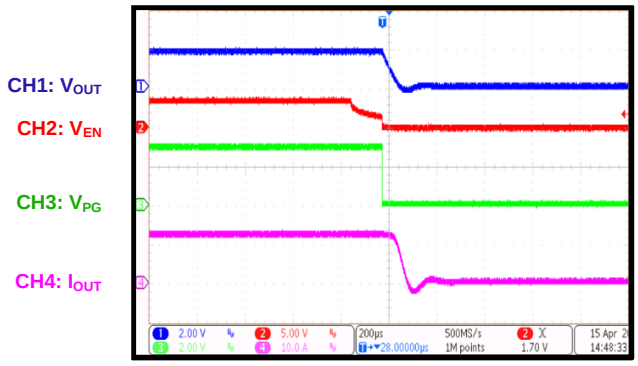
Start-Up through ENx
I_{OUT} = 12A



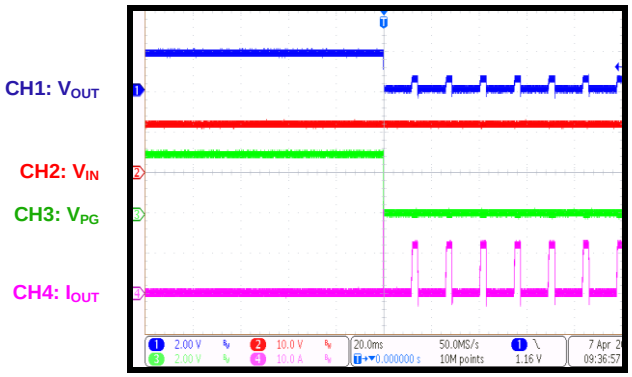
Shutdown through ENx
I_{OUT} = 0A



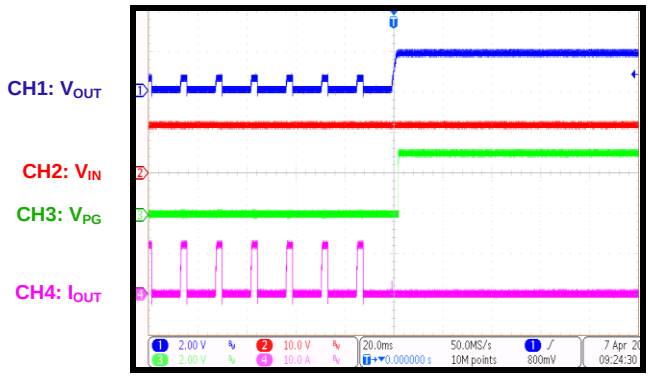
Shutdown through ENx
I_{OUT} = 12A



SCP Entry
I_{OUT} = 0A



SCP Recovery
I_{OUT} = 0A



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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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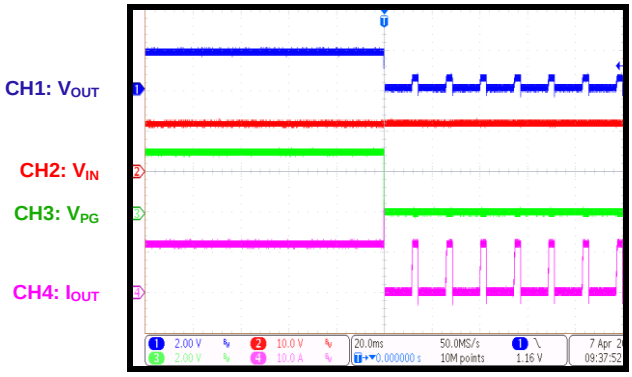
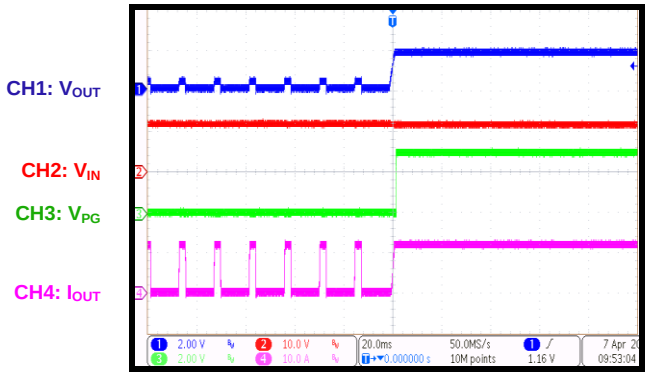
SCP Entry

I_{OUT} = 12A



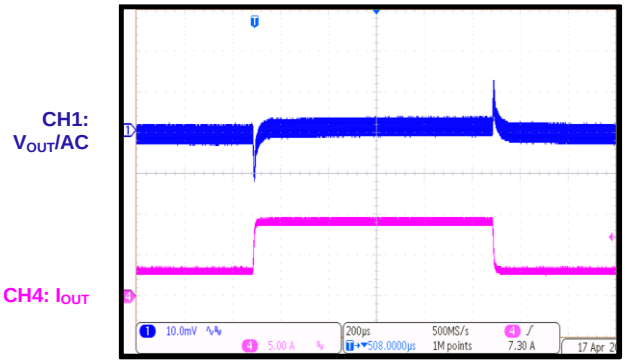
SCP Recovery

I_{OUT} = 12A



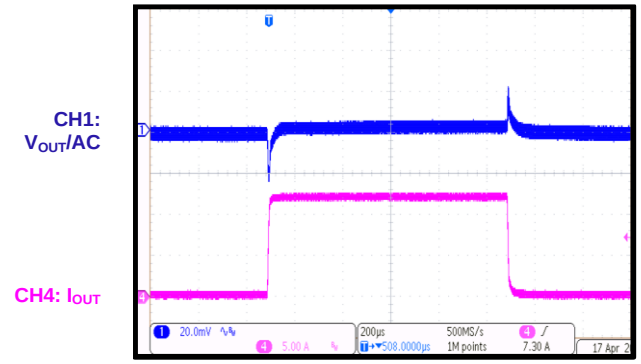
Load Transient Response

3A to 9A load step, 2.5A/µs



Load Transient Response

0A to 12A load step, 2.5A/µs



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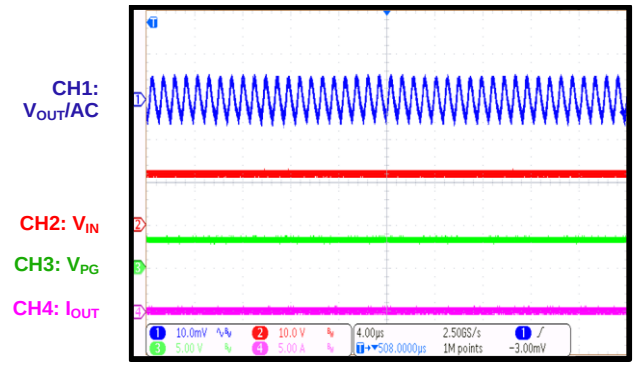
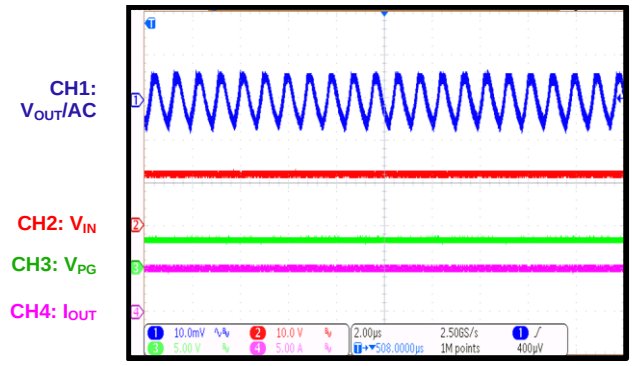
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

5A channel, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz, C_{OUT} = 5 x 47µF ceramic capacitor, T_A = 25°C, unless otherwise noted.

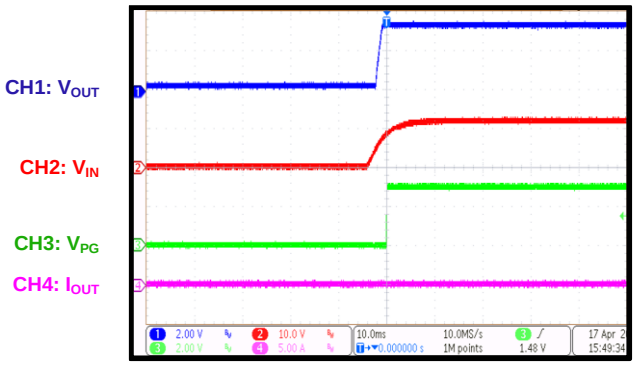
Steady State
I_{OUT} = 0A



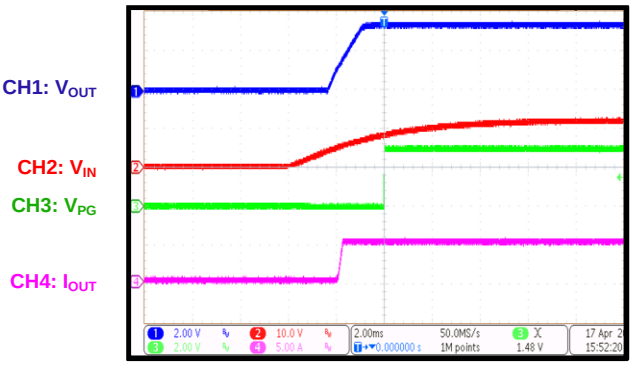
Steady State
I_{OUT} = 5A



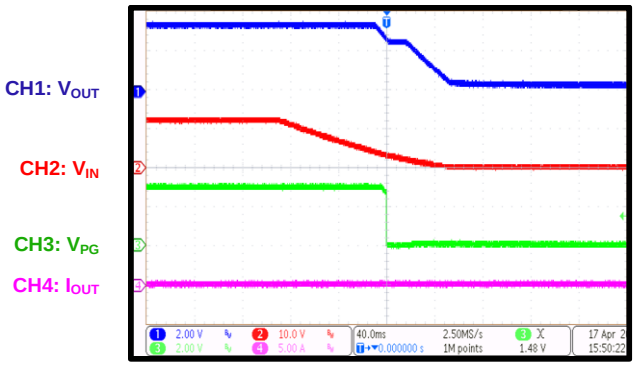
Start-Up through VINx
I_{OUT} = 0A



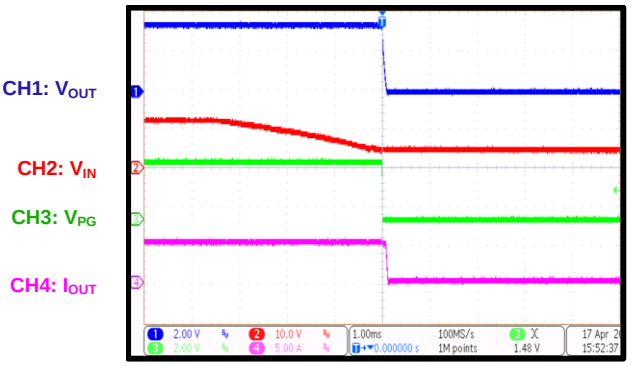
Start-Up through VINx
I_{OUT} = 5A



Shutdown through VINx
I_{OUT} = 0A



Shutdown through VINx
I_{OUT} = 5A



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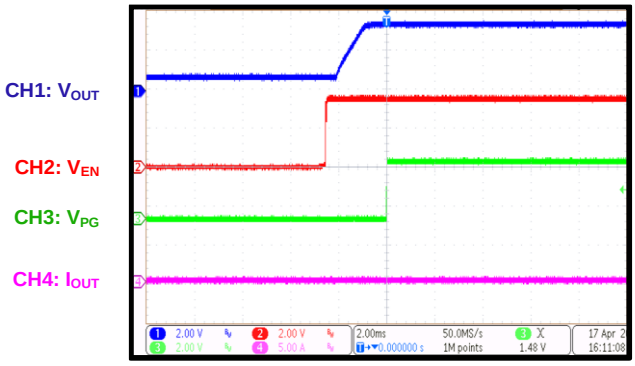
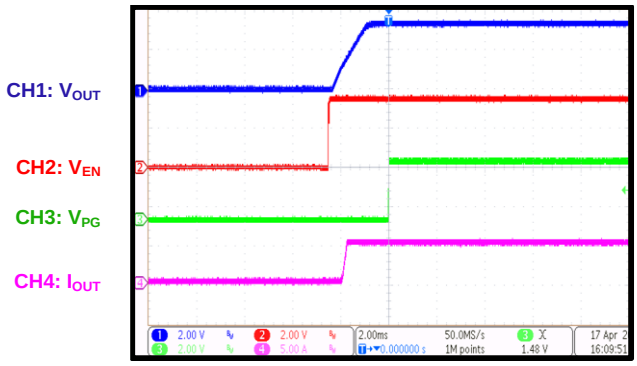
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

5A channel, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz, C_{OUT} = 5 x 47µF ceramic capacitor, T_A = 25°C, unless otherwise noted.

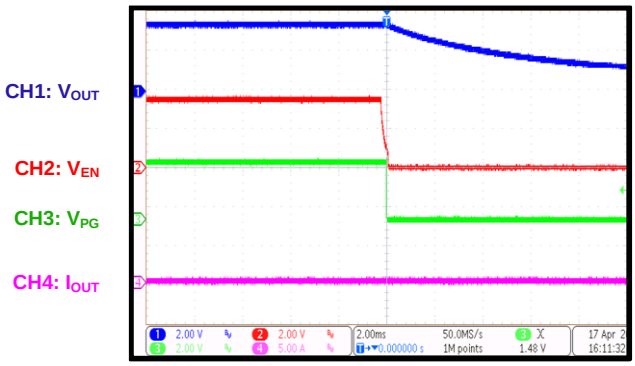
Start-Up through ENx
I_{OUT} = 0A



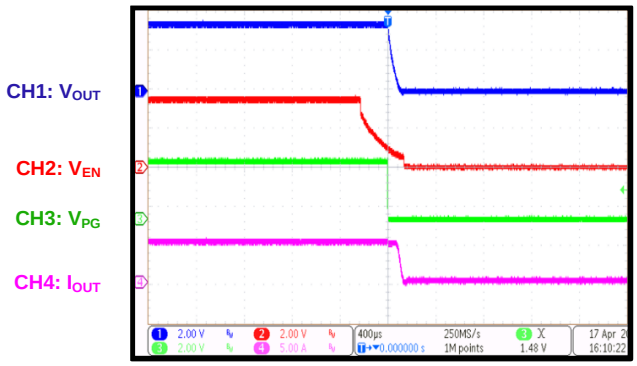
Start-Up through ENx
I_{OUT} = 5A



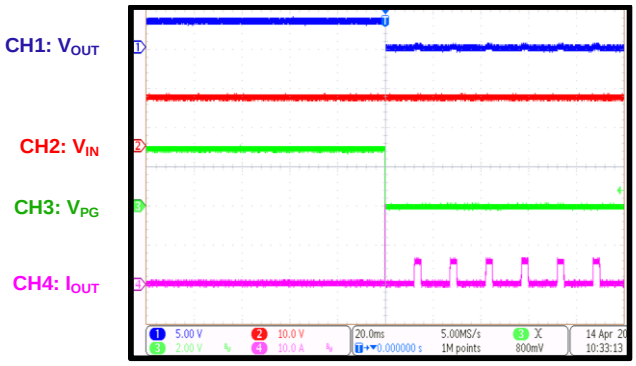
Shutdown through ENx
I_{OUT} = 0A



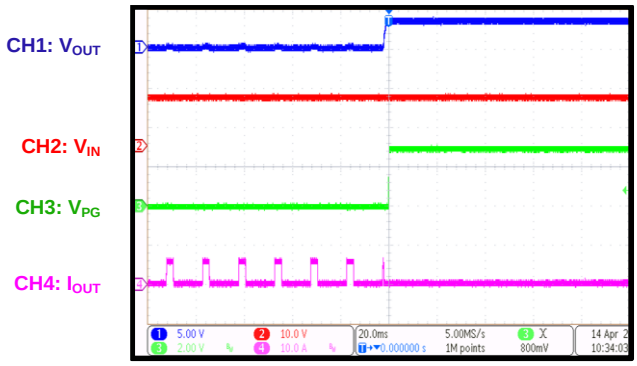
Shutdown through ENx
I_{OUT} = 5A



SCP Entry
I_{OUT} = 0A



SCP Recovery
I_{OUT} = 0A



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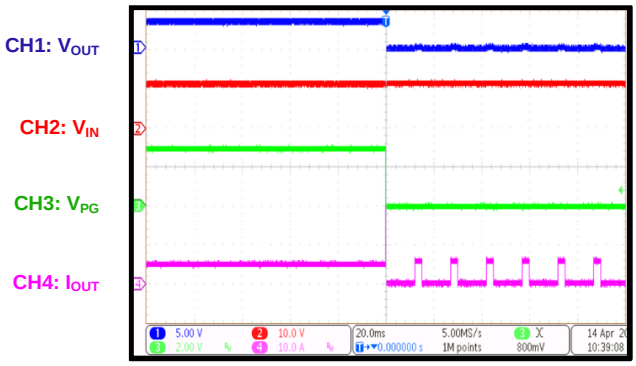
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

5A channel, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz, C_{OUT} = 5 x 47µF ceramic capacitor, T_A = 25°C, unless otherwise noted.

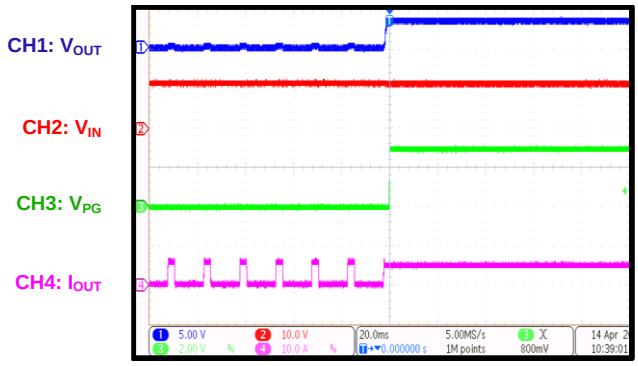
SCP Entry

I_{OUT} = 5A



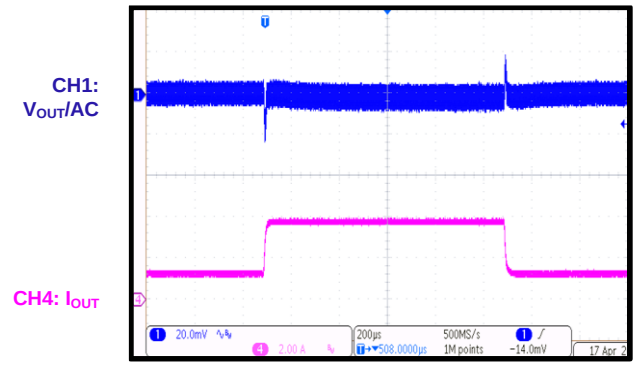
SCP Recovery

I_{OUT} = 5A



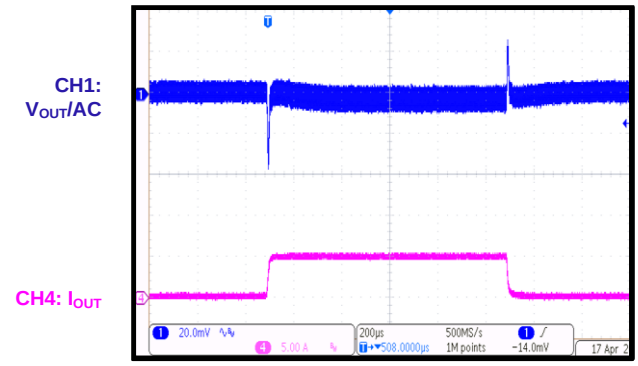
Load Transient

1.25A to 3.75A load step, 2.5A/µs



Load Transient

0A to 5A load step, 2.5A/µs



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FUNCTIONAL BLOCK DIAGRAM

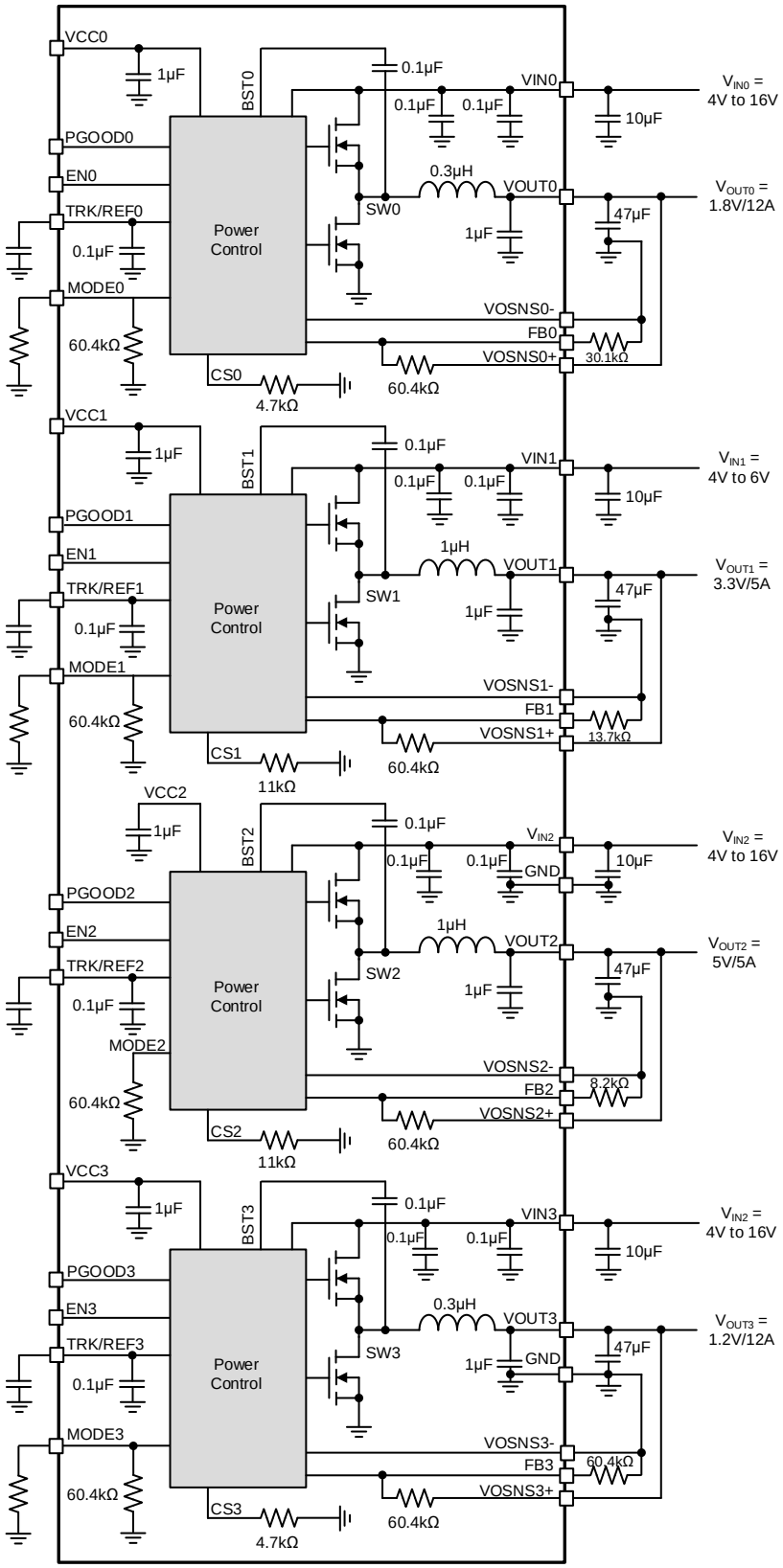

Figure 1: Functional Block Diagram

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OPERATION

Constant-On-Time (COT) Control

The MPM81204 employs constant-on-time (COT) control to achieve fast load transient response. Figure 2 shows the details of COT control.

The operational amplifier (op amp) corrects voltage errors between the feedback (FB) voltage (V_{FB}) and the reference voltage (V_{REF}). It also provides excellent load regulation across the entire output voltage (V_{OUT}) range.

Internal ramp compensation supports low-ESR MLCC output capacitor (C_{OUT}) solutions. The adjustable internal ramp, in conjunction with a proper output L/C filter design, stabilizes the MPM81204 across both the operating input voltage (V_{IN}) range and the output voltage (V_{OUT}) range.

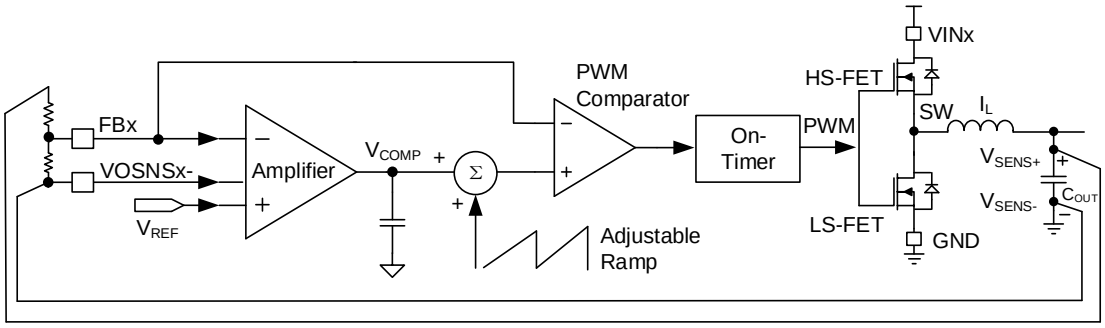

Figure 2: Constant-On-Time (COT) Control

Pulse-Width Modulation (PWM) Mode

The amplifier corrects voltage errors between V_{FB} and V_{REF}, and generates a smooth DC COMP voltage (V_{COMP}). The internal ramp is superimposed onto V_{COMP}, which is compared to V_{FB}. If V_{FB} drops below V_{COMP}, then the high-side MOSFET (HS-FET) turns on. The HS-FET remains on for a fixed on time (t_{ON}). t_{ON} is determined by V_{IN}, V_{OUT}, and the switching frequency (f_{SW}). After t_{ON} elapses, the HS-FET turns off. It turns on again once V_{FB} drops below V_{COMP}. The MPM81204 regulates V_{OUT} by repeating this operation. Figure 3 shows PWM mode.

To minimize conduction loss, the low-side MOSFET (LS-FET) turns on once the HS-FET turns off. If both the HS-FET and LS-FET turn on at the same time, then a dead short occurs between the VINx pin and GND. This is known as shoot-through. To avoid shoot-through, a dead time (DT) is inserted between the HS-FET off period and the LS-FET on period, and vice versa.

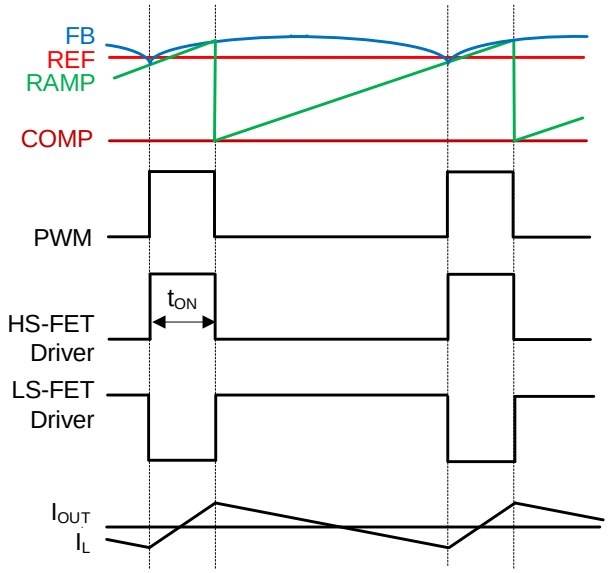

Figure 3: Pulse-Width Modulation (PWM) Mode

Enable (EN) Configuration

The MPM81204's enable (EN) pins (EN0, EN1, EN2, and EN3) enable and disable their respective channel's regulator. Pull ENx high to turn the regulator on; pull ENx low to turn the regulator off. Do not float ENx. If necessary, all four EN pins can be connected together. ENx can also be driven by an analog or digital control signal to turn the MPM81204 on and off.

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The device's accurate EN thresholds allow a resistor divider connected between VINx and GND to configure the start-up V_{IN} threshold.

It is recommended to use the configurable V_{IN} threshold for applications that do not have a dedicated EN control signal. This prevents triggering the under-voltage lockout (UVLO) threshold during start-up and shutdown. The resistor divider value (R_{UP} + R_{DOWN}) can be calculated with Equation (1):

$$V_{IN\_START}(V) = V_{EN\_RISING} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (1)$$

Where V_{IN_START} is the start-up threshold, and V_{EN_RISING} is typically 1.22V.

Choose the R_{UP} and R_{DOWN} values so that the EN voltage (V_{EN}) does not exceed 3.6V once V_{IN} reaches its maximum value.

ENx can also be directly connected to VINx via a pull-up resistor (R_{UP}). Choose R_{UP}'s resistance so that the maximum current flowing to ENx is 50μA. The pull-up resistance (R_{UP}) can be calculated with Equation (2):

$$R_{UP}(k\Omega) = \frac{V_{IN\_MAX}(V)}{0.05(mA)} \quad (2)$$

Forced Continuous Conduction Mode (FCCM)

The MPM81204 operates in forced continuous conduction mode (FCCM) by default. In FCCM, f_{SW} is fairly constant, and the V_{OUT} ripple remains about the same across the entire V_{OUT} range.

Mode Selection

The MPM81204 has three selectable switching frequencies. The resistor connected between the MODE pin and GND sets f_{SW}. Table 1 shows the MODEx selections and their corresponding f_{SW}.

Table 1: Selectable f_{SW} for Different MODEx Settings

MODEx	f_{SW}
MODEx is connected to GND directly	600kHz
MODEx is connected to GND via a 60.4kΩ resistor	800kHz
Floating	1000kHz

Soft Start (SS)

The minimum soft-start time (t_{SS}) is 1.67ms. To increase t_{SS}, add a soft-start capacitor (C_{SS}) between the TRK/REF pin and GND.

C_{SS} can be calculated with Equation (3):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 36\mu A}{0.6(V)} \text{-}100nF \quad (3)$$

Output Voltage Tracking and Output Voltage Reference

The MPM81204 provides four analog input pins (TRK/REF0, TRK/REF1, TRK/REF2, and TRK/REF3) to track external power supplies or to accept an external reference. If an external voltage is connected to TRK/REFx, then this external voltage acts as a reference for V_{OUT}. V_{FB} follows this external voltage signal and ignores all soft-start settings. The TRK/REFx input voltage signal can range from 0.3V to 1.4V. To ensure proper operation, the TRK/REFx voltage ($V_{TRK/REF}$) must reach or exceed 600mV during start-up. After start-up, $V_{TRK/REF}$ can be between 0.3V and 1.4V.

Pre-Biased Start-Up

The MPM81204 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, then the IC turns off the HS-FET and LS-FET until $V_{TRK/REF}$ exceeds the sensed V_{OUT} at the FBx pin. If the BST voltage (V_{BST}) from BSTx to SW is below 2.3V before $V_{TRK/REF}$ reaches FB's pre-biased level, then the LS-FET turns on to allow V_{BST} to be charged via V_{CC}. The LS-FET turns on for very narrow pulses, making the pre-biased voltage drop insignificant.

Output Voltage Discharge

A shutdown through ENx enables V_{OUT} discharge mode. V_{OUT} discharge mode causes both the HS-FET and LS-FET to latch off. A discharge FET connected between SW and GND turns on to discharge V_{OUT}. This FET's on resistance is typically 80Ω. If V_{FB} drops below 10% of V_{REF}, the discharge FET turns off.

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Current Sense (CS) and Over-Current Protection (OCP)

The MPM81204 features an on-die current sense (CS). Once the MPM81204 turns on, the current limit (I_{LIMIT}) is active. During the LS-FET on period, the inductor current (I_L) is sensed and mirrored to I_{CS} with the current-sense gain (G_{CS}) ratio. There is an internally integrated resistor (R_{CS}) connected between CS and GND. The CS voltage (V_{CS}) is proportional to the cycle-by-cycle SW current (I_{SW}). During the LS-FET on period, the HS-FET can only turn on once V_{CS} drops below the over-current protection (OCP) threshold (V_{OCP}), which limits I_{SW} cycle by cycle.

After start-up, there is a 3ms delay time (t_{DELAY}) and then the device enables OCP hiccup mode. If an over-current (OC) condition is detected for 31 consecutive cycles, then the part enters hiccup mode. In hiccup mode, the HS-FET turns off and the LS-FET turns off after zero-current detection (ZCD). Meanwhile, the TRK/REF capacitor is discharged. After about 11ms, the MPM81204 initiates a soft start (SS) to turn the device on again. If the OC condition is still present after the 3ms t_{DELAY}, then the device repeats this operation until the OC condition is removed and V_{OUT} reaches its regulation level.

Negative Inductor Current Limit

If the LS-FET detects a -7.5A current, then it turns off for 200ns to limit the negative current.

Output Sink Mode (OSM)

The MPM81204 employs output sink mode (OSM) to regulate V_{OUT} at its target value. If V_{FB} exceeds 104% of V_{REF}, but is below the over-voltage protection (OVP) threshold (V_{OVP}), then OSM is triggered. In OSM, the LS-FET remains on until it reaches its -5.5A negative current limit (I_{LIM_NEG}). Once the LS-FET reaches its -5.5A I_{LIM_NEG}, the LS-FET turns off for 200ns and the HS-FET on for 200ns. After 200ns, the LS-FET turns on again and the HS-FET turns off. The device repeats this operation until V_{FB} drops below 102% of V_{REF}. Once V_{FB} drops below 102% of V_{REF}, the part exits OSM after 15 consecutive FCCM cycles.

Over-Voltage Protection (OVP)

The MPM81204 monitors V_{OUT} by connecting FBx to the tap of the V_{OUT} feedback resistor divider. This detects whether an over-voltage (OV) condition has occurred. It also provides OVP hiccup mode.

If V_{FB} exceeds 116% of V_{REF}, then OVP is triggered. The power good (PGx) pin is pulled low until it reaches its $I_{LIM\_NEG\_LS}$. Once PGx reaches $I_{LIM\_NEG\_LS}$, then the LS-FET turns off for 200ns and the HS-FET on for 200ns. After 200ns, the LS-FET turns on again and the HS-FET turns off.

The device repeats this operation until the output OV condition is removed. Once V_{FB} drops below 105% of V_{REF}, the part exits OVP discharge mode.

Thermal Shutdown

Thermal shutdown protects the internal circuitry from overheating. The IC monitors the junction temperature (T_J) internally. If T_J exceeds the threshold value (typically 160°C), then the converter turns off and discharges the TRK/REF capacitors. Once T_J drops to about 130°C, a SS is initiated to restart the part and resume normal operation. Thermal shutdown is a non-latch protection. The hysteresis is about 30°C.

Power Good (PG)

For all four channels, the MPM81204 has a corresponding power good (PG) output (PG0, PG1, PG2, PG3). PGx is the open-drain of a MOSFET. Use a 10kΩ pull-up resistor to connect PGx to VCCx or an external voltage source below 3.6V. After applying V_{IN}, the MOSFET turns on and PGx is pulled to GND before TRK/REFx is ready. Once V_{FB} reaches 92.5% of V_{REF}, PGx is pulled high after a 0.9ms delay.

If V_{FB} drops below 80% of V_{REF} or exceeds 116% of V_{REF}, PGx is pulled low. PGx can only be pulled high again once another SS has been initiated.

If the input supply fails to power the device, then PGx is clamped low (even though it is tied to an external DC source via a pull-up resistor).

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Figure 4 shows the relationship between the PGx voltage (V_{PG}) and the PGx pull-up current (I_{PG}).

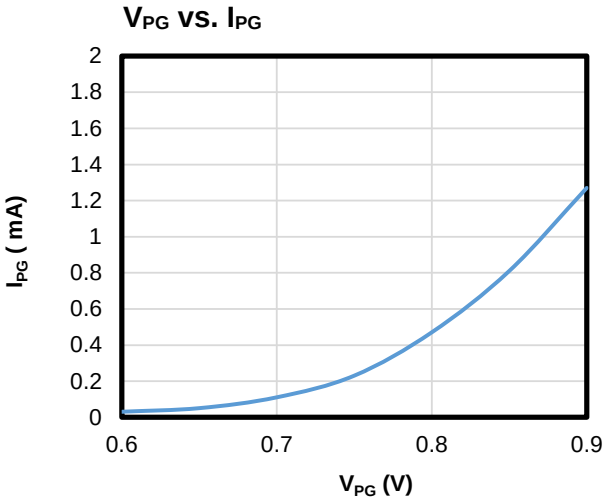

Figure 4: Clamped V_{PG} vs. Pull-Up Current

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APPLICATION INFORMATION

Setting the Output Voltage and Remote Output Voltage Sensing

For all four channels, R1 is integrated internally. Connect R2 between FBx and VOSNSx-. Connect VOSNSx- to the negative side of the voltage-sense point for the remote sense (see Figure 5).

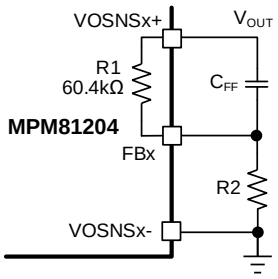

Figure 5: Feedback (FB) Network

R2 can be calculated with Equation (4):

$$R2(k\Omega) = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1(k\Omega) \quad (4)$$

A feed-forward capacitor (C_{FF}) is required in parallel with R1 to stabilize the system and optimize load transient response. Table 2 lists feedback resistor (R2) values and C_{FF} for common output voltages.

Table 2: Common Output Voltages

V_{OUT} (V)	R2 (kΩ)	C_{FF} (pF)
1	90.9	100
1.2	60.4	100
1.5	40.2	100
1.8	30.1	100
2.5	19.1	100
3.3	13.7	100
5.0	8.2	100

R1 and C_{FF} add an extra zero to the system, which improves loop response. Choose R1 and C_{FF} so that the zero formed by them is between 20kHz and 60kHz. The zero's frequency (f_{ZERO}) can be calculated with Equation (5):

$$f_{ZERO} = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (5)$$

Selecting the Input Capacitor

The buck converter has a discontinuous input current, and requires a capacitor to supply the AC current to the module while maintaining the DC V_{IN}. For the best performance, use ceramic capacitors. Place the input capacitors as close to the VINx pin as possible.

The capacitance can vary significantly with the temperature. X5R and X7R ceramic dielectric capacitors are recommended due to their stability across a wide temperature range.

The capacitors should have a ripple current rating that exceeds the converter's maximum input ripple current. The input ripple current (I_{CIN}) can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current.

The input capacitance (C_{IN}) determines the converter's V_{IN} ripple. Choose a capacitor that meets the application's relevant input voltage ripple requirements. The input voltage ripple (ΔV_{IN}) can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where C_{IN} is the input capacitor.

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

The output capacitor maintains the DC V_{OUT}. The V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

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When using ceramic capacitors, the capacitance dominates the impedance at f_{SW}. The V_{OUT} ripple is determined by the output capacitance. For simplification, the V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

When using large-ESR capacitors (e.g. POSCAP, OSCON, etc.), the ESR dominates the impedance at f_{SW}. The V_{OUT} ripple is determined by the ESR.

For simplification, the V_{OUT} ripple (ΔV_{OUT}) can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. To minimize high-frequency noise, place the ceramic input capacitors as close as possible to the VIN, VOUT, and GND pins.
2. Use wide copper planes for VIN, VOUT, and GND to minimize the parasitic impedance, PCB conduction loss, and thermal stress.
3. To minimize parasitic impedance and thermal stress, place multiple vias close to GND. Do not put vias directly on the pad, unless they are capped or plated over.
4. For remote sense, route VOSNS+ and VOSNS- as differential signals.
5. Route the VOSNS+ and VOSNS- traces away from the input plane and high-speed signals.

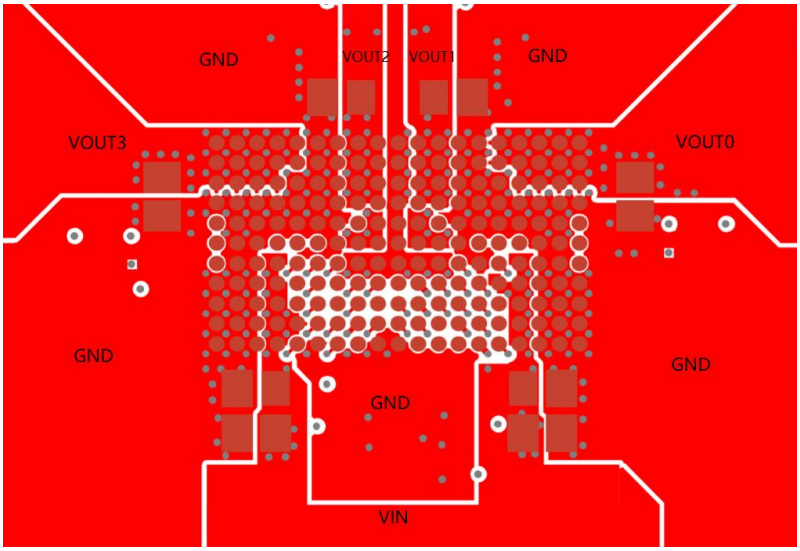

Figure 6: Recommended PCB Layout (Top Layer)

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TYPICAL APPLICATION CIRCUIT

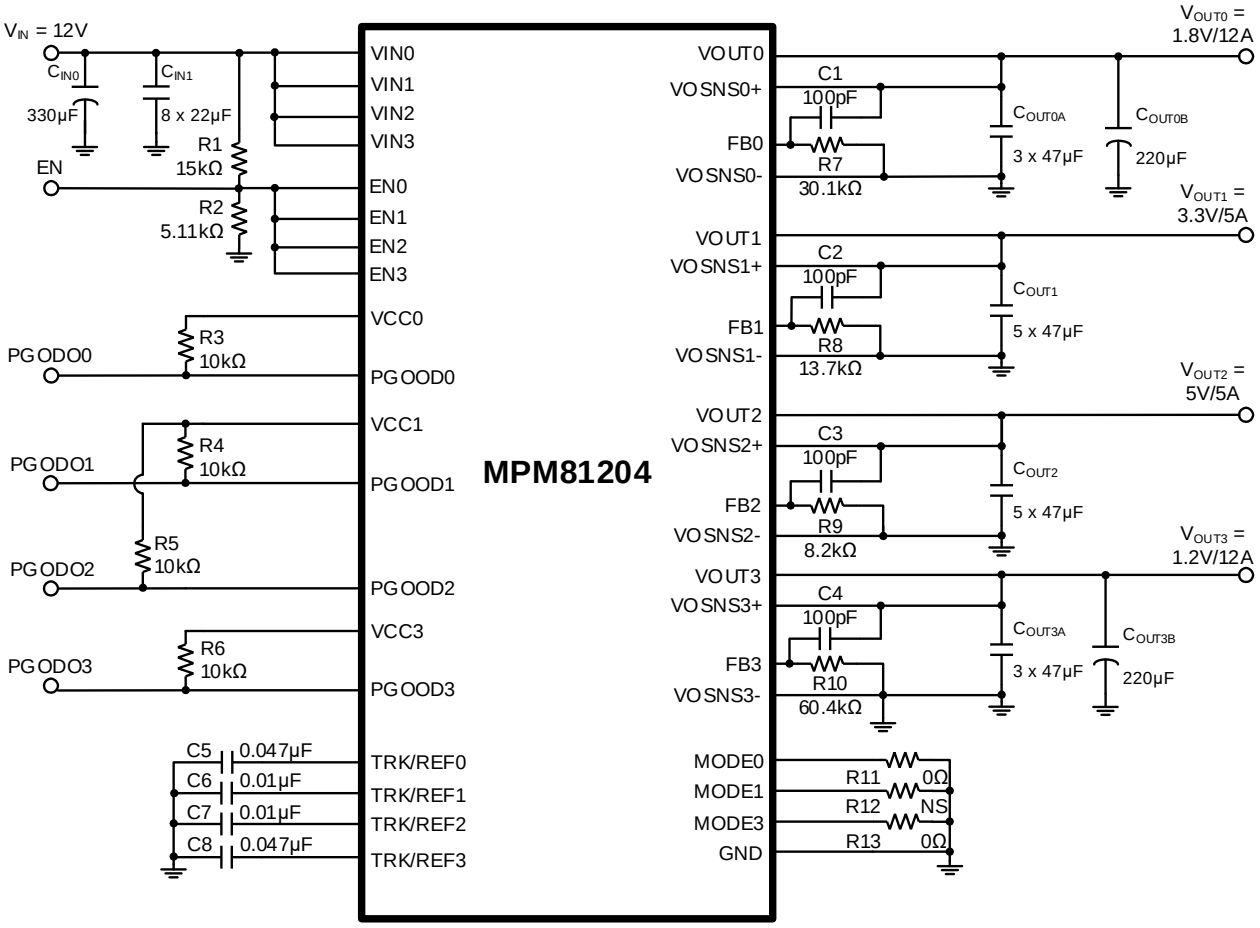

Figure 7: Typical Application Circuit

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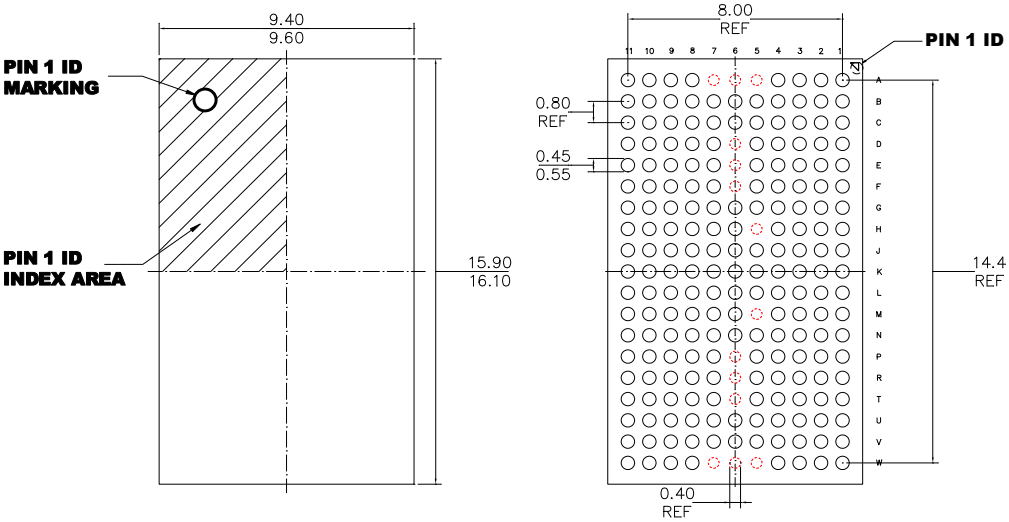
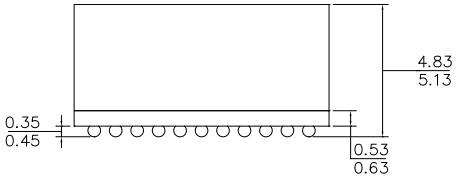
PACKAGE INFORMATION

BGA (9.5mmx16mmx4.98mm)

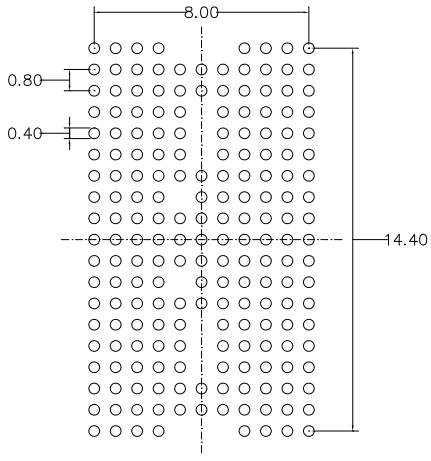


TOP VIEW

BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) THE RED DASHED CIRCLES REPRESENT THE EXPOSED PAD (NO SOLDER BALL).
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-275A.
5) DRAWING IS NOT TO SCALE.

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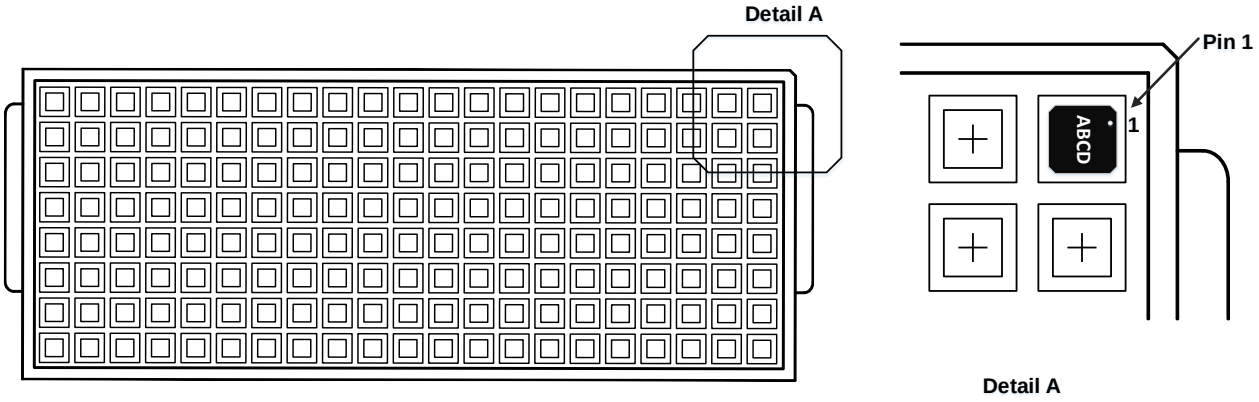
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM81204GBC-T	BGA (9.5mmx16mmx 4.98mm)	N/A	N/A	112	N/A	N/A	N/A

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/29/2021	Initial Release	-

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