R41Z-TA

Stand-alone Bluetooth 4.2 low energy and IEEE 802.15.4 module

Data sheet

Abstract

This technical data sheet describes the R41Z stand-alone Bluetooth® low energy and IEEE 802.15.4 module. The OEMs can embed their own application on top of the integrated Bluetooth low energy stack using the NXP MCUXpresso SDK and integrated development environment (IDE).

Document information

Title	**R41Z-TA**
Subtitle	Stand-alone Bluetooth 4.2 low energy and IEEE 802.15.4 module
Document type	Data sheet
Document number	UBX-19033355
Revision and date	R10 15-Nov-2024
Disclosure restriction	C1-Public

Product status	Corresponding content status	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	IN / PCN reference	Product status
R41Z	R41Z-TA-R-00	UBX-20017684	Obsolete
R41Z	R41Z-TA-R-10	N/A	Mass production

Contents

1 Functional description

The R41Z module from u-blox is a highly integrated, ultra-low power module that enables Bluetooth low energy and IEEE 802.15.4 connectivity based on the Kinetis KW41Z SoC from NXP Semiconductors. With an ARM® Cortex™ M0+ processor, embedded 2.4 GHz transceiver supporting FSK/GFSK and O-QPSK modulations, and integrated antenna, the R41Z provides a complete RF solution with no additional RF design allowing faster time to market. Equipped with the ability to concurrently communicate over Bluetooth, Thread, and Zigbee connections, the R41Z offers an unprecedented level of connectivity in a single module. With an internal DC-DC Converter and a wide supply voltage range of 0.9 V to 4.2 V, the R41Z can be directly powered by sources ranging from a single alkaline cell to lithium polymer batteries.

1.1 Features

- Based on the NXP Kinetis KW41Z SoC
- Complete RF solution with an integrated DC-DC converter
- Bluetooth 4.2 1M PHY
- IEEE 802.15.4 with Thread and Zigbee support
- ARM® Cortex™-M0+ 32-bit processor
- Serial Wire Debug (SWD)
- Over-the-Air (OTA) firmware updates
- 512 KB embedded flash memory
- 128 KB RAM
- 25 GPIO, 2 dedicated analog pins
- 16-bit / 500KSPS ADC
- 12-bit DAC
- – 40 °C to +85 °C temperature range
- 16 capacitive touch sensing Inputs
- Two SPI master/slave (12 Mbps)
- Two I2C master/slave
- UART (w/ CTS/RTS and DMA)
- Low power comparator
- Temperature sensor
- Infrared communication interface
- Nine low power modes
- True random number generator
- 128-bit AES HW encryption
- 32-bit Real-Time Clock (RTC)
- Wi-Fi coexistence support
- Dimensions: 10.6 x 16.2 x 2.0 mm

1.2 Applications

- Beacons – iBeacon™, Eddystone, AltBeacon, and so on.
- Low-power sensors
- Fitness devices
- Wearables
- Climate control
- Lighting
- Safety and security
- Home appliances
- Access control

- Internet of Things
- Home health care
- Advanced remote controls
- Smart energy management
- Low-power sensor Networks
- Interactive entertainment
- Key fobs
- Environmental monitoring
- Hotel automation
- Office automation

1.3 Block diagram

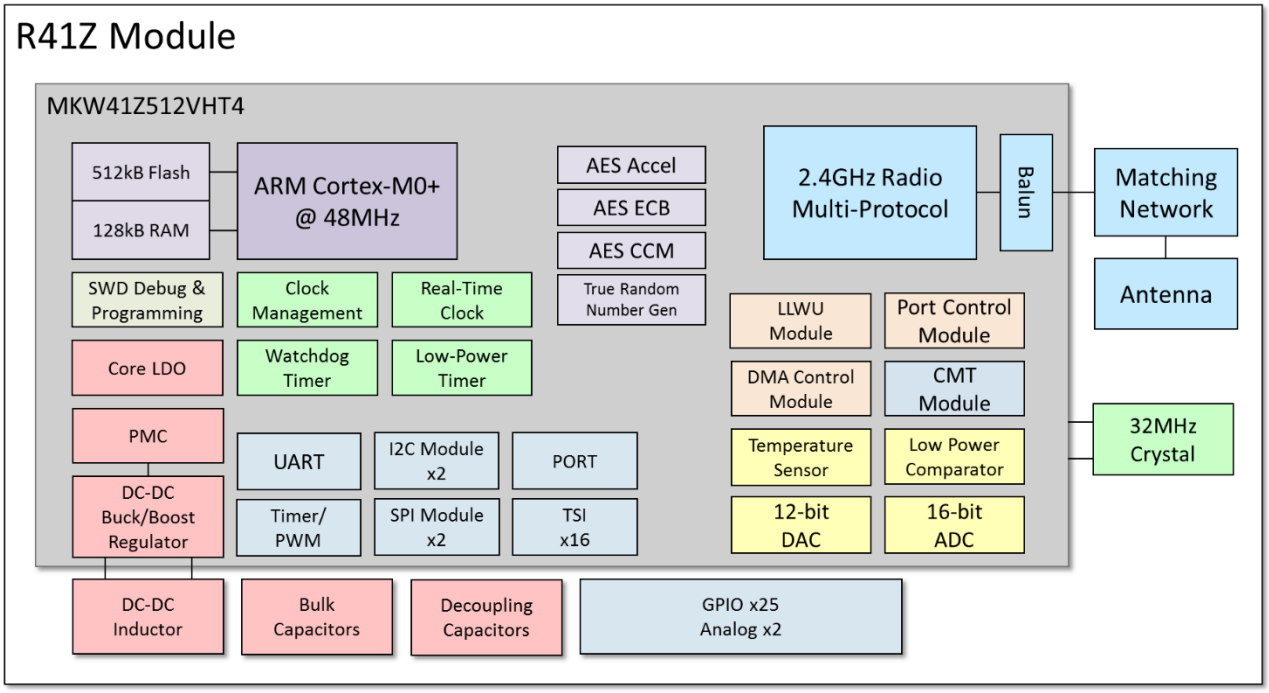


Figure 1: Block diagram of R41Z

1.4 Product specifications

Detail	Description
Bluetooth	
Bluetooth version	Bluetooth 4.2
Security	AES-128
LE connections	2
Thread / Zigbee	
Version	Thread 1.1, Zigbee 3.0
Stack	NXP KW41Z Thread stack, NXP KW41Z Zigbee stack
Security	AES-128
Radio	
Frequency	2.360 GHz to 2.483 GHz
Modulations	GFSK at 1 Mbps, OQPSK @ 250 Kbps
Transmit power	+3.5 dBm
Receiver sensitivity	– 95 dBm (Bluetooth low energy), – 100 dBm (IEEE 802.15.4)
Antenna	Integrated (-1 dBi peak)

Detail	Description
Current consumption	
TX only @ 0 dBm, bypass mode	14.7 mA
TX only @ 0 dBm, DCDC enabled, 3.6 V Vin	6.1 mA
RX only bypass mode	16.2 mA
RX only, DCDC enabled, 3.6 Vin	6.7 mA
Normal Run CPU @ 48 MHz @ 3.0 V, DCDC enabled	4.8 mA
Very-Low-Power Run CPU @ 4 MHz @ 3.0 V, DCDC enabled	137 µA
Very-Low-Leakage Stop 3 (RAM retained) @ 3.0 V @ 25 °C, DCDC enabled	1.8 µA
Very-Low-Leakage Stop 0 @ 3.0 V @25 °C, bypass mode	182 nA
Dimensions	
R41Z	Length: 16.2 mm ± 0.3 mm
	Width: 10.6 mm ± 0.3 mm
	Height: 2.0 mm ± 0.1 mm
Hardware	
Interfaces	SPI Master/Slave x 2 UART x 1 Touch Sense Interface x 16 Two-Wire Master/Slave (I2C) x2 GPIO x 25 Analog input x 6
Power supply	Boost mode: 0.9 V to 1.8 V, 1.1 V required to startup Bypass mode: 1.71 V to 3.6 V Buck mode: 1.8 V to 4.2 V, 2.1 V required to startup
Temperature range	-40 °C to +85 °C
Certifications	
USA (FCC)	FCC part 15 modular certification FCC ID: 2AA9B07
Canada (ISED)	Industry Canada RSS-210 modular certification IC: 12208A-07
Europe (CE)	EN 62368-1:2014+A11:2017: Health and Safety of the User EN 301 489-1 V2.1.1 & 3.1 (b): Electromagnetic Compatibility EN 301 489-17 V3.1.1 EN 300 328 V2.1.1 3.2: Effective use of spectrum allocated
Japan (MIC)	Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan MIC: 210-109448
Australia / New Zealand (RCM) Bluetooth	AS/NZS 4268:2017, Radio equipment and systems – Short range devices RF-PHY Component (Tested) – DID: D035037; QDID: 95459
Radio chip	
NXP KW41Z	Additional details: MKW41Z Data Sheet Software & Tools

2 Pin definition

2.1 Pin assignment

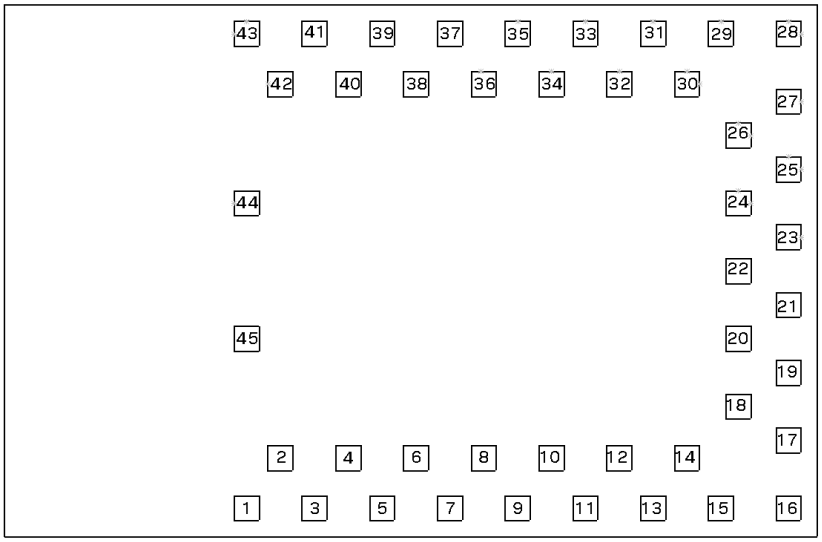


Figure 2: R41Z pin assignment

Pin	Name	Direction	Description	Default State at POR	KW41Z pin	Remarks
2	PTC1	I/O	GPIO	Disabled	PTC1	
3	PTC2	I/O	GPIO	Disabled	PTC2	
4	PTC3	I/O	GPIO	Disabled	PTC3	
5	PTC4	I/O	GPIO	Disabled	PTC4	
6	PTC5	I/O	GPIO	Disabled	PTC5	
7	PTC6	I/O	GPIO	Disabled	PTC6	
8	PTC7	I/O	GPIO	Disabled	PTC7	
10	PTC16	I/O	GPIO	Disabled	PTC16	
11	PTC17	I/O	GPIO	Disabled	PTC17	
12	PTC18	I/O	GPIO	Disabled	PTC18	
13	PTC19	I/O	GPIO	Disabled	PTC19	
14	PTA0	I/O	GPIO	SWDIO, Pullup EN	PTA0	
15	PTA1	I/O	GPIO	SWCLK, Pulldown EN	PTA1	
17	PTA2	I/O	GPIO	Reset, Pullup EN	PTA2	
18	PTA16	I/O	GPIO	Disabled	PTA16	
19	PTA17	I/O	GPIO	Disabled	PTA17	
20	PTA18	I/O	GPIO	Disabled	PTA18	
21	PTA19	I/O	GPIO	Disabled	PTA19	
30	PTB0	I/O	GPIO	XTAL_OUT_EN	PTB0	See e10224 in NXP KW41Z errata
31	PTB1	I/O	GPIO	Disabled	PTB1	
32	PTB2	I/O	GPIO	Disabled	PTB2	
33	PTB3	I/O	GPIO	Disabled	PTB3	
34	PTB16	I/O	GPIO	EXTAL32K	PTB16	
36	PTB17	I/O	GPIO	XTAL32K	PTB17	

Pin	Name	Direction	Description	Default State at POR	KW41Z pin	Remarks
37	PTB18	I/O	GPIO	Non-maskable Interrupt req	PTB18	
38	ADC0_P	In	ADC/Comparator input	N/A	ADC0_P	
39	ADC0_N	In	ADC/Comparator input	N/A	ADC0_N	

Table 1: R41Z GPIO / Analog pin-out

2.1.1 Reference

Pin	Name	Direction	Description	Remarks
40	XTAL_OUT	Out	32 MHz Clock output	
41	VREF	I/O	Analog reference voltage. Internally or externally sourced	
42	VDDA	Power	Analog supply. Internally sourced	VDDA is connected to V1P8 through a power filtering circuit on the module

Table 2: Pin descriptions – Reference

2.1.2 Power

Pin	Name	Direction	Description	Remarks
1	GND	Power	Electrical Ground	
9	GND	Power	Electrical Ground	
16	GND	Power	Electrical Ground	
22	PSWITCH	Input	DCDC start signal	For information about signal usage and DCDC modes, see DCDC converter operation
23	DCDC_CFG	Input	DCDC mode	
24	GND	Power	Electrical Ground	
25	VCC	Power	DCDC input	
26	DCDC_LP	Power	DCDC signal	
27	V1P8	Power	DCDC IO and peripheral voltage	
28	GND	Power	Electrical Ground	
29	V1P5	Power	DCDC RF supply	For information about signal usage and DCDC modes, see DCDC converter operation
35	GND	Power	Electrical Ground	
43	GND	Power	Electrical Ground	
44	GND	Power	Electrical Ground	
45	GND	Power	Electrical Ground	

Table 3: Power

Internal peripherals on the R41Z (such as UART and I2C) can be routed to multiple pin options using multiplexing. However, each pin can only be used with certain peripherals. See the following sections for details on which pins can be used for a given function.

Signal options for a pin are selected using a pin mux value. On many pins, there are multiple signals that are accessed with the same pin mux value. See the NXP KW41Z Reference Manual for details on configuring these functions.

2.2 GPIO and LLWU signals

To use a Pin as GPIO or as a Low Leakage Wake-Up source, use pin mux ALT1. The LLWU pins can be used to trigger interrupts that can bring the module out of Low Leakage sleep modes.

Signal	Direction	Description	Pin	Port	Mux Alt	Remarks
PTC1	I/O	GPIO	2	PTC1	ALT1	
PTC2 / LLWU_P10	I/O	GPIO, LLWU	3	PTC2	ALT1	
PTC3 / LLWU_P11	I/O	GPIO, LLWU	4	PTC3	ALT1	
PTC4 / LLWU_P12	I/O	GPIO, LLWU	5	PTC4	ALT1	
PTC5 / LLWU_P13	I/O	GPIO, LLWU	6	PTC5	ALT1	
PTC6 / LLWU_P14	I/O	GPIO, LLWU	7	PTC6	ALT1	
PTC7 / LLWU_P15	I/O	GPIO, LLWU	8	PTC7	ALT1	
PTC16 / LLWU_P0	I/O	GPIO, LLWU	10	PTC16	ALT1	
PTC17 / LLWU_P1	I/O	GPIO, LLWU	11	PTC17	ALT1	
PTC18 / LLWU_P2	I/O	GPIO, LLWU	12	PTC18	ALT1	
PTC19 / LLWU_P3	I/O	GPIO, LLWU	13	PTC19	ALT1	
PTA0	I/O	GPIO	14	PTA0	ALT1	
PTA1	I/O	GPIO	15	PTA1	ALT1	
PTA2	I/O	GPIO	17	PTA2	ALT1	
PTA16 / LLWU_P4	I/O	GPIO, LLWU	18	PTA16	ALT1	
PTA17 / LLWU_P5	I/O	GPIO, LLWU	19	PTA17	ALT1	
PTA18 / LLWU_P6	I/O	GPIO, LLWU	20	PTA18	ALT1	
PTA19 / LLWU_P7	I/O	GPIO, LLWU	21	PTA19	ALT1	
PTB0 / LLWU_P8	I/O	GPIO, LLWU	30	PTB0	ALT1	See e10224 in NXP KW41Z errata
PTB1	I/O	GPIO	31	PTB1	ALT1	
PTB2	I/O	GPIO	32	PTB2	ALT1	
PTB3	I/O	GPIO	33	PTB3	ALT1	
PTB16	I/O	GPIO	34	PTB16	ALT1	
PTB17	I/O	GPIO	36	PTB17	ALT1	
PTB18	I/O	GPIO	37	PTB18	ALT1	

Table 4: GPIO and LLWU signal map

2.3 UART signals

Signal	Direction	Description	Pin	Port	Mux Alt
LPUART0_RX	In	UART Data Receiver	3	PTC2	ALT4
			7	PTC6	ALT4
			11	PTC17	ALT4
LPUART0_TX	Out	UART Data Transmit	4	PTC3	ALT4
			8	PTC7	ALT4
			12	PTC18	ALT4
LPUART0_CTS_b	In	UART Clear to Send	5	PTC4	ALT4
			13	PTC19	ALT4
LPUART0_RTS_b	Out	UART Request to Send	2	PTC1	ALT4
			6	PTC5	ALT4
			10	PTC16	ALT4

Table 5: UART signal map

2.4 SPI signals

Signal	Direction	Description	Pin	Port	Mux Alt
SPI0_SCK	I/O	SPI0 Clock	10	PTC16	ALT2
SPI0_SOUT	Out	SPI0 Serial Out	11	PTC17	ALT2
SPI0_SIN	In	SPI0 Serial In	12	PTC18	ALT2
SPI0_PCS0	I/O	SPI0 Chip Select / Slave Select 0	13	PTC19	ALT2
SPI0_PCS1	I/O	SPI0 Chip Select / Slave Select 1	14	PTA0	ALT2
SPI0_PCS2	I/O	SPI0 Chip Select / Slave Select 2	8	PTC7	ALT2
SPI1_SCK	I/O	SPI1 Clock	20	PTA18	ALT2
SPI1_SOUT	Out	SPI1 Serial Out	18	PTA16	ALT2
SPI1_SIN	In	SPI1 Serial In	19	PTA17	ALT2
SPI1_PCS0	I/O	SPI1 Chip Select / Slave Select 0	15	PTA1	ALT2
			21	PTA19	ALT2

Table 6: SPI signal map

2.5 I2C signals

Signal	Direction	Description	Pin	Port	Mux Alt
I2C0_SDA	I/O	I2C0 Serial Data Line	2	PTC1	ALT3
			10	PTC16	ALT3
			31	PTB1	ALT3
I2C0_SCL	I/O	I2C0 Serial Clock Line	13	PTC19	ALT3
			30	PTB0	ALT3
I2C1_SDA	I/O	I2C1 Serial Data Line	4	PTC3	ALT3
			8	PTC7	ALT3
			12	PTC18	ALT3
			36	PTB17	ALT3
I2C1_SCL	I/O	I2C1 Serial Clock Line	3	PTC2	ALT3
			7	PTC6	ALT3
			11	PTC17	ALT3
			34	PTB16	ALT3
			37	PTB18	ALT3

Table 7: I2C signal map

2.6 Touch sensing input (TSI) signals

TSI signals are the inputs used by the R41Z's capacitive touch sensing system. See NXP Application Note AN3863 for electrical and PCB layout recommendations.

Signal	Direction	Description	Pin	Port	Mux Alt
TSI0_CH0	In	TSI0 channel 0	5	PTC4	ALT0
TSI0_CH1	In	TSI0 channel 1	6	PTC5	ALT0
TSI0_CH2	In	TSI0 channel 2	7	PTC6	ALT0
TSI0_CH3	In	TSI0 channel 3	8	PTC7	ALT0
TSI0_CH4	In	TSI0 channel 4	10	PTC16	ALT0
TSI0_CH5	In	TSI0 channel 5	11	PTC17	ALT0
TSI0_CH6	In	TSI0 channel 6	12	PTC18	ALT0
TSI0_CH7	In	TSI0 channel 7	13	PTC19	ALT0
TSI0_CH8	In	TSI0 channel 8	14	PTA0	ALT0
TSI0_CH9	In	TSI0 channel 9	15	PTA1	ALT0
TSI0_CH10	In	TSI0 channel 10	18	PTA16	ALT0
TSI0_CH11	In	TSI0 channel 11	19	PTA17	ALT0
TSI0_CH12	In	TSI0 channel 12	20	PTA18	ALT0
TSI0_CH13	In	TSI0 channel 13	21	PTA19	ALT0
TSI0_CH14	In	TSI0 channel 14	3	PTC2	ALT0
TSI0_CH15	In	TSI0 channel 15	4	PTC3	ALT0

Table 8: TSI signal map

2.7 Timer/PWM module (TPM) signals

Signal	Direction	Description	Pin	Port	Mux Alt
TPM0_CH0	I/O	TPM0 channel 0	18	PTA16	ALT5
			37	PTB18	ALT5
TPM0_CH1	I/O	TPM0 channel 1	4	PTC3	ALT5
			30	PTB0	ALT5
TPM0_CH2	I/O	TPM0 channel 2	2	PTC1	ALT5
			31	PTB1	ALT5
TPM0_CH3	I/O	TPM0 channel 3	10	PTC16	ALT5
			17	PTA2	ALT5
TPM1_CH0	I/O	TPM1 channel 0	5	PTC4	ALT5
			14	PTA0	ALT5
			32	PTB2	ALT5
TPM1_CH1	I/O	TPM1 channel 1	6	PTC5	ALT5
			15	PTA1	ALT5
			33	PTB3	ALT5
TPM2_CH0	I/O	TPM2 channel 0	7	PTC6	ALT5
			20	PTA18	ALT5
			34	PTB16	ALT5
TPM2_CH1	I/O	TPM2 channel 1	8	PTC7	ALT5
			21	PTA19	ALT5
			36	PTB17	ALT5
TPM_CLKIN1	In	TPM external clock signal	19	PTA17	ALT5
EXTRG_IN	In	TPM/ADC External Trigger signal	5	PTC4	ALT3

Table 9: TPM signal map

2.8 Radio signals

2.8.1 Wi-Fi/Bluetooth low energy coexistence signals

Signal	Direction	Description	Pin	Port	Mux Alt
BLE_RF_ACTIVE	Out	External radio disable signal	2	PTC1	ALT7
			13	PTC19	ALT7
RF_NOT_ALLOWED	In	R41Z radio disable signal	6	PTC5	ALT2
			32	PTB2	ALT2

Table 10: Wi-Fi/Bluetooth LE Coexistence signal map

2.8.2 Direct test mode (DTM) signals

Signal	Direction	Description	Pin	Port	Mux Alt
DTM_RX	In	Direct Test Mode receive signal	3	PTC2	ALT7
			11	PTC17	ALT7
			31	PTB1	ALT2
DTM_TX	Out	Direct Test Mode transmit signal	4	PTC3	ALT7
			12	PTC18	ALT7
			32	PTB2	ALT3
RF_RESET	In	Radio reset signal	19	PTA17	ALT1

Table 11: DTM signals

2.8.3 IEEE 802.15.4 Bit streaming mode (BSM) signals

Signal	Direction	Description	Pin	Port	Mux Alt
BSM_DATA	I/O	Bit Streaming Mode Data signal	5	PTC4	ALT7
			8	PTC7	ALT7
			12	PTC18	ALT5
BSM_CLK	Out	Bit Streaming Mode clock signal	6	PTC5	ALT7
			13	PTC19	ALT5
			36	PTB17	ALT7
BSM_FRAME	Out	Bit Streaming Mode Frame signal	7	PTC6	ALT7
			11	PTC17	ALT5

Table 12: BSM signal map

2.9 Carrier modulator timer (CMT) signal

Signal	Direction	Description	Pin	Port	Mux Alt
CMT_IRO	Out	Carrier Modulator Timer out signal	3	PTC2	ALT5
			30	PTB0	ALT7

Table 13: CMT signal map

2.10 Single wire debug (SWD) and reset signals

Signal	Direction	Description	Pin	Port	Mux Alt
SWD_DIO	I/O	SWD data signal	14	PTA0	ALT7
SWD_CLK	In	SWD clock signal	15	PTA1	ALT7
RESET_b	I/O	System reset signal, bidirectional	17	PTA2	ALT7

Table 14: SWD and reset signals

2.11 RTC and clock signals

Signal	Direction	Description	Pin	Port	Mux Alt	Remarks
XTAL_OUT_EN	In	EN input for XTAL_OUT (Pin 40)	7 30	PTC6 PTB01	ALT1 ALT1	See e10224 in NXP KW41Z errata
CLKOUT	Out	Internal clocks monitor	30 33	PTB0 PTB3	ALT7 ALT4	
RTC_CLKOUT	Out	RTC 1 Hz clock signal	33	PTB3	ALT7	
EXTAL32K	In	32 kHz external clock/oscillator	34	PTB16	ALT0	
XTAL32K	In	32 kHz external clock	36	PTB17	ALT0	

Table 15: RTC and clock signal map

2.12 Analog signals

Signal	Direction	Description	Pin	Port	Mux Alt
CMP0_OUT	Out	Comparator 0 output	30	PTB0	ALT4
CMP0_IN0	In	Comparator 0 Single-ended input 0	38	-	-
CMP0_IN1	In	Comparator 0 Single-ended input 1	39	-	-
CMP0_IN2	In	Comparator 0 Single-ended input 2	37	PTB18	ALT0
CMP0_IN3	In	Comparator 0 Single-ended input 3	32	PTB2	ALT0
CMP0_IN4	In	Comparator 0 Single-ended input 4	33	PTB3	ALT0
CMP0_IN5	In	Comparator 0 Single-ended input 5	31	PTB1	ALT0
ADC0_SE0	In	ADC Channel 0 Single-ended input 0	31	PTB1	ALT0
ADC0_SE1	In	ADC Channel 0 Single-ended input 1	33	PTB3	ALT0
ADC0_SE2	In	ADC Channel 0 Single-ended input 2	32	PTB2	ALT0
ADC0_SE3	In	ADC Channel 0 Single-ended input 3	37	PTB18	ALT0
ADC0_SE4	In	ADC Channel 0 Single-ended input 4	21	PTA19	ALT0
ADC0_DP0	In	ADC Channel 0 Differential input positive	38	-	-
ADC0_DN0	In	ADC Channel 0 Differential input negative	39	-	-
DAC0_OUT	Out	DAC Channel 0 Single-ended output	37	PTB18	ALT0

Table 16: Analog signals

3 Electrical specifications

⚠ Stressing the device above one or more of the ratings listed in the Absolute maximum ratings can cause permanent damage. These are stress ratings only. Operating the module at these or at any conditions other Operating conditions should be avoided. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

☞ All given application information is only advisory and does not form part of the specification.

3.1 Absolute maximum ratings

Symbol	Description	Condition	Min	Max	Unit
V_{CC_MAX}	Voltage on supply pin	DCDC Boost Mode	–0.3	1.8	V
		DCDC Bypass Mode	–0.3	3.6	V
		DCDC Buck Mode	–0.3	4.2	V
V_{1P8_MAX}	Voltage on V1P8 and GPIO pins	All DCDC modes	–0.3	3.6	V
V_{RF_MAX}	Voltage on V1P5	All DCDC modes	–0.3	3.6	V
T_S	Storage Temperature	-	–40	125	°C

Table 17: Absolute maximum ratings

⚠ The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in Table 17, must be limited to values within the specified boundaries by using appropriate protection devices.

3.2 Operating conditions

☞ Unless otherwise specified, all operating condition specifications are at an ambient temperature of 25 °C and a supply voltage of 3.0 V.

⚠ Operation beyond the specified operating conditions is not recommended and extended exposure beyond them may affect device reliability.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{cc}	Voltage on Supply Pin	DCDC Boost Mode	0.9[1]	1.5	1.8	V
		DCDC Bypass Mode	1.71	3.3	3.6	V
		DCDC Buck Mode	1.8[2]	3.3	4.2	V
V_{1P8}	Voltage on V1P8 and GPIO	All DCDC modes	1.45	3.3	3.6	V
V_{RF}	Voltage on V1P5	All DCDC modes	1.8	3.3	3.6	V
I_{1P8}	V1P8 output current	DCDC Buck Mode, 1.8 Vout	-	-	45	mA
		DCDC Buck Mode, 3.0 Vout	-	-	27	mA
		DCDC Boost Mode, 1.7 Vin, 1.8 Vout	-	-	45	mA
		DCDC Boost Mode, 0.9 Vin, 3.0Vout	-	-	10	mA
T_A	Ambient Temperature	-	–40	25	85	°C

Figure 3: Operating conditions

☞ 1: In Boost mode, a minimum of 1.1 V is required to start the DCDC converter. Once started, the converter can operate at 0.9 V.

☞ 2: In Buck mode, a minimum of 2.1 V is required to start the DCDC converter.

3.3 DCDC converter operation

The R41Z module contains an integrated DCDC converter which allows for three modes of operation without additional components. When operating in DCDC Buck mode, power consumption from using the radio can be reduced compared to DCDC Bypass mode. DCDC Boost mode allows the use of a single alkaline or other low voltage source. While it is possible to switch between these modes in a single design, for example the R41Z Evaluation Board, it is not recommended to switch between modes while power is applied.

3.3.1 DCDC bypass mode

Mode	Pin	Name	Net connection
Bypass	22	PSWITCH	Ground
	23	DCDC_CFG	1.71 V - 3.6 V Source IN
	25	VCC	1.71 V - 3.6 V Source IN
	26	DCDC_LP	No Connection
	27	V1P8	1.71 V - 3.6 V Source IN
	29	V1P5	1.45 V - 3.6 V Source IN

Table 18: Bypass mode pin connections

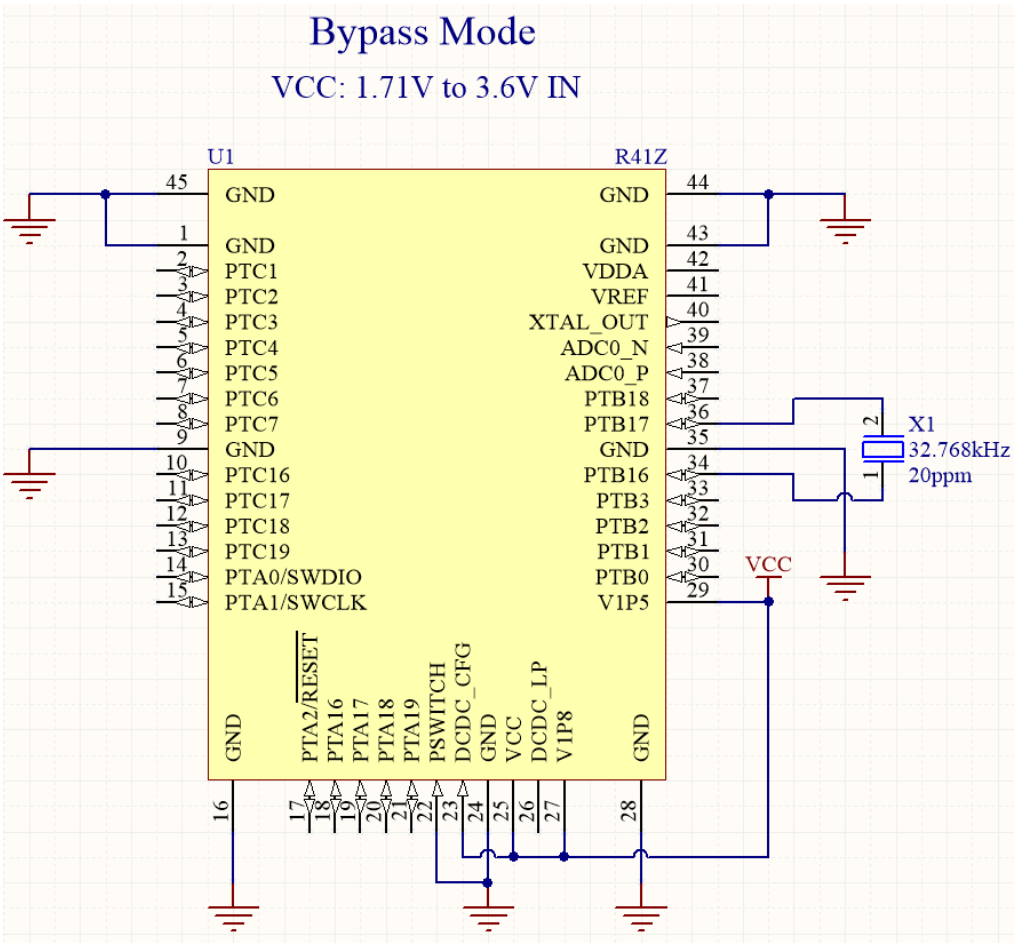


Figure 4: Schematic: DCDC bypass mode example

3.3.2 DCDC buck mode

Mode	Pin	Name	Net Connection
Buck	22	PSWITCH[1]	1.8 V - 4.2 V Source IN
	23	DCDC_CFG	1.8 V - 4.2 V Source IN
	25	VCC	1.8 V - 4.2 V Source IN
	26	DCDC_LP	No Connection
	27	V1P8	No Connection or 1.8 V – 3.0 V OUT[2]
	29	V1P5	No Connection

1: In Buck mode, PSWITCH can inhibit the DCDC converter from starting when the source voltage is applied. When PSWITCH is connected to the source voltage, the DCDC converter will start. Once started, PSWITCH can be reconnected to GND without disrupting the DCDC converter's operation.

2: V1P8 is the R41Z's IO voltage when the DCDC converter is running in either Buck or Boost mode. V1P8 can source a limited number of additional peripheral devices (sensors, LEDs, etc.) that connect directly to the R41Z's IO. In Buck mode, V1P8 cannot output a voltage greater than the source voltage.

Table 19: DCDC buck mode pin connections

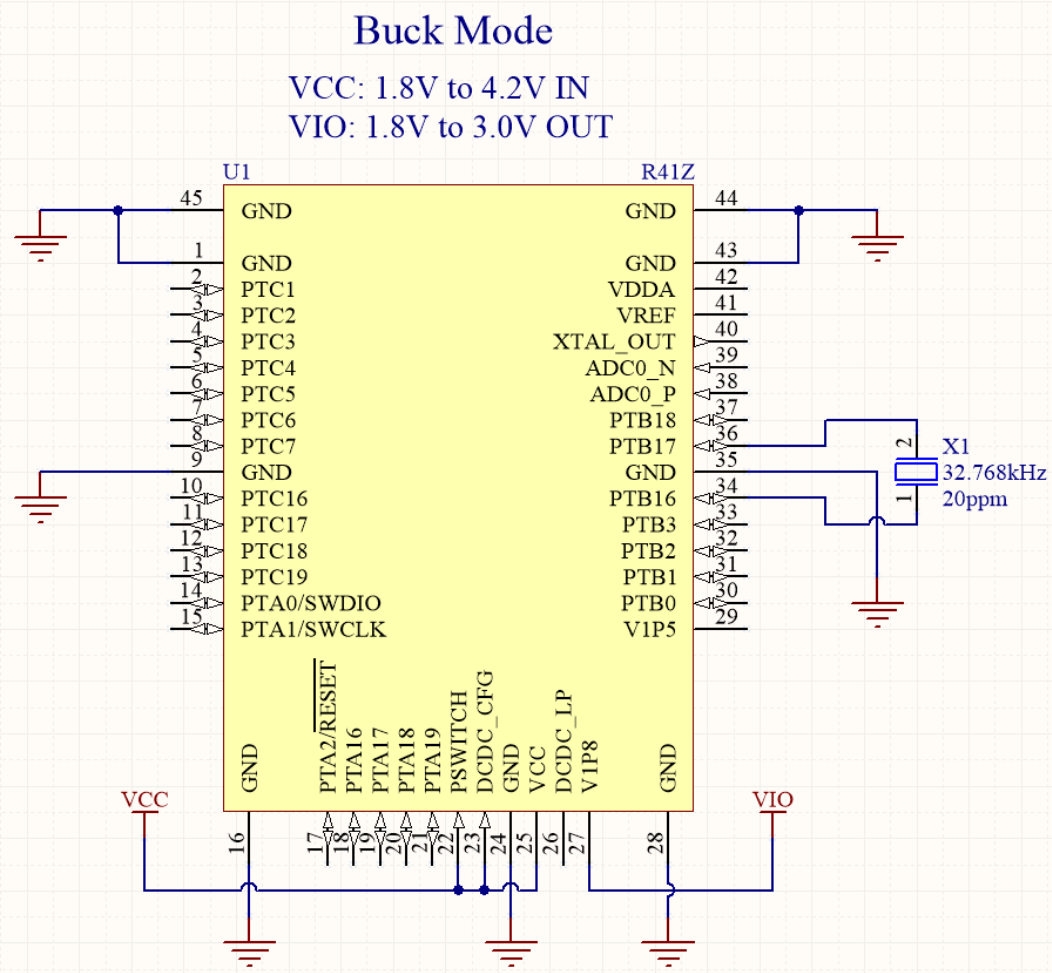


Figure 5: Schematic: DCDC buck mode example

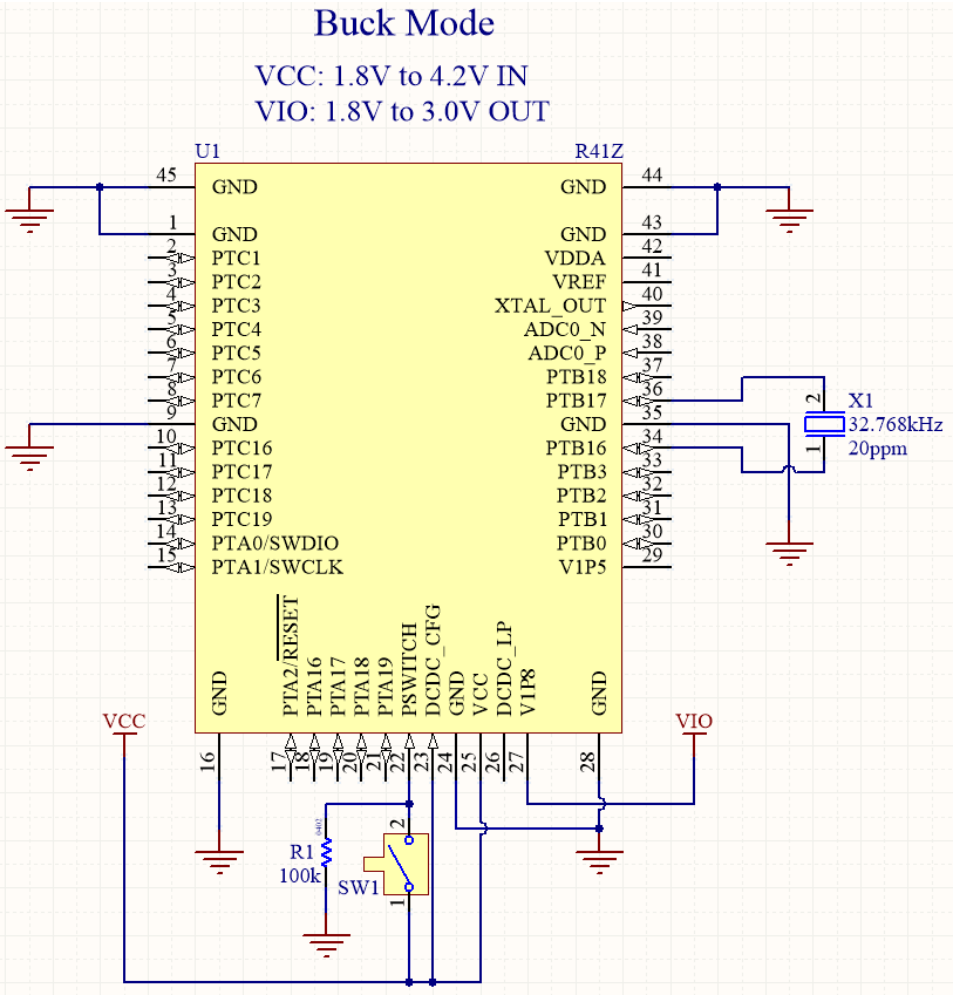


Figure 6: Schematic: DCDC buck mode PSWITCH example

3.3.3 DCDC boost mode

Mode	Pin	Name	Net Connection	Remarks
Boost	22	PSWITCH	0.9 V – 1.8 V Source IN	
	23	DCDC_CFG	Ground	
	25	VCC	0.9 V – 1.8 V Source IN	
	26	DCDC_LP	0.9 V – 1.8 V Source IN	
	27	V1P8	No Connection or 1.8 V – 3.0 V OUT	V1P8 is the R41Z's IO voltage when the DCDC converter is running in either Buck or Boost mode. V1P8 can source a limited number of additional peripheral devices (sensors, LEDs, and so on.) that connect directly to the R41Z's IO.
	29	V1P5	No Connection	

Table 20: DCDC boost mode pin connections

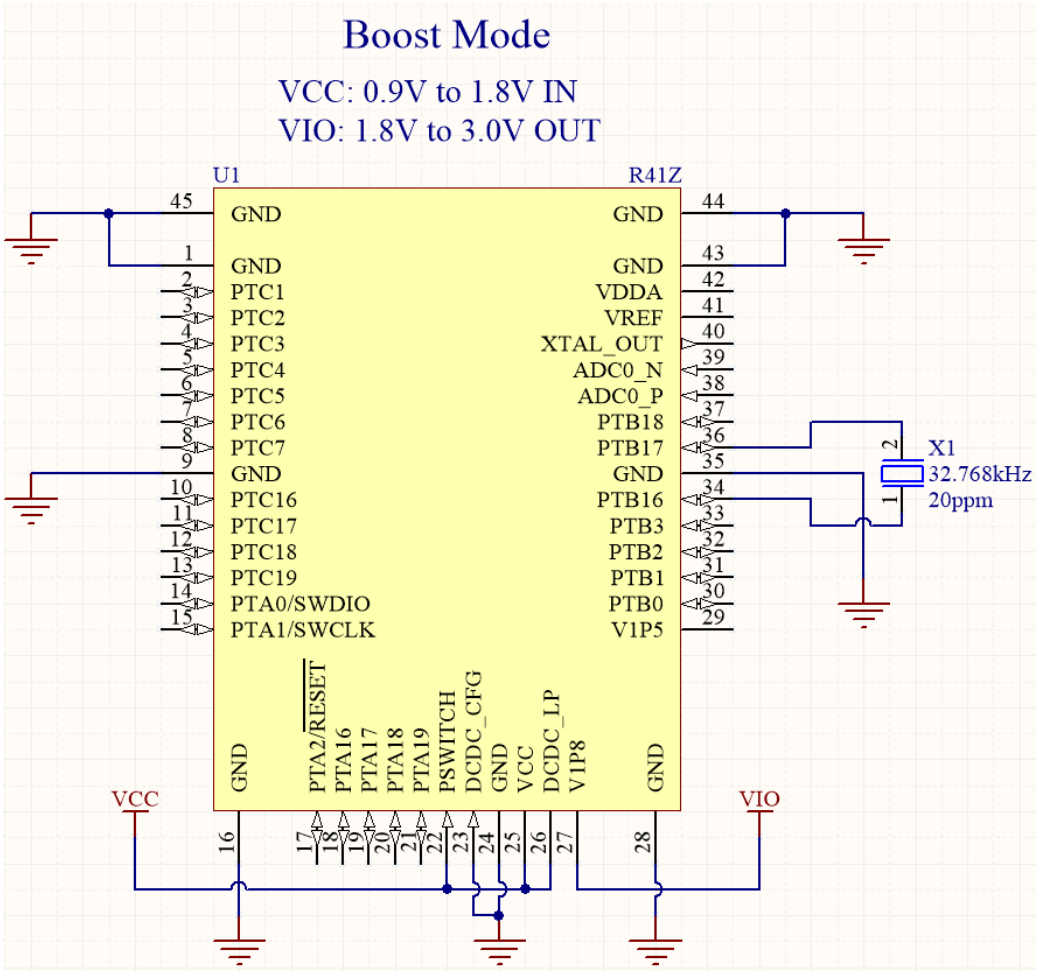


Figure 7: Schematic: DCDC boost mode example

When using Boost Mode care should be taken to ensure that DCDC_LP (Pin 26) is connected to **VCC** (Pin 25) with a trace wide enough to carry the full current expected to be drawn from the R41Z module and any peripherals sourced by the module. The connection should also be as short as possible.

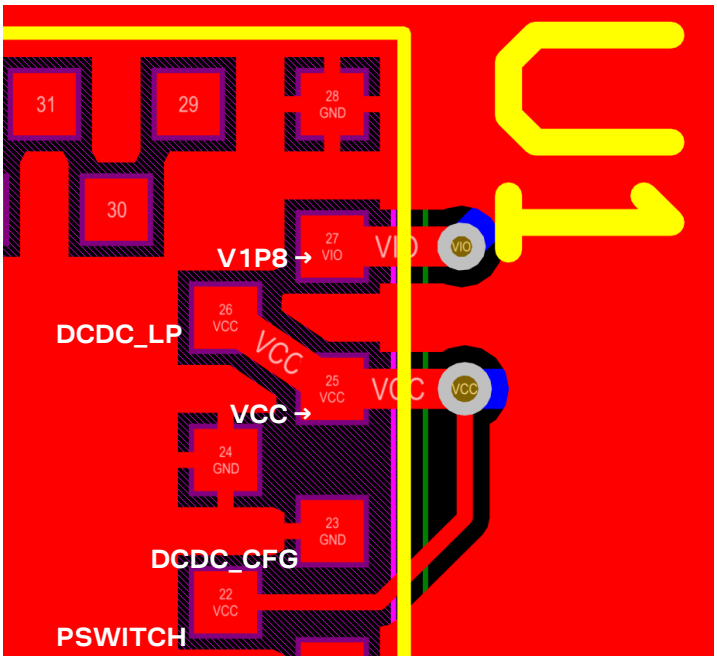


Figure 8: PCB: Boost mode suggested layout

3.4 General purpose I/O and ports

The general-purpose I/O is organized as three ports (A, B, and C) that enable access and control to each of the 25 available GPIO pins. Each GPIO can be configured individually through a Pin Control Register (PCR) and Port Data Direction Register (PDDR) with the following available features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Trigger interrupts and/or DMA from input
- Read and clear interrupt flags
- Enable passive input filter
- Fast/slow slew rate selection
- Control pin multiplexing to internal modules

To use a pin as GPIO set the Pin Mux Control field of the pin to ALT1 in the PCR. Ports must have their clock source enabled in the System Clock Gating Control Register 5 (SIM_SCGC5) before accessing any port registers. Attempting to access port registers without the port clock enabled will cause program execution to immediately vector to the default exception handler. Disabling the clock to ports that are not being used will reduce power consumption. Ports should be disabled before turning off the clock.

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage, 2.7 V ≤ V_{IO} ≤ 3.6 V Input High Voltage, 1.7 V ≤ V_{IO} ≤ 2.7 V	0.7 x V_{IO} 0.75 x V_{IO}	- -	V
V_{IL}	Input Low Voltage, 2.7 V ≤ V_{IO} ≤ 3.6 V Input Low Voltage, 1.7 V ≤ V_{IO} ≤ 2.7 V	- -	0.35 x V_{IO} 0.3 x V_{IO}	V
V_{HYS}	Input Hysteresis	-	0.6 x V_{IO}	V
V_{OH}	Output high voltage	V_{IO} – 0.5	-	V
V_{OL}	Output low voltage	-	0.5	V
R_P	Pull resistance	20	50	kΩ

Table 21: GPIO properties

3.5 Analog I/O and VREF

3.5.1 Analog signals

Symbol	Parameter	Min	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	V_{1P8}	-	V
V_{REF_OUT}	VREF internally sourced, factory trim	1.190	1.1950	1.200	V
V_{REFH}	VREF externally sourced	1.13	V_{DDA}	V_{DDA}	V
V_{ADIN}	16-bit, differential mode	GND	-	31/32 × V_{REFH}	V
	16-bit, All other modes	GND	-	V_{REFH}	V
V_{ACIN}	CMP/6-bit ADC analog input voltage	GND – 0.3	-	V_{1P8}	V
V_{ACIO}	CMP/6-bit ADC analog input voltage offset	-	-	20	mV
I_{CMPHS}	CMP current, High-speed mode	-	-	200	µA
I_{CMPLS}	CMP current, Low-speed mode	-	-	20	µA
V_{CMPH}	Comparator output high	V_{1P8} – 0.5	-	-	V
V_{CMPL}	Comparator output low	-	-	0.5	V

Table 22: Analog properties

3.5.2 VDDA and VREF

The source voltage for the analog sub-system, **VDDA**, is supplied by **V1P8** through a filtering circuit onboard the R41Z module. The voltage reference pin, **VREF**, has two sourcing options: internal or external. When externally supplied, **VREF** should be referenced to **VDDA**. Internal **VREF** is provided by a resistor trimmed circuit. For details on using the analog modules, see the KW41Z Data Sheet.

3.6 Module reset

Pin 17, **PTA2**, is used as an external reset source by default. This pin can be used for other functions, such as GPIO, by setting the RESET_PIN_CFG option bit of the FTFA_FPORT register to 0. This bit is retained through system resets and low power modes.

3.7 Debug and programming

The R41Z module supports the two pin Serial Wire Debug (SWD) interface and offers flexible mechanisms for non-intrusive debugging of program code. Breakpoints, single stepping, and instruction trace capture of code execution flow are part of this support. The R41Z also supports Micro Trace Buffer (MTB) which provide lightweight program trace capabilities using system RAM. SWD pins can be repurposed as additional GPIO by the application.

The R41Z module does not support resets through the SWD interface. Resets from programmers and test fixtures must be asserted through the reset pin.

3.8 Clocks

3.8.1 General parameters

The R41Z requires two clocks: a high frequency clock and a low frequency clock.

The high frequency clock is provided on-module by a high accuracy 32 MHz crystal. The low frequency clock is required for Real Time Clock (RTC) operation and radio Deep Sleep Mode (DSM). In most applications, an external crystal oscillator is required to provide the low frequency clock.

For normal run modes, an internal oscillator can provide the low frequency clock. However, to make full use of reduced power modes an external crystal must be present.

For most applications with the low frequency crystal, external capacitors are not required. Internal, programmable capacitors are provided on the R41Z module. To maintain accurate time keeping, these internal capacitors should be adjusted for the PCB's and crystal's characteristics during hardware initialization. Internal capacitance can be configured in 2pF increments using the RTC_CR configuration register.

An external clock source can be used in place of the low frequency crystal. In this case, the clock source should be connected to the **EXTAL32K** pin (PTB16) and **XTAL23K** (PTB17) should be left unconnected.

The R41Z's internal 32MHz clock can be provided to other devices using the **XTAL_OUT** signal on pin 40. This clock output can be toggled via software or externally enabled with the **XTAL_OUT_EN** signal. For information about the **XTAL_OUT_EN** signal mapping options, see also Single wire debug (SWD) and reset signals.

3.8.2 Low frequency crystal

Symbol	Parameter	Typ.	Max.	Unit
F_{NOM_LFXO}	Crystal frequency	32.768	-	kHz
$F_{TOL\_LFXO\_BLE}$	Frequency tolerance, Bluetooth LE applications	±20	±250	ppm
C_{L_LFXO}	Load capacitance	7	12.5	pF

Table 23: Low frequency crystal recommended specifications

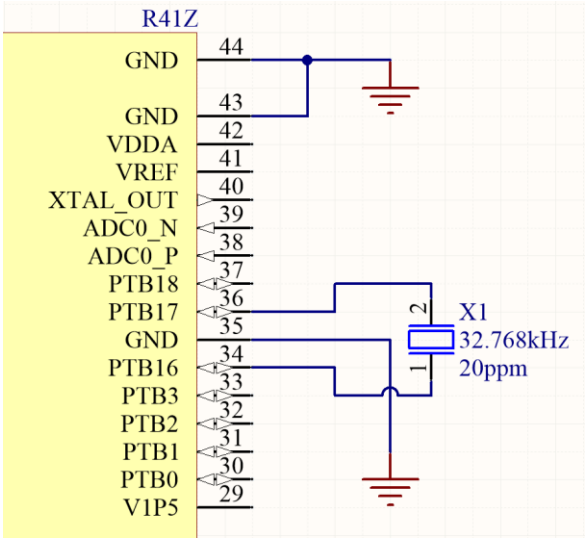


Figure 9: Schematic: Low frequency crystal

4 Firmware

Projects for the R41Z should utilize the MCUXpresso SDK, IDE and other utilities provided by NXP Semiconductors. This will allow access to the very latest Bluetooth support from NXP Semiconductors and provide an ongoing path as new features are released.

4.1 Factory image

The R41Z module is not loaded with a factory firmware image and is assigned firmware code “00”. This code is either marked or encoded within the 2D data matrix. See also Module marking.

☞ When the R41Z does not have firmware loaded that can be executed out of Power-on Reset (POR), the R41Z module re-asserts POR. This should be considered when connecting the R41Z to other devices on a shared reset circuit.

4.2 Bluetooth device address

The R41Z module is assigned a unique public Bluetooth device address that consists of the IEEE Organizationally Unique Identifier (OUI) combined with six unique hexadecimal digits. The entire Bluetooth device address is encoded within a 2D data matrix and the last six digits in human-readable text printed on the module label, as described in Module marking.

☞ This value is not pre-programmed into flash. The Bluetooth device address is typically located in flash as part of the firmware image and accessed as a global constant. The Bluetooth device address is printed encoded within the 2D data matrix and human readable text on the top of the module.

☞ When loading custom firmware to the module, the MAC address must be inserted into the image. This can be done using a 2D barcode scanner and suitable factory programmer tools. When loading a new application to the module, care should be taken to ensure the MAC address is not overwritten.

5 Mechanical specifications

5.1 Dimensions

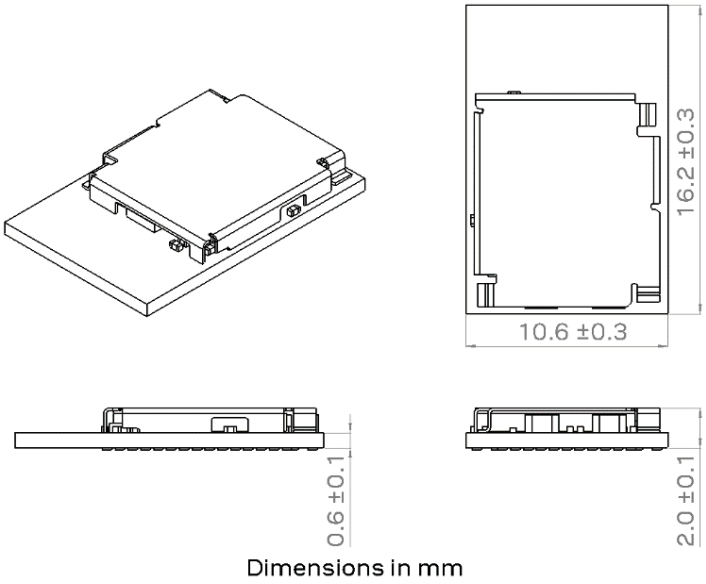


Figure 10: Mechanical drawing

5.2 Recommended PCB land pads

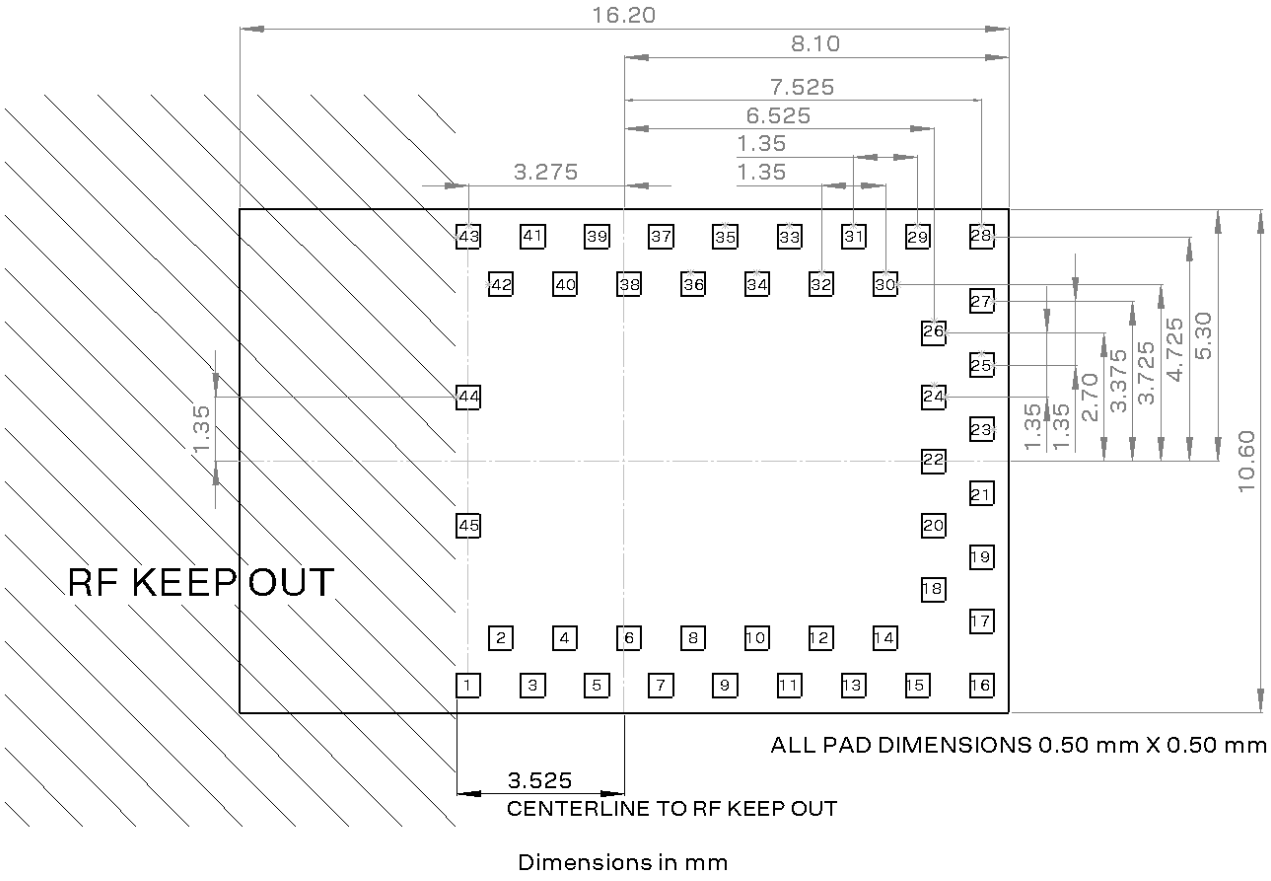


Figure 11: Recommended PCB land pads

☞ The RF keep-out area extends vertically to the board edges

5.3 Module marking

5.3.1 Module marking for type number R41Z-TA-R-00

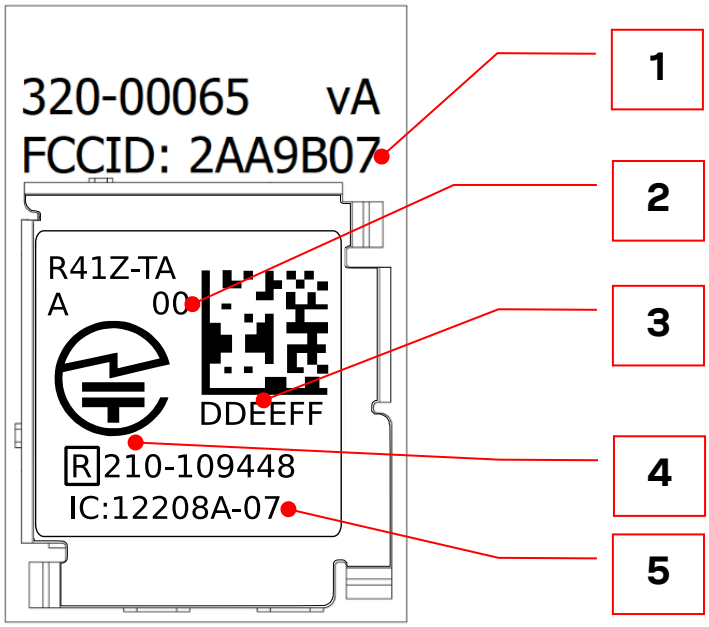


Figure 12: Module marking for type number R41Z-TA-R-00

Reference	Description
1	FCC ID (USA)
2	Firmware version (00 = no factory firmware loaded)
3	Data Matrix with unique serial number of six alphanumeric symbols, also in human-readable form. The full Bluetooth address consists of the IEEE OUI (94:54:93) with the six symbols appended: Example value: 94:54:93:XX:YY:ZZ
4	MIC ID and Giteki mark (Japan)
5	ISED ID (Canada)

Table 24: Module marking for type number R41Z-TA-R-00

5.3.2 Module marking for type number R41Z-TA-R-10

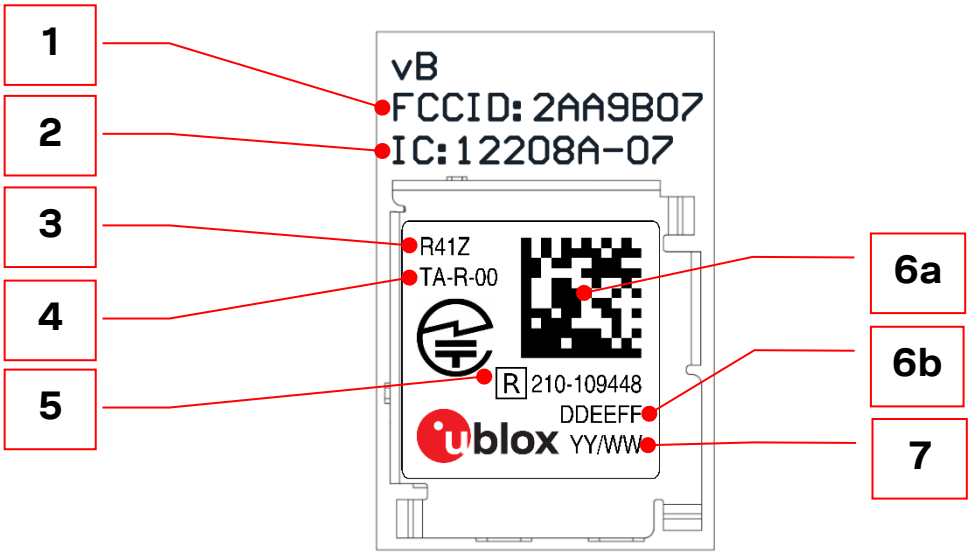


Figure 13: Module marking for type number R41Z-TA-R-10

Reference	Description
1	FCC ID (USA)
2	ISED ID (Canada)
3	Product name
3 + 4	Type number
5	MIC (Japan) Giteki mark and Certification ID
6a	Data Matrix with unique serial number of 19 alphanumeric symbols. The first 3 symbols represent module type number unique to each module variant, the next 12 symbols represent the unique hexadecimal Bluetooth device address of the module AABBCCDDEEFF, and the last 4 symbols represent the hardware and firmware version encoded HHFF. The IEEE OUI is in the first three bytes of the Bluetooth device address (AABBCC) and is one of the following values: D4:CA:6E, CC:F9:57, 60:09:C3, 6C:1D:EB. The remaining hexadecimal digits (DDEEFF) are unique.
6b	Second half of Bluetooth device address in human-readable format (DDEEFF above)
7	Date of production encoded YY/WW (year / week)

Table 25: Module marking for type number R41Z-TA-R-10

6 RF design notes

6.1 Recommended RF layout and ground plane

The integrated antenna on the R41Z module requires a suitable ground plane to radiate effectively. The module antenna has been tuned for having a PCB directly below with no copper or any other metal present. The module should be placed at the edge of the PCB with the antenna edge facing out. For best performance, the ground plane should be on the same layer as the module or as close as possible. If this is not possible in a design, ground planes on multiple layers generously connected with vias may also be used. Reduced ground plane size will result in reduced radio performance.

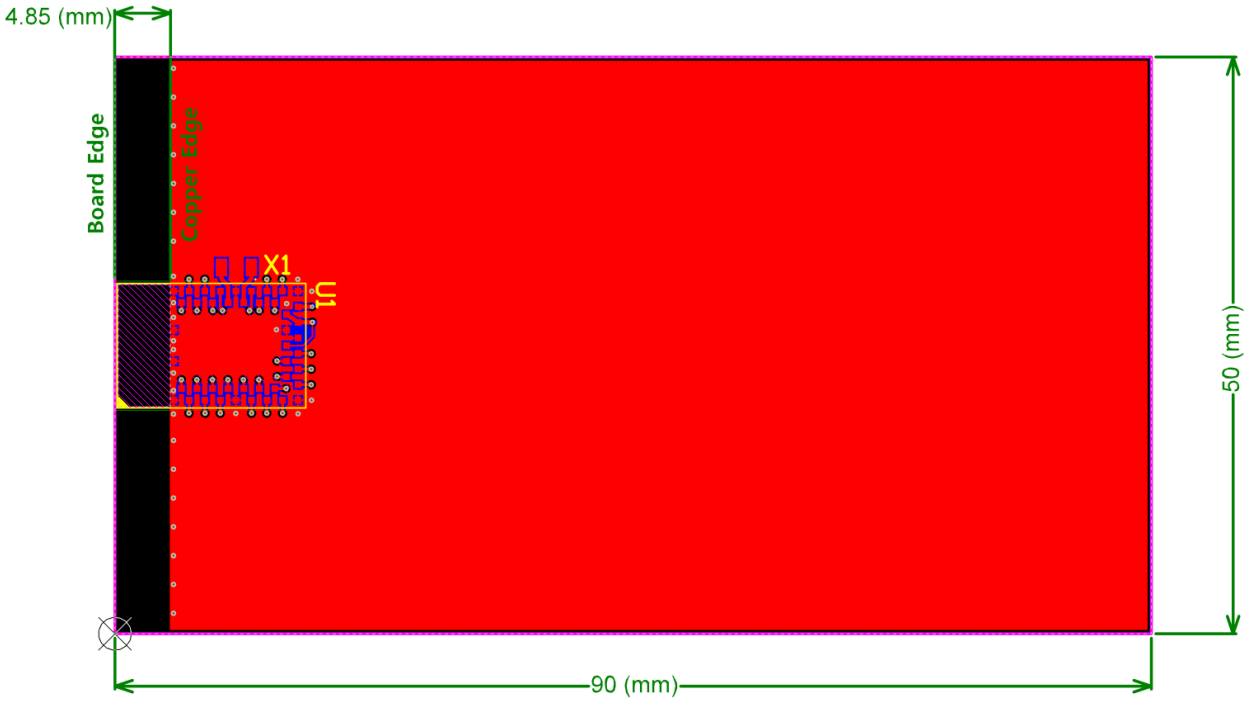


Figure 14: R41Z RF Example based on evaluation board

6.2 Mechanical enclosure

Care should be taken when designing and placing the module into an enclosure. Metal should be kept clear from the antenna area, both above and below. Any metal around the module can decrease RF performance.

The module is designed and tuned to be in free air. Any potting, epoxy fill, plastic over-molding, or conformal coating can negatively impact RF performance and must be evaluated by the customer. If potting must be used, the compound should have a low dielectric constant and should be designed for use with 2.4 GHz RF electronics.

6.3 Antenna patterns

Antenna patterns are based on the R41Z evaluation kit with a ground plane size of 82 mm x 56 mm. The X-Y-Z orientation is shown in Figure 15.

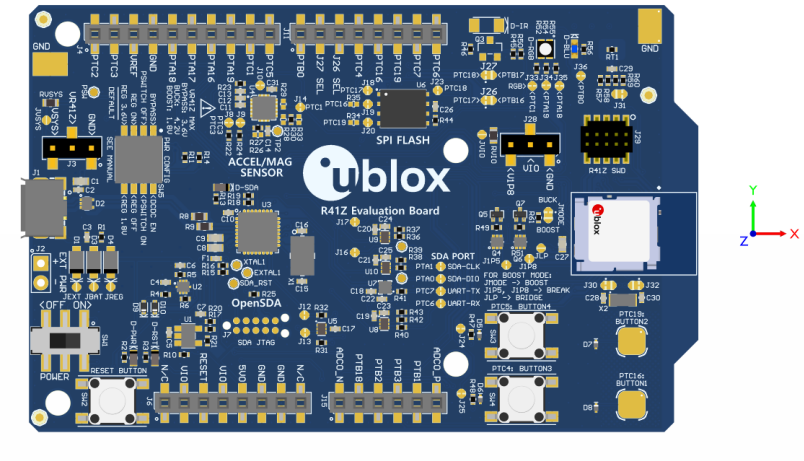


Figure 15: X-Y-Z antenna orientation

6.3.1 X-Y plane

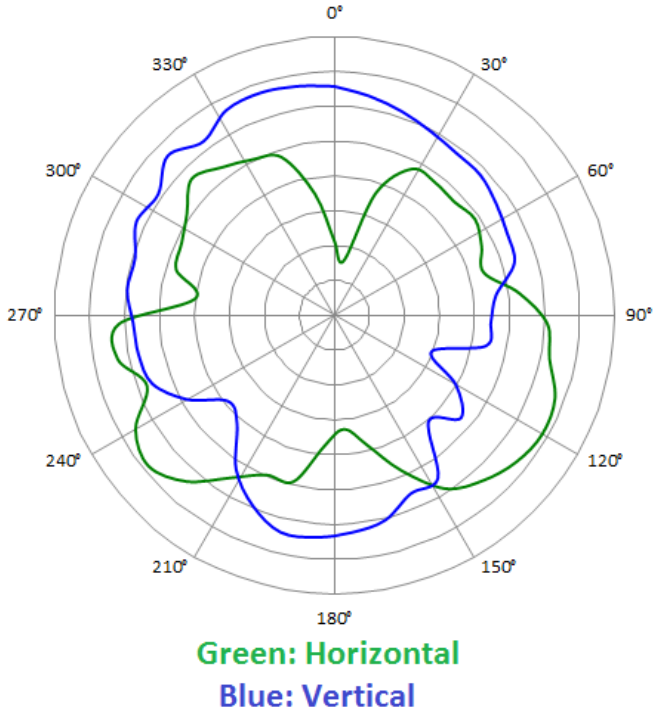


Figure 16: X-Y plane antenna pattern

6.3.2 Y-Z plane

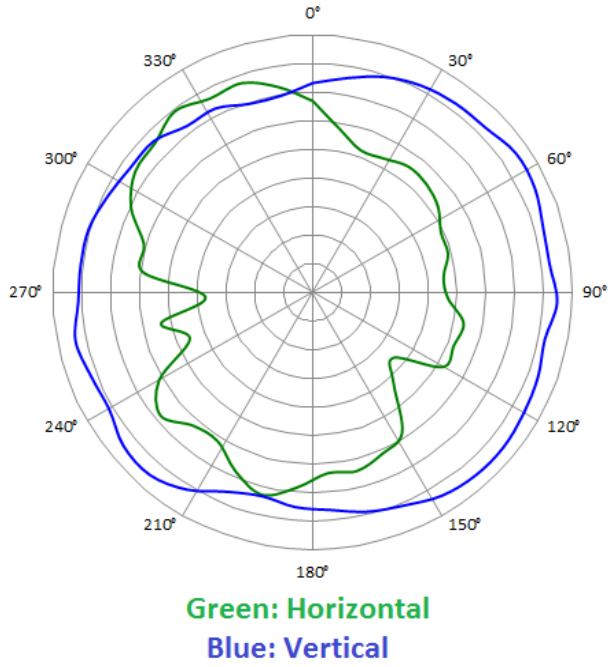


Figure 17: Y-Z plane antenna pattern

6.3.3 X-Z plane

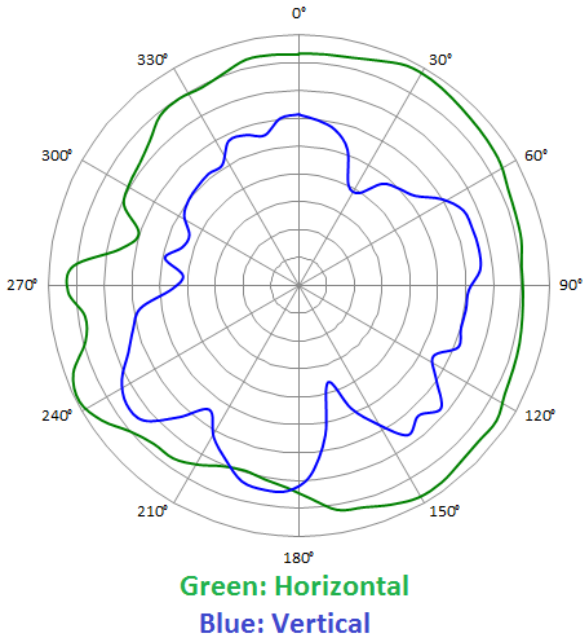


Figure 18: X-Z plane antenna pattern

7 Evaluation development kit

u-blox has developed a full featured evaluation board that provides on-board programming and debugging, power, and virtual COM port over USB, 32.768 kHz crystal, Arduino style IO headers two mechanical user buttons, two capacitive touch buttons, 3-axis accelerometer/magnetometer (I^2C), and a 4 Mbit flash chip (SPI). The evaluation board also allows for easy use of all the R41Z's DCDC power modes and can be powered from an adjustable LDO regulator, CR2032 coin cell battery, or through an external power header. Power consumption can be measured through onboard current sensing resistors and headers.

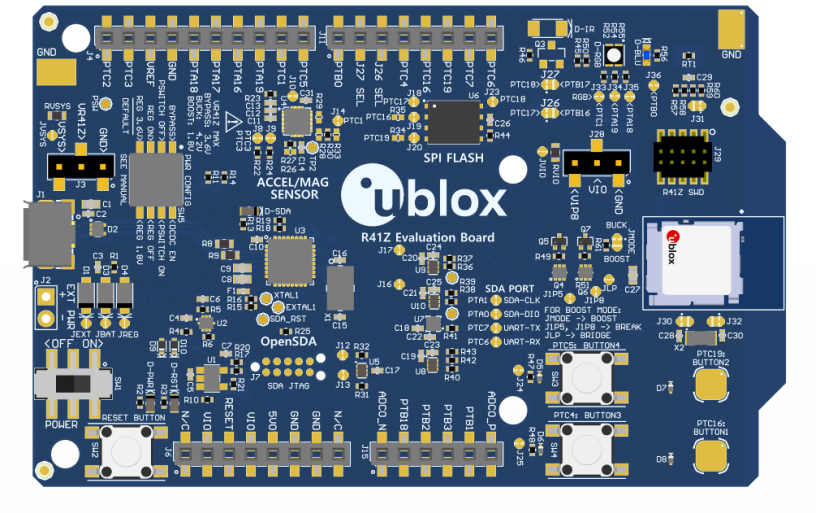


Figure 19: R41Z evaluation board

8 Qualification and approvals

8.1 United States (FCC):

The R41Z module has received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” modular approval in accordance with Parts 15.212 and 15.247. The modular approval allows the end user to integrate the module into a finished product without obtaining subsequent and separate FCC approvals for intentional radiation, provided no changes or modifications are made to the module circuitry. Changes or modifications could void the user’s authority to operate the equipment. The end user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

The finished product is required to comply with all applicable FCC equipment authorizations regulations, requirements and equipment functions not associated with the transmitter module portion. For example, compliance must be demonstrated to regulations for other transmitter components within the host product; to requirements for unintentional radiators (Part 15 Subpart B “Unintentional Radiators”), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (that is, Verification, or Declaration of Conformity) (for example, transmitter modules may also contain digital logic functions) as appropriate.

☞ Modification to this product will void the users’ authority to operate this equipment.

⚠ The OEM is still responsible for verifying end product compliance with FCC Part 15, subpart B limits for unintentional radiators through an accredited test facility.

8.1.1 Labeling and user information requirements

The R41Z is assigned the FCC ID number: 2AA9B07

If the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must also display a label referring to the enclosed module. This exterior label can use the following or similar wording:

> Contains FCC ID: 2AA9B07

In addition to marking the product with the appropriate FCC ID, the end product shall bear the following statement in a conspicuous location on the device (FCC Rules, Title 47, Subchapter A, Part 15, Subpart B, Chapter §15.19):

> This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

When the device is so small or for such use that it is impracticable to label it with the statement specified above in a font that is four-point or larger, and the device does not have a display that can show electronic labeling, then the information required by this paragraph shall be placed in the user manual and must also either be placed on the device packaging or on a removable label attached to the device.

The user manual may also require specific information based on the digital device classification. Refer to the FCC Rules, Title 47, Subchapter A, Part 15, Subpart B, Chapter §15.105 for specific wording of these notices.

8.1.2 RF exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

This module is approved for installation into mobile and/or portable host platforms and must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter guidelines. End users must be provided with transmitter operating conditions for satisfying RF Exposure compliance.

8.2 Canada (ISED)

The R41Z module is certified for use in Canada under Innovation, Science and Economic Development Canada (ISED) Radio Standards Specification (RSS) RSS-247 Issue 2 and RSSGen.

8.2.1 Labeling and user information requirements

The R41Z is assigned the IC ID number: 12208A-07

Labeling Requirements for the Host Device (from Section 3.2.1, RSS-Gen, Issue 3, December 2010): The host device shall be properly labeled to identify the module within the host device. The Industry Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labeled to display the Industry Canada certification number of the module, preceded by the words “Contains transmitter module”, or the word “Contains”, or similar wording expressing the same meaning, as follows:

> Contains transmitter module IC: 12208A-07

User Manual Notice for License-Exempt Radio Apparatus (from Section 7.1.3 RSS-Gen, Issue 3, December 2010): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

> This device complies with Industry Canada license exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.
> Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.
> Transmitter Antenna (from Section 7.1.2 RSS-Gen, Issue 3, December 2010): User manuals for transmitters shall display the following notice in a conspicuous location:
> Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.
> Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

8.2.2 RF exposure

All transmitters regulated by IC must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands). This module is approved for installation into mobile and/or portable host platforms and must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with Industry Canada's multi-transmitter guidelines. End users must be provided with transmitter operating conditions for satisfying RF Exposure compliance.

8.3 European Union regulatory compliance

Information about regulatory compliance of the European Union for the R41Z module is available in the R41Z Declaration of Conformity.

8.3.1 Radio Equipment Directive (RED) 2014/53/EU

The R41Z module complies with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

8.4 Australia / New Zealand (RCM)

The R41Z has been tested to comply with the AS/NZS 4268:2017, Radio equipment and systems – Short range devices – Limits and methods of measurement. The report may be obtained from your local FAE and may be used as evidence in obtaining permission to use the Regulatory Compliance Mark (RCM).

Information on registration as a Responsible Party, license and labeling requirements may be found at the following websites:

Australia: http://www.acma.gov.au/theACMA/radiocommunications-short-range-devices-standard-2004
New Zealand: http://www.rsm.govt.nz/compliance

Only Australian-based and New Zealand-based companies who are registered may be granted permission to use the RCM. An Australian-based or New Zealand-based agent or importer may also register as a Responsible Party to use the RCM on behalf of a company not in Australia or New Zealand.

8.5 Japan (MIC)

The R41Z module has received type certification and is labeled with its own technical conformity mark and certification number as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan. Integration of this module into a final end product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed. Additional testing may be required:

- If the host product is subject to electrical appliance safety (for example, powered from an AC mains), the host product may require Product Safety Electrical Appliance and Material (PSE) testing. The integrator should contact their conformance laboratory to determine if this testing is required.
- There is a voluntary Electromagnetic Compatibility (EMC) test for the host product administered by VCCI: http://www.vcci.jp/vcci_e/index.html

The label on the end product which contains a R41Z module must follow the MIC marking requirements. Labeling requirements for Japan available at the Ministry of Internal Affairs and Communications (MIC) website: http://www.tele.soumu.go.jp/e/index.htm.

The R41Z module is labeled with its assigned technical conformity mark and certification number. The end-product in which this module is being used must have an external label referring to the type certified module inside:

Contains transmitter module with certificate number:

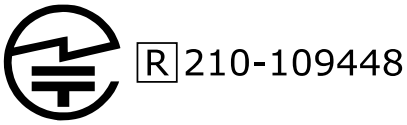


Figure 20: Japan MIC Mark

8.6 Bluetooth qualification

The Bluetooth SIG maintains the Bluetooth Specification and ensures that products are properly tested and comply with the Bluetooth license agreements. Companies that list products with the Bluetooth SIG are required to be members of the SIG and submit the listed fees. Refer to this link for details: https://www.bluetooth.com/develop-with-bluetooth/qualification-listing

The R41Z Bluetooth Low Energy module based on the NXP Semiconductors KS41Z is listed as a "Tested Component" with QDID 95459. This allows an end-product based on a R41Z module to inherit the component listings without the need to run through all of the tests again. The end-product will often inherit several QDIDs that are identified on a "Declaration of Compliance".

9 Environmental

9.1 RoHS

The R41Z module is in compliance with Directive 2011/65/EU, 2015/863/EU of the European Parliament and the Council on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

9.2 REACH

The R41Z module does not contain the SVHC (Substance of Very High Concern), as defined by Directive EC/1907/2006 Article according to REACH Annex XVII.

9.3 California proposition 65 (P65)

This product can expose you to Nickel (metallic), which is known to the State of California to cause cancer. For more information go to www.P65Warnings.ca.gov.

☞ Warnings are not required where the listed chemical is inaccessible to the average user of the end product.

10 Product handling

10.1 Packaging

10.1.1 Reel packaging

Modules are packaged on 330 mm reels loaded with 1000 modules. Each reel is placed in an antistatic bag with a desiccant pack and humidity card and placed in a 340x350x65 mm box. An antistatic warning and reel label are adhered to the outside of the bag.

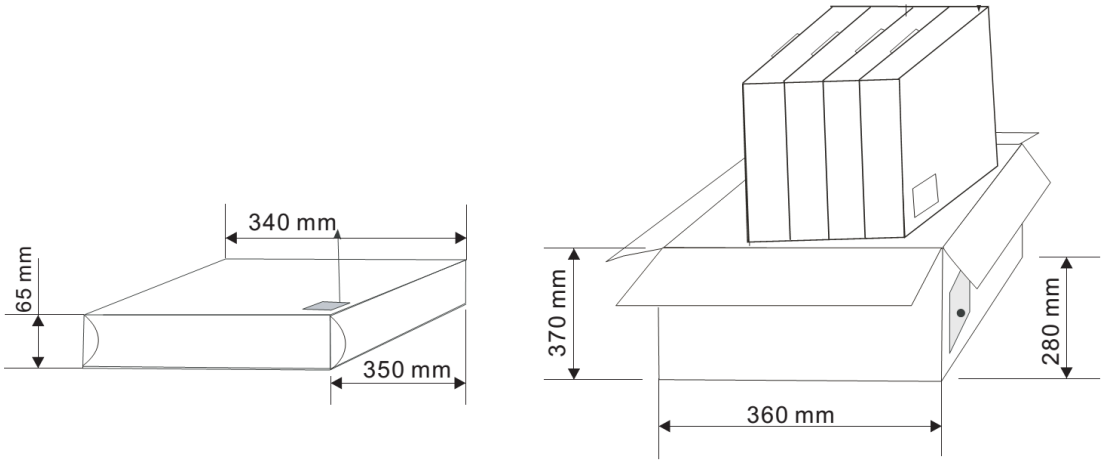
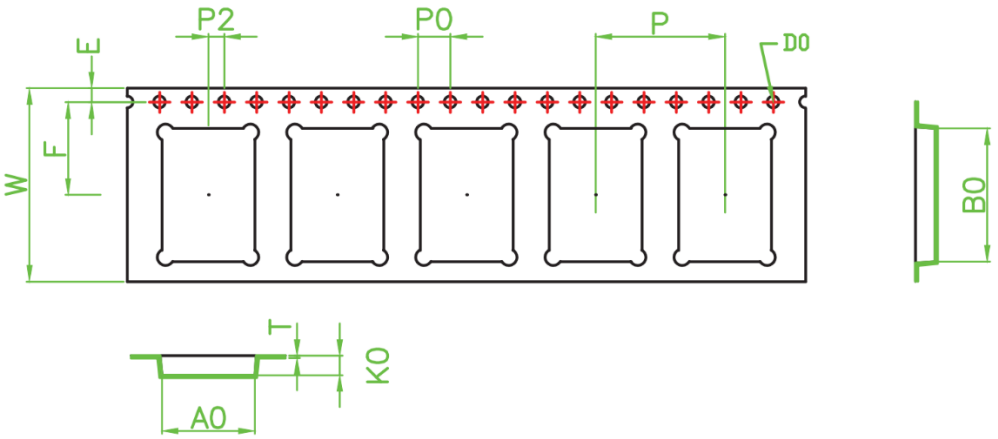


Figure 21: Reel cartons

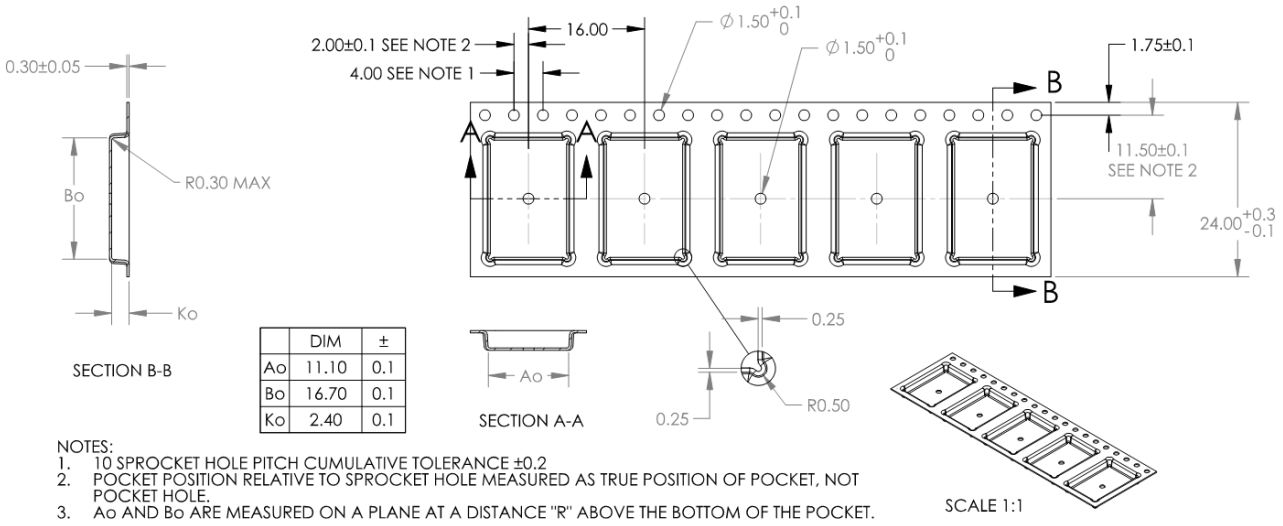
10.1.2 Carrier tape dimensions for type number R41Z-TA-R-00



W	24.00±0.30	P	16.00±0.10	A0	11.50±0.10	B0	16.50±0.10
S	0.00±0.10	P0	4.00±0.10	A1		B1	
E	1.75±0.10	P2	2.00±0.10			B2	
F	11.50±0.10	D0	ø1.50 +0.10 0	K0	2.40±0.10	K1	
T	0.30±0.05	D1					

Figure 22: Carrier tape dimensions for type number R41Z-TA-R-00

10.1.3 Carrier tape dimensions for type number R41Z-TA-R-10



	DIM	±
Ao	11.10	0.1
Bo	16.70	0.1
Ko	2.40	0.1

Figure 23: Carrier tape dimensions for type number R41Z-TA-R-00

10.2 Carrier tape orientation

R41Z modules are positioned in the carrier tape with the red u-blox logo dot on the label in quadrant 3. See Figure 24.

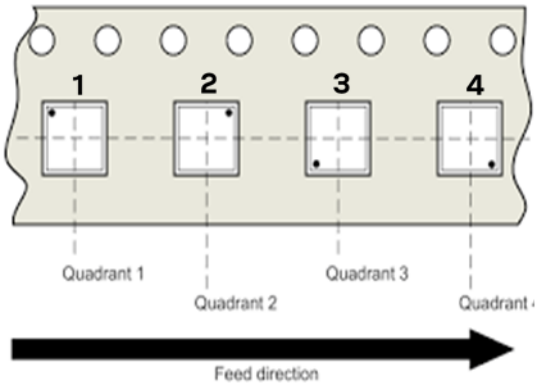


Figure 24: Carrier tape quadrants

☞ "Feed direction" is defined in such a way that at the customer's assembly line a module is first picked at position "4" and then picked at positions "3", "2" and "1".

10.3 Moisture sensitivity level

The R41Z series is rated for MSL 3, 168-hour floor life after opening.

10.4 Reflow soldering

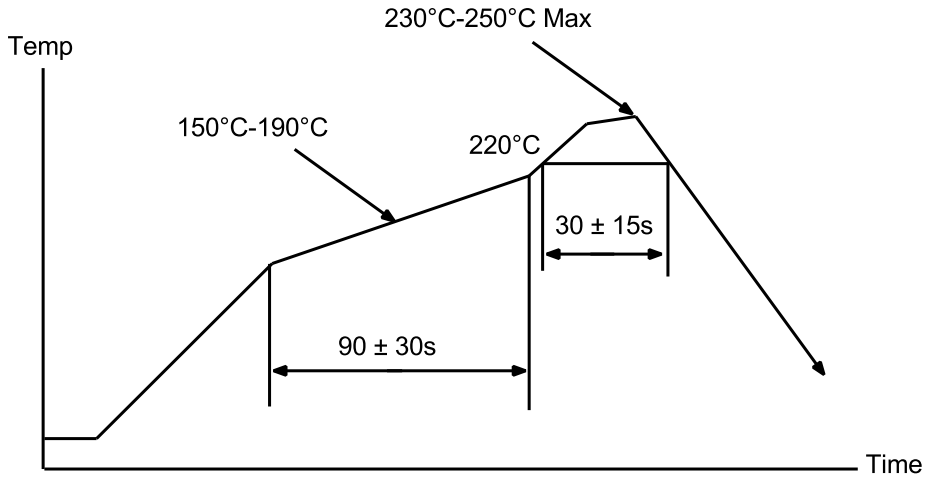


Figure 25: Reflow profile for lead-free solder

10.5 ESD precautions

⚠ The R41Z module contains highly sensitive electronic circuitry and is an Electrostatic Sensitive Device (ESD). Handling the R41Z module without proper ESD protection may destroy or damage them permanently.

Proper ESD handling and packaging procedures must be applied throughout the processing, handling, and operation of any application that incorporates the R41Z module. Failure to observe these recommendations can result in severe damage to the device.

11 Ordering information

Ordering Code	Product
R41Z-TA-R	R41Z module, Rev A, Tape and Reel, 1000-piece multiples
R41Z-Eval	R41Z evaluation kit with OpenSDA programmer

Table 26: Product ordering codes

12 Life support and other high-risk use warnings

This product is not designed nor intended for use in a life support device or system, nor for use in other fault-intolerant, hazardous, or other environments requiring fail-safe performance, such as any application in which the failure or malfunction of the product could lead directly or indirectly to death, bodily injury, or physical or property damage (collectively, “High-Risk Environments”).

⚠ u-blox expressly disclaims any express or implied warranty of fitness for use in high-risk environments.

The customer using this product in a high-risk environment agrees to indemnify and defend u-blox from and against any claims and damages arising out of such use.

Related documents

[1] u-blox Package information guide, UBX-14001652
[2] R41Z Evaluation board user guide, UBX-19033357
[3] NXP KW41Z Fact sheet
[4] NXP BLE Mobile Toolbox
[5] NXP KW41Z Data sheet
[6] NXP KW41Z Reference manual
[7] NXP KW41Z Errata sheet
[8] NXP AN3863: Designing touch sensing electrodes

For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
0.9	20-Oct-2016		Initial release.
1.0	21-Dec-2016		Added: Certifications, Antenna patterns, Carrier tape info. Images updated
1.1	21-Apr-2017		Added: Additional pin mux tables, errata note in section 6.
2.0	01-Feb-2019		Updated to new format Updated Life Support and other High-Risk Use Warning
2.1	07-May-2019		Included references to Zigbee, now part of the NXP SDK
R06	07-Jan-2020	brec	Document converted from Rigado R41Z data sheet to u-blox R41Z data sheet.
R07	02-Feb-2021	brec	Added type number R41Z-TA-R-10, updated product photos, corrected operating temperature range, updated polar plot image orientation for consistency with other products, updated Bluetooth device address description, corrected module marking information for type number R41Z-TA-R-00 and added module marking and tape and reel dimensions information for type number R41Z-TA-R-10, updated safety standard to EN 62368, updated height dimension, updated drawings with u-blox font.
R08	17-Feb-2021	brec	Added Bluetooth device address OUI information to Table 25.
R09	22-Jun-2022	brec	Added Carrier tape orientation. Removed ambiguous description of operating condition ranges in Electrical specifications. Added ESD precautions. Revised contact information. Changed status for old type number R41Z-TA-R-00 (replaced by R41Z-TA-R-10) to obsolete and corrected the typo that the PCN/IN reference UBX-20017684 relates to R41Z-TA-R-00 instead of R41Z-TA-R-10.
R10	15-Nov-2024	lalb	Updated product status for R41Z-TA-R-10 to Mass Production.

Contact

u-blox AG

Address: Zürcherstrasse 68
8800 Thalwil
Switzerland

For further support and contact information, visit us at www.u-blox.com/support.