

PE43205

Document category: Product Specification

UltraCMOS® RF Digital Attenuator, 2-bit, 18 dB, 35–6000 MHz



Features

- Attenuation: 6-dB and 12-dB steps to 18 dB
- Fast switching time: 29 ns
- Low attenuation error:
 - 0.10 dB @ 2 GHz
 - 0.15 dB @ 3 GHz
- High linearity: +61 dBm IIP3 @ 1950 MHz
- Wide supply range: 2.3–5.5V
- 1.8V control logic compatible
- 105 °C operating temperature
- ESD performance:
 - 2000V HBM on all pins
 - 100V MM on all pins
 - 1000V CDM on all pins
- Parallel control
- Packaging: 12-lead 3×3 mm QFN

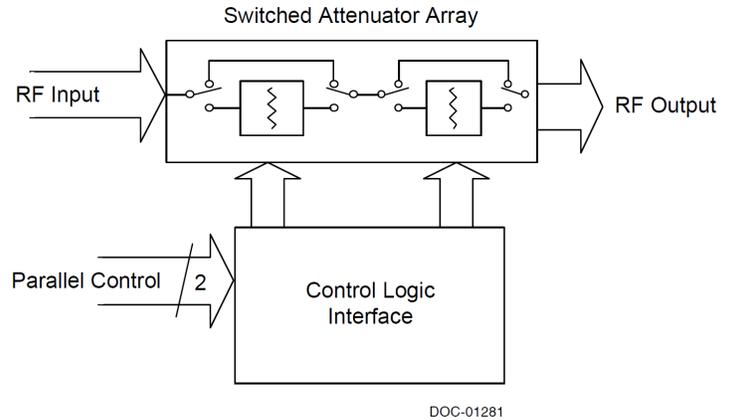


Figure 1. PE43205 functional diagram

Product description

The PE43205 is a 50Ω, HaRP™ technology-enhanced fast switching 2-bit RF digital step attenuator (DSA) designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This DSA is a pin-compatible upgraded version of the pSemi PE43204 with a wider frequency and power supply range, and an extended operating temperature range.

Covering an 18 dB attenuation range in 6-dB and 12-dB steps, the PE43205 maintains high RF performance and low power consumption from 35 MHz through 6 GHz. The PE43205 is offered in a 12-lead 3×3 mm QFN package. No external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE43205 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

 Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

 When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE43205 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Voltage on any digital input	V_I	-0.3	3.6	V
Storage temperature range	T_{ST}	-65	+150	°C
Maximum input power	$P_{MAX,ABS}$	–	+27.5	dBm
ESD voltage HBM, on all pins ⁽¹⁾	$V_{ESD,HBM}$	–	2000	V
ESD voltage MM, on all pins ⁽²⁾	$V_{ESD,MM}$	–	100	V
ESD voltage CDM, on all pins ⁽³⁾	$V_{ESD,CDM}$	–	1000	V



1. Human Body Model (MIL-STD 883 Method 3015.7).
2. Machine Model (JEDEC JESD22-A115).
3. Charged Device Model (JEDEC JESD22-C101).

Recommended operating conditions

Table 2 lists the PE43205 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE43205 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	–	5.5	V
Supply current	I_{DD}	–	130	200	μA
Digital input high	V_{IH}	1.17	–	3.6	V
Digital input low	V_{IL}	-0.3	–	0.6	V
Digital input leakage	–	–	–	10	μA
RF input power, CW: - 35 MHz–4 GHz - > 4 GHz–6 GHz	$P_{MAX,CW}$	–	–	See Figure 2 +24	dBm
RF input power, pulsed:(*) - 35 MHz–4 GHz - > 4 GHz–6 GHz	$P_{MAX,PULSED}$	–	–	See Figure 2 +27	X dBm
Operating temperature range	T_{OP}	-40	+25	+105	$^{\circ}\text{C}$

 * Pulsed, 5% duty cycle of 4620 μs period, 50 Ω .

Electrical specifications

Table 3 lists the PE43205 key electrical specifications at +25 °C and $V_{DD} = 2.3\text{--}5.5\text{V}$, unless otherwise specified.

Table 3. PE43205 electrical specifications at +25 °C

Parameter	Condition	Min	Typ	Max	Unit
Frequency range	–	35	–	6000	MHz
Attenuation range	6-dB and 12-dB steps	–	0–18	–	dB
Insertion loss	35 MHz–2 GHz	–	0.50	0.60	dB
	2–3 GHz		0.60	0.70	
	3–4 GHz		0.70	0.80	
	4–5 GHz		0.85	1.10	
	5–6 GHz		1.05	1.30	
Attenuation error	0–18 dB attenuation settings:				dB
	35 MHz–2 GHz	-0.45	0.10	0.40	
	> 2–3 GHz	-0.45	0.15	0.50	
	> 3–4 GHz	-0.15	0.45	1.05	
	> 4–5 GHz	-0.15	0.55	1.25	
> 5–6 GHz	-0.30	0.75	1.55		
Return loss	35 MHz–2 GHz	–	17	–	dB
	2–3 GHz		14		
	3–4 GHz		11		
	4–5 GHz		10		
	5–6 GHz		9		
Relative phase	All states:				deg
	35 MHz–2 GHz	–	9	–	
	2–3 GHz		12		
	3–4 GHz		17		
	4–5 GHz		22		
5–6 GHz		25			
Input 0.1dB compression point ⁽¹⁾	200 MHz–6 GHz	–	30	–	dBm
IIP3	1950 MHz	–	61	–	dBm
Switching time ⁽²⁾	50% DC CTRL to 90% or 10% RF	–	29	–	ns



1. The input 0.1 dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see [Table 2](#).
2. The PE43205 has a maximum 25 kHz switching rate. The switching rate is defined as the speed at which the DSA can be toggled across attenuation states. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Table 4 lists the PE43205 key electrical specifications at +105 °C and $V_{DD} = 2.3\text{--}5.5\text{V}$, unless otherwise specified.

Table 4. PE43205 electrical specifications at +105 °C

Parameter	Condition	Min	Typ	Max	Unit
Frequency range	–	35	–	6000	MHz
Attenuation range	6-dB and 12-dB steps	–	0–18	–	dB
Insertion loss	35 MHz–2 GHz	–	0.60	0.70	dB
	2–3 GHz		0.65	0.80	
	3–4 GHz		0.80	0.90	
	4–5 GHz		0.95	1.20	
	5–6 GHz		1.15	1.45	
Attenuation error	0–18 dB attenuation settings:				dB
	35 MHz–2 GHz	-0.35	-0.03	0.25	
	> 2–3 GHz	-0.45	-0.10	0.30	
	> 3–4 GHz	-0.45	-0.15	0.65	
	> 4–5 GHz	-0.35	0.25	0.85	
> 5–6 GHz	-0.45	0.40	1.15		
Return loss	35 MHz–2 GHz	–	18	–	dB
	2–3 GHz		15		
	3–4 GHz		11		
	4–5 GHz		10		
	5–6 GHz		9.5		
Relative phase	All states:				deg
	35 MHz–2 GHz	–	9	–	
	2–3 GHz		13		
	3–4 GHz		17		
	4–5 GHz		23		
5–6 GHz		25			
Input 0.1 dB compression point ⁽¹⁾	200 MHz–6 GHz	–	30	–	dBm
IIP3	1950 MHz	–	63	–	dBm
Switching time ⁽²⁾	50% DC CTRL to 90% or 10% RF	–	31	–	ns



1. The input 0.1 dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see [Table 2](#).
2. The PE43205 has a maximum 25 kHz switching rate. The switching rate is defined as the speed at which the DSA can be toggled across attenuation states. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE43205 typical low-frequency spurious performance is –135 dBm.

Truth table

Table 5. PE43205 attenuation word truth table

C1	C2	Attenuation setting RF1–RF2
L	L	Reference insertion loss
H	L	6 dB
L	H	12 dB
H	H	18 dB

Power de-rating curve

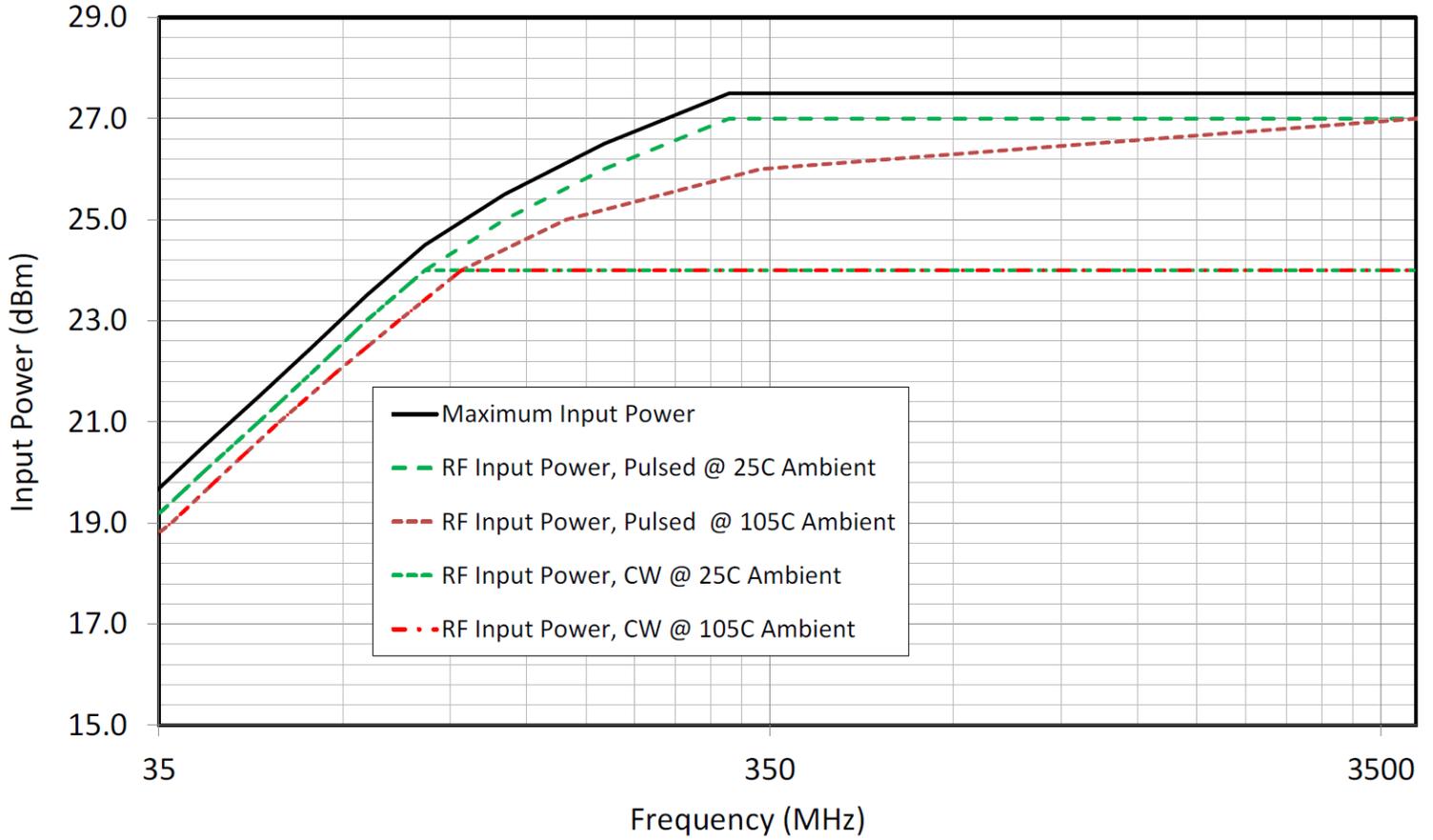


Figure 2. Power de-rating curve for 35 MHz–4 GHz

Typical performance data

Figure 3–Figure 10 show the typical performance data at +25 °C and $V_{DD} = 3.3V$, unless otherwise specified.

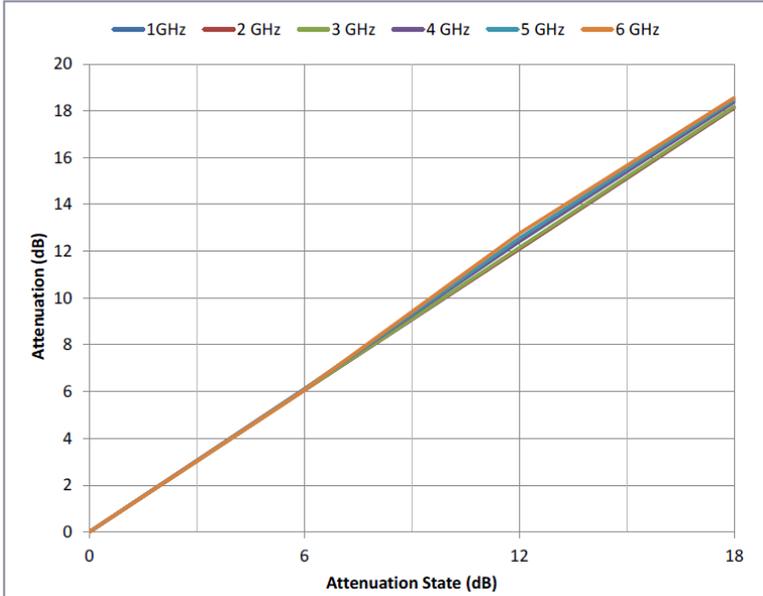


Figure 3. Attenuation vs. attenuation setting

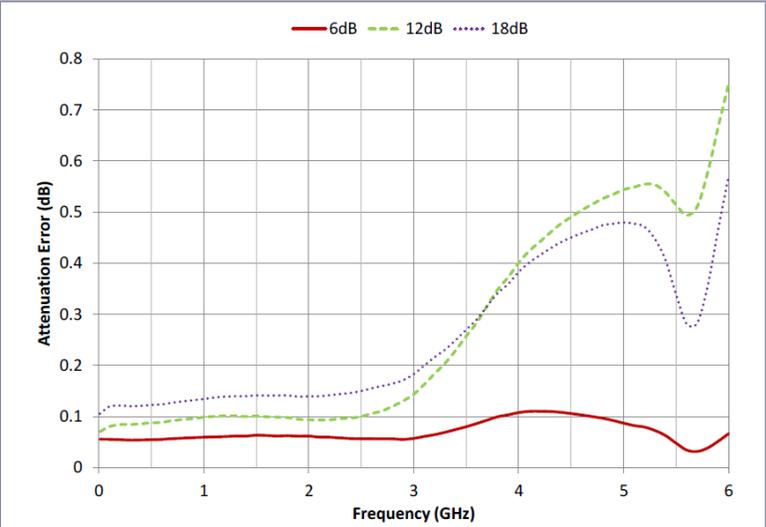


Figure 4. Attenuation error vs. frequency

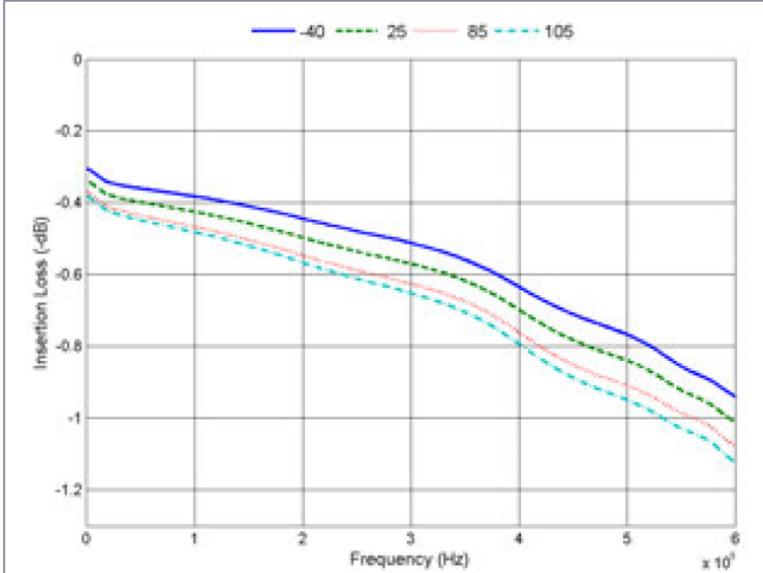


Figure 5. Insertion loss vs. temperature

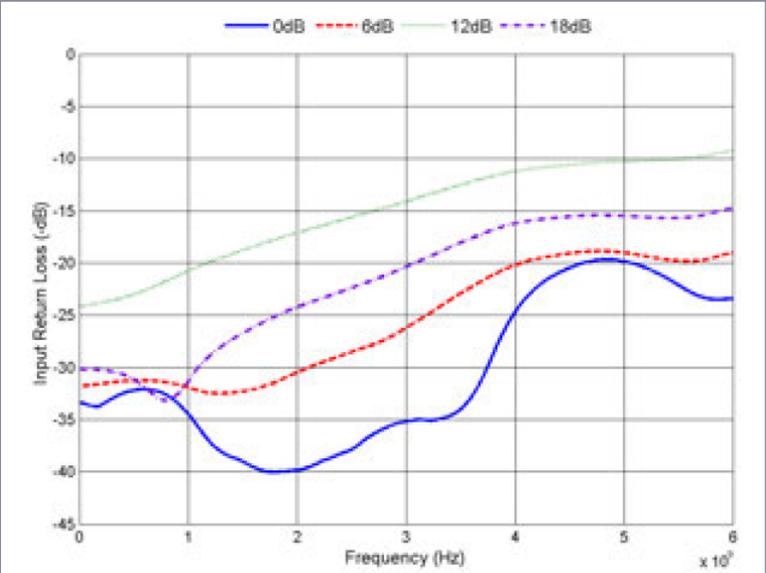


Figure 6. Input return loss vs. attenuation state

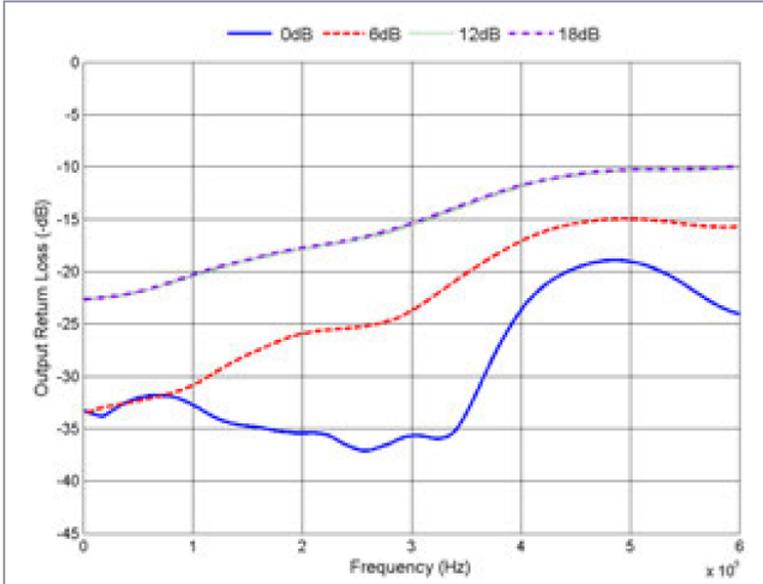


Figure 7. Output return loss vs. attenuation state

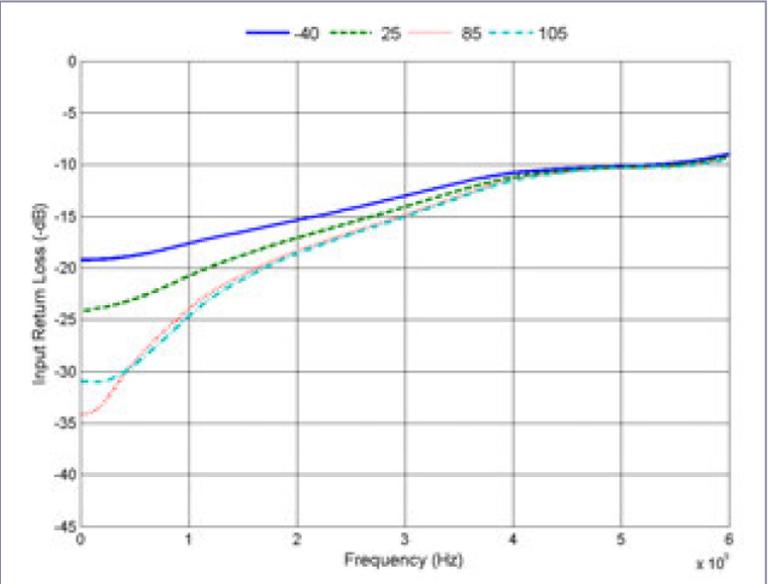


Figure 8. Input return loss vs. temperature @ 12 dB state

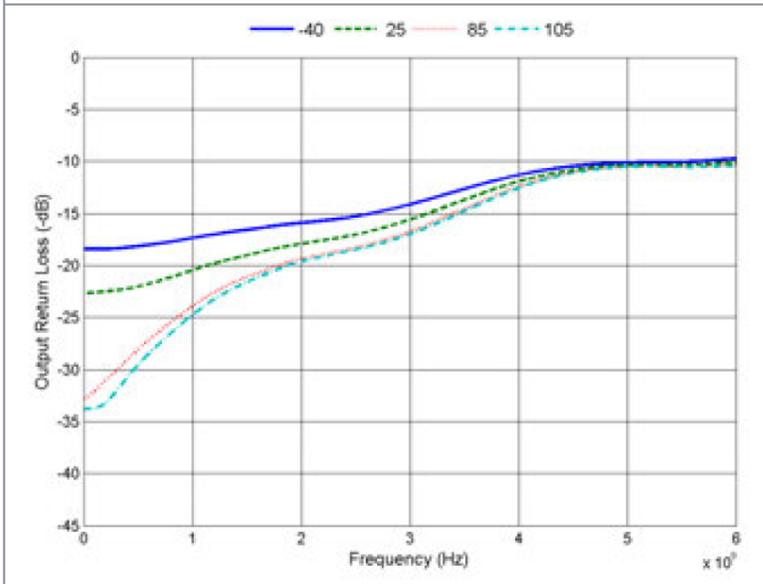


Figure 9. Output return loss vs. temperature @ 12 dB state

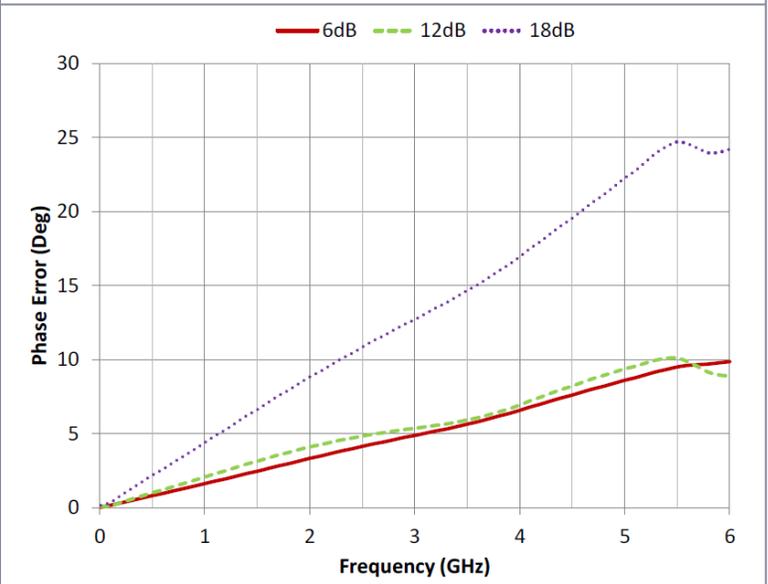


Figure 10. Relative phase vs. frequency

Evaluation kit

pSemi designed the 2-bit DSA evaluation kit board to ease your evaluation of the pSemi PE43205.

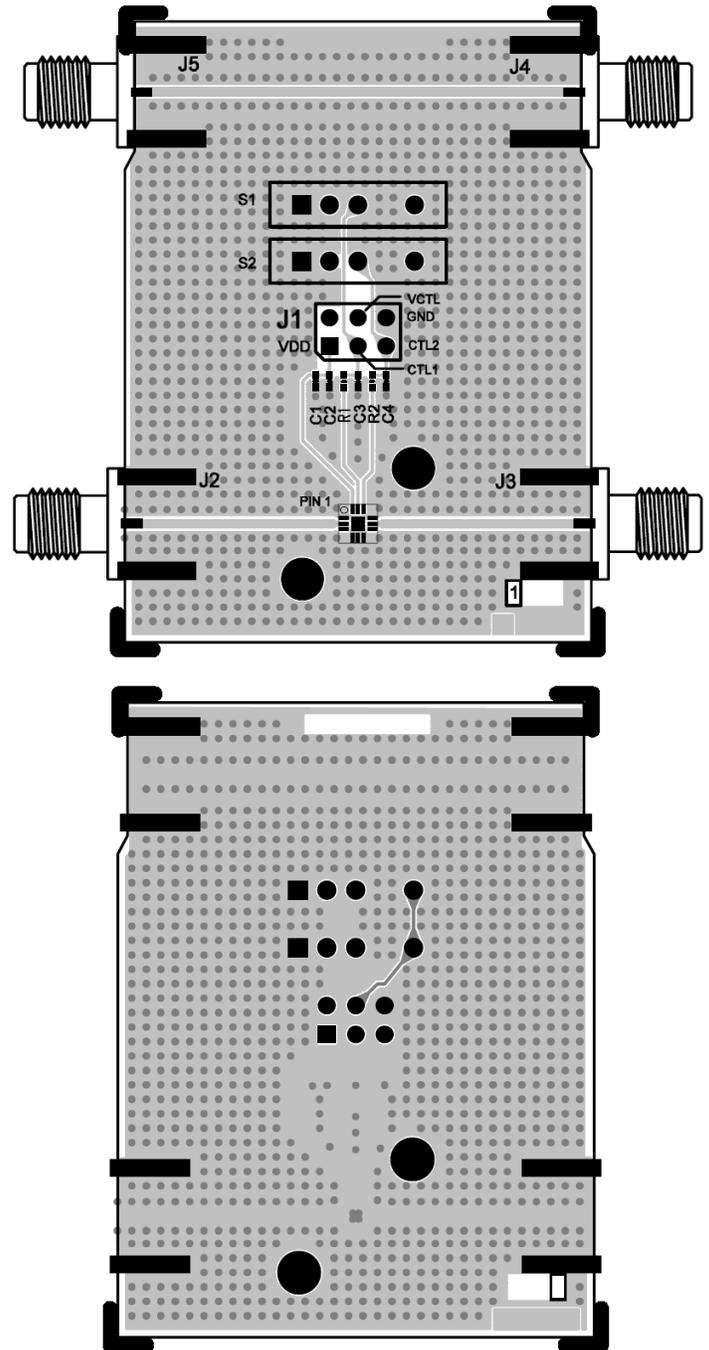
To evaluate the PE43205, apply 3.3V to the VDD header pin and ground to the GND header pin. The DUT can be controlled two ways:

- *Use the mechanical switches with the VCTL pin:* Apply the preferred control voltage to the VCTL header pin. The top mechanical switch controls the 6-dB stage, and the bottom mechanical switch controls the 12-dB stage. For each switch, the left position is the 0V condition, and the right position is the VCTRL condition. The middle position leaves the control pin floating.
- *Use the CTL1 and CTL2 pins:* Each pin directly controls the 6-dB and 12-dB stage, respectively. The VCTL pin on the header is left open. Leave the mechanical switches uninstalled or keep them in the middle position.

To accurately measure the PE43205 fast-switching performance, remove C3 and C4.

Power-up control settings

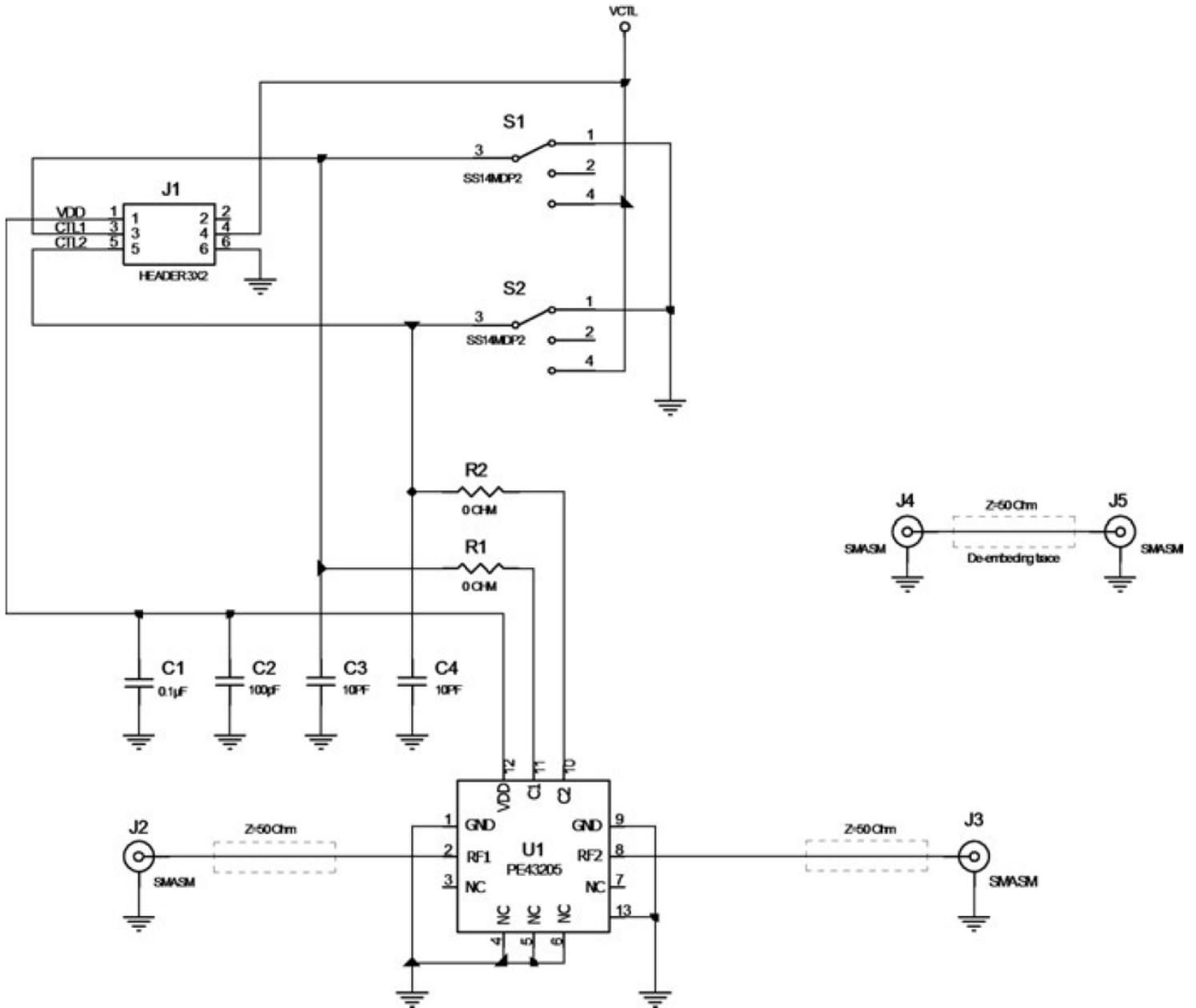
The PE43205 always powers up into the state determined by the voltages on the two control pins. The DSA can be preset to any state within the 18 dB range by pre-setting the parallel control pins before power-up. There is a 10- μ s delay between the time that the DSA is powered-up and the time that the preferred state is set. If the control pins are left floating during power-up, the device defaults to the minimum attenuation setting (insertion loss state).



PRT-53374

Figure 11. Evaluation board layout

Evaluation board schematic



- Notes: 1. Use PCB part number PRT-53374.
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

DOC-30927

Figure 12. Evaluation board schematic

Pin information

Figure 13 shows the PE43205 pin map for the 12-lead 3×3 mm QFN package, and Table 6 lists the description for each pin.

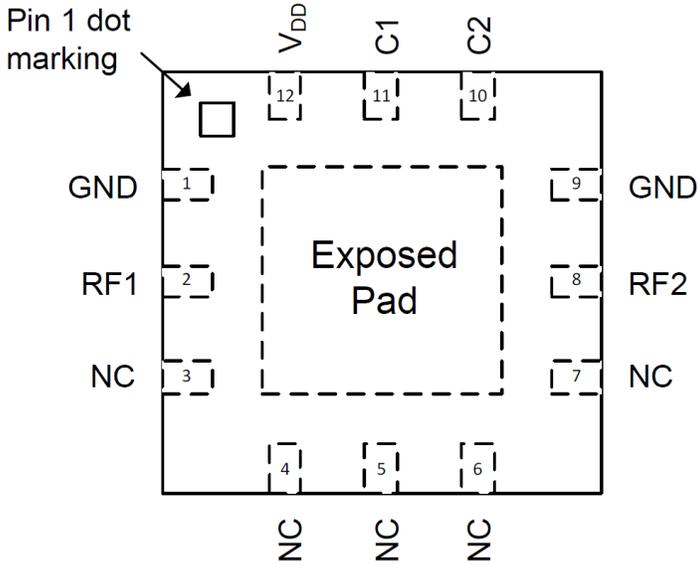


Figure 13. Pin configuration (top view)

Table 6. PE43205 pin descriptions

Pin no.	Pin name	Description
1, 9	GND	Ground
2 ⁽¹⁾	RF1	RF port 1
3–7 ⁽²⁾	NC	No connect
8 ⁽¹⁾	RF2	RF port 2
10	C2	Attenuation control bit, 12 dB
11	C1	Attenuation control bit, 6 dB
12	V _{DD}	Supply voltage (nominal 3.3V)
Pad	GND	Exposed pad. Ground for proper operation.



1. RF pins 2 and 8 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. Pins 3 through 7 can be tied to ground if preferred, but they are not connected to ground within the package.

Packaging information

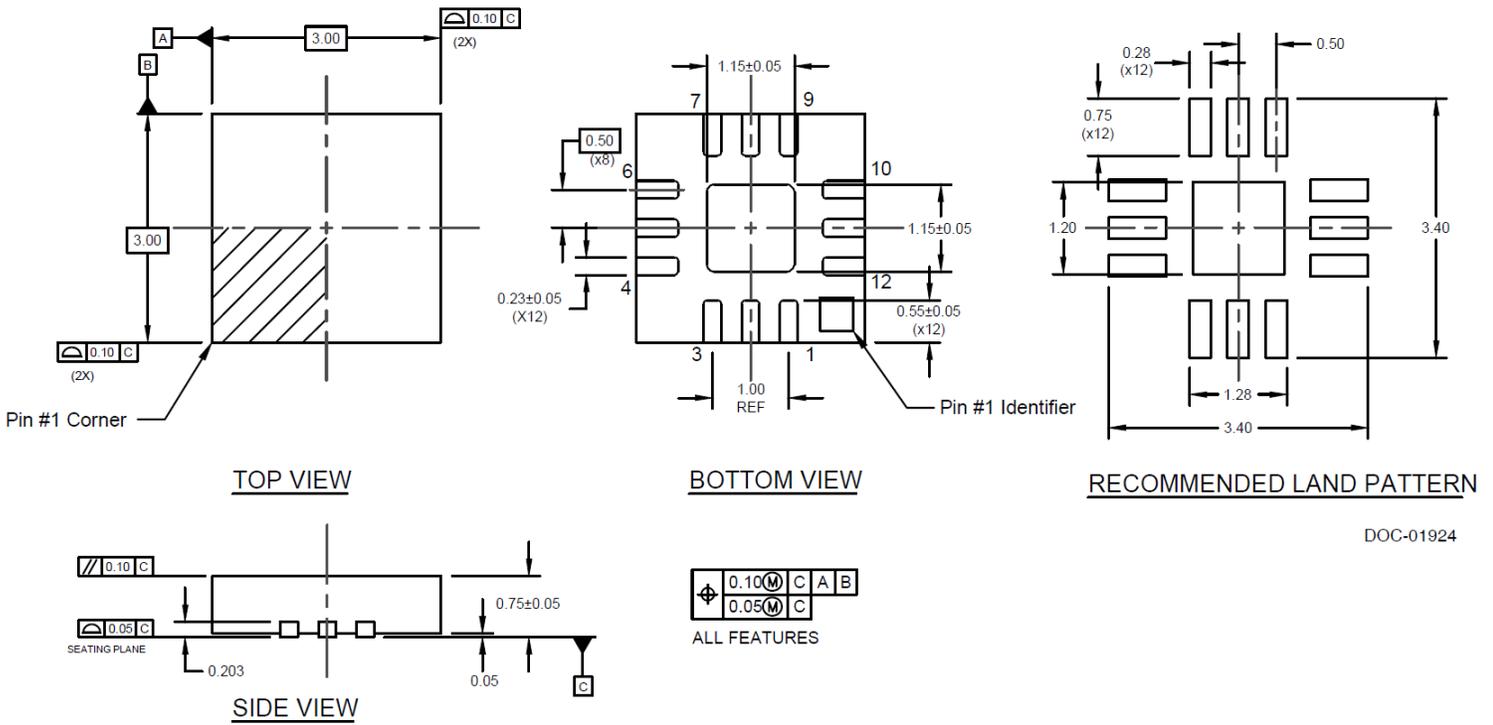
This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE43205 moisture sensitivity level rating for the 12-lead 3×3 mm QFN package is MSL1.

Package drawing



DOC-01924

Note: Pin 1 identification tab is electrically connected to the exposed ground paddle.

Figure 14. Package mechanical drawing for the 12-lead 3×3 mm QFN package

Top-marking specification



DOC-51207

- = Pin 1 designator
- 43205 = Five digit part number
- YYWW = Date Code, last two digits of the year and work week
- ZZZZZZ = Maximum six characters of the assembly lot code

Figure 15. PE43205 package marking specification

Tape and reel specification

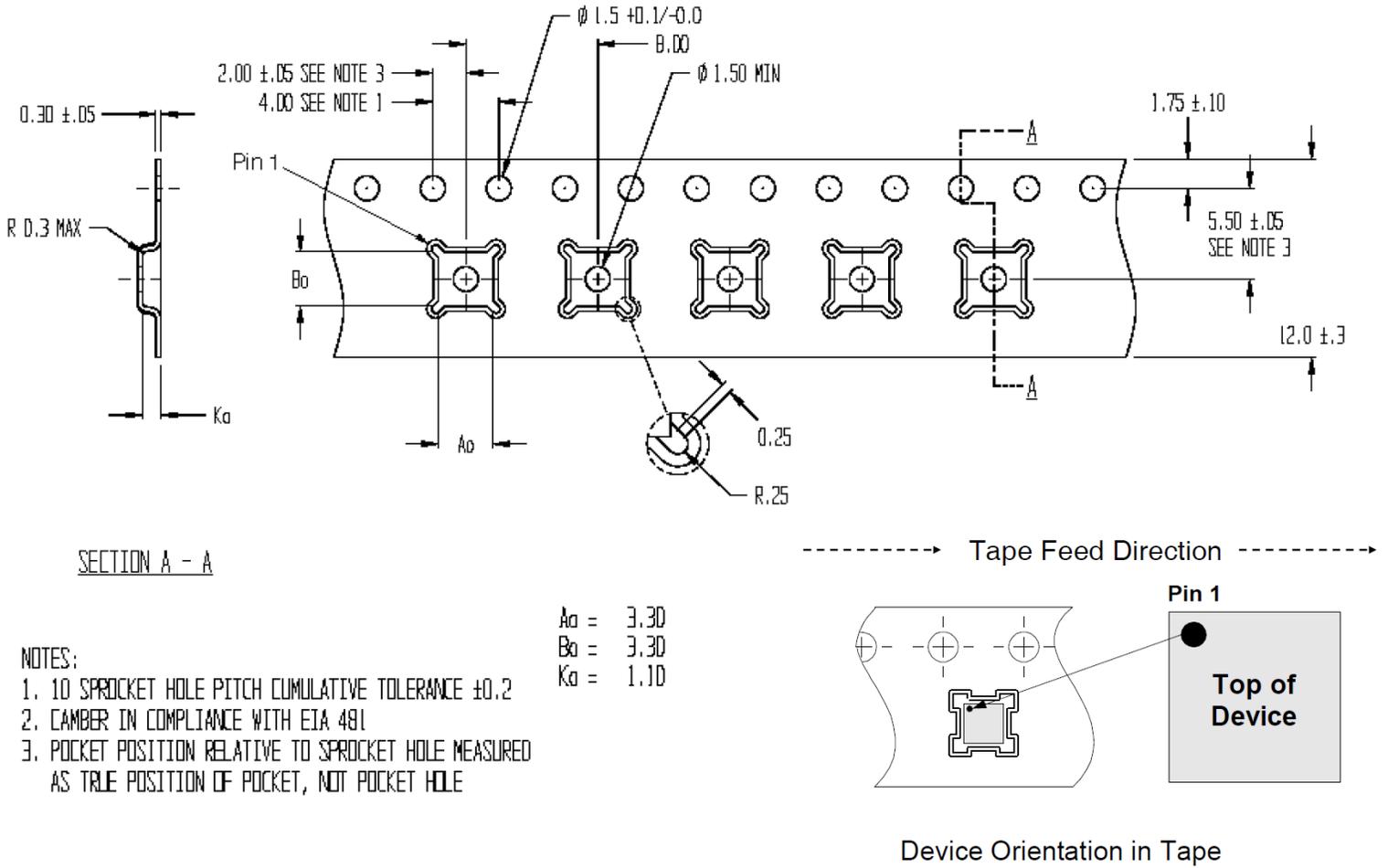


Figure 16. Tape and reel specification for the 12-lead 3×3 mm QFN package

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE43205B-Z	PE43205 digital step attenuator	Green 12-lead 3×3 mm QFN	3000 units/T&R
EK43205-2	PE43205 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
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