ACT43750

RF POL Drain-Switch Driver / Gate-bias Regulator

BENEFITS and FEATURES

- **Wide Operating Range**
  - Vin = 10V to 55V
  - Vgate = -6V to -1.5V
- **RF PA Biasing Solution**
  - Turn on and off sequencing
  - Negative gate voltage supply
  - Supports GaN and Silicon FETs
  - High-speed drain switching
  - Autonomous Bias Point Calibration
- **Autonomous $I_{DQ(DRAIN)}$ calibration**
  - Resistor Setpoint Range: 10mA to 2A
  - Digitally adjustable ±31% of setpoint in 1% steps
- **Space and Cost savings**
  - Fully integrated gate drive voltage
  - High switching frequency: 2.05 MHz
  - Integrated FETs and small chip inductor
  - 37-pin, 5 mm x 5 mm, 0.4-mm pitch QFN package
- **High-Performance Negative Gate Drive Supply**
  - REGG input voltage: +12V (TYP)
  - REGG output voltage: -6V to -1.5V by 732µV step
  - REGG output source current: 300mA
  - REGG output sink current: -100mA
  - REGG output noise: <200µVRMS
- **Protection**
  - UVLO, OVLO, OVP, UVP, OCP, TSD

APPLICATIONS

- Military Radar System
- Civilian Radar System
- RF GaN / GaAs PA Power Supply

GENERAL DESCRIPTION

The ACT43750, part of Qorvo's RF POL regulator family, is the last stage of a three-chip radar power supply solution. This three-stage solution, developed with the ACT43950, ACT43850, and ACT43750, forms a compact, complete power supply system for radio frequency (RF) power amplifiers (PAs) that demand fast transient, high current pulse loads. The first stage, ACT43950 converts a high voltage dc input voltage into a regulated dc constant-current (CC) to charge bulk capacitor. The second stage, ACT43850, regulates the capacitor voltage into a tightly regulated DC voltage to power the drain for GaN RF power amplifiers.

The third stage, ACT43750, provides several functions specifically designed to optimize GaN performance. It operates either standalone or as the third stage in a multiple stage power solution. It provides the RF PA negative gate voltage using an ultra-low noise inverting buck dc-to-dc regulator with integrated FETs and programmable voltage reference. It provides the required GaN power up and power down sequencing between the drain and gate voltages. All GaN RF PAs require calibrating the gate voltage to set the desired operating point. The ACT43750 automatically calibrates and stores the optimal gate voltage. This operating point changes with time and temperature. The IC can recalculate and adjust the optimal gate voltage in the field without waiting for a maintenance cycle. The ACT43750 also enables drain switching in pulsed radar applications.

The ACT43750 is available in a 37-pin, 5 mm x 5 mm, 0.4 mm pitch QFN package.

SYSTEM BLOCK DIAGRAM

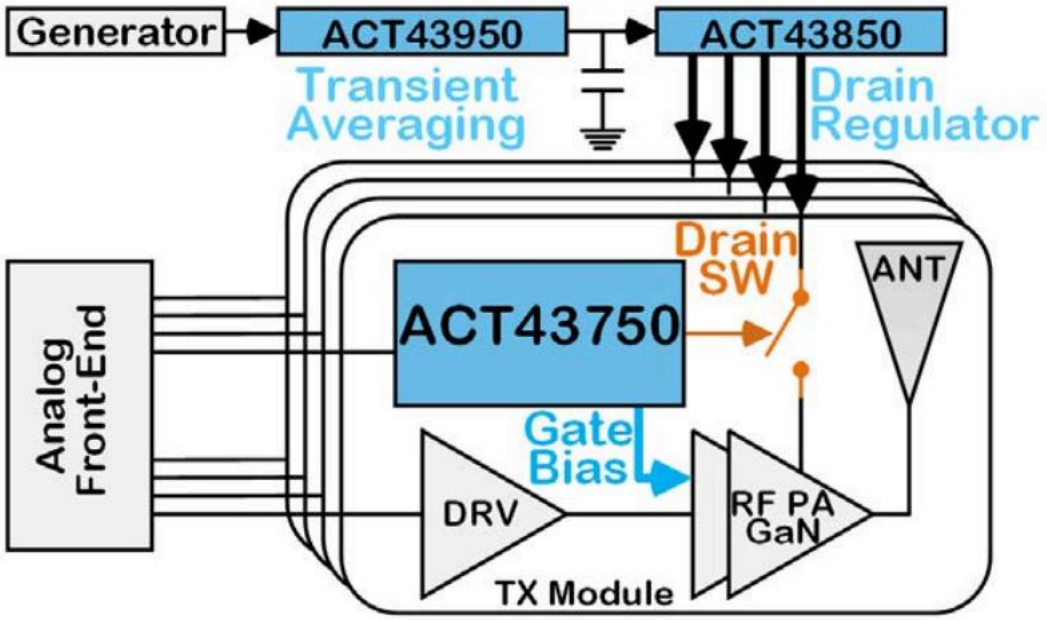


Figure 1. 3 Chip System Block Diagram

TYPICAL APPLICATION BLOCK DIAGRAM

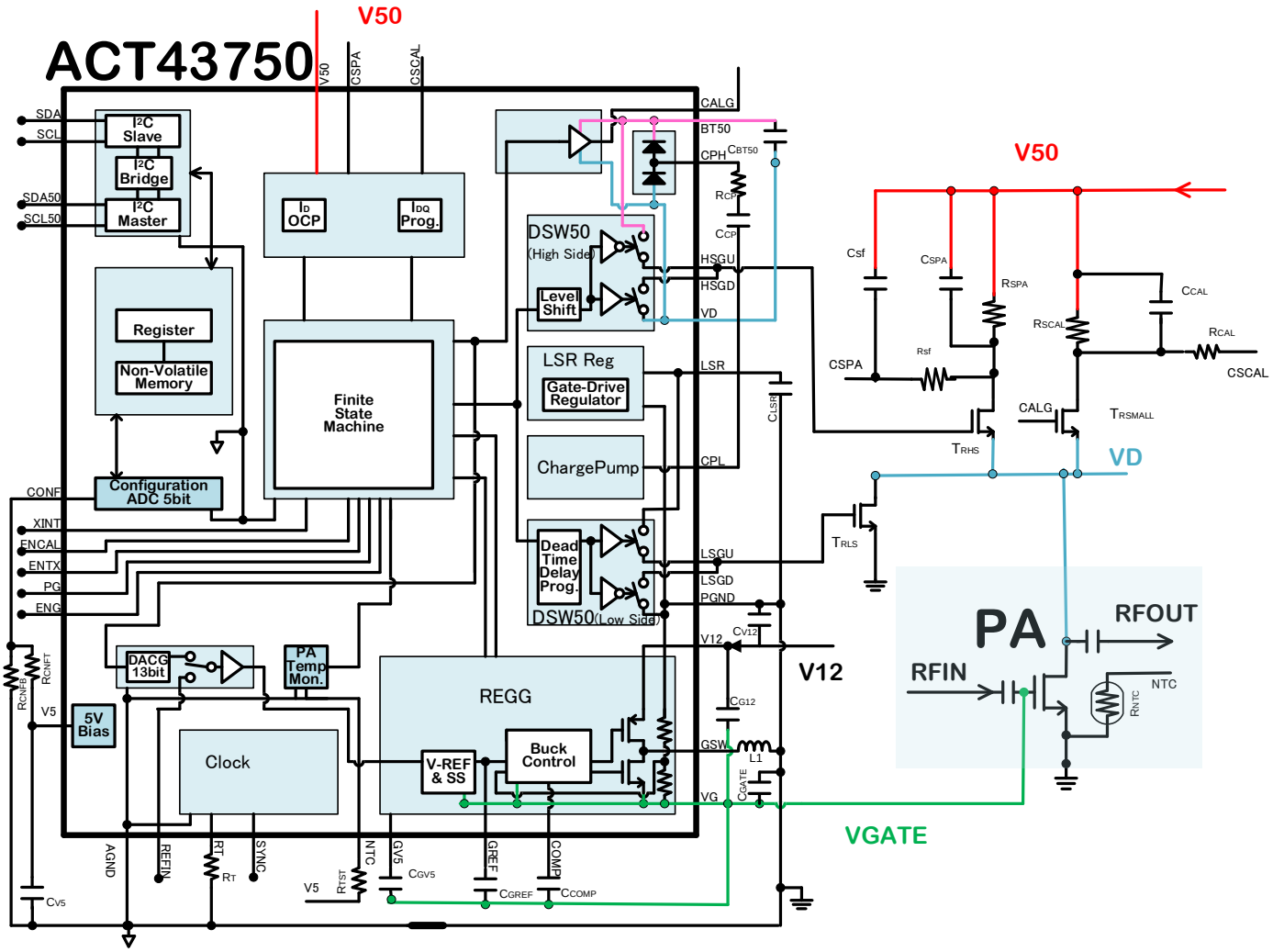
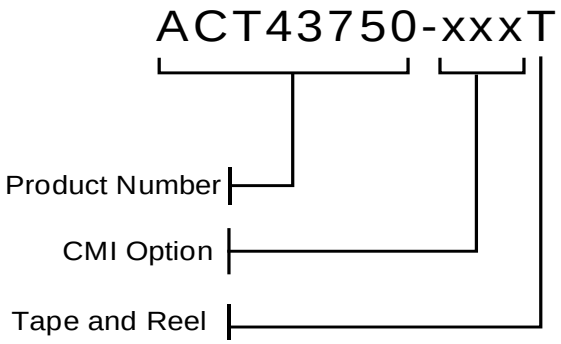


Figure 2. ACT43750 Typical Application Block Diagram

ORDERING INFORMATION

PART NUMBER	Min RF PA Gate Voltage	Max RF PA Gate Voltage	Power FET Type	Power FET Gate Voltage (LSR regulator)	Targeted Qorvo RFPA
ACT43750-101T	-4.5V	-1.5V	GaN	5V	Generic Use
ACT43750-102T (proposed functions)	-4.5V	-1.5V	Si	10V	Generic Use



Note 1: Standard product options are identified in this table. Contact the factory for custom options, a minimum order quantity is required.

Note 2: “xxx” represents the CMI (Code Matrix Index) option The CMI identifies the IC’s default register settings.

PIN CONFIGURATION

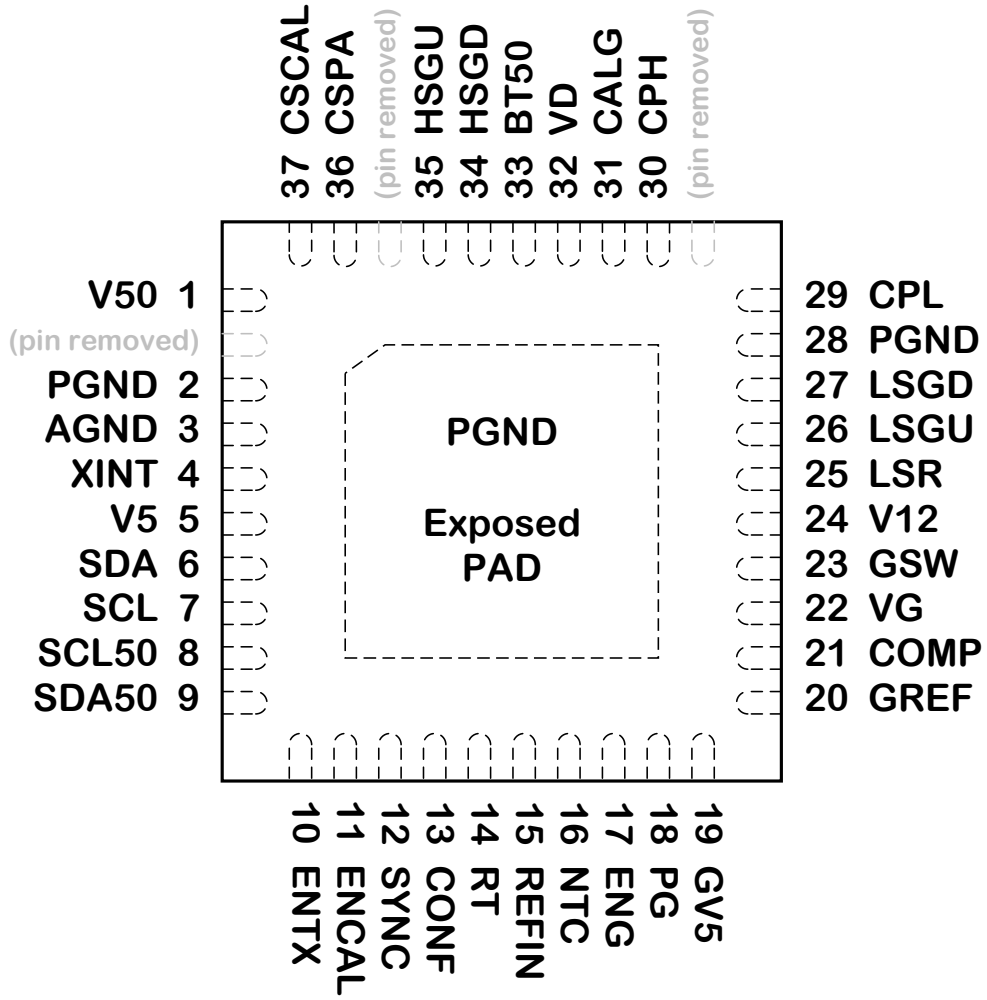


Figure 3: Pin Configuration – Top View – 37 pin QFN, 5 mm x 5mm, 0.4 mm pitch

PIN DESCRIPTIONS

Pin	NAME	DESCRIPTION
1	V50	Input power to the DSW50 control section of the IC.
2, 28	PGND	Dedicated power ground for the DSW50 gate drive. Connect to AGND with a Kelvin connection.
3	AGND	Ground pin for the analog blocks. Connect to PGND with a Kelvin connection.
4	XINT	Interrupt output. Open drain. Connect it through a pull-up resistor to V5.
5	V5	5V Bias regulator output. Requires a 2.2uF capacitor to AGND
6	SDA	I^2C Data Pin for Slave mode
7	SCL	I^2C Clock Pin for Slave mode
8	SCL50	I^2C Data Pin for Master mode
9	SDA50	I^2C Clock Pin for Master mode
10	ENTX	Enable input for the DSW50 block. Don't float this pin. Connect it through a 100kΩ resistor to AGND. ENTX pin needs to be logic low when startup.
11	ENCAL	Enable input to start an autocalibration routine. Don't float this pin. Connect it through a 100kΩ resistor to AGND.
12	SYNC	External clock synchronization input
13	CONF	External configuration resistor input. Connect a resistor between CONF and V5 and between CONF and AGND to configure IC settings.
14	RT	Sets the negative gate voltage switching frequency. Connect a resistor between RT and AGND.
15	REFIN	External voltage reference input. Leave open if not used.
16	NTC	Negative temperature coefficient resistor input.
17	ENG	Enable input for the REGG block (negative voltage regulator). Don't float this pin. Connect it through a 100kΩ resistor to AGND.
18	PG	Power good output. Open drain. Connect it through a pull-up resistor to V5.
19	GV5	Floating negative gate voltage output. Connect a 2.2uF capacitor between GV5 and VG.
20	GREF	The local voltage reference for the REGG output. Connect a 100nF capacitor between GREF and VG.
21	COMP	Compensation input. Connect a 470pF capacitor between COMP and VG.
22	VG	Feedback input for the REGG output. Connect a 10nF capacitor between VG and V12.
23	GSW	REGG switching node.
24	V12	External 12V bias input pin. Connect a 10uF capacitor between V12 and PGND. Connect a 10nF capacitor between V12 and VG.
25	LSR	Low-side gate drive regulator for the DSW50 block. Connect a 2.2uF capacitor between LSR and PGND.
26	LSGU	Pullup output for the low-side FET gate.
27	LSGD	Pulldown output for the low-side FET gate.
29	CPL	High-side gate drive regulator flying capacitor terminal. Connect a 47nF capacitor and a 33Ω resistor in series between CPL and CPH.
30	CPH	High-side gate drive regulator flying capacitor terminal. Connect a 47nF capacitor and a 33Ω resistor in series between CPH and CPL.
31	CALG	Calibration FET gate output.
32	VD	DSW50 output voltage for the high side FET. Connect a 10uF capacitor between VD and BT50.
33	BT50	High-side gate drive regulator bootstrap output. Connect a 10uF capacitor between BT50 and VD.
34	HSGD	Pulldown output for the high-side FET gate.
35	HSGU	Pullup output for the high-side FET gate.
36	CSPA	Overcurrent sense resistor input for the drain FET
37	CSCAL	Calibration current sense resistor input for the calibration FET.
-	Exposed PAD	Exposed thermal pad. Connect directly to PGND.

ABSOLUTE MAXIMUM RATINGS (NOTE 1) (NOTE 2)

Parameter	Value	Unit
V_{50}	-0.3 to +65	V
V_{CSPA}, V_{CSCAL} (Referenced to V_{50})	-5 to +0.3	V
V_{BT50} (Referenced to V_D)	-0.3 to +10	V
V_D	-0.3 to (V_{50} + 0.3)	V
V_{12}	-0.3 to +15.0	V
V_{SDA}, V_{SCL}, V_{SCL50}, V_{SDA50}, V_{ENCAL}, V_{ENG}, V_{PG}, V_{XINT}, V_{ENTX}, V_{SYNC}, V_{NTC}, V_{REFIN}, V_{CONF}	–0.3 to +6.0	V
V_G	–10.0 to +0.3	V
V_{GSW} – with respect to V_G	–0.3 to ($\|V_{12} – V_{PGND}\|$ + 0.3)	V
V_{AGND} to V_{PGND}	–0.3 to +0.3	
Junction to Case Thermal Resistance (Note 3)	6.03	°C/W
Junction to Ambient Thermal Resistance (Note 3)	24.37	°C/W
Operating Junction temperature	-40 to 125	°C
Storage temperature	-55 to 150	°C
V_ESD_HBM (All pins) (Human body model per JEDEC JS-001)	2500	V
V_ESD_CDM (All pins) (Charged device model JEDEC JS-002)	1250	V
MSL	MSL3	

Note 1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Note 2: All voltages with respect to PGND unless otherwise noted.
Note 3: Measured on Qorvo Evaluation board, which has 1oz copper and 163.5mm x 229mm board area.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Typ.	Max.	Units
V_{12}: Supply voltage	+10.8	+12.0	+13.2	V
V_{50}: Supply voltage	+10.0		+55	V
V_{CSPA}, V_{CSCAL}, V_D: DSW50 block voltage	0		V50	
IO(V5): V5 bias output current			20	mA
V_{REFIN}, V_{NTC}, V_{CONF}: Analog input voltage	0		+5.0	V
V_{ENCAL}, V_{ENG}, V_{ENTX}, V_{SYNC}: Logic input voltage	0		+5.5	V
V_{SDA}, V_{SCL}, V_{PG}, V_{XINT}: Open-drain pull-up voltage	+3.3		+5.5	V
$I_{OL(SDA)}$, $I_{OL(SDA50)}$, $I_{OL(SCL50)}$, $I_{OL(PG)}$, $I_{OL(XINT)}$: Current into open-drain pins			+1	mA
L_1: REGG output filter coil value		6.8		µH
C_{GATE}: REGG output filter capacitor value		22		µF
C_{COMP}: REGG loop compensation capacitance		470		pF
R_{RT}: REGG switching frequency programming resistance		120		kΩ
$C_{TOTAL(SCL50)}$, $C_{TOTAL(SDA50)}$: Total bus-node capacitance			400	pF

All voltage values are to ground unless otherwise specified. The AGND and PGND pins are shorted together with the shortest PCB traces.

ELECTRICAL SPECIFICATIONS

V_D = V50 = 50V, V12 = 12V, VG = –2.5V, V_{BT50} = 55.2V, V_{SCL} = V_{SDA} = V_{ENCAL} = V_{ENG} = V_{ENTX} = V_{SCL50} = V_{SDA50} = V_{NTC} = 5V, V_{REFIN} = 0V, T_A = –40 to +125 °C, unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
Supply Rails, System Main						
$I_{Q(V12)}$	V12 Standby Current	V_{SDA}=V_{SCL}=V_{ENTX}=V_{ENCAL}=V_{ENG}=0V		1.5		mA
$I_{I(V12)}$	V12 Consumption Current			4		mA
$V_{IT+(OV12)}$	V12 Input Over Voltage		14			V
$V_{IT-(UV12)}$	V12 Input Under Voltage				10	V
$I_{I(V50,H)}$	V50 Consumption Current	VD = 50V		200		µA
$I_{I(V50,L)}$	V50 Consumption Current	VD = 0V		200		µA
$V_{IT+(OV50)}$	V50 Input Over Voltage		65			V
$V_{IT+(UV50)}$	V50 Input Under Voltage				10	V
T_{SD}	Thermal Shutdown	T_J, die temperature rising to disable		160		°C
$T_{SD(OFF)}$	Thermal Shutdown Release	T_J, die temperature falling to enable		145		°C
T_{WARN}	Thermal Warning	T_J, die temperature warning		140		°C
REFERENCE SYSTEM						
V_5	V5 Bias Regulator Output Voltage	$I_{O(V5)}$ = 0 to 20 mA	4.85	5	5.15	V
$R_{PD(REFIN)}$	REFIN Input Pull-down Resistance	REFIN to AGND		100		kΩ
V_{GREF}/V_{REFIN}	REFIN to GREF Conversion Ratio (ratio of the floating reference voltage to the external reference voltage)	(V_{GREF} - V_G)/(V_{REFIN} – V_{AGND}), external reference level-shift gain		+1		
$\Delta(V_{GREF}/V_{REFIN})$	REFIN to GREF Conversion Ratio	(V_{GREF} - V_G)/(V_{REFIN} – V_{AGND}), V_{REFIN} = 0.75 V and 3.0 V	99%		101%	
V_{GREF}/V_{DACG}	VDACG to GREF Conversion Ratio (ratio of the floating reference voltage to the DAC voltage)	(V_{GREF} - V_G)/(V_{DACG} – V_{AGND}), internal DAC level-shift gain		+1		
$V_{REFIN(MAX)}$	REFIN Window-comparator Threshold	High-side valid input window		3.0		V
$V_{REFIN(MIN)}$	REFIN Window-comparator Threshold	Low-side valid input window, Below device-internal DACG value		V_{DACG}		
$V_{GREF, DAC 100\%}$	DACG Reference Accuracy	Monitor V_{GREF} V_G w.r.t. DACG[12:0] = 0x1FFFh	2.925	3.00	3.075	V
$V_{GREF, DAC25\%}$	DACG Reference Accuracy	Monitor V_{GREF} V_G w.r.t. DACG[12:0] = 0x0400h	0.735	0.75	0.765	V
$\Delta_{VGREF, DAC}$	DACG Reference Accuracy	V_{GREF} difference DACG[12:0] code from “N-1” to “N”	0	+ 366		µV

Parameter		Conditions	Min	Typ	Max	Units
$V_{T+(GREF,chg)}$	GREF $I_{o(GREF)}$ Fast-Charge Upper Threshold	((Internal reference) – V_{GREF}) threshold to use $I_{o(GREF)}$ fast-charging. And hysteresis points to exit. See Reference Voltage Noise Reduction.		> +35		mV
$V_{T+(GREF, hys)}$	GREF $I_{o(GREF)}$ Fast-Charge Upper Hysteresis			<+20		mV
$V_{T-(GREF, chg)}$	GREF $I_{o(GREF)}$ Fast-Charge Lower Threshold			<-35		mV
$V_{T-(GREF, hys)}$	GREF $I_{o(GREF)}$ Fast-Charge Lower Hysteresis			>-20		mV
$R_{o(GREF, chg)}$	GREF $I_{o(GREF)}$ Fast-Charge Output Resistance	During $I_{o(GREF)}$ fast-charging		480		Ω
$R_{o(GREF)}$	GREF Output Resistance	0xEh [3:2] = 00		0.5		kΩ
		0xEh [3:2] = 01		4.5		kΩ
		0xEh [3:2] = 10		25		kΩ
		0xEh [3:2] = 11		250		kΩ
$I_{O(GREF)}$	GREF Pre-Charge Current	0xEh [1:0] = 00		5		µA
		0xEh [1:0] = 01		10		µA
		0xEh [1:0] = 10		100		µA
		0xEh [1:0] = 11		200		µA
V_{LSR}	LSR Voltage Reference	All 0x0Fh [3:0] options	-5%		+5%	V
I²C Slave for MCUs/Controllers						
$V_{IT+(SCL)}$,$V_{IT+(SDA)}$	SCL, SDA Input Threshold	Falling edge for H_{LOGIC}			0.55	V
$V_{IT-(SCL)}$,$V_{IT-(SDA)}$		Rising edge for H_{LOGIC}	1.25			V
$I_{LKG(SDA)}$	SDA Leakage Current	VSDA = 5V			1	µA
$V_{OL(SDA)}$	SDA Output Voltage	5mA Current into SDA pin			0.35	V
$C_{I(SCL)}$, $C_{I(SDA)}$	SCL, SDA Terminal Capacitance				10	pF
I²C Master for ACT43850 and External Memory						
$V_{IT+(SDA50)}$	SDA50 Input Threshold	Falling edge for H_{LOGIC}			0.55	V
$V_{IT-(SDA50)}$		Rising edge for H_{LOGIC}	1.25			V
$I_{LKG(SCL50)}$ $I_{LKG(SDA50)}$	SCL50, SDA50 Leakage Current	V_{SCL50} = V_{SDA50} = 5 V			1	µA
$V_{OL(SCL50)}$ $V_{OL(SDA50)}$	SCL50, SDA50 Output Voltage	5mA Current into SDA50 and SCL50 pins			0.35	V
$C_{I(SCL50)}$, $C_{I(SDA50)}$	SCL50, SDA50 Terminal Capacitance				10	pF
$R_{PU(SDA50)}$,$R_{PU(SCL50)}$	SDA50, SCL50 Pull-up Resistance	Internal pull-up	3.3			kΩ

Parameter		Conditions	Min	Typ	Max	Units
Logic I/O						
$V_{OL(PG)}$,$V_{OL(XINT)}$	PG, XINT Output Voltage	1 mA Current into the device from the PG, XINT pin		0.4		V
$V_{IT+(SYNC)}$	SYNC Input Threshold	V_{SYNC} rising edge detection	1.425	1.5	1.575	V
$V_{HYS(SYNC)}$	SYNC Input Hysteresis	V_{SYNC} falling edge detection		-0.1		V
V_{IT+}	ENCAL, ENG, ENTX, PG Input Threshold	Rising edge for H_{LOGIC}	1.25			V
V_{IT-}	ENCAL, ENG, ENTX, PG Input Threshold	Falling edge for H_{LOGIC}			0.55	V
Signal Pin I/O						
$V_{IT-(NTC)}$	NTC Input Threshold	Falling to detect over temp, ratio to V_{V5}	28%*V_{V5}	30%*V_{V5}	32%*V_{V5}	V
$V_{IT+(NTC)}$	NTC Input Threshold	Rising to recover, hysteresis		0.1		V
$V_{IT+(CSCAL)}$	CSCAL Comparator Threshold Voltage	IDQAdj[5:0]=0x00h, (V_{50}-V_{CSCAL}), T_A = 25 °C	-1%	1.5	+1%	V
		IDQAdj[5:0]=0x00h, (V_{50}-V_{CSCAL})	-2%	1.5	+2%	V
ΔV_{CSCAL}	CSCAL Threshold Programming Resolution			15		mV/Step
N_{CSCAL}	CSCAL Threshold Programming Steps		-31		+31	Steps
$V_{DIS(V50)}$	V50 Discharge Detection Threshold	(V50 – V_{CSCAL})		0.4		V
$V_{IT+(CSPA)}$	CSPA Input Threshold	Rising to detect PA drain over current	30	35	40	mV
$V_{HYS(CSPA)}$	CSPA input hysteresis	Falling to release		-20		mV
DSW50 Gate Drivers						
$R_{PU(HSGU)}$	HSGU High-side Driver Pull-up Output Resistance			2	4	Ω
$R_{PD(HSGD)}$	HSGD High-side Driver Pull-down Output Resistance			1	2	Ω
$R_{PU(LSGU)}$	LSGU Low-side Driver Pull-up Output Resistance			2	4	Ω
$R_{PD(LSGD)}$	LSGD Low-side Driver Pull-down Output Resistance			1	2	Ω
REGG Regulator System						
V_G/V_{GREF}	GREF to V_G Conversion Ratio (ratio of the gate voltage to the floating reference voltage)	(V_G – V_{PGND}) / (V_{GREF} – V_G) gain of REGG as VG floating circuit. V_G is referenced to PGND and V_{GREF} is referenced to V_G.		-2		
V_G	VG Feedback Voltage Accuracy		-1%		+1%	V
$V_{IT-(PG)}$	PG Detection Threshold	Ratio of (V_G – V_{PGND}) / (V_{GREF} – V_G)	89.5	92		%
$V_{HYS(PG)}$	PG Detection Hysteresis			0.8		%
I_{OCP}	REGG Over Current Protection			1		A
$V_{IT-(OVP)}$	VG Over Voltage Protection	Ratio of (V_G – V_{PGND}) / (V_{GREF} – V_G)		106.5	109.5	%
$V_{IT+(UVP)}$	VG Under Voltage Protection	Ratio of (V_G – V_{PGND}) / (V_{GREF} – V_G)	89	91		%

Parameter		Conditions	Min	Typ	Max	Units
Clock System						
f_{SYNC}	SYNC Clock Input Frequency Range	Difference from the target set by R_{RT}	-20		+20	%
D_{SYNC}	SYNC Clock Input Pulse Duty Cycle		40		60	%
I²C Slave for MCUs/Controllers						
f_{SCL}	SCL Clock Frequency	(no internal time out)	0		1000	kHZ
$t_{LOW(SCL)}$	SCL Pulse Width, Low		0.5			µs
$t_{HIGH(SCL)}$	SCL Pulse Width, High		0.26			µs
$t_{SU(SDA)}$	SDA Set-up Time		50			ns
$t_{H(SDA)}$	SDA Hold Time		0			ns
$t_{FALL(SDA)}$	SDA Fall Time	SDA pull-up to 5V source via 10kΩ			120	ns
$t_{SU(START)}$	I²C START Set-up Time		260			ns
$t_{SU(STOP)}$	I²C STOP Set-up Time		260			ns
I²C Master for ACT43850 and external I²C Memory						
$t_{FALL(SDA50)}$	SDA50 Fall Time	Slave devices (ACT43850 and external I²C memory) driving SDA50			120	ns
Logic I/F						
$t_{L(Logic)}$ (Note 1)	ENCAL, ENG, ENTX, PG Pulse Width, Low	Minimum pulse width	40			µs
$t_{H(ENTX)}$ (Note 1)	ENTX Pulse Width, High	Minimum pulse width	12			µs

Note 1, Operating below the minimum pulse width moves the IC to the Error Bias State. To return to normal operation, turn off the drain supply voltage and bias voltage, then power up normally.

V_D = V50 = 50V, V12 = 12V, VG = –2.5V, V_{BT50} = 55.2V, V_{SCL} = V_{SDA} = V_{ENCAL} = V_{ENG} = V_{ENTX} = V_{SCL50} = V_{SDA50} = V_{NTC} = 5V, V_{REFIN} = 0V, T_A = –40 to +125 °C, unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
I²C Master for ACT43850 and external I²C memory						
f_{SCL50}	SCL50 Output Clock Frequency	0x17h [3:2] = 00		100		kHz
		0x17h [3:2] = 01		200		kHz
		0x17h [3:2] = 10		333		kHz
		0x17h [3:2] = 11		1000		kHz
$t_{LOW(SCL50)}$	SCL50 Pulse Width, Low			50% x ($1/f_{SCL50}$)		µs
$t_{HIGH(SCL50)}$	SCL50 Pulse Width, High			50% x ($1/f_{SCL50}$)		µs
$t_{SU(SDA)}$	SDA50 Set-up Time			25% x ($1/f_{SCL50}$)		ns
$t_{H(SDA)}$	SDA50 Hold Time			25% x ($1/f_{SCL50}$)		ns
$t_{SU(START50)}$	I²C START Set-up Time			50% x ($1/f_{SCL50}$)		ns
$t_{SU(STOP50)}$	I²C STOP Set-up Time			50% x ($1/f_{SCL50}$)		ns
I_{DRAIN} Calibrator						
$N_{AUTOCal}$	Delta-calibration Automatic Re-Calibration Cycles			100		cycle
DSW50 Gate Drivers						
t_{DEAD}	Deadtime range (note 1)		-30		100	ns
$t_{R(HSGU)}$	HSGU Turn ON Time	10% to 90%, no gate resistor $C_{GATE(FET)}$ = 1.3nF		15		ns
$t_{F(HSGD)}$	HSGD Turn OFF Time	90% to 10%, no gate resistor, $C_{GATE(FET)}$ = 1.3nF		8		ns
$t_{R(LSGU)}$	LSGU Turn ON Time	10% to 90%, no gate resistor $C_{GATE(FET)}$ = 1.3nF		15		ns
$t_{F(LSGD)}$	LSGD Turn Off Time	90% to 10%, no gate resistor, $C_{GATE(FET)}$ = 1.3nF		8		ns
t_D(CAL-TX)	Wait Time before ENTX Ready	(Internal calibration comp) to ENTX ready		10		ms
$t_{D(HSGU)}$	HSGU Propagation Delay	ENTX ↑ to HSGU = H		100		ns
$t_{D(LSGU)}$	LSGU Propagation Delay	ENTX ↓ to LSGU = L		100		ns
$t_{D(PG, Rise)}$	PG Propagation Delay	From internal PG detection to V_{PG} up		5		µs
$t_{D(PG, Fall)}$	PG Propagation Delay	From internal PG detection to V_{PG} down		0.2		µs

V_D = V50 = 50V, V12 = 12V, VG = –2.5V, V_{BT50} = 55.2V, V_{SCL} = V_{SDA} = V_{ENCAL} = V_{ENG} = V_{ENTX} = V_{SCL50} = V_{SDA50} = V_{NTC} = 5V, V_{REFIN} = 0V, T_A = –40 to +125 °C, unless otherwise specified

REGG Regulator System						
$f_{sw(MIN)}$	REGG Minimum Switching Frequency	R_{RT} = 215kΩ	-5%	1080	+5%	kHz
$f_{sw(MAX)}$	REGG Maximum Switching Frequency	R_{RT} = 115kΩ	-10%	2050	+10%	kHz
f_{SPSP}	REGG Spread-Spectrum Dithering Range			+/-7		%
N_{SPSP}	REGG Spread-Spectrum Cycle			64		cycle
$t_{MIN(GSW)}$	GSW Output Pulse, MIN			50		ns
$t_{MAX(GSW)}$	GSW Output Pulse, Max			50% x ($1/f_{SW}$)		
$t_{H(GREF)}$	GREF Holding Time	Operation change from $I_{O(GREF)}$ to $R_{O(GREF)}$		5		ms
f_C	Unity Gain Frequency/Loop Bandwidth			10% f_{sw}		Hz
PM	Phase Margin		45°			
Gain	100 Hz Gain		60			dB

Note 1:Specified as a device internal logic delay, not an actual dead time at the VD pin

OVERVIEW

General

The ACT43750 is a highly integrated power and sequencing solution for RF GaN FET radar applications. Its functionality is optimized for driving GaN FETs in RF applications. It supports both continuous and pulsed drain voltages between 10V and 55V. The DSW50 block controls two switching FETs that apply power to the RF PA. These two FETs work in a half-bridge topology to support fast drain-switching radar applications. The Drain FET applies the drain voltage to the RF PA, and the bottom FET quickly turns it off by pulling the drain voltage to the ground. The ACT43750 provides synchronized timing to prevent shoot-through. The DSW50 block supports standard silicon and GaN power FETs. The REGG block converts a positive 12V bias voltage into the RF PA's negative gate voltage using a low-noise inverting buck regulator with integrated switching FETs. The REGG block also includes an autonomous autocalibration routine that finds the optimum gate voltage that biases the RF PA at the proper bias quiescent current, Idq. This fully automated procedure eliminates the system-level design's need for discrete calibration circuitry. The autocalibration routine can be run at any time to compensate for changes in RF PA performance due to aging, temperature, or voltage changes. The DSW50 and REGG circuitry work together to provide the RF PA gate and drain voltage sequencing required to prevent RF PA damage at turn-on and turn-off. The ICs contain an I²C slave bus that allows the user to dynamically change the IC's settings. It also contains an I²C master, which controls companion devices ACT43850 and external I²C memory, on the sub-I²C bus. The IC also contains protection circuitry to prevent RF PA damage in the event of temperature, RF power, bias power, and current faults.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT43750 uses standard I²C commands. The ACT43750 contains two separate I²C buses. One operates as a Master, and one operates as a Slave. There is no timeout function in the I²C packet processing state machine; however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

I²C slave commands are communicated using the SCL and SDA pins. The I²C master commands are communicated using the SCL50 and SDA50 pins. All pins are open drain, so the user must use external pullup resistors. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

Slave Address

The I²C slave functions allow customers to read the IC register settings, read device status, and change register settings to adjust the IC's behavior. Refer to Qorvo's ACT43750 Register Definition Application Note for more details about each register's function.

The Slave functions are accessed using a 7-bit slave address followed by an eighth bit, indicating whether the transaction is a read or write operation. The IC supports 16 slave addresses to provide flexibility to populate many ICs on the same I²C bus. The IC's 7-bit slave address is a function of both the IC's CMI and external component settings. The first two bits of the slave address are fixed at 0x01b. The IC's CMI sets bit 5 with register bit 0x11h [3]. Bit 4 is always 0. I²C register 0x11h [2:0] defines the last three bits. The last three bits are set at startup by the RCONF resistors. Table 1 shows all available I²C slave address options.

Table 1. ACT43750 I²C Addresses

7-Bit Slave Address		8-Bit Read Address	8-Bit Write Address
0x20h	010 0000b	0x40h	0x41h
0x21h	010 0001b	0x42h	0x43h
0x22h	010 0010b	0x44h	0x45h
0x23h	010 0011b	0x46h	0x47h
0x24h	010 0100b	0x48h	0x49h
0x25h	010 0101b	0x4Ah	0x4Bh
0x26h	010 0110b	0x4Ch	0x4Dh
0x27h	010 0111b	0x4Eh	0x4Fh
0x30h	011 0000b	0x60h	0x61h
0x31h	011 0001b	0x62h	0x63h
0x32h	011 0010b	0x64h	0x65h
0x33h	011 0011b	0x66h	0x67h
0x34h	011 0100b	0x68h	0x69h
0x35h	011 0101b	0x6Ah	0x6Bh
0x36h	011 0110b	0x6Ch	0x6Dh
0x37h	011 0111b	0x6Eh	0x6Fh

Master Address

The ACT43750 provides a Master I²C bus that gives the system additional flexibility to automatically control and adjust IC functionality that can optimize RF PA functionality in the system. Examples include using an external memory IC containing a lookup table to automatically adjust the voltages and currents. The Master can perform the following functions.

- Scans to check if companion devices are on the Master I²C bus.
- Enable and disable the ACT43850 companion IC.
- Provide bypass control from a system-host, through the ACT43750 to the ACT43850.
- Program or adjust the ACT43850 output voltage. This is the RF PA drain voltage.
- Read an external I²C memory IC to set the ACT43850 output voltage.
- Read an external I²C memory IC to set the ACT43750 Idq calibration current.
- Read an external I²C memory IC to set the ACT43750 negative gate voltage.

A system host, via the I²C Slave, can turn ON or OFF the I²C master block using register 0x17h [1]. The host can also change the I²C master clock speed using register 0x17h [3:2].

Scanning for I²C Companion Devices

The IC automatically scans for I²C slave devices on the Master bus when the state machine enters the REG50 Ramp state. The Master bus can only have a single ACT43850 connected. It can also have a single I²C memory device connected. If an ACT43850 slave device is found, the IC sets register 0x99h [0] = 1 and stores the slave's I²C address in register 0x98 [7:1]. If an I²C memory device is found, the ACT43750 sets register 0x99h [1] to 0.

I²C Bypass

The ACT43750 provides an I²C bridge logic between the I²C Slave and the I²C Master blocks. A system host can turn on the bypass function by setting register 0x17h [0] = 1. In bypass mode, the ACT43750 will pass-through commands from the system host on the Slave bus (SDA, SCL), to the ACT43850 on the Master bus(SDA50, SCL50). It also transfers the ACT43850 responses back to the system host.

To avoid communication issues, when the ACT43750 executes I²C on the Master bus, it sets register 0x99h [2] = 1 to let the system host know that it must wait until the Master bus communication is complete. When the Master bus communication is complete, the IC clears this bit.

Device initialization /configuration

The ACT43750 provides multiple layers/steps to select its configuration and operation modes. At startup, the IC reads internal I²C registers and external component values to configure its operation. After startup, users can change functionality by changing the internal register settings with standard I²C commands.

Factory Programming Options / CMI I2C Registers

The ACT43750 contains several 8-bit registers that are preprogrammed at the factory. The default register values are set at the factory. These default values are referred to as the CMI (Code Matrix Index), and they are stored in non-volatile memory (NVM). Each different CMI is referred to by a three-digit number which results in a unique orderable part number. The I²C registers can be changed via the I²C Slave bus. Refer to the ACT43750 Register Definition Application Note for more details about the available register settings. Examples of functionality that can be changed via I²C are below. Refer to the Register Map Application Note for more details.

Table 2. ACT43750 I²C Functions

IC Function	Register
REGG output voltage range and resolution	0x06h-0x07h
Spread-spectrum behavior details	0x10h
External and internal clock synchronization	0x11h
Internal clock oscillator output control	0x11h
External clock synchronization polarity selection	0x11h
DSW50 dead-time control adjustment	0x12h
LSR voltage (power FET gate voltage)	0x0Fh
RSCAL calibration target adjustment	0x13h
Internal or external reference selection	0x0Fh
Interrupt Mask	0x09h-0x0Ah
REGG soft-start time	0x0Eh
Power good delay time	0x10h

External Configuration Resistors

The ACT43750 contains additional functionality programmed with external resistors connected to the CONF pin. During power-up, the ACT43750 uses a five-bit analog-to-digital converter (5-bit ADC) to read the voltage at the CONF pin. It calculates the voltage on CONF as a percentage of the V5 voltage (typically 5V) and generates a 5-bit output. The resulting 5 bits (RCONF[4:0]) overwrite the default bits except bit [3] in register 0x11h resulting in modified functionality from the default CMI settings. The external configuration resistors change the following functionality.

- Sets the clock as a master or slave
- Enables or disables the SYNC pin as an output in slave mode
- Sets the SYNC pin input polarity as rising or falling edges when in slave mode
- Sets the Slave I²C Address

Not all the RCONF[4:0] bits translate directly into the bits in register 0x11h. Table 3 shows how each 0x11h register bit is populated after startup.

Table 3. Register 0x11 Bits

Register 0x11h Bit	RCONF[4:0] bit
0x11h Bit 7	Not used
0x11h Bit 6	RCONF[4]
0x11h Bit 5	RCONF[3]
0x11h Bit 4	RCONF[3]
0x11h Bit 3	Set by the default CMI
0x11h Bit 2	RCONF[2]
0x11h Bit 1	RCONF[1]
0x11h Bit 0	RCONF[0]

Refer to Table 5 and the ACT43750 register definition application note for details. Shorting CONF to ground disables the CONF startup routine and keeps the default register values.

Figure 4 shows the CONF resistor connection, and Table 5 shows the required resistor divider values and the resulting 5-bit binary value.

I2C Slave Address

The 7-bit I²C Slave address is generated by a combination of fixed values, a default register setting defined by the CMI, and the RCONF values. The table 4 shows how the 7-bit I²C Slave address is generated. It is a simplified version of Table 5

Table 4. 7-Bit I2C Slave Address Bits

7–Bit I2C Slave Address Bits	
Bit 7	Always = 0
Bit 6	Always = 1
Bit 5	= Reg11[3]
Bit 4	Always = 0
Bit 3	=Reg11[3]=RCONF[2]
Bit 2	=Reg11[2]=RCONF[1]
Bit 1	=Reg11[1]=RCONF[0]
Bit 0	I2C Read/Write Bit

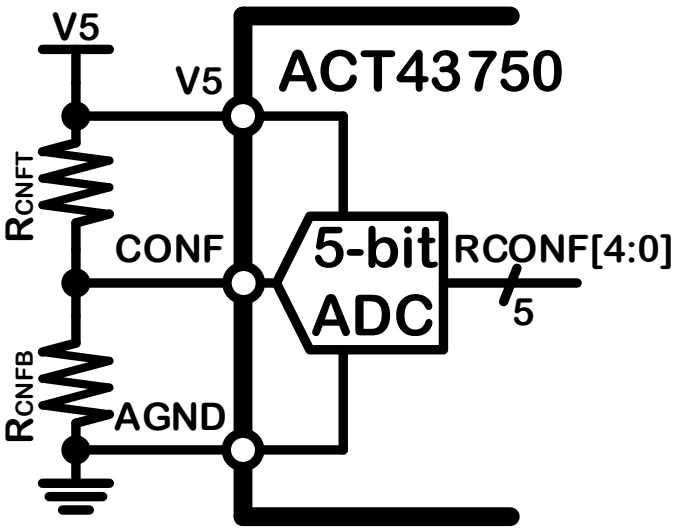


Figure 4. The CONF Pin Connection

Table 5. Register-wise RCONF[4:0] assignments, R_{CNFT} & R_{CNFB} and 7-bit I²C Slave Address

ADC Binary Target Value RCONF[4:0]	R_{CNFT} (kΩ)	R_{CNFB} (kΩ)	V_{CONF}/V5 (%)	Clock Master Slave Setting, reg11[6]	SYNC Pin Setting, reg11[5]	Slave Clock Polarity, reg11[4]	7-bit I2C Slave Address, reg11[2:0] (Note 1) (Note 2)
00000b	(open)	(short)	0.00	Master	No output	n/a. The clock is not a slave	
00000b	715	11.5	1.58				01# 0000_
00001b	1150	36.5	3.08				01# 0001_
00010b	1150	56.2	4.66				01# 0010_
00011b	422	28.7	6.37				01# 0011_
00100b	422	36.5	7.96				01# 0100_
00101b	1100	115	9.47				01# 0101_
00110b	866	115	11.72				01# 0110_
00111b	649	115	15.05				01# 0111_
01000b	1150	249	17.80		Output		01# 0000_
01001b	422	115	21.42				01# 0001_
01010b	1150	365	24.09				01# 0010_
01011b	487	187	27.74				01# 0011_
01100b	562	274	32.78				01# 0100_
01101b	464	274	37.13				01# 0101_
01110b	442	332	42.89				01# 0110_
01111b	442	442	50.00				01# 0111_
10000b	332	442	57.11	Slave	n/a. The clock is not a master	Rising edge triggered	01# 0000_
10001b	332	562	62.86				01# 0001_
10010b	274	562	67.22				01# 0010_
10011b	187	487	72.26				01# 0011_
10100b	365	1150	75.91				01# 0100_
10101b	115	422	78.58				01# 0101_
10110b	249	1150	82.20				01# 0110_
10111b	115	649	84.95				01# 0111_
11000b	115	866	88.28			Falling edge triggered	01# 0000_
11001b	115	1100	90.53				01# 0001_
11010b	68.1	787	92.04				01# 0010_
11011b	61.9	909	93.62				01# 0011_
11100b	56.2	1150	95.34				01# 0100_
11101b	36.5	1150	96.92				01# 0101_
11110b	11.5	715	98.42				01# 0110_
11111b	0	(open)	100				01# 0111_

Note 1: "# " is value of reg11[3]
Note 2: "_" is R/W bit.
Note 3: External Configuration resistors never override the reg11[3] bit, always factory code used.
All the other registers are initialized only by the Factory Programming Options.
Note 4: Last 3 bits of the 7-bit address are programmed by reg11[2:0]

DETAILED FUNCTIONAL BLOCK DIAGRAM

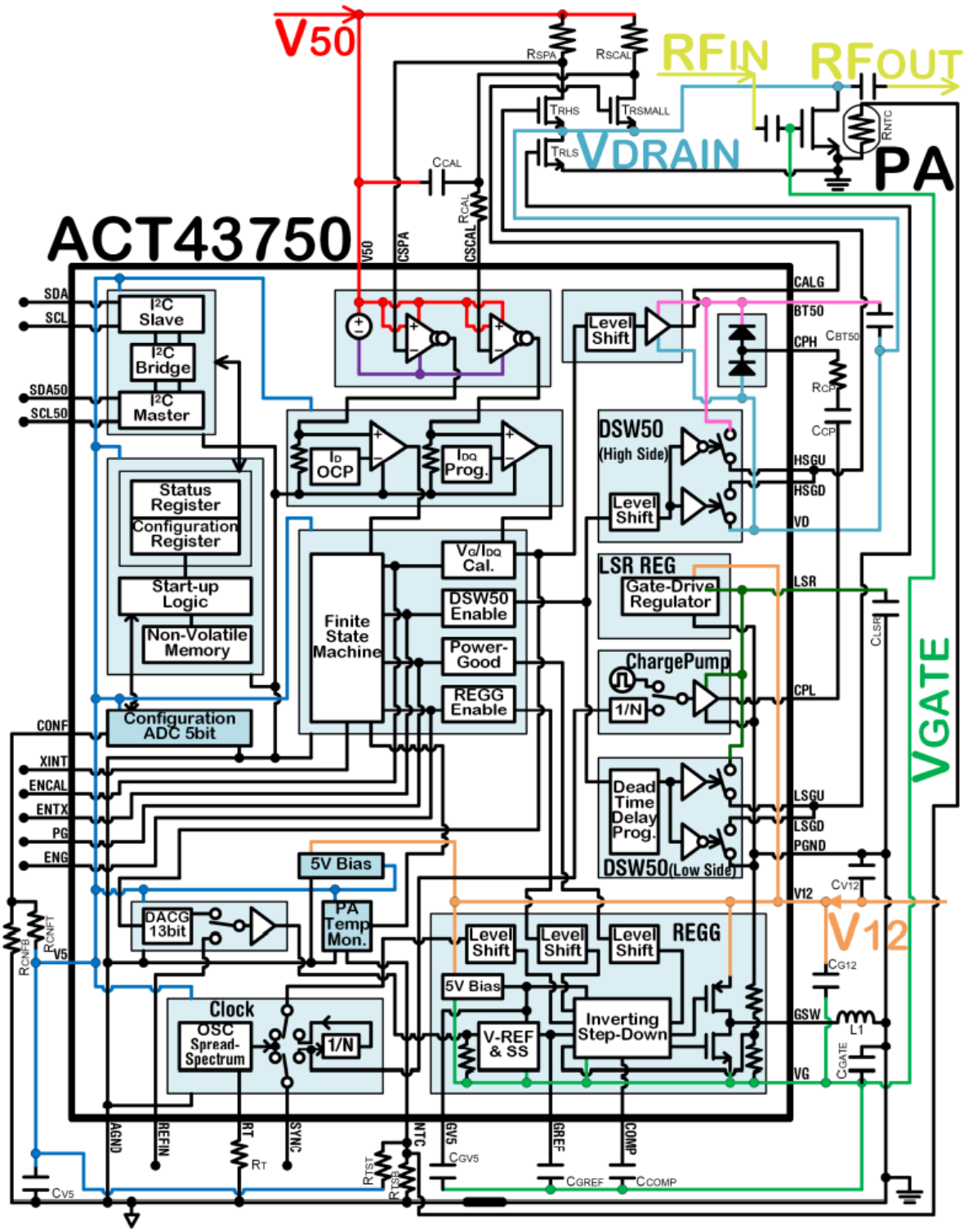


Figure 5. The Detailed Functional Block Diagram

Figure 5 shows the ACT43750 detailed functional blocks.

The ACT43750 provides the following three (3) major functions.

1. **REGG**: generates the negative gate voltage
2. **DSW50**: generates the RF PA drain voltage
3. **I_{DRAIN} Calibrator**: calibrates the RF PA's gate voltage to optimize the RF PA performance.

To support these 3 blocks, the device integrates the following supporting function blocks.

- **Logic Interface**
  - I2C Slave
  - I2C Master
  - I2C Bypass
- **Finite State Machine**
- **Device Initialization / Configuration**
  - External Configuration Resistors
  - Factory Programming Defaults
  - I^2C Registers
- **Device Bias / Reference System**
  - 5-V Bias Regulator
  - Floating 5-V Bias Regulator
  - Low-side Gate Drive Regulator
  - High-side Gate Drive Regulator
  - Switching Clock Generator
  - DACG
- **Protection Circuitry**

State Machine

The ACT43750 integrates a state machine to control the overall IC behavior and operation. The following section describes each state.

No Power

The IC starts up in this state and remains there until the V12 input bias voltage goes above its UVLO, typically 10V.

Bias Ramp

When the V12 bias voltage goes above ULVO, the state machine moves to the Bias Ramp stage. In this state, the IC initializes and loads the default CMI values from NVM into working memory. It reads the voltage on CONF and loads the resulting value into register 0x11h. It reads bit 0x11h [6] and decides to use the internal clock, which is set by the R_{RT} resistor, or synchronize with the external clock. It loads the REGG voltage reference to set the default negative gate voltage. After these steps are complete and the bias voltages are ready, the IC moves to the Bias Ready state.

Bias Ready

In the Bias Read state, the IC waits for an input trigger to turn on the negative gate voltage, REGG.

REGG Ramp

When a REGG enable event is triggered, the device starts up the REGG negative gate drive voltage.

REG50 Ramp

When the REGG voltage is ready, the V_{PG} pin goes open drain. This allows the IC to enable an external drain voltage regulator if available. This state is intended to enable the ACT43850 via I^2C. It does this by automatically using the Master I^2C bus to write a 1 to the ACT43850 register 0x08 bit[0].

TX Ready

When both the REGG and REG50 are ready, the IC enters this state and waits for a command to enter one of the following states: DSW50 ON, RSCAL CAL, REGG to MIN, and REGG Programming.

DSW50 ON

In this state, the drain FET is turned on, and the drain voltage is applied to the RF PA. Before the IC enters this state, it must have entered either the RSCAL CAL, REGG to MIN, or REGG Programming states.

RSCAL CAL

In this state, an autocalibration routine is performed to find the proper gate voltage to bias the RF PA at the desired drain current, Idq.

REGG to MIN

In this state, the REGG gate voltage slews to the minimum programmed value to turn off the RF PA.

REGG Programming

The IC enters this state when an I^2C command changes the DACG register value. This value sets the REGG negative gate voltage to the RF PA. The gate voltage can only be changed when ENTX is low. That means the IC can only enter this state when the drain voltage is off.

Error REGG MIN

The IC enters this state when it detects an overcurrent or over-temperature on the RF PA. The device turns off the drain voltage and drives the REGG gate voltage to the minimum programmed voltage.

V50 Discharge

The IC only enters this state when the system uses Qorvo's ACT43850 to generate the RF PA drain voltage. When the IC receives a command to disable REGG, it moves to this state to activate the I_{DRAIN} Calibrator block to discharge the drain supply voltage node before it disables REGG.

REGG Shutdown

As a result of the REGG disable event, the IC drives the DACG toward 0 V (zero). This state does the opposite of the soft start.

Bias Error

When the IC detects an error, it immediately turns off REGG and turns off the external RF PA drain FET. The IC turns off the RFPA drain voltage and then turns off the REGG gate voltage. It stays in this state until the 12V bias voltage at V12 is cycled off and back on. I^2C is still active in this state. The following faults force the IC into this state:

5V Bias Regulator under-voltage

V12 under-voltage

V12 over-voltage

Floating 5V Bias Regulator under-voltage

Low-side Gate Drive Regulator under-voltage

High-side Gate Drive Regulator under-voltage

Thermal shutdown, TSD

External Clock Synchronization error

REGG under-voltage

REGG over-current

5-bit ADC read error

Operation Frequency Selection / R_{RT} read error

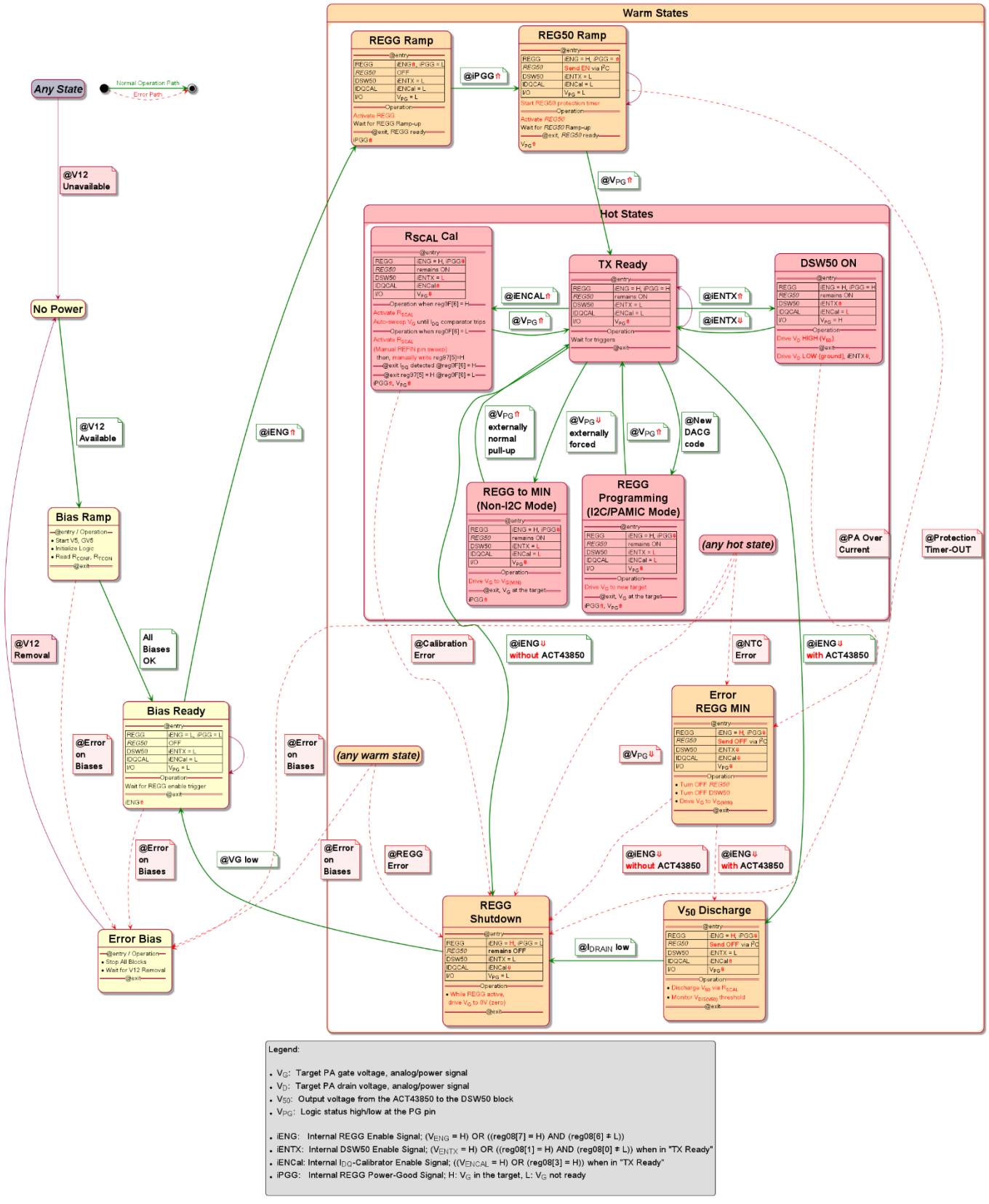


Figure 6. State Diagram

PIN DESCRIPTIONS

This section describes the ACT43750 pins and their functionality.

V50

The V50 pin is the power input for the IC's DSW50 block. It is also used as the positive input reference for both the RF PA overcurrent and calibration current inputs. V50 requires a 0.1uF ceramic capacitor to ground.

PGND

PGND is the ground pin for the DSW50 block. It must be directly connected to the exposed pad. PGND and AGND should be connected with a Kelvin connection to separate the power ground currents from the analog ground currents.

AGND

AGND is the analog ground reference for the internal ADC, voltage reference, DAC, etc. This "quiet" ground reference is kept separate from the higher current power grounds. AGND and PGND should be connected with a Kelvin connection to separate the analog ground currents from the power ground currents.

XINT

XINT is the open drain interrupt output pin. It should be connected to a pull-up resistor to a proper logic voltage source.

V5

V5 is the 5V internal bias voltage output pin. It requires a 2.2µF ceramic capacitor to AGND. V5 is not intended to power any external circuitry.

SCL, SDA

These are the IC's I^2C clock and data pins. They have standard I^2C functionality. If I^2C is not needed, these pins should be tied to either ground or V5. See the System Control section for the IC's available slave addresses. Note that SCL and SDA do not have internal pullup resistors.

ENTX

ENTX is a digital input that enables the transmit function in RF PA applications. When using the ENTX pin to enable the DSW50 drain voltage to the RF PA, pull the ENTX pin high. Pull it low to disable the drain voltage. Note that even if ENTX is low, the drain voltage can still be enabled by I^2C. Refer to the DSW50 Enable Input Logic paragraph for the detailed conditions to enable and disable the drain voltage.

ENTX is a digital input and must be actively terminated high or low. To ensure ENTX is low by default at turnon, connect a 100kΩ resistor from this pin to the ground. Don't float this pin.

The REGG block can only be enabled when ENTX is low. In other words, the RF PA REGG gate voltage can only be changed when ENTX is low.

ENCAL

ENCAL is a digital input that initiates the RF PA Idq calibration routine. ENCAL is a digital input and must be actively terminated high or low. To ensure ENCAL is low by default at turnon, connect a 100kΩ resistor from this pin to ground. Don't float this pin.

SYNC

SYNC is the synchronization pin. It operates as either a master sync output or a slave sync input. See Table 3 for details on programming the SYNC pin functionality.

CONF

CONF uses two resistors to configure additional IC functionality.

RT

RT uses a resistor to AGND to set the oscillator frequency. It is only functional when the CONF pin programs the oscillator as a Master.

REFIN

External reference voltage input. An external reference can be used to provide a low noise reference voltage for the REGG block for the negative gate drive. Register 0x0F bit 6 must be set to 0 to use an external reference.

NTC

RF PA over temperature protection input. NTC typically uses a thermistor and a resistor to set the over-temperature threshold. It also accepts digital logic input from another IC. If not used, connect NTC to V5.

ENG

ENG is the enable pin for the REGG block. When using the ENG pin to enable the REGG block, pull ENG high enable REGG and pull the ENG pin low to disable the REGG block. Note that even if ENG is low, the REGG block can still be enabled by I^2C. Refer to the REGG Enable Input Logic paragraph for the detailed conditions to enable and disable the REGG block.

Note that ENG must be low when bias power is applied to the IC. To ensure ENG is low by default at turnon, connect a 100kΩ resistor from this pin to the ground. Do not float this pin.

PG

PG is an open drain power good output for the REGG block. It should be connected to a pull-up resistor to a proper logic voltage source. PG is pulled high when the REGG power is good. PG can also be connected to other devices' power good outputs. It has an input monitor that detects if an external device pulls PG low. If PG is pulled low, the ACT43750 finite state machine is no longer in the power-good status, and it moves to the one of error states.

GV5

GV5 is the REGG 5V reference voltage output. The GV5 output voltage is referenced to the VG output voltage. GV5 requires a 2.2µF capacitor to VG.

GREF

GREF is the reference voltage for the REGG power supply. The GREF voltage is referenced to the VG output voltage. GREF requires a 100nF capacitor to VG.

COMP

COMP is the loop compensation capacitor input pin for the REGG power supply. The REGG power supply is designed to use a single capacitor value for all operating conditions. COMP requires a 470pF capacitor to VG.

VG

VG is the REGG output voltage pin. This is the negative gate voltage output pin that connects directly to the RF PA gate. A 22uF capacitor is needed between this pin and PGND.

GSW

GSW is the REGG switching node. The GSW pin requires an LC filter connected between GSW and VG. The REGG inverting buck topology requires a 6.8µH inductor between GSW and PGND. It then requires a 22µF ceramic capacitor connected between PGND and VG. The capacitor must be connected directly between the inductor and the VG pin.

V12

V12 is the external 12V bias supply input to the IC. Connect a 10µF ceramic capacitor between V12 and PGND. It also requires a 10nF ceramic capacitor between V12 and VG.

LSR

Low-side gate drive regulator. Connect a good quality 2.2µF or higher ceramic capacitor between this pin and the PGND pin.

LSGU

DSW50 pull-up output pin for the low-side gate.

LSGD

DSW50 pull-down input pin for the low-side gate.

CPL

High-side gate drive regulator flying capacitor terminal. Connect a good quality 47nF C_{CP} capacitor and a 33Ω R_{CP} resistor, in series, between this pin and the CPH pin.

CPH

High-side gate drive regulator flying capacitor terminal. Connect a good quality 47nF C_{CP} capacitor and a 33Ω R_{CP} resistor, in series, between this pin and the CPL pin.

CALG

I_{DRAIN} calibrator external FET gate drive output.

VD

DSW50 output voltage node. Connect a good quality 10µF or higher capacitor C_{BT50} between this pin and the BT50 pin.

BT50

High-side gate drive regulator output, bootstrap for the DSW50. Connect a good quality 10µF or higher capacitor C_{BT50} between this and the VD pin.

HSGD

DSW50 pull-down input pin for the high-side gate.

HSGU

DSW50 pull-up output pin for the high-side gate.

CSPA

I_{DRAIN} over current protection current-sense input pin. Connect a 3mΩ (TYP) sense resistor R_{SPA} between the drain of high-side FET and the V50 pin. Connect an RC filter to this pin. Refer to the ACT43750 EVK for the values and connection details.

CSCAL

I_{DRAIN} calibration current-sense input pin. Connect a R_{SCAL} sense resistor between the calibration FET drain and V50. Connect RC filter R_{CAL} and C_{CAL} to this pin.

PGND

Ground terminal for power blocks.

IC BIAS CIRCUITRY

The ACT43750 supports both controlled positive and negative output voltages. This requires multiple reference voltage and ground references.

V12 Bias Regulator

The IC requires an external 12V bias input. This bias voltage is applied to the V12 pin, which requires at least a 10µF X5R or X7R ceramic capacitor, C_{V12}, to AGND. The 12V bias voltage should be relatively clean with less than 100mV of ripple. This voltage powers the ICs and generates the other reference voltages and the negative gate voltage.

5V Bias Regulator

An internal linear regulator provides a 5V bias at the V5 pin. This bias voltage directly powers most of the internal circuitry. The 5V bias voltage should be relatively clean with less than 50mV of ripple. It requires a 2.2µF X5R or X7R ceramic capacitor, C_{V5}, to AGND

Floating 5V Bias Regulator

Because the ACT43750 provides a negative gate voltage, it needs a 5V bias that is referenced to the negative gate voltage, VG. The ACT43750 generates this floating 5V bias with a linear regulator output at the GV5 pin. This regulator biases all circuitry that is referenced to the VG voltage. It requires a 2.2µF X5R or X7R ceramic capacitor, C_{GV5}, to the VG pin.

Low-side Gate Drive Regulator

The ACT43750 provides a linear regulator to power the low-side gate driver at the LSR pin. This allows the user to optimize the gate drive voltage for the specific FETs used in the design. Note that the voltage on LSR is used for both the low-side and high-side FETs. The VoLSR[3:0] bits in register 0x0Fh [3:0] set the default gate drive voltage. The default LDO voltage is set at the factory. This voltage cannot be changed on the fly. Contact Qorvo if a different default voltage is needed. The low-side gate drive regulator requires a 2.2µF ceramic capacitor to PGND.

High-side Gate Drive Regulator

Note that the high-side FET gate voltage is the same as the low-side FET. The ACT43750 provides a charge-pump regulator to power the high-side gate driver at the BT50 pin. This charge pump transfers the LSR voltage, referenced to PGND, to the CBT50 capacitor, referenced to VD, the drain voltage. The high side gate drive regulator requires a 47nF capacitor (C_{CP}) in series with a 33ohm resistor (R_{CP}) between the CPL and CPH pins. The charge pump resistor R_{CP} power dissipation is a function of drain voltage, frequency, and capacitance. Use the following equation to calculate the R_{CP} power dissipation.

$$P = 0.5 * C * V^2 * F \quad (1)$$

Where:

P – power loss of charge pump resistor, unit Watt.

C – charge capacitance, the unit is F.

F – drain voltage switching frequency, the unit is Hz.

V – drain voltage, the unit is Volt.

The R_{CP} resistor power rating should be higher than power loss and have at least a 50% margin.

PMIC OPERATION

The following sections describe the available ACT43750 functionality. The detailed functional diagram is shown in Figure 5.

DSW50 Drain Voltage

The DSW50 block provides drain switch control for RF PA GaN FETs. It does this by driving two separate FETs to apply the drain voltage to the RF PA and remove the drain voltage from the RF PA. This block supports both enhanced-mode power GaN and traditional Si (silicon) power FETs.

High-Side Driver: The high-side FET driver has two separate output pins that provide a push-pull output to drive the drain FET. The HSGU pin turns the drain FET on by applying a floating voltage to the FET gate referenced to the VD pin's drain voltage. The HSGD pin turns the drain FET off by pulling the gate to the VD voltage.

Low-Side Driver: The low-side FET driver also has two separate output pins that provide a push-pull output to drive the bottom FET. The LSGU pin turns the bottom FET on by applying the gate voltage to the FET gate. This voltage is ground-referenced. The LSGD pin turns the bottom FET off by pulling the gate to the ground.

Gate Drive Voltage: The gate drive voltage is set by the programmable internal regulator at the LSR pin. It is programmable between 5V and 10V to support many different FET topologies. The default voltage is set by register 0x0Fh but can be changed via I²C after power up. The LSR voltage is transferred to the high-side driver by a charge pump at the CPL and CPH pins. The switching frequency is set by register 0x12h. It is synchronized to the SYNC pin input clock when an external clock is used.

Drain Switching: The ENTX pin controls the voltage to the RF PA in both drain switching and continuous RF applications. Pulling ENTX high applies the drain voltage and pulling it low removes the drain voltage. In drain switching applications, the minimum on-time is 10µs. The maximum on-time is unlimited. External gate driver resistors between the driver outputs and the FET gates are recommended to control the gate drive voltage slew rates. The gate drive voltage is controlled by I²C.

Dead-Time Control: The IC provides high-side and low-side FET dead-time control to eliminate shoot-through during drain switching. The dead-time between the high side gate drive turning off and the low side gate drive turning on is set by register 0x12h [7:4]. The user can modify the default dead time to optimize performance with their specific FETs. The dead-time between the low side gate drive turning off to the high side gate drive turning on is fixed at 50ns. If the dead time is too small, the drain and low-side FETs will experience a shoot-through current from the V50 drain voltage to PGND. Unlike a standard power supply power stage, the ACT43750 deadtime adjustment does not affect the overall efficiency because there is no inductor in the ACT43750 power stage. Note that it is still important to prevent the high and low side FETs from turning on at the same time.

DSW50 Enable Input Logic

The ACT43750 provides two methods to turn the DSW50 block ON and OFF.

Hardware Enable Pin. Enable the DSW50 block by applying a logic H to the ENTX pin (enable transmit). Disable DSW50 by applying a logic low to ENTX.

I²C Slave Bus. Enable the DSW50 block by writing a 1 into the EN_DSW50 bit in register 0x08h [1]. Disable DSW50 by writing a 1 into DIS_DSW50 bit in register 0x08h [0].

Note that the EN_DSW50 and DIS_DSW50 bits are automatically cleared after the I²C write. Reading these two bits always returns a 0.

The IC uses the logic OR of the ENTX pin and the I²C registers to enable DSW50. Pulling the ENTX pin high or writing 1 to EN_DSW50 enables DSW50. If ENTX is high, writing a 1 into DIS_DSW50 disables the DSW50 block. Note that ENTX and I²C enable functions are ANDed with the PG status. This requires that the PG pin be high and the VG output voltage to be in regulation before the IC enters the DSW50 ON state.

Power-good Indicator Output (PG) and Monitor

The ACT43750 provides an open drain power good output, PG, to show the IC's power good status. This PG pin requires an external pullup resistor. When the PG pin voltage is logic H, the power is good. When the PG pin voltage is logic L, the power is not good.

The user can also read the PG status via I²C. If the value in register 0x00h [3:0] = 0101b (TX Ready) or 1001 (DSW50 ON), the PG status should be logic H by default. Power-good status by the I²C Interface

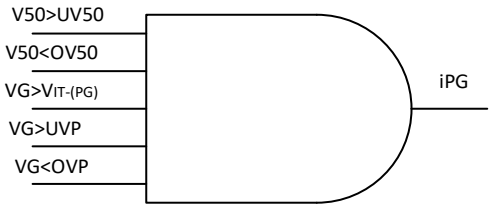


Figure 7. Power Good Logic

PG Wired-OR Monitor

Because the PG pin is an open drain output, it functions as a logic OR for showing that the power good status is "not good". The ACT43750 monitors the PG pin voltage with a logic input buffer. When any external device pulls PG low, the ACT43750 state machine detects this and acts accordingly as if the ACT43750 had pulled PG low. This function is typically used with the ACT43850 companion chip to provide system-level fault tolerance.

REGG Negative Gate Drive

The REGG block is an ultra-low noise inverting step-down dc-to-dc regulator with integrated FETs. This block supports 300mA (500mA peak) of sourcing output current (current into load devices) and 100 mA of sinking current (current into the ACT43750). The negative gate voltage at the VG output is referenced to PGND. When the REGG block is enabled, the gate voltage slews to the value set in DACGMAX (Register 0x15). The ACT43750 provides an autocalibration routine to automatically find the correct gate voltage that drives the RF PA GaN FET at its optimum bias point.

Voltage Reference

The ACT43750 provides a programmable reference voltage system for the REGG that consists of the following sub-blocks.

• DACG: 13-bit DAC with output voltage from 0.75 V to 3.00 V. Note that the resulting gate voltage is scaled to -2x the DACG voltage.

• External reference input at the REFIN pin. The user can supply an external reference voltage to replace the internal DAC reference voltage.

• DACG Digital Servo that controls the gate voltage slew rate when changing from one voltage to another.

• Soft-start control by adjusting charge current to capacitor C_{GREF}.

• Reference voltage noise reduction circuits to minimize noise applied to the RF PA gate.

DACG

The ACT43750 provides multiple methods of programming the 13-bit DAC between 0.75 V to 3.00 V. The DACG block contains several registers that set the DACG voltage. The actual DAC output voltage is set by the 13 bits in registers 0x07h [7:0] and 0x06h [4:0]. Register 0x07h contains the upper 8 msb and register 0x06h[4:0] contains the lower 5 msb. These two registers are combined to create a 13-bit register, DACG.

The DACG register sets the DACG output voltage, which can be programmed between 0.75V and 3.0V in 366.2µV steps. Setting DACG below 0.75V is not allowed.

DACG Voltage = DACG * 366.2µV

Where DACG is the decimal equivalent of the 13 bits in the hex-based register. Table 6 shows several example DACG register values converted to the DACG voltage and the resulting gate drive voltage. Note that the resulting gate drive voltage is -2 times the DACG voltage.

DACGMIN and DACGMAX are 8-bit registers that program the minimum and maximum DACG clamp voltage. These two registers define the starting and stopping points in the autocalibration routine and provide safety clamps to place known limits on the RF PA gate voltage. DACGMIN is in register 0x14h and DACGMAX is in register 0x15h. These registers correspond to the 8 most significant bits of DACG.

Table 6. DACG Register Values

Reg07[7:0]	Reg06[7:0]	Reference Voltage Target	Output Voltage Target
		(V_{GREF}-V_G), (V_{DACG}-V_{AGND})	(V_G-V_{PGND})
0100 0000	0000 0000	+0.750V	-1.500V
		…….	
0101 0101	0000 1010	+0.9997V	-1.9995V
0101 0101	0000 1011	+1.0001V	-2.0002V
0101 0101	0000 1100	+1.0005V	-2.0009V
		…….	
0110 1010	0001 0101	+1.250V	-2.500V
		…….	
1000 0000	0000 0000	+1.500V	-3.000V
		…….	
1100 0000	0000 0000	+2.250V	-4.500V
		…….	
1111 1111	0001 1111	+3.000V	-6.000V

There are multiple ways to program the DACG bits.

1. At startup, the State Machine automatically loads the maximum value, DACGMAX. This gives the lowest (farther negative) output voltage VG to ensure that the RF PA is fully turned off.

2. When the autocalibration routine is run, the algorithm automatically finds the optimal gate voltage value and programs the corresponding DACG value into the 0x07h [7:0] and 0x06h [4:0] registers.

3. The user can directly set the DACG value via the I^2C slave bus.

4. The user can use I^2C to write a DACG Adjust value into register 0x05h [7:0] to increment/decrement the existing value in the DACG registers.

5. Use the I^2C Master and Delta-Calibration to follow an external I^2C memory bank to set the DACG value.

The second method ("2.") with the I_{DRAIN} Calibrator ensures that the RF PA gate is at the right value for the ideal $I_{Q(DRAIN)}$ bias point. When working with external micro-controllers, the third and fourth methods ("3." and "4.") provide an interface for processor base control loops.

The third method ("3.") forces the DAC output to the code input into the register, by ignoring the DACGMIN and DACGMAX register values.

DACG Digital SERVO

When the DACG register value changes, the gate voltage does not instantaneously change. The ACT43750 contains a digital servo that steps the gate voltage from the starting value to the new target value with one DAC step at a time. This provides a very controlled gate voltage change with no over or undershoot. The DACGSlew bits in register 0x10h [1:0] set the step time to 8, 16, 32, or 64µs. If register 0x10h [7] = 0, these step times are 4x longer. Table 7 shows the resulting step times based on these two register settings.

Table 7. DACG Digital Servo Step Times

Value (Bin)	DACG Digital SERVO Step Times	
reg10[1:0]	reg10[7]=1	reg10[7]=0
00	8µs	32µs
01	16µs	64µs
10	32µs	128µs
11	64µs	256µs

DACG Code-loading Protection

Because there are two registers, 0x07h [7:0] and 0x06h [4:0] that hold the 13-bit DAC target code, the IC implements a procedure to make sure that both registers are correctly loaded before transferring the full 13 bits to the DAC. The register values are only transferred to the DAC when a 1 is written into the DACG_Load bit in register 0x04h[0]. This does not require user intervention. The IC automatically writes a 1 into DACG_Load every time a new value is written into the register 0x07h, the upper 8 msb of the DACG code. This requires that when the user updates the 13-bit DACG code, they first write the 5 lsb into register 0x06h and then write the 8 msb into register 0x07h.

External Voltage Reference

The ACT43750 allows the user to use an external voltage reference as the input to the DAC. This allows the system to use a low noise reference input or to change the reference voltage, and ultimately the gate voltage, without using the ACT43750 I^2C bus. The IC accepts the external voltage on the REFIN pin when the following two conditions are met.

1. GREFSel bit in Register 0x0Fh [6] = 0
2. The external reference voltage at the VREFIN is between $V_{REFIN(MIN)}$ and $V_{REFIN(MAX)}$ range. $V_{REFIN(MIN)}$ is the DACG output voltage set by the 13-bit DACG register. $V_{REFIN(MAX)}$ = 3.0V.

External Voltage Reference Noise Reduction

The VG output noise voltage can be reduced by connecting a bypass capacitor, C_{GREF}, to the GREF pin. The typical value is 100nF. The REGG soft-start (or slow-start) function is also controlled by C_{GREF}. To charge C_{GREF} in a controlled time at a start-up event, the GREF pin is driven by a current-limited buffer. After the start-up sequence is complete, this output buffer goes into a higher impedance mode to reduce noise on the reference voltage.

REGG Enable Input Logic external

The ACT43750 provides two methods to turn the REGG block ON and OFF.

Hardware Enable Pin. Enable the REGG block by applying a logic H to the ENG pin (enable gate). Disable REGG by applying a logic low to ENG.

I²C Slave Bus. Enable the REGG block by writing a 1 into the EN_REGG bit in register 0x08h [7]. Disable REGG by writing a 1 into the DIS_REGG bit in register 0x08h [6].

Note that the EN_REGG and DIS_REGG bits are automatically cleared after the I²C write. Reading these two bits always returns a 0.

The IC uses the logic OR of the ENG pin and the I²C registers to enable the IC. Pulling the ENG pin high or writing 1 to EN_REGG enables the REGG block. Pulling the ENG pin low disables the REGG block. Writing a 1 into DIS_REGG disables the REGG block, even if ENG is high.

REGG Soft start

The REGG soft start is controlled by the C_{GREF} capacitor on the GREF pin by applying a constant current output to this capacitor at startup. The soft start time can be increased or decreased by adjusting the C_{GREF} capacitor value or by adjusting the constant current output. The constant current output is controlled to 5µA, 10µA, 100µA, or 200µA by the IchgGREF bits in register 0x0Eh. Reducing the soft start time requires higher output current and a higher peak current in the gate drive supply inductor. Qorvo recommends keeping the gate current below 500mA during softstart.

I_{dq} Bias Point Calibration

The ACT43750 provides a calibration routine that calibrates the proper RF PA gate voltage bias point. The calibration routine operates in the RSCAL State. The typical RF PA datasheet provides an I_{dq} value that defines the proper drain current with no RF applied. This drain current is achieved by properly controlling the RF PA gate voltage. The ACT43750 autocalibration routine sweeps the negative gate voltage while measuring I_{dq}. When the RF PA sinks the proper I_{dq}, the IC saves the resulting gate voltage in registers 0x06h and 0x07h and uses that value to bias the RF PA.

The bias point calibration routine utilizes a dedicated FET and current sense resistor that is sized for the required I_{dq} current. When the routine is enabled, the IC turns off the main drain FET, $T_{RHS.}$ The actual autocalibration routine depends on the previous state of the system. The following equation calculates the correct calibration resistor value to bias the RF PA to the correct Idq.

$$Rscal = \frac{1.5V}{Idq} \qquad (2)$$

Where:

Idq – RFPA dc bias current, unit A

Rscal- Calibration resistor, unit Ω

Initial Calibration Routine. For the first calibration routine after power up, the IC sets the DACG voltage to the value defined by DACGMAX, which sets the gate voltage, VG, to the farthest negative value. This ensures that the RF PA is in pinch-off when the drain voltage is applied. At this time, no current flows through the FET or current sense resistor. It then turns on the smaller calibration FET, T_{RSMALL}, and starts sweeping the DACG voltage lower, which makes the V_G gate voltage go higher (more positive). Note that gate voltage is negative two times the DAC voltage. This starts increasing the I_{dq} to the desired setpoint. The IC decreases DACG voltage one step at a time with the delay time between steps set by the DACG Servo settings. When the correct I_{dq} current is reached, the REGG voltage is held constant and the corresponding DACG value is saved in registers 0x06h and 0x07h. The IC automatically moves to the TX Ready State.

The ACT43750 measures the I_{dq} current by sensing the voltage across the current sense calibration resistor, R_{SCAL}. It compares this voltage to a 1.5V internal reference threshold, $V_{IT+(CSCAL)}$. Note that the current sense voltage is measured between the V50 and CSCAL pins. Qorvo recommends connecting a 20kΩ Rcal resistor between CSCAL and the T_{RSMALL} FET. Connect a 100nF filter capacitor across R_{SCAL} and the filter capacitor as shown in Figure 8.

The calibration routine can be started by either applying a logic H to the ENCAL pin or by writing a 1 into the RunCal bit in register 0x08h [3]. The RunCal bit is automatically cleared back to a 0 when the calibration routine starts. The typical auto calibration time is approximately 30ms. This can be increased or decreased by changing the starting gate voltage and by adjusting DAC servo speed control. The actual calibration time depends on the bias voltage starting point and the DACG digital servo speed control. Register 0x10h programs DACG voltage transition time, which will make the calibration time shorter or longer.

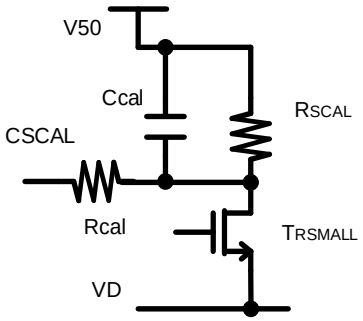


Figure 8. RC filter for Calibration Current Sense

Follow-on Calibration

After the initial calibration routine, all the following calibration routines start with the existing value in the DACG register. Start a follow-on calibration using the same procedure as when starting the initial calibration.

In both the initial and follow-on calibration routines, the IC automatically exits the calibration routine and moves to the TX Ready State when it finds the bias point. No user intervention is required to stop the calibration routine.

Calibration Error

The V_G minimum and maximum safety clamps are set by the DACGMIN (register 0x14h [7:0]) or DACGMAX (register 0x15h [7:0]) register values. If the DACG value reaches one of these clamp values before the internal comparator flips, the IC ends the calibration procedure with an error. The IC turns off the drain voltage and then moves to the REGG shutdown state, setting V_G = 0V.

Note that the DACGMIN and DACGMAX digital clamp works after the IC enters the R_{SCAL} CAL state. If the V_G has a very high voltage potential (near the ground), the RF PA may experience a very high drain current until the state machine detects that DACG is outside of the clamp values and can turn off the gate voltage.

I_{dq} Bias Point Adjustment

The ACT43750 provides the user with a calibration adjustment value. This can be used to provide preprogrammed adjustments based on system-level considerations. Register 0x13h [4:0] allows the user to adjust the $V_{IT+(CSCAL)}$ threshold between -31% and +31% of the 1.5V nominal value in 1% increments.

Manual (External) Calibration

When using the external reference voltage at the REFIN pin, with register 0x0Fh bit 6 = 0, an external sequencer can sweep the V_{REFIN} and monitor the register 0x00h bit 4 to perform a manual calibration. In this manual operation, the Finite State Machine does not automatically exit from the R_{SCAL} CAL state, so the external sequencer must send a command to register 0x97h bit 5.

Delta-Calibration

With an external I²C memory bank and the I²C Master block, the ACT43750 allows the user to digitally calibrate Idq without having to turn on the calibration FET.

Every time the state machine exits the DSW50 ON state, the I²C Master reads the latest VGATE target code from an external EEPROM on the master I²C and stores it in the register 0x91h [7:0] and register 0x90h [4:0]. Then the delta-calibration block calculates a code difference between the previous reading (of the target VGATE code) and this current reading. Once calculation finishes, the DACG Digital SERVO block drives the DACG code by this delta amount. Also, this delta amount is stored in register 0x95h [7:0] and 0x94h [4:0]. The positive or negative sign bit is stored in register 0x96h bit 0.

Continuous use of this delta-calibration accumulates digitizing errors, so the actual $I_{Q(DRAIN)}$ may off the target. The user must periodically perform a standard calibration routing to correlate the $I_{Q(DRAIN)}$ and V_G values.

To avoid accumulating the digitizing errors of the delta calibration, the ACT43750 provides automatic execution of the R_{SCAL} Calibration. This function triggers the R_{SCAL} Calibration sequence for every $N_{AutoCal}$ cycle of the Delta-Calibration. The two bits of reg08[5,4] enable and disable this auto-re-calibration function.

Interrupt Indicator Output / (xINT)

The ACT43750 sends out an active-low, open-drain, interrupt signal to external controllers (MCUs) on the XINT pin. Whenever any one of the interrupt bits is set, in registers 0x01h, 0x02h and 0x03h (Refer to the Register Definition App Note for more details), xINT goes active low. xINT clears back to a high level after the fault bits are read and the fault is cleared.

When the XINT pin is logic H, there are no interrupts.

When the XINT pin is logic L, one of the interrupt bits is triggered.

I²C Interface

The ACT43750 complies with the industry standard I²C-bus specification (UM10204). The ACT43750 contains two separate I²C buses.

I²C Slave

The ACT43750 operates as a slave on the SDA and SCL pins. These connect to a system level controller that acts as a master to write to and read from the ACT43750 register. The ACT43750 follows commands from the controller.

I²C Master

The ACT43750 operates as a master on the SDA50 and SCL50 pins. These pins connect to companion devices like the ACT43850 and to an external EEPROM. The ACT43750 operates as a master to read from and write to the registers in these slave devices.

I²C Broadcasting Address

The ACT43750 supports an I²C slave broadcasting address of 0x20h. This becomes 0x41h when writing to the ACT43750 ICs. This allows the I²C master connected to the SCL and SDA pins to configure and control multiple ACT43750 ICs simultaneously.

Only use this broadcasting address for "write" commands. Any "read" command should be issued to an individual I²C address.

I²C Master Interface to a Host

I²C registers at 0x90h to 0x9Fh control the I²C Master functions (below).

Scans to check for any companion devices on this sub-I²C bus like the ACT43850 or an external EEPROM.

- Enables and disables the ACT43850.
- Provides bypass control from a system-host to the ACT43850.
- (Re-)Programs the drain rail target voltage at the ACT43850.
- Reads target drain voltage from the external I²C memory.
- Reads target drain bias current from the external I²C memory.
- Reads target gate voltage from the external I²C memory.

The system host can turn the I²C master bus on and off by writing into register bit 0x17h [1]. When 0x17h [1] = 0, the master function is enabled. When 0x17h [1] = 1, the master function is disabled.

Also, the host can change the I²C master clock speed using 0x17h [3:2].

Scanning for Companion Devices

The IC automatically scans the master I²C bus for companion devices when the IC enters the REG50 Ramp state. The IC only supports two external components on this bus, one ACT43850 and one external EEPROM. If a device is found, the ACT43750 sets register 0x99h [0] = 1 to indicate there's an ACT43850 device on the sub-I²C bus and its I²C address gets stored in 0x98h [7:1]. If an external EEPROM is found, the IC sets bit 0x99h [1] = 1.

I²C Bypass

The ACT43750 provides an I²C bridge logic between the I²C Slave and the I²C Master blocks. The system host can enable the bypass function by setting 0x17h [0] = 1. When in bypass mode, the ACT43750 will pass-through commands from the system host at (SDA, SCL) port, to the ACT43850 on the SDA50/SCL50 pins. It also transfers responses back to the main SCL/SDA I²C bus.

Note that when the ACT43750 executes its own automatic communication procedures on the I²C Master block, the flag bit 0x99h [2] indicates the master block is busy and the system host needs to wait until this flag bit is cleared.

Internal Clock Generator

The ACT43750 contains an internal clock generator block for the REGG switching converter. This oscillator can operate stand-alone, or it can be synchronized to or from an external clock. This allows the system to synchronize the REGG switching frequency to an external oscillator.

Internal Clock Oscillator

When bit 0x11h [6] = 0, the clock generator uses its internal oscillator. This oscillator generates its switching frequency based on a resistor value connected to the RT pin. The target switching frequency f_{SW} follows equation (3). Table 8 provides some example values.

$$f_{sw}(\text{MHz}) = \frac{221}{RT^{0.982}(k\Omega)} \quad (3)$$

Table 8. Resistor value vs. Switching Frequency

RT Value (kΩ)	Switching Frequency of REGG (KHZ)
< 111	(error)
115	2043
125	1880
136	1728
150	1567
167	1407
188	1250
215	1093
> 231	(error)

When bit 0x11h [5] = 1, the IC shares this clock signal with other regulator devices by sending it out from the SYNC pin.

When 0x11h [5] bit = 0, the IC does not share the clock, and operates in stand-alone operation.

Spread-spectrum.

When using the internal oscillator, this oscillator block can enable/disable a spread-spectrum function. When register 0x10h [3] = 1, the device enables the spread spectrum. When 0x10h [3] = 0, the device disables the spread spectrum, and the output clock is fixed / steady. The spread-spectrum function modulates, or dithers, the internal clock frequency. The switching frequency varies +/- 7% from the oscillator's programmed frequency, and repeats the dithering every 64 cycles.

External Clock Synchronization

When register 0x11h [6] = 1, the clock generator synchronizes to an external clock input at the SYNC pin. When 0x11h [4] = 0, the internal clock is synchronized to the rising edge of the SYNC pin, and when it = 1, it's synchronized to the falling edge. When the SYNC pin is configured as a slave input, the external frequency can be divided down to switch at a slower frequency. The f_{SYNC} bits in 0x0Eh [7:5] can divide the SYNC frequency down by a factor of 1 to 8.

Operation Frequency Selection / R_{RT}

When using the Internal Clock Oscillator, equation 3 calculates the correct RT resistor value. This resistor value is read by the IC at startup. It uses the value to optimize internal settings such as compensation, protection settings, etc. The RT resistor must be used even if the IC is configured as a slave. The RT value must be chosen so that equation 3 calculates a switching frequency that is within +/- 20% of the actual SYNC input frequency.

If RT is not detected at startup, the IC logs an RT fault error in 0x00h [6:5]. The RT value cannot be changed after startup.

When using an external clock at the SYNC pin, dynamic changes of the external input clock, for example, external spread-spectrum, is only supported for the range of ±20% from the target switching frequency set by RT. When using the IC in slave operation, the user should choose one of the seven RT values in Table 8.

PROTECTION

The ACT43750 IC provides extensive IC and system-level protection mechanisms.

Startup Sequencing

GaN RF PAs require very specific startup and shutdown sequencing. The ACT43750 provides the required sequencing between the DSW50 and VG voltages. Because GaN RF PAs are depletion mode devices, at turn on, the negative gate voltage must be applied before the drain voltage is applied. The gate is pulled low (the lowest negative voltage) to put the GaN FET in pinch-off before the drain voltage is applied. After the drain voltage is applied, the gate voltage is slewed positively to properly bias the GaN FET. At turn-off, the gate is pulled to the most negative voltage again to put the GaN FET back into pinch-off. Any fault conditions move the IC to the Bias Error state.

I_{DRAIN} Over Current Protection

The I_{DRAIN} Over Current Protection block is an over-current protection of RF PA drain. By utilizing a small valued current sense resistor R_{SPA}, the DSW50 block protects the system from over-current conditions. This over-current protection is optimized to be fast acting to shut down the power supply to the RF PA devices. This protection is activated when the ENTX input is a logic H.

PA Over Temperature Protection

The PA Over Temperature Protection block is an over-temperature protection of RF PA. The device monitors the NTC pin voltage for over-temperature conditions. When V_{NTC} goes below the $V_{IT-(NTC)}$ target, the device shuts down the power supply to the RF PA. The $V_{IT-(NTC)}$ threshold is 30% of the voltage at the V5 pin. The input circuit block at the NTC is designed to accept regular logic signals too. When using a logic signal for the over-temperature input to NTC, a logic L indicates an over-temperature.

Thermal Warning (TWARN) and Shutdown - TSD

The IC provides an internal temperature sensor that monitors the IC's internal junction temperature, T_J. When T_J exceeds the T_{WARN} threshold, typically 140 deg C, 0x02h [0] = 1. When T_J exceeds the T_{SD} threshold, typically 160 deg C, the IC detects a thermal fault and shuts down the DSW50 block. The drain voltage for the RF PA is turned off and the IC moves into the Bias Error state and sets 0x02h [1] = 1. After shutting down, the IC can restart when T_J drops below 145 deg C.

OVLO

The IC provides overvoltage protection on both the V50 and V12 input voltages. If V50 or V12 exceed 65V or 14V respectively, the IC locks out, registers an overvoltage condition, and moves to the Error Bias state.

UVLO

The IC provides undervoltage protection on both the V50 and V12 input voltages. If V50 or V12 is under 10V, the IC locks out, registers an Undervoltage condition, and moves to the Error Bias state.

VG OVP

The IC provides overvoltage protection for the VG output. If VG exceeds 106.5% of the setpoint, the IC shuts down, registers an OVP fault, and moves to the Error Bias state.

VG UVP

The IC provides undervoltage protection for the VG output. If VG drops below 91% of the setpoint, the IC shuts down, registers a UVP fault, and moves to the Error Bias state.

OCP – Gate Current

The IC provides overcurrent protection on the VG output. If the gate current exceeds 1A, the IC shuts down, registers an OCP fault, and moves to the Error Bias state.

OCP – Drain Current

The IC provides overcurrent protection for the RF PA Drain current by monitoring the voltage across the current sense resistor connected to the drain side of the drain FET. OCP monitors the voltage difference between the V50 and CSPA pins. Use a Kelvin connection across the sense resistor to ensure an accurate measurement. The overcurrent threshold voltage is 35mV. The current sense resistor can be adjusted to configure any desired overcurrent setting. If the measured current exceeds the fault threshold, the IC shuts down, registers an OCP fault, and moves to the Error Bias state. The following equation calculates the correct overcurrent resistor value for the desired overcurrent threshold.

$$R_{SPA} = \frac{35mV}{ID} \qquad (4)$$

Where:

ID - RFPA drain current, unit A

R_{SPA} – Current limit sense resistor, unit mΩ

Bias Error State

As a reminder, when the IC enters the Bias Error State, it turns off all blocks and waits for the user to cycle V12 off and back on to clear the faults.

APPLICATION INFORMATION

Input Bypass Capacitors

C_{V12}

The C_{V12} capacitor is connected between the V12 and AGND pins. This capacitor must be at least 10µF and should be a high-quality ceramic capacitor like X7R.

C_{V5}

The C_{V5} capacitor is connected between the V5 and AGND pins. This capacitor must be at least 2.2µF and should be a high-quality ceramic capacitor like X7R.

C_{GV5}

The C_{GV5} capacitor is connected between the GV5 and VG pins. This capacitor must be at least 2.2µF and should be a high-quality ceramic capacitor like X7R.

C_{G12}

The C_{G12} capacitor is connected between the V12 and VG pins. This capacitor must be at least 10nF and should be a high-quality ceramic capacitor like X7R.

Bootstrap Capacitor

C_{BT50}

The C_{BT50} capacitor is connected between the BT50 and VD pins. This capacitor must be at least 10µF and should be a high-quality ceramic capacitor like X7R.

Configuration Resistors

R_{CNFT} and R_{CNFB}.

The R_{CNFT} and R_{CNFB} form a voltage bias network between the V5 and AGND pins. Its center tap is connected to the CONF pin. See External Configuration Resistors in Table 5 for the details on how to choose these resistors.

R_{RT}

The R_{RT} resistor is connected between the RT and AGND pins. See the Internal Clock Oscillator section for the details.

Pull-up Resistors

R_{SCL}

R_{SCL} is a pull-up resistor of an I^2C slave clock port. Connect this pull-up resistor at the SCL pin to a proper logic interface voltage source.

R_{SDA}

R_{SDA} is a pull-up resistor of an I^2C slave data bus. Connect this pull-up resistor to the SDA pin to a proper logic interface voltage source.

R_{PG}

R_{PG} is a pull-up resistor for the power-good indicator, PG. Connect this pull-up resistor to the PG pin to a proper logic interface voltage source.

R_{XINT}

R_{XINT} is a pull-up resistor for the interrupt indicator. Connect this pull-up resistor to the XINT pin to a proper logic interface voltage source.

REGG Output Filter

L_1

L_1 is the inductor for the gate drive inverting buck converter's LC filter. Connect a good quality 6.8µH inductor between the GSW and PGND pins. The inductor saturation current should be more than the IC current limit setting.

The following equations (5 – 7) can calculate the inductor saturation current:

The inductor ripple current:

$$\Delta I = \frac{(V12-VG)*Ton}{L1} \quad (5)$$

Where:

ΔI – Inductor ripple current (A)

L1 – Output inductance (H)

V12 – 12V bias voltage (V)

VG – Gate voltage (V)

f_{sw} – Switching Frequency of REGG (Hz)

Ton – On time (s)

$$Ton = \frac{VG*-1}{V12-VG} * \frac{1}{fsw} \quad (6)$$

$$Ipeak = \Delta I + IG \quad (7)$$

IG – Output current of the gate (A)

Choose an inductor with a saturation current higher than the Ipeak calculation above. Also take the inductor's RMS rating into account.

C_{GATE}

C_{GATE} is the capacitor for the gate drive inverting buck-boost converter's LC filter. Connect a good quality 22µF capacitor between the VG and PGND pins. This capacitor must be a high-quality ceramic capacitor like X7R.

REGG External Components

C_{COMP}

C_{COMP} is an external loop compensation capacitor. Connect a 470pF capacitor between the COMP and VG pins. It should be a high-quality ceramic capacitor like X7R.

C_{GREF}

C_{GREF} is the negative gate drive reference bypass capacitor. Connect a 100nF capacitor between the GREF and VG pins. It should be a high-quality ceramic capacitor like X7R.

C_{LSR}

C_{LSR} is the bypass capacitor that for the LSR (low side regulator) output voltage. Connect a 2.2-µF capacitor between the LSR and PGND pins. It should be a high-quality ceramic capacitor like X7R.

DSW50 External Components

R_{SPA}

R_{SPA} is the I_{DRAIN} current sense resistor. Connect a good quality 3mΩ (TYP) resistor between the V50 and CSPA pins. This resistor value can be adjusted to change the GaN PA FET current limit.

R_{SCAL} and C_{CAL}

These two components are connected in parallel. R_{SCAL} is an I_{DRAIN} bias current sense resistor that is used to set the GaN RF PA I_{dq} bias current. Connect a good quality resistor between the V50 and the T_{RSMALL} FET. The resistor value can be adjusted to change the GaN PA FET I_{dq} calibration current. C_{CAL} is a filter capacitor for the I_{DRAIN} bias current sensing. Connect a 100nF capacitor between the V50 and the T_{RSMALL} component. It should be a high-quality ceramic capacitor like X7R.

R_{TST} and R_{TSB}

R_{TST} and R_{TSB} work together with an NTC to form a temperature-sense resistor network. R_{TST} and R_{TSB} are placed by the IC while the NTC is typically placed near the main RF PA FET. Adjust the R_{TST} and R_{TSB} values to set the desired overtemperature fault threshold. The $V_{IT-(NTC)}$ parameter (1.5V) sets the target threshold voltage. When using an IC-type temperature sense with a logic output stage, R_{TST} and R_{TSB} are not needed.

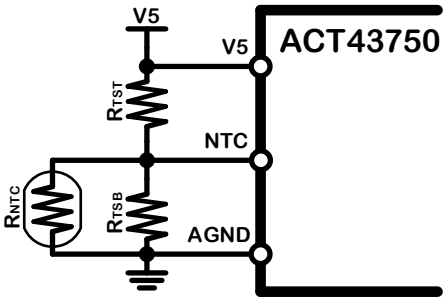


Figure 9. NTC Resistor Network

T_{RHS} and T_{RLS}

The T_{RHS} and T_{RLS} FETs form a half-bridge output of the DSW50 block. The ACT43750 supports both GaN and Si FETs. Be sure to use the correct gate drive voltage for the FETs being used.

T_{RSMALL}

The T_{RSMALL} FET controls the current through the I_{DQ} bias current calibration path.

C_{CP}

The C_{CP} capacitor is the charge-pump capacitor. Connect a good quality 47nF capacitor in series with R_{CP}. The series combination of C_{CP} and R_{CP} are connected between the CPH and CPL pins.

R_{CP}

The R_{CP} resistor is a current-limit resistor for the charge pump. Connect a 33Ω resistor in series with C_{CP}. The R_{CP} power dissipation is a function of the C_{CP} capacitance, the V50 drain voltage, and the switching frequency of the drain pulses. The equation below calculates the R_{CP} power dissipation.

$$P = 0.5 * C * V^2 * F \qquad (8)$$

Where:

P – charge pump resistor power loss, the unit is W.

C – charge pump capacitance, the unit is F.

F – drain switching frequency, the unit is Hz.

V – drain voltage, the unit is Volt.

The R_{CP} resistor power rating should be higher than power loss and have at least a 50% margin.

R_{CAL}

The R_{CAL} resistor is a filter for the I_{DRAIN} bias current sensing. Connect a good quality 20kΩ resistor between the CSCAL pin and the center tap of T_{RSMALL} and R_{SCAL}. Figure 8 shows the component Rscal, Ccal and Rcal.

R_{sf}, C_{sf} and C_{SPA}

The R_{sf} resistor, C_{Sf} and C_{SPA} capacitors form a RC filter for the I_{DRAIN} current sensing.

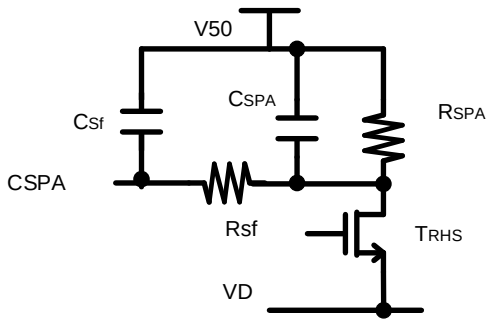


Figure 10. RC Filter for Drain Current Sense

R_{sf} is 51Ω resistor, C_{sf} and C_{SPA} are 0.1µF ceramic capacitors.

Typical Startup Procedure

The typical startup procedure is outlined below.

1. The ENTX, ENCAL, and ENG digital input signals must be actively terminated low. The most common system level startup errors occur when these signals are not actively terminated low.
2. The RT, NTC, and CONF resistors must be populated with the correct values for the desired operation.
3. Apply the V12 bias voltage and the V50 drain voltage. These can be applied in any order.
4. Enable the gate voltage by driving the ENG pin high. The user can also enable REGG via I²C by writing a 1 into register 0x08h [7], the EN_REGG bit. If using the Qorvo GUI, click the Enable Vgate button. This enables the negative gate voltage and programs it to the most negative value as defined by register 15.
5. Momentarily drive the ENCAL pin high to initiate a calibration routine to bias the RF PA with the correct gate voltage to achieve the desired Idq current. ENCAL must be pulled low before moving to the next step. The user can also enable calibration via I²C by writing a 1 into 0x08h [3], the RunCal bit. If using the Qorvo GUI, click the Autocalibration button. Note that excessive RF PA drain capacitance can result in a large inrush current that creates an overcurrent condition when main power FET turns on to apply the drain voltage to the RF PA. Refer to App Note 5 in the user's guide for details and limitations on the RF PA drain capacitance.
6. For systems with drain switching, drive the ENTX pin high and low with the desired frequency and duty cycle. For systems that operate with a continuous drain voltage, simply drive ENTX high. If using the Qorvo GUI, click the Enable Vdrain button.
7. If a calibration routine is needed at any time during operation, pull ENTX low or disable the drain voltage via I²C. Then enable the calibration routing by toggling the ENCAL pin high. The user can also enable a recalibration routine via I²C by writing a 1 into 0x08h [3], the RunCal bit. If using the Qorvo GUI, click the Autocalibration button. Then enable the drain voltage again with ENTX or via I²C. Note that it's possible to perform a recalibration in between transmission pulses if the off-time is longer than the calibration time.

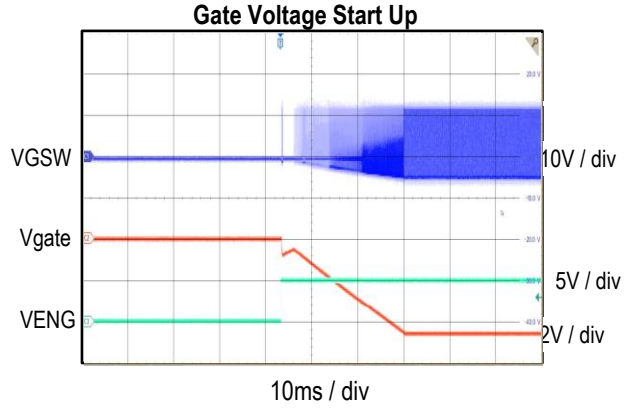
Typical Turnoff Procedure

The typical turnoff procedure is outlined below.

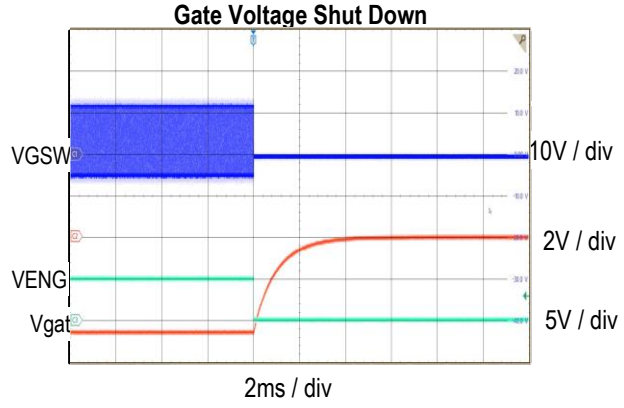
1. Turn off the drain switch by pulling the ENTX pin to a low logic level. For continuous operation, the drain switch can be disabled via I²C by clicking Disable Vdrain in GUI.
2. Adjust the gate voltage to the minimum programmed voltage defined by register 15. This puts the RF PA in pinchoff and turns off the GaN FET.
3. Power off the drain power supply.
4. After the drain voltage decays to less than 10V, turn off the 12V bias power supply

TYPICAL OPERATIONAL CHRACTERISTICS

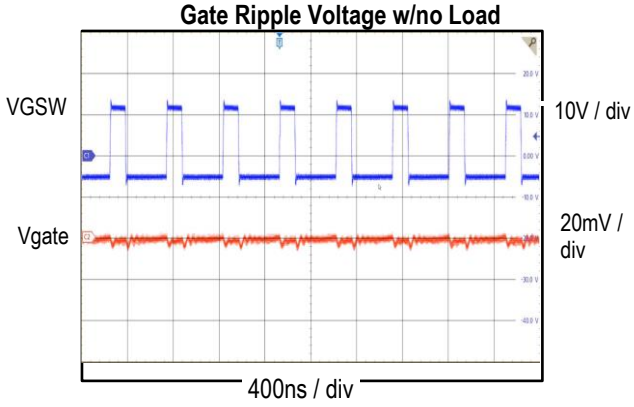
Gate Voltage Start Up



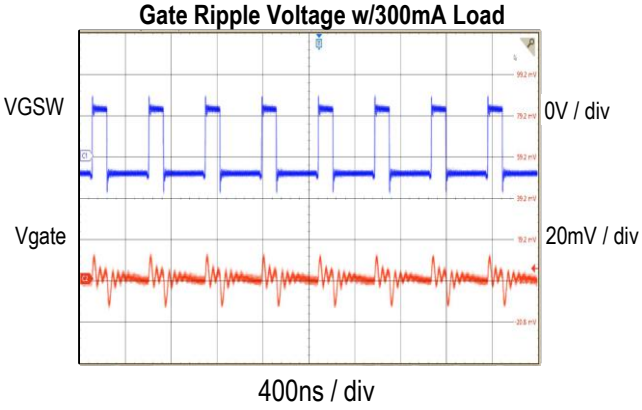
Gate Voltage Shut Down



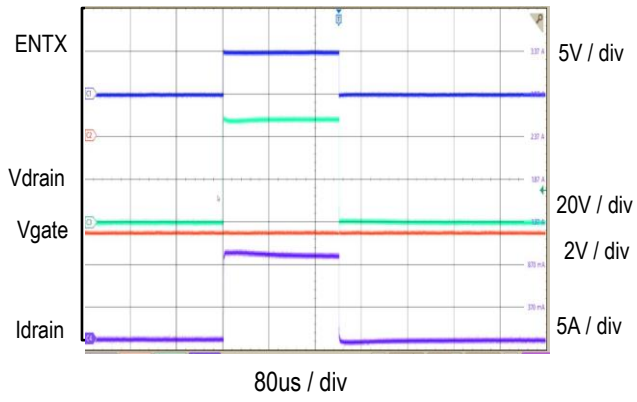
Gate Ripple Voltage w/no Load



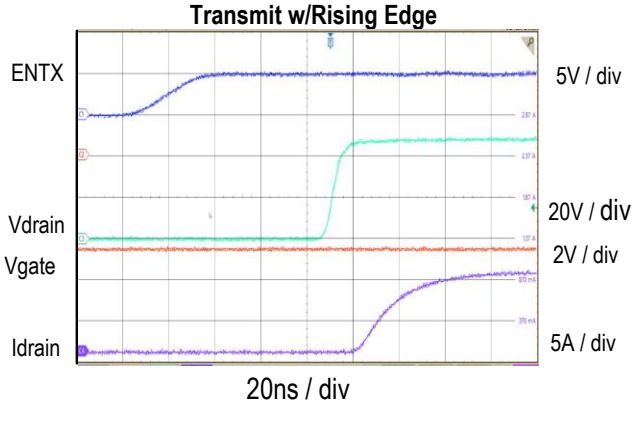
Gate Ripple Voltage w/300mA Load



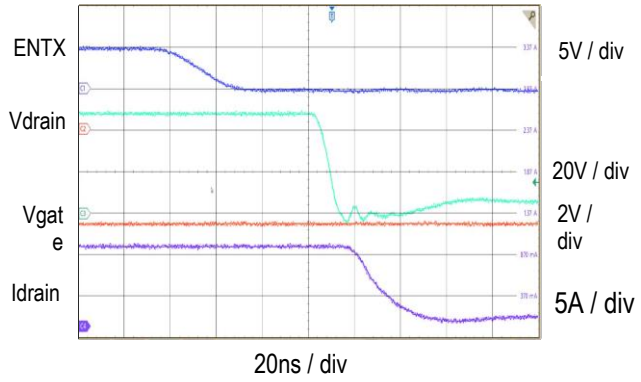
Transmit w/Resistive Load



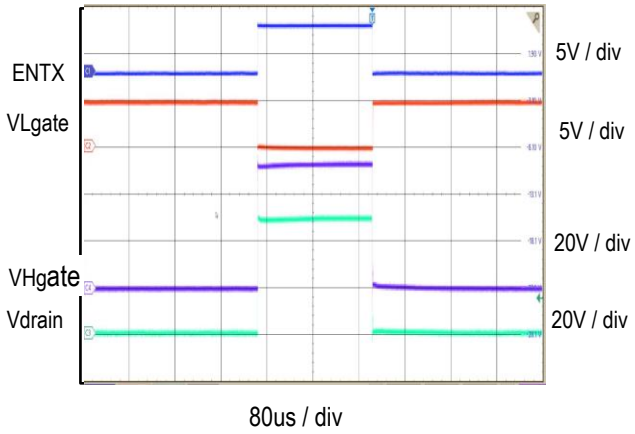
Transmit w/Rising Edge



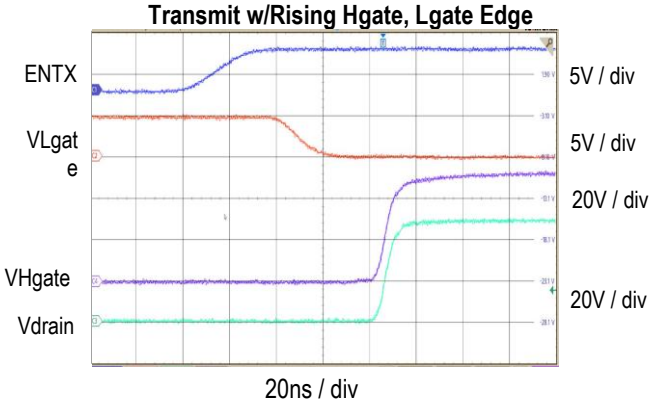
Transmit w/falling edge



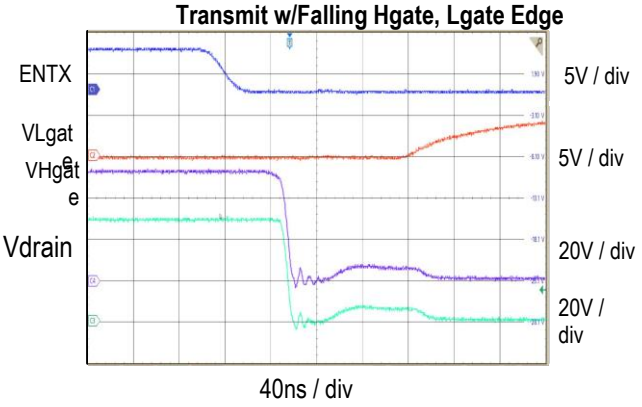
Transmit w/Hgate, Lgate



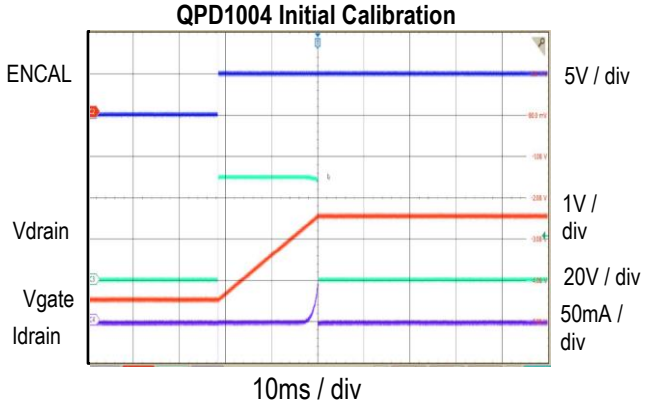
Transmit w/Rising Hgate, Lgate Edge



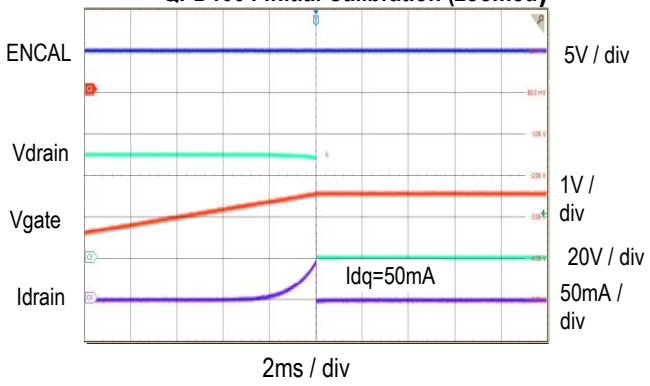
Transmit w/Falling Hgate, Lgate Edge



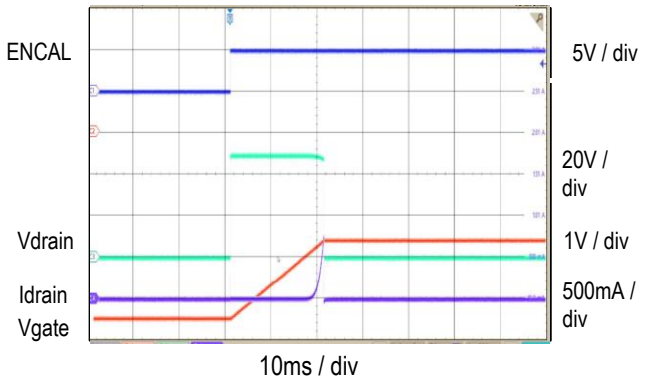
QPD1004 Initial Calibration



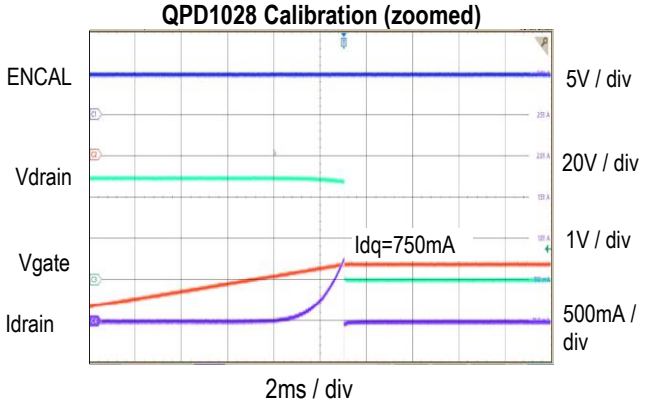
QPD1004 Initial Calibration (zoomed)



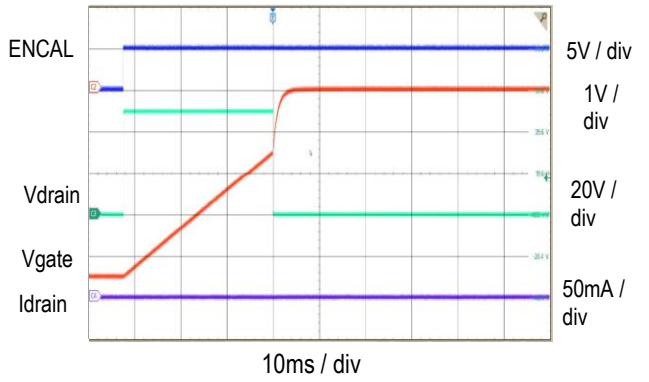
QPD1028 Calibration



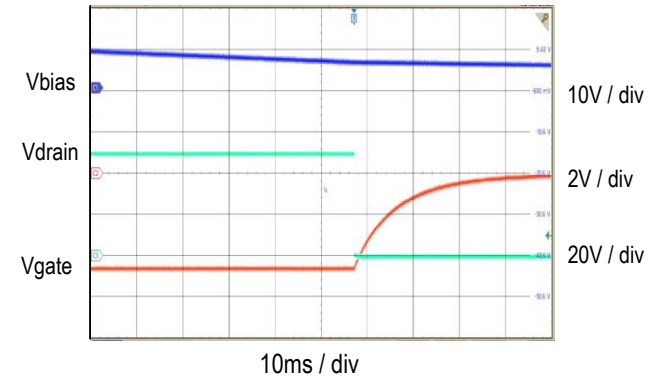
QPD1028 Calibration (zoomed)



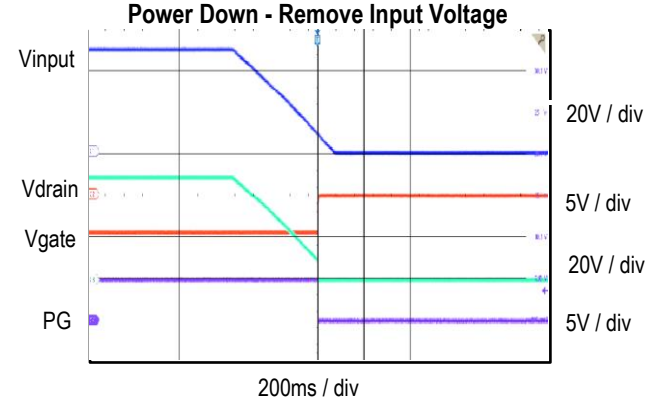
Calibration Failure



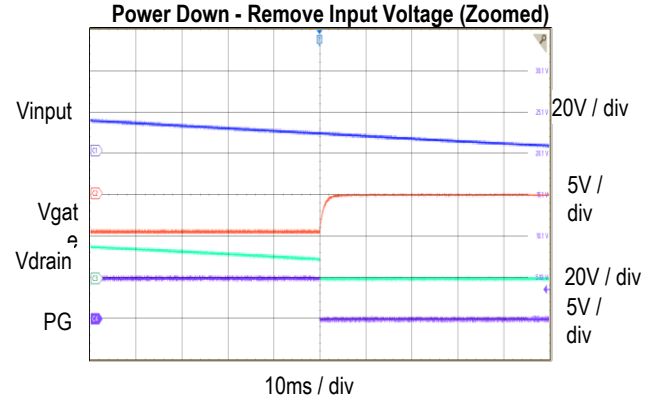
Power Down - Remove Bias



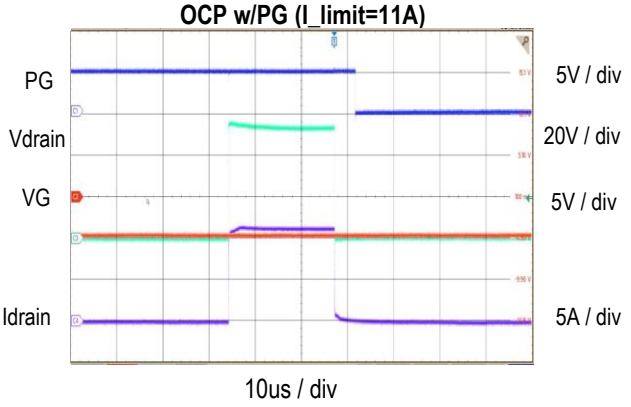
Power Down - Remove Input Voltage



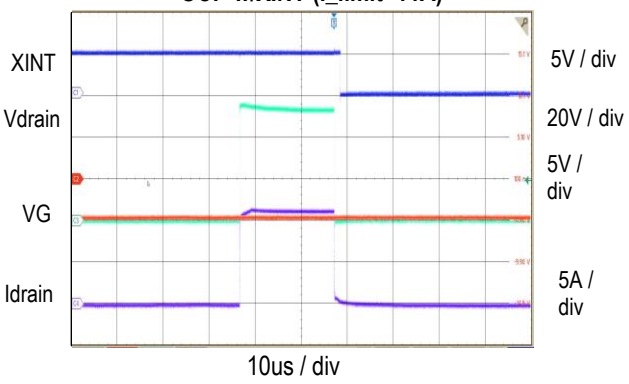
Power Down - Remove Input Voltage (Zoomed)



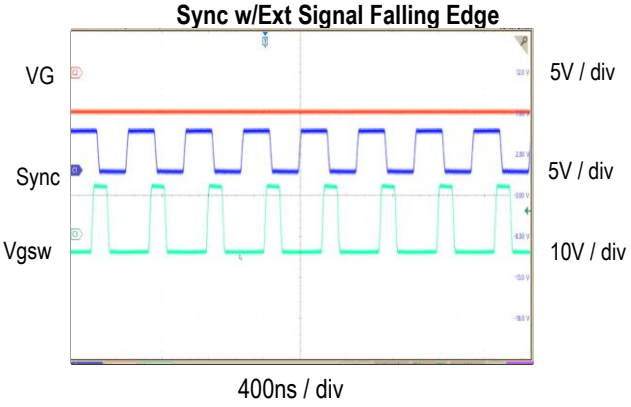
OCP w/PG (I_limit=11A)



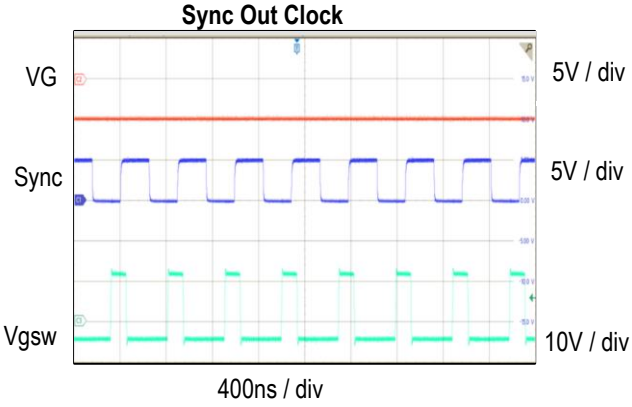
OCP w/XINT (I_limit=11A)



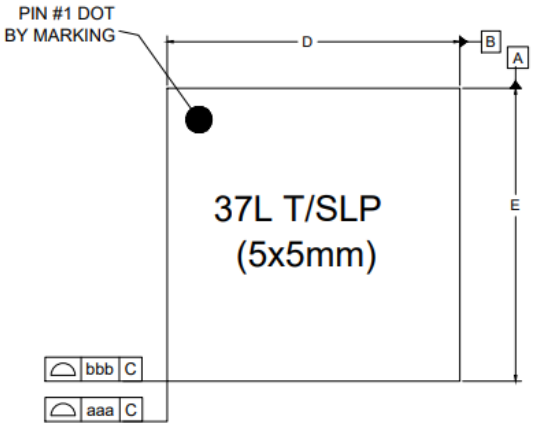
Sync w/Ext Signal Falling Edge



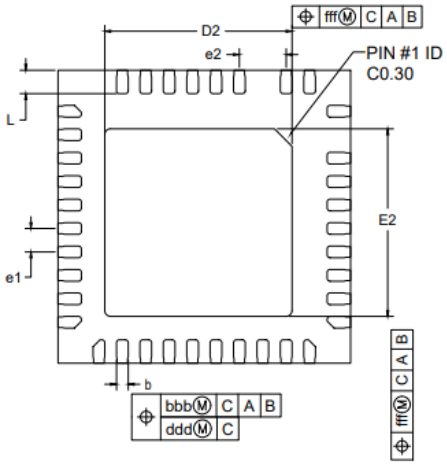
Sync Out Clock



PACKAGE OUTLINE AND DIMENSIONS

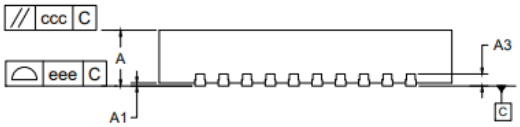


TOP VIEW



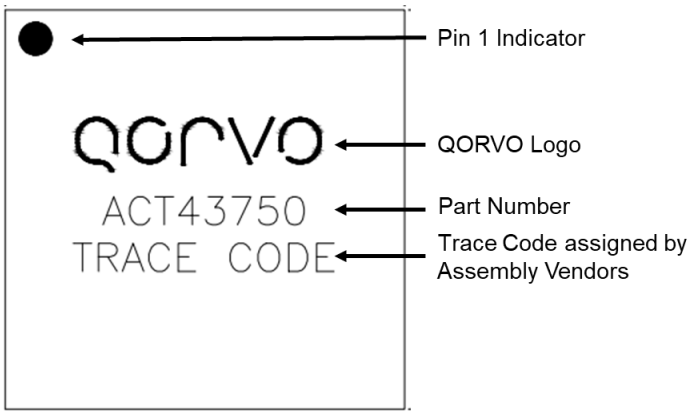
BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	---	---	0.050
A3	0.203 Ref.		
D	4.950	5.000	5.050
E	4.950	5.000	5.050
D2	3.150	3.200	3.250
E2	3.150	3.200	3.250
b	0.150	0.200	0.250
e1	0.400 BSC		
e2	0.800 BSC		
L	0.350	0.400	0.450
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		



SIDE VIEW

PART MARKING



Handling Precautions

Parameter	Rating	Standard
ESD — Human Body Model (HBM)	Class 1C[1]	ANSI/ESDA/JEDEC JS-001
ESD — Charged Device Model (CDM)	Class C2a[2]	ANSI/ESDA/JEDEC JS-002
MSL — Moisture Sensitivity Level		IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

[1] Refer to the chapter "10 Recommendations for a New ESD Target Level"
in the JEDEC document Recommended ESD Target Level for HBM Qualification (JEP155B)
[2] Refer to the chapter "9 Recommendations for Realistic CDM Target Levels for the Present and an Outlook for the Future" in the JEDEC document Recommended ESD-CDM Target Levels (JEP157)

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- SVHC Free
- PFOS Free
- Antimony Free
- TBBP-A (C15H12Br402) Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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