TS8541L - 50W/125Wp CW GaN Broadband RF Switch SP4T

1.0 Features

- Low insertion loss: 0.25dB @ 800MHz
- High isolation: 45dB @ 800MHz
- High linear power handling capability
- No external DC blocking capacitors on RF lines
- Versatile 2.6-5.5V power supply
- Frequency range 30MHz to 4300MHz

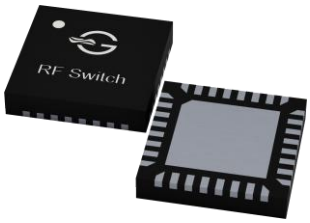


Figure 1 Device Image
(32 Pin 4.0×4.0×0.75mm^3 QFN Package)

2.0 Applications

- Private mobile radio handsets
- Public safety handsets
- Cellular infrastructure
- Small cells

RoHS/REACH/Halogen Free Compliance

3.0 Description

The TS8541L is a symmetrical reflective Single Pole Four Throws (SP4T) switch designed for broadband, high power switching applications. Its broadband behavior from 30MHz to 3.0GHz frequencies makes the TS8541L an excellent switch for all the applications requiring low insertion loss, high isolation and high linearity within a small package size. Part can also be used below 30MHz with reduced power handling.

The TS8541L is packaged into a compact Quad Flat No lead (QFN) 4.0x4.0mm^2 32 leads plastic package.

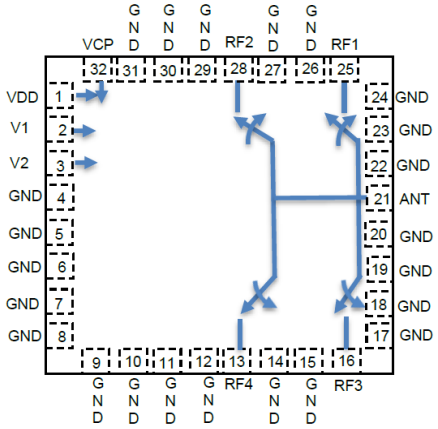


Figure 2 Function Block Diagram
(Top View)

4.0 Ordering Information

Table 1 Ordering Information

Device Part Number	Package Type	Notes
TS8541L	32 Pin 4.0×4.0×0.75mm^3 QFN	Core part number
TS8541L-EVK	Evaluation Board	
TS88541LMTRPBF	330mm reel, 3 000 pcs	Full Reel

5.0 Pin Description

Table 2 Pin Definition

Pin Number	Pin Name	Description
1	VDD	DC power supply
2	V1	Switch control input 1
3	V2	Switch control input 2
4,5,6,7,8,9,10,11,12,14,15,17, 18,19,20,22,23,24,26,27,29,30,31	NC	No internal connection, can be grounded
13	RF4	RF port 4
16	RF3	RF port 3
21	ANT	Antenna port
28	RF2	RF port 2
25	RF1	RF port 1
32	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.

Note: The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

6.0 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings @T_A=+25°C Unless Otherwise Specified

Parameter	Symbol	Value	Unit
Electrical Ratings			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	T_{st}	-55 to +125	°C
Operating Temperature Range	T_{op}	-40 to +85	°C
Maximum Junction Temperature	T_J	+140	°C
RF Input Power CW, 30MHz-3000MHz	RFx	48	dBm
RF Input Power CW, 3000MHz -4300MHz	RFx	47	dBm
RF Input Peak Power CW, 30MHz-3000MHz, 1% DC, 10 µs PW	RFx	51	
RF Input Peak Power, 3000MHz -4300MHz, 1% DC, 10 µs PW	RFx	51	
Maximum RF input power (30…4300MHz, VSWR 8:1)	RFx/ANT	46	dBm
Maximum RF input Peak Voltage (30…4300MHz, VSWR 8:1)	RFx/ANT	100	V
Thermal Ratings			
Thermal Resistance (junction-to-case) – Bottom side	$R_{\theta JC}$	5	°C/W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	≤ 37	°C/W
Soldering Temperature	T_{SOLD}	260	°C
ESD Ratings			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	≥1000	V
Moisture Rating			
Moisture Sensitivity Level	MSL	1	-

Attention:
Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

We recommend to store unused components in dry pack to ensure long term solderability.

7.0 Electrical Specifications

Table 4 Electrical Specifications @T_A=+25°C Unless Otherwise Specified; VDD=+3.3V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating Frequency		30		4300	MHz
Insertion Loss, RFx	400MHz		0.20		dB
	800MHz		0.25		
	3000MHz		0.87		
	3000MHz (matched)		0.55		
	4300MHz (matched)		0.80		
Isolation, ANT-RFx	400MHz		55		dB
	800MHz		45		
	3000MHz		24		
	3000MHz (matched)		23		
	4300MHz (matched)		20		
Return Loss, ANT-RFx	400MHz		28		dB
	800MHz		25		
	3000MHz		10		
	3000MHz (matched)		18		
	4300MHz (mathed)		20		
H2	800MHz, Pin=40dBm		-84		dBc
H3	800MHz, Pin=40dBm		-86		dBc
IIP3	800MHz		70		dBm
P0.1dB[1]	30MHz – 3.0GHz, CW	47			dBm
P0.1dB[1]	3.0 GHz – 4.3GHz, CW	46			dBm
Peak P0.1dB	30MHz – 4300MHz, 1% dutycycle,10 μs pulse width	50			dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3)		2.3		μs
Control Voltage	Power supply VDD	2.6	3.3	5.5	V
Control Voltage Control Current	All control pins high, V_{ih}	1.0	3.3	5.25	V
	All control pins low, V_{il}	-0.3		0.5	V
	All control pins low, I_{il}		0		μA
Control Current Current Consumption, IDD	All control pins high, I_{ih}			7.5	μA
	Active mode		170	220	μA

Note: [1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

8.0 Switch Truth Table

Table 5 Switch Truth Table

V1	V2	Active RF Path
0	0	ANT-RF1
1	0	ANT-RF2
0	1	ANT-RF3
1	1	ANT-RF4

Attention: [1] VDD should be applied first before V1 and V2, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on V1 and V2 control pins, therefore the switch state at start-up without any control voltage applied will be ANT-RF1 on by default.

9.0 Evaluation Board Schematic

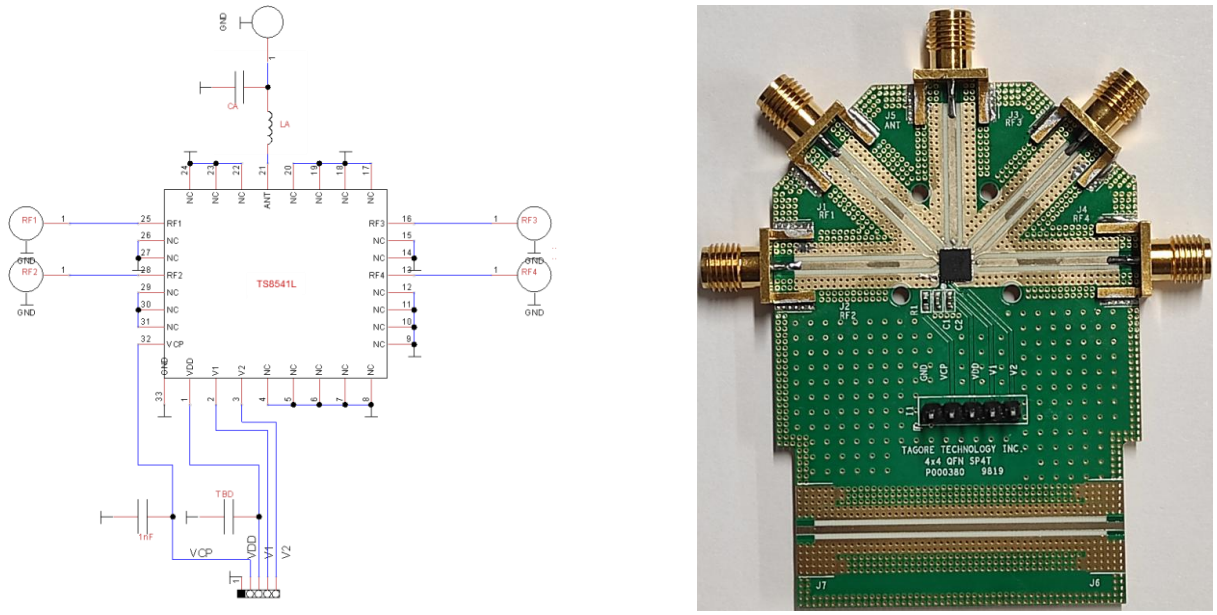


Figure 3 Evaluation Board Schematic and Picture (No Match)

Attention:
[1] **33 refers to the center pad of the device. Multiple Plugged through hole vias should be added to this Ground Pad and adequate heat sinking should be used.**
[2] The purpose of the connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.
[3] Place matching components close to pin of the part.

10.0 Typical Characteristics (unmatched)

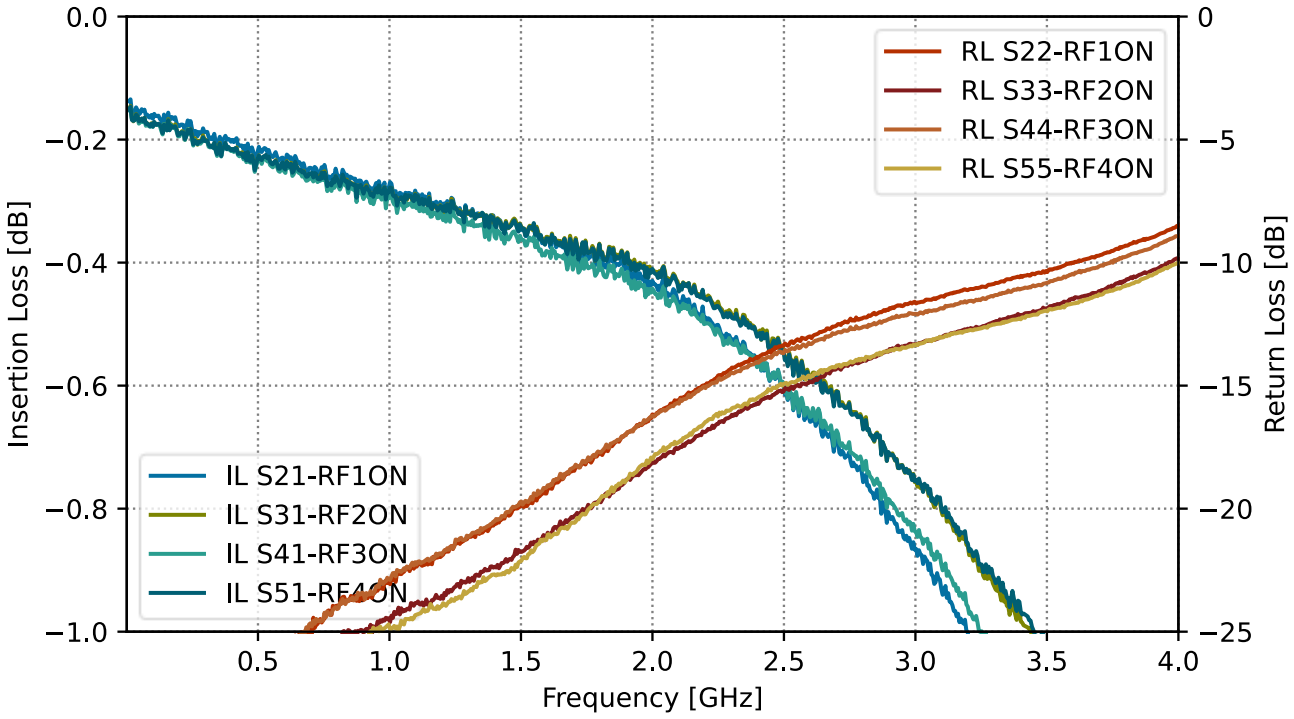


Figure 4 RF1 to RF4 Insertion Loss and Return Loss (no matching components on the EVB)

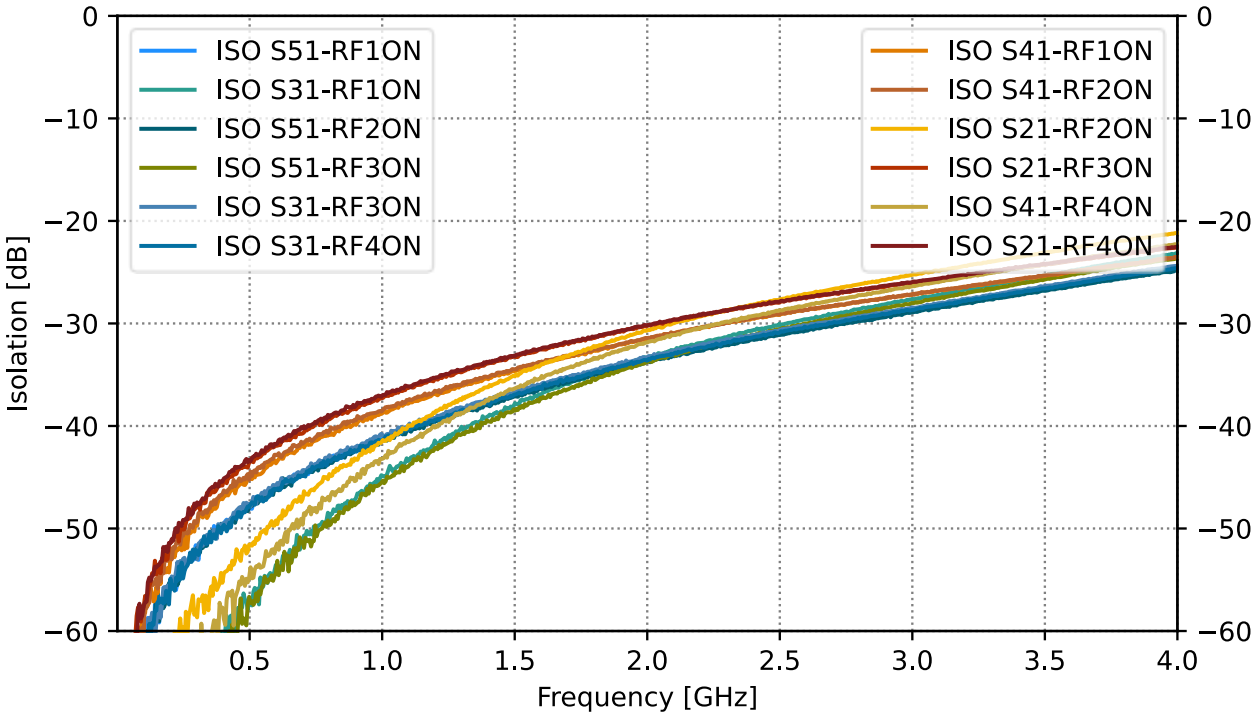


Figure 5 RFC to unused RF port isolations (no matching components on the EVB).

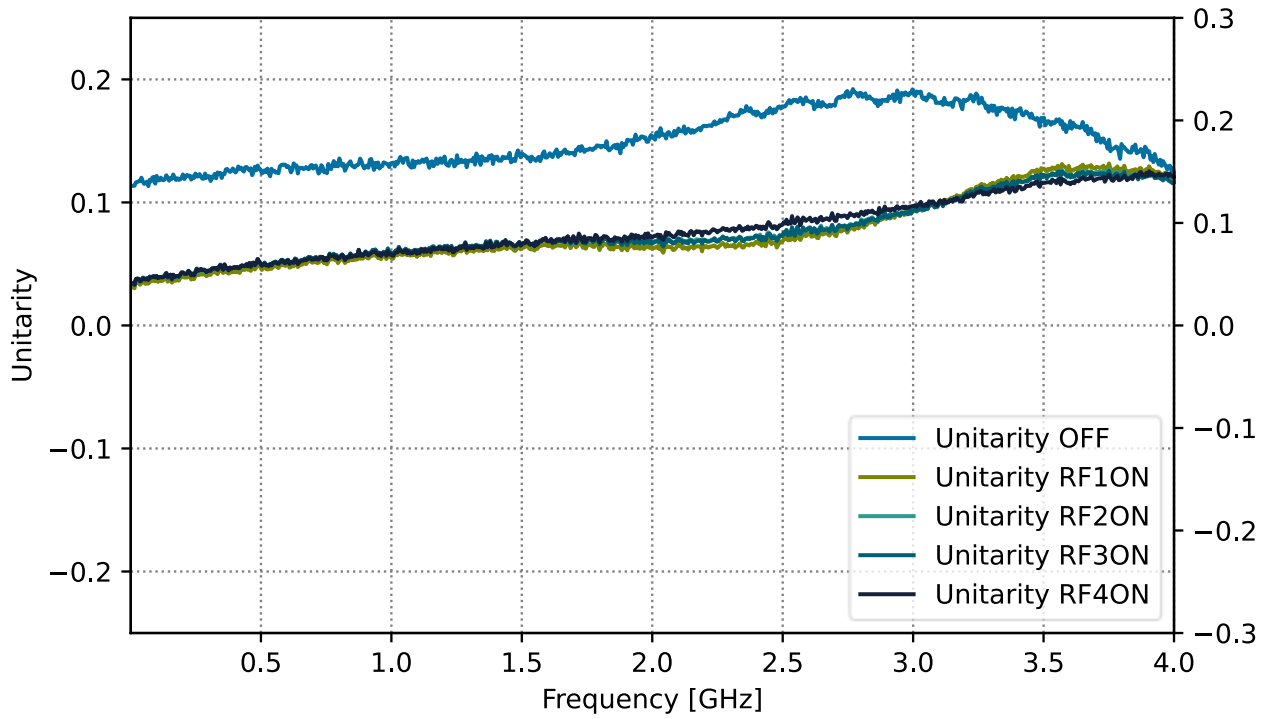


Figure 6 Unitarity (power absorption by RF Switch)

10.0 Typical Characteristics (matched upto 4300MHz)

Matching network
Shunt capacitor 0.4 pF at common port, 5.2 mm from edge of switch to center of cap
Shunt capacitor 0.2 pF at RF ports, 4.5 mm from edge of switch to center of cap

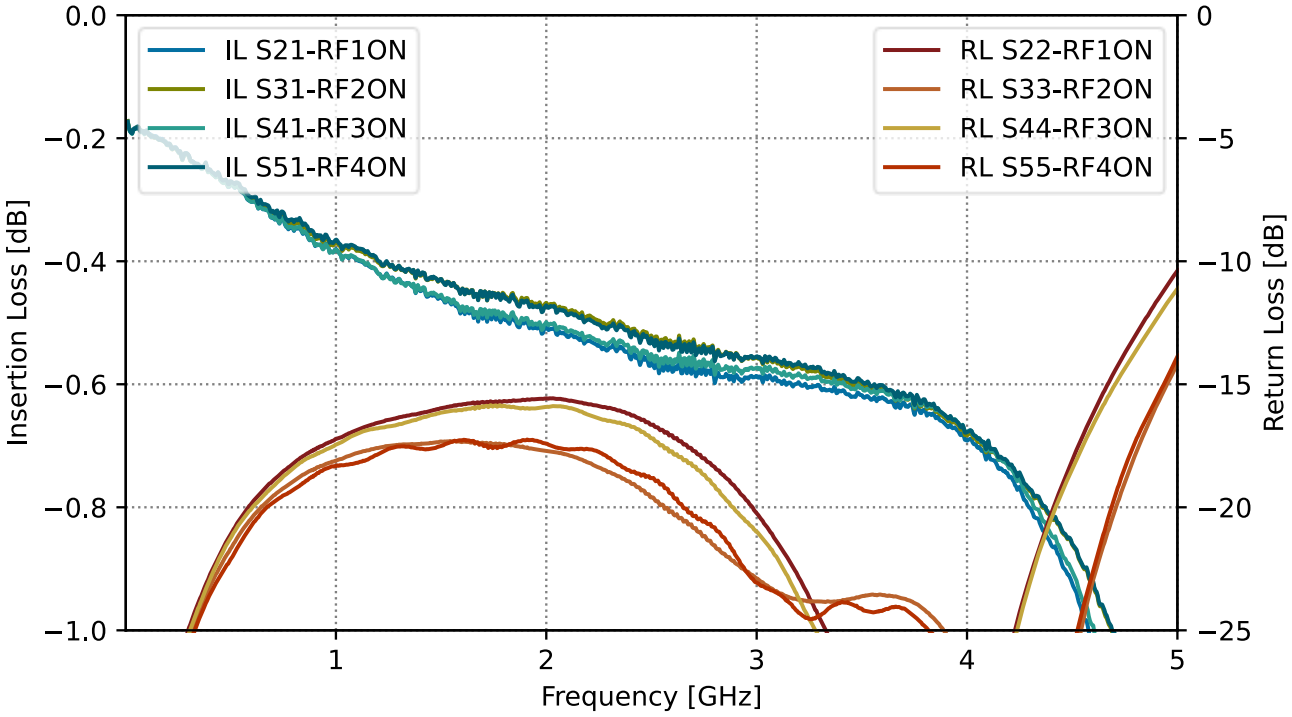


Figure 7 RF1 to RF4 Insertion Loss and Return Loss (matched upto 4300MHz)

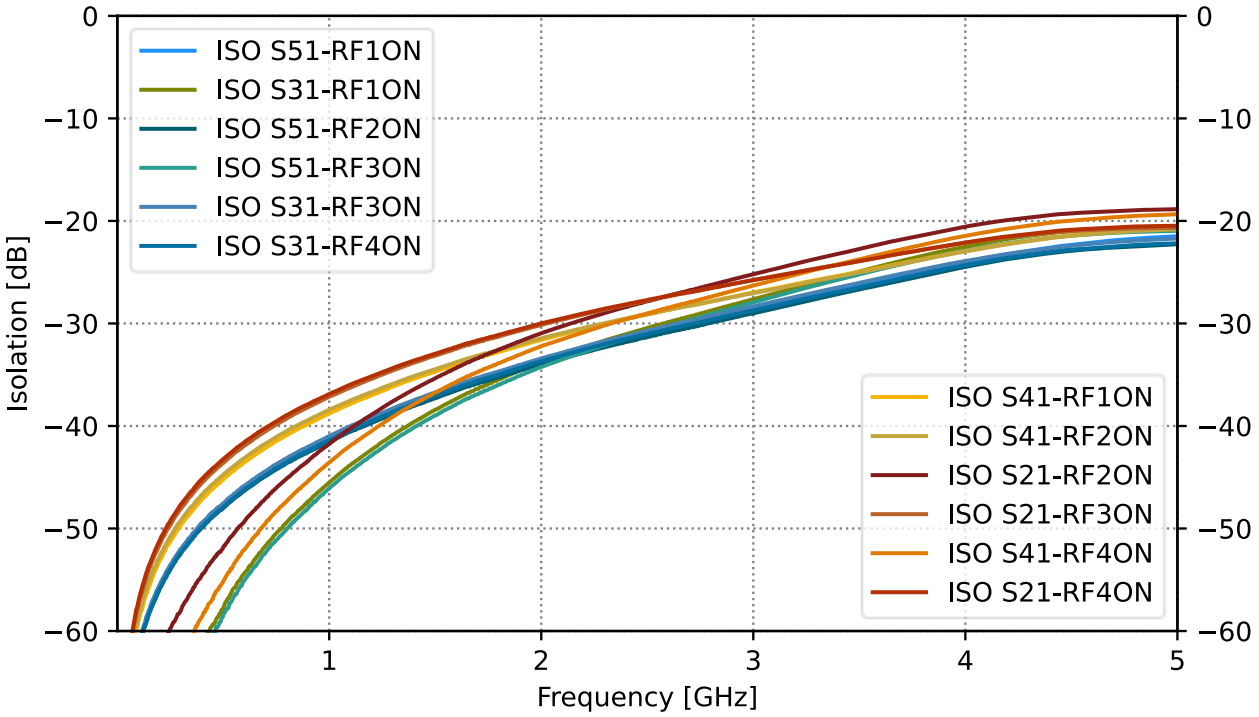


Figure 8 RFC to unused RF port isolations (matched upto 4300MHz)

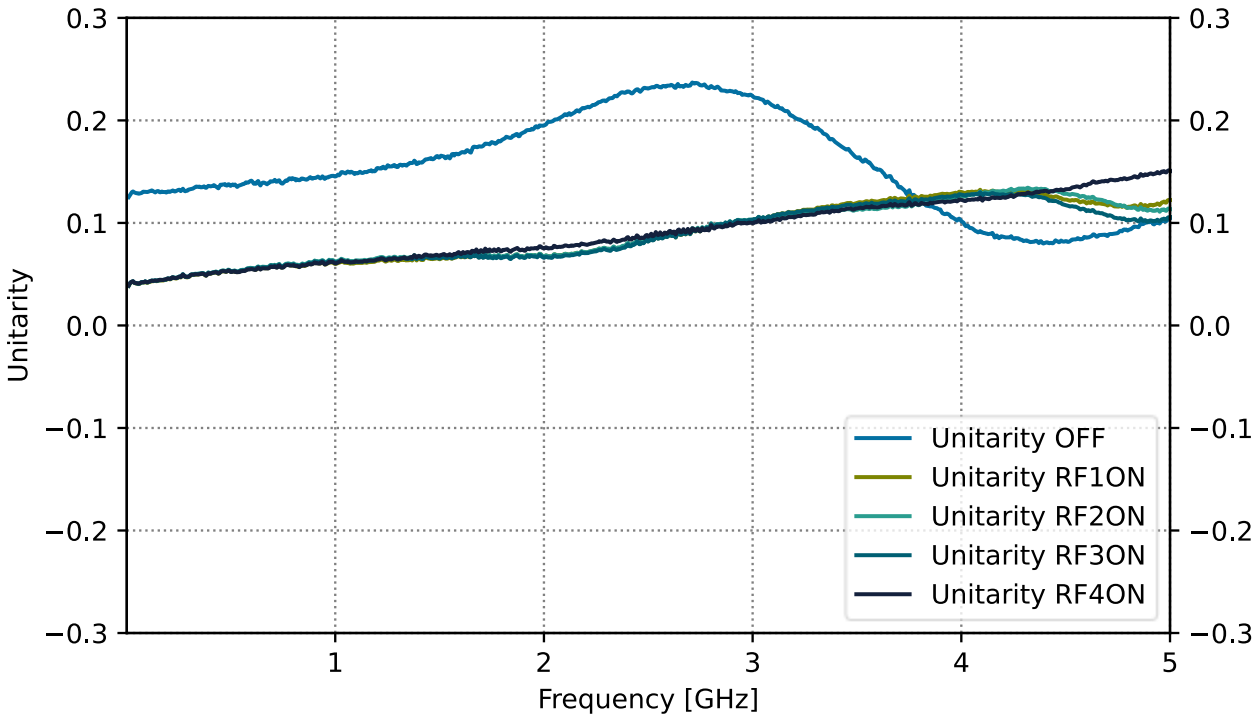


Figure 9 Unitarity (Power absorption of switch), matched upto 4300MHz

11.0 Device Package Information

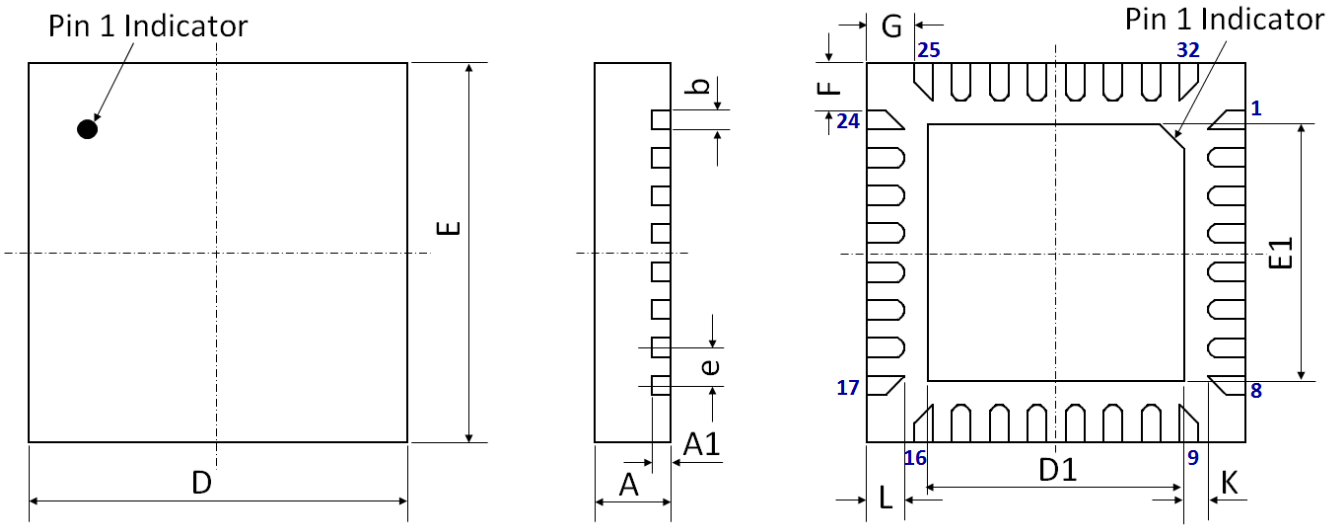


Figure 8 Device Package Drawing
(All dimensions are in mm)

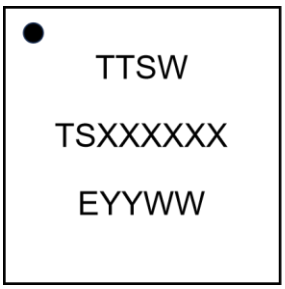
Table 6 Device Package Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A	0.75	±0.05	E	4.00 BSC	±0.05
A1	0.203	±0.02	E1	2.70	±0.05
b	0.20	+0.05/-0.07	F	0.50	±0.05
D	4.00 BSC	±0.05	G	0.50	±0.05
D1	2.70	±0.05	L	0.40	±0.05
e	0.40 BSC	±0.05	K	0.25	±0.05

Note: Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

Attention:
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering-related guidelines.

Top-marking specification:



● = Pin 1 indicator
TTSW = Tagore Technology SWitch
TSXXXXXX = Part number (8 digits max)
E = A fixed letter before the date code
YY = Last two digits of assembly year
WW = Assembly work week

12.0 PCB Land Design

Guidelines:
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 4(X)×4(Y)=16.

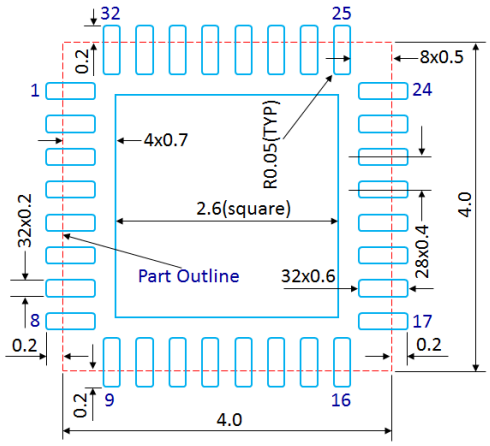
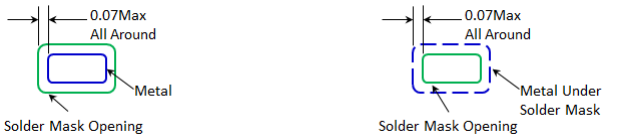


Figure 9 PCB Land Pattern
(Dimensions are in mm)



Non-Solder Mask Defined (Preferred)

Solder Mask Defined

Figure 10 Solder Mask Pattern
(Dimensions are in mm)

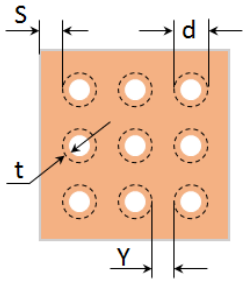


Figure 11 Thermal Via Pattern
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

13.0 PCB Stencil Design

Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

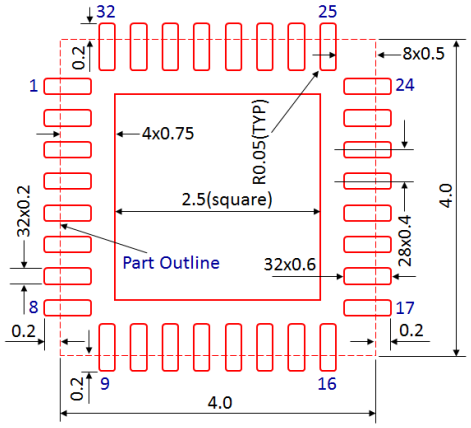


Figure 12 Stencil Openings
(Dimensions are in mm)

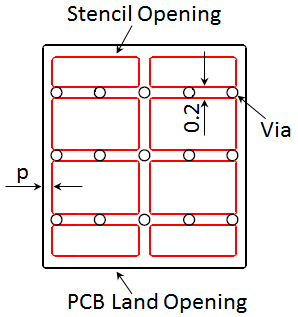


Figure 13 Stencil Openings Shall not Cover Via Areas If Possible
(Dimensions are in mm)

14.0 Tape and Reel Information

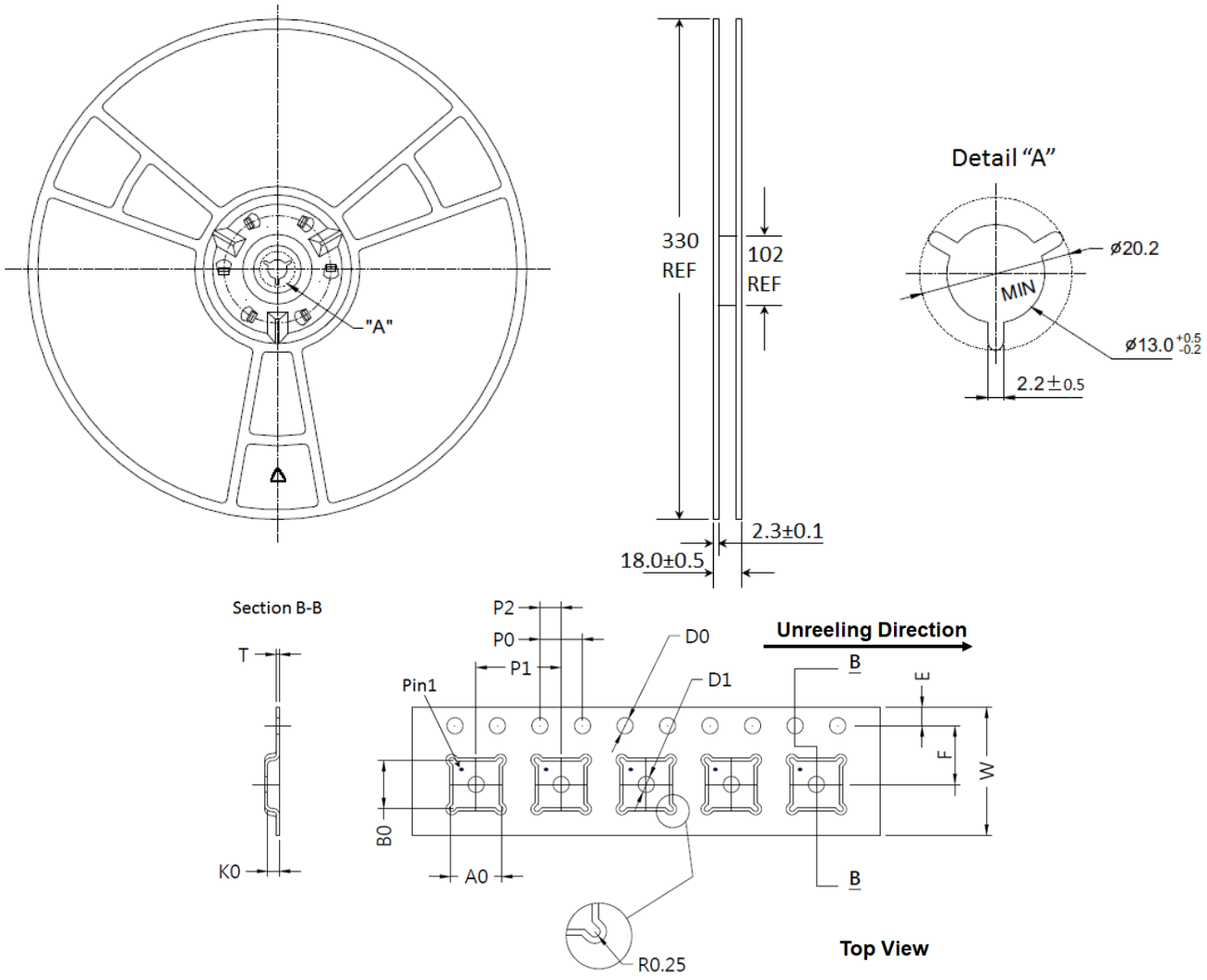


Figure 14 Tape and Reel Drawing

Table 7 Tape and Reel Dimensions

Dimension (mm)	**Value** (mm)	**Tolerance** (mm)	**Dimension** (mm)	**Value** (mm)	**Tolerance** (mm)
A0	4.35	±0.10	K0	1.10	±0.10
B0	4.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

Edition Revision 2.2 - 2025-10-17

Published by
TagoreTech Inc.
601 Campus Drive, Suite C1
Arlington Heights, IL 60004, USA

©2024-2025 All Rights Reserved

Legal Disclaimer
The information provided in this document shall in no event be regarded as a guarantee of conditions or characteristics. TagoreTech assumes no responsibility for the consequences of the use of this information, nor for any infringement of patents or of other rights of third parties which may result from the use of this information. No license is granted by implication or otherwise under any patent or patent rights of TagoreTech. The specifications mentioned in this document are subject to change without notice.

Information
For further information on technology, delivery terms and conditions and prices, please contact TagoreTech: support@tagoretech.com.

Latest datasheet
You can download latest datasheet from https://www.tagoretech.com/Product_Doc/TS8541L.pdf