PE42850

Document category: Product Specification

UltraCMOS® SP5T RF Switch, 30–1000 MHz

Features

- Dual mode operation: SP5T or SP3T
- HaRP™ technology enhanced:
  - Fast settling time
  - No gate and phase lag
  - No drift in insertion loss and phase
- Up to 45 dBm instantaneous power in 50Ω
- Up to 40 dBm instantaneous power < 8:1 VSWR
- 36 dB TX to RX isolation
- Low harmonics of $2f_o$ and $3f_o$ = –90 dBc (1.15:1 VSWR)
- ESD performance: 1.5 kV HBM on all pins
- Packaging: 32-lead 5 × 5 mm QFN

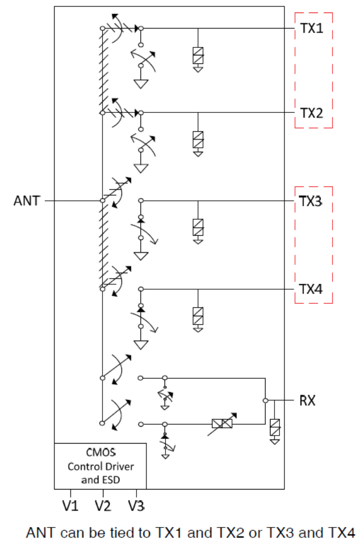


Figure 1. SP3T configuration functional diagram

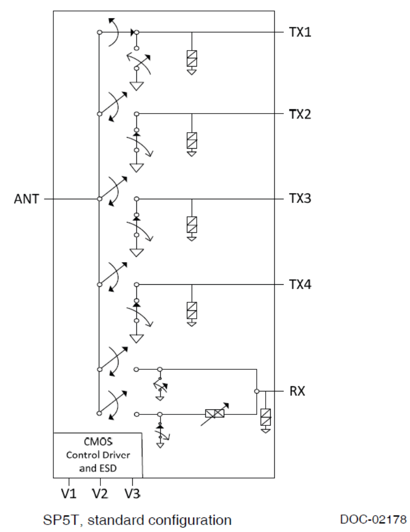


Figure 2. SP5T configuration functional diagram

Product description

The PE42850 is a HaRP™ technology-enhanced SP5T high-power RF switch supporting wireless applications up to 1 GHz. It offers maximum power handling of 42.5 dBm continuous wave (CW). It delivers high linearity and excellent harmonics performance. It has both standard and attenuated Rx modes. No blocking capacitors are required if no DC voltage is present on the RF ports.

pSemi manufactured the PE42850 using its UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42850 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (V1, V2, and V3)	V_{CTRL}	-0.3	3.6	V
TX RF input power (50Ω)(1)	$P_{IN\text{-}TX}$	–	45	dBm
TX RF input power (VSWR ≤ 8:1)(1)	$P_{IN\text{-}TX}$	–	40	dBm
ANT RF input power, unbiased (VSWR ≤ 8:1)	$P_{IN\text{-}ANT}$	–	27	dBm
RX RF input power (VSWR ≤ 8:1)(1)	$P_{IN\text{-}RX}$	–	27	dBm
Storage temperature range	T_{ST}	-65	150	°C
Maximum case temperature	T_{CASE}	–	85	°C
Peak maximum junction temperature (10 seconds max)	T_J	–	200	°C
ESD voltage HBM, all pins(2)	$V_{ESD,HBM}$	–	1500	V
ESD Voltage MM, all pins(3)	$V_{ESD,MM}$	–	200	V

1. Supply biased.
2. Human Body Model (MIL-STD 883 Method 3015).
3. Machine Model (JEDEC JESD22-A115).

Recommended operating conditions

Table 2 lists the PE42850 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42850 operating conditions[1]

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage (normal mode, V_{SS_EXT} = 0V)	V_{DD}	2.3	–	5.5	V
Supply voltage (bypass mode, V_{SS_EXT} = –3.4V, V_{DD} ≥ 3.4V for full spec. compliance)	V_{DD}	2.7	3.4	5.5	V
Negative supply voltage (bypass mode)	V_{SS_EXT}	-3.6	–	-3.2	V
Supply current (normal mode, V_{SS_EXT} = 0V)	I_{DD}	–	130	200	µA
Supply current (bypass mode, V_{SS_EXT} = –3.4V)	I_{DD}	–	50	80	µA
Negative supply current (bypass mode, V_{SS_EXT} = –3.4V)	I_{SS}	-40	-16	–	µA
Digital input high (V1, V2, and V3)	V,	1.17	–	3.6	V
Digital input low (V1, V2, and V3)	V_{IL}	-0.3	–	0.6	V
TX RF input power (VSWR ≤ 8:1)[2][3]	P_{IN-TX}	–	–	40	dBm
TX RF input power (50Ω source/load impedance)[2][3]	P_{IN-TX}	–	–	45	dBm
TX RF input power (50Ω source/load impedance, CW)[2]	P_{IN-TX}	–	–	42.5	dBm
ANT RF input power, unbiased (VSWR ≤ 8:1)	P_{IN-ANT}	–	–	27	dBm
RX RF input power (VSWR ≤ 8:1)[2]	P_{IN-RX}	–	–	27	dBm
Operating temperature range (case)	T_{OP}	-40	–	85	°C
Operating junction temperature	T_J	–	–	135	°C

1. In a 2TX–1RX SP3T configuration, TX1 and TX2 are tied and TX3 and TX4 are tied, respectively. For the SP3T performance data, see *Application Note 35: Configuring the PE42850 as an SP3T or SP5T*.
2. Supply biased.
3. Pulsed, 10% duty cycle of 4620 µs period.

Electrical specifications

Table 3 lists the PE42850 key electrical specifications at -40 to +85 °C, V_{DD} = 2.3–5.5V, V_{SS_EXT} = 0V or V_{DD} = 3.4–5.5V, V_{SS_EXT} = -3.4V (Z_S = Z_L = 50Ω), unless otherwise specified.(1)

Table 3. PE42850 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	30	–	1000	MHz
Insertion loss(2)	ANT–TX	Active TX port 1, 2, 3, or 4 at rated power (–40 °C, +25 °C)				
		30–520 MHz	–	0.25	0.30	dB
		520–1000 MHz	–	0.35	0.45	
	ANT–TX	Active TX port 1, 2, 3 or 4 at rated power (+85 °C)				
		30–520 MHz	–	0.30	0.35	dB
		520–1000 MHz	–	0.45	0.55	
Insertion loss, un-attenuated state(2)	ANT–RX	Active RX port (–40 °C, +25 °C)				
		30–520 MHz	–	0.50	0.60	dB
		520–1000 MHz	–	0.65	0.80	
	ANT–RX	Active RX port (+85 °C)				
		30–520 MHz	–	0.60	0.70	dB
		520–1000 MHz	–	0.70	0.85	
	ANT–RX	1575 MHz for GPS RX, < –10 dBm, +25 °C	–	1	1.2	dB
Insertion loss, un-attenuated state(2)	ANT–RX	Active RX port, 30–1000 MHz	15.2	16	16.8	dB
Isolation, supply biased	TX–TX	30–520 MHz	33	36	–	dB
		520–1000 MHz	29	30	–	
	TX–RX	30–520 MHz	34	36	–	dB
		520–1000 MHz	29	30	–	
Unbiased isolation V_{DD}, V1, V2, V3 = 0V	ANT–TX	+27 dBm	6	–	–	dB
	ANT–RX	+27 dBm	14	–	–	dB
Return loss(2)	ANT–TX	30–520 MHz	21	28	–	dB
		520–1000 MHz	15	17	–	
	ANT–RX	Un-attenuated state				
		30–520 MHz	22	27	–	dB
		520–1000 MHz	18	22	–	

Parameter	Path	Condition	Min	Typ	Max	Unit
	ANT–RX	1575 MHz for GPS RX, < –10 dBm, +25 °C	10	14	–	dB
	ANT–RX	Attenuated state, optimized without attenuator engaged				
		30–520 MHz	16	21	–	dB
		520–1000 MHz	13	18	–	
Second and third harmonic (< 1.15:1 VSWR)	TX	30–520 MHz at +40.0 dBm	–	-90	-81	dBc
		521–870 MHz at +38.5 dBm				
		871–1000 MHz at +37.5 dBm				
Second and third harmonic (< 8:1 VSWR)	TX	Pulsed signal at 10% duty cycle(3)				
		30–520 MHz at +40.0 dBm	–	-82	-74	dBc
		521–870 MHz at +38.5 dBm				
		871–1000 MHz at +37.5 dBm				
Second and third harmonic (50Ω source/load impedance)	TX	30–1000 MHz at +45.0 dBm (pulsed signal, at 10% duty cycle)(3)	–	-80	-71	dBc
		30–1000 MHz at +42.5 dBm (CW)	–	-84	-75	
Input 0.1dB compression point(4)	ANT–TX	1000 MHz	–	45.5	–	dBm
IIP3	RX	Un-attenuated state	42	–	–	dBm
		Attenuated state	33	–	–	
Settling time	–	From 50% control until harmonics within specifications	–	30	70	μs
Switching time(5)	–	50% CTRL to 90% or 10% RF	–	15	–	μs

1. In a 2TX–1RX SP3T configuration, TX1 and TX2 are tied and TX3 and TX4 are tied, respectively. For the SP3T performance data, see *Application Note 35: Configuring the PE42850 as an SP3T or SP5T*.
2. To improve impedance matching, narrow trace widths are used near each port. For details, see the evaluation board layouts (Figure 21) and schematic (Figure 22).
3. 10% of 4620 μs period.
4. The input 0.1dB compression point is a linearity figure of merit. For the RF input power (P_{IN}), see Table 2.
5. The PE42850 has a maximum 10 kHz switching rate when the internal negative voltage generator is used (pin 16 = GND). The rate at which the PE42850 can be switched is only limited to the switching time if an external negative supply is provided (pin 16 = V_{SS_EXT}). The switching frequency describes the time duration between switching events. The switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Optional external V_{SS} control (V_{SS_EXT})

For proper operation, the V_{SS_EXT} control pin (pin 16) must be grounded or tied to the V_{SS} voltage specified in Table 2. When the V_{SS_EXT} control pin is grounded, the FETs in the switch are biased with an internal voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Spurious performance

The PE42850 typical spurious performance is –130 dBm when V_{SS_EXT} = 0V (pin 16 = GND). To improve performance, disable the internal negative voltage generator by setting V_{SS_EXT} = –3.4V.

Thermal data

Though the insertion loss for the PE42850 is quite low, when handling high power RF signals, the junction temperature can rise significantly.

VSWR conditions that present short circuit loads to the part can cause significantly more power dissipation than with proper matching.

Make special consideration in the PCB design to properly dissipate the heat away from the part and maintain the 85 °C maximum case temperature. Use best design practices for high-power QFN packages: multi-layer PCBs with thermal vias in a thermal pad soldered to the slug of the package. Take extreme care to alleviate solder voiding under the part.

Table 4. Theta JC

Parameter	Typ	Unit
Theta JC (+85 °C)	20	°C/W

SP5T control logic

Table 4. PE42850 truth table

Path	V3	V2	V1
ANT–RX attenuated	L	L	L
ANT–TX1	L	L	H
ANT–TX2	L	H	L
ANT–TX1 and TX2(*)	L	H	H
ANT–RX	H	L	L
ANT–TX3	H	L	H
ANT–TX4	H	H	L
ANT–TX3 and TX4(*)	H	H	H

* In a 2TX–1RX SP3T configuration, TX1 and TX2 are tied and TX3 and TX4 are tied, respectively. For the SP3T performance data, see *Application Note 35: Configuring the PE42850 as an SP3T or SP5T*.

Typical performance data

Figure 3–Figure 20 show the typical performance data at +25 °C and V_{DD} = 3.4V, unless otherwise specified.

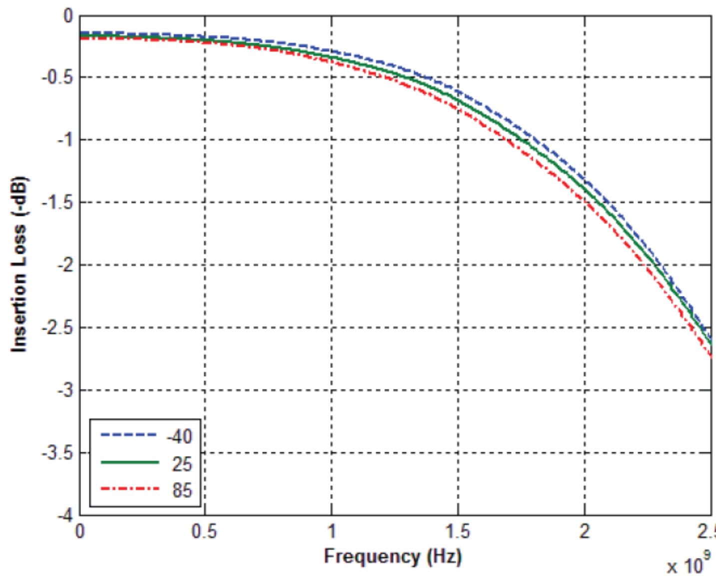


Figure 3. Insertion loss vs. temperature (TX)

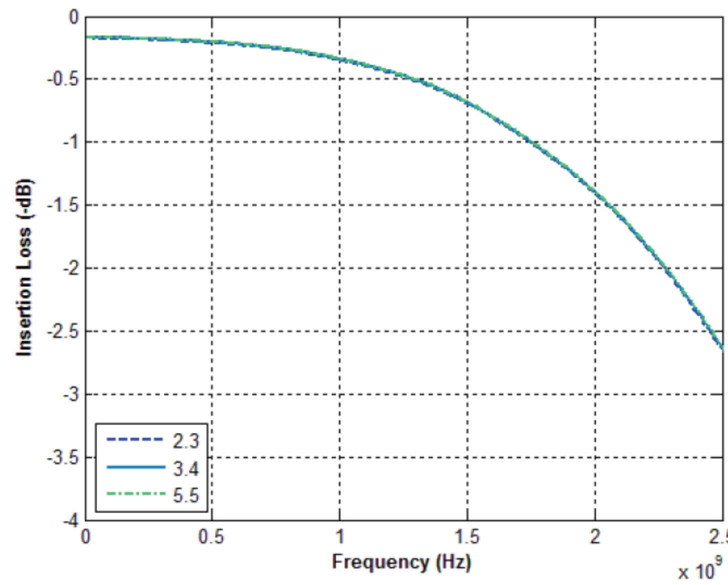


Figure 4. Insertion loss vs. V_{DD} (TX)

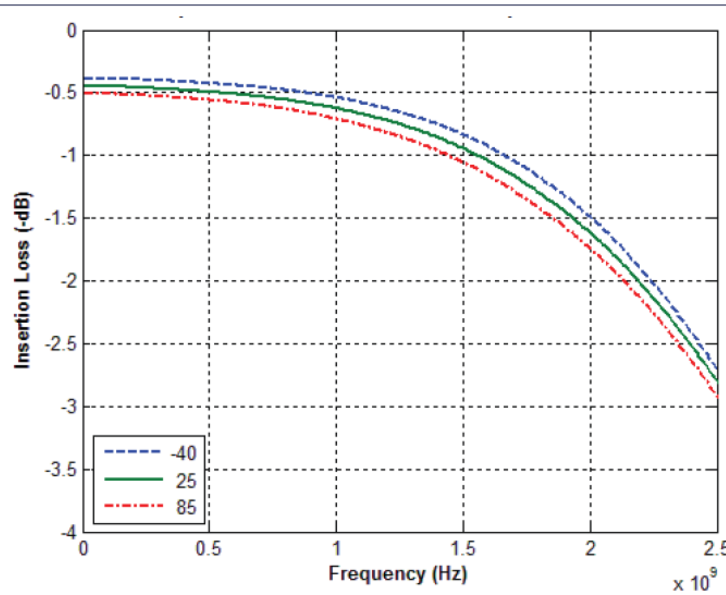


Figure 5. Insertion loss vs. temperature (RX, un-attenuated)

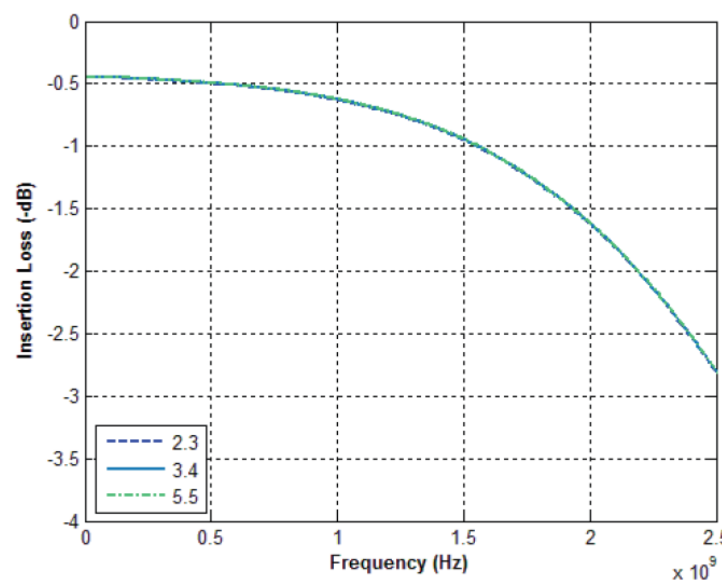


Figure 6. Insertion loss vs. V_{DD} (RX, un-attenuated)

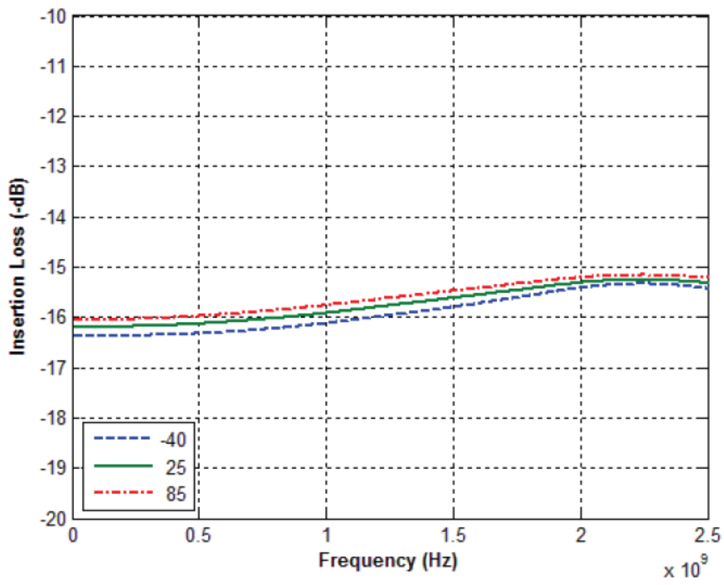


Figure 7. Insertion loss vs. temperature (RX, attenuated)

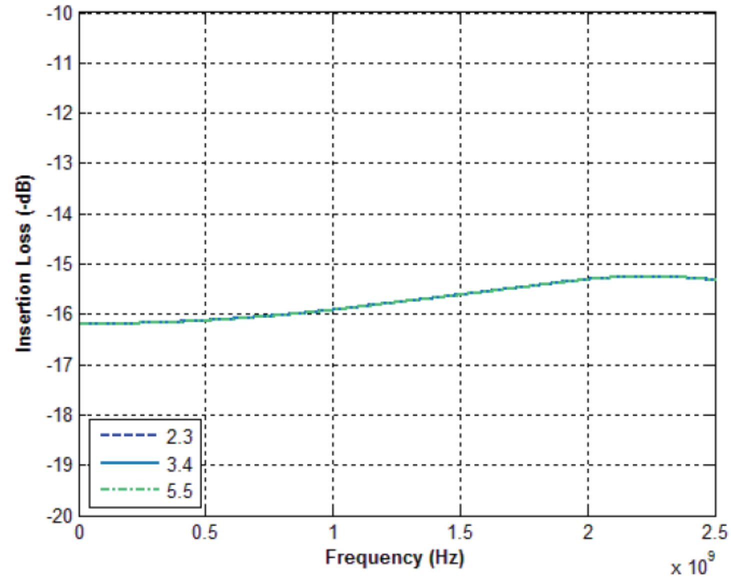


Figure 8. Insertion loss vs. V_{DD} (RX, attenuated)

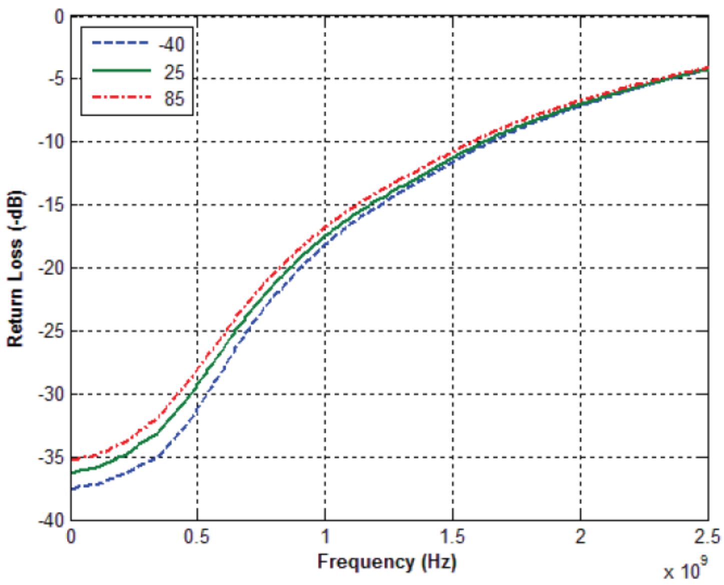


Figure 9. Return loss vs. temperature (ANT)

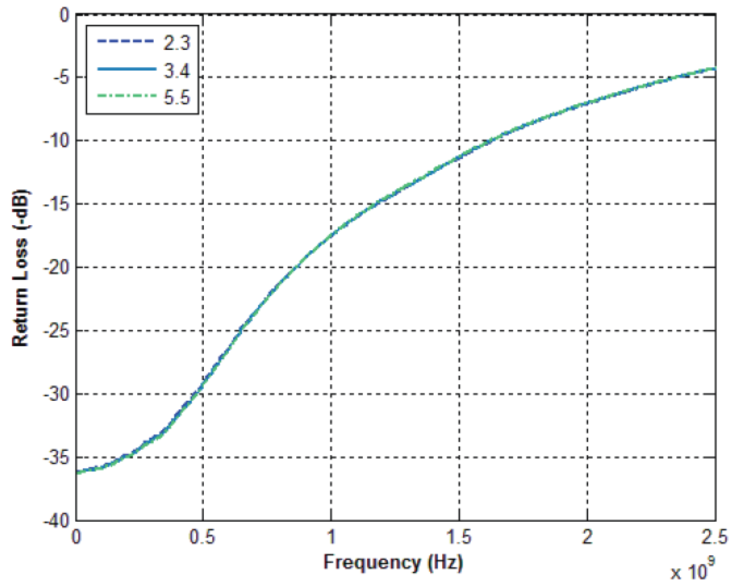


Figure 10. Return loss vs. V_{DD} (ANT)

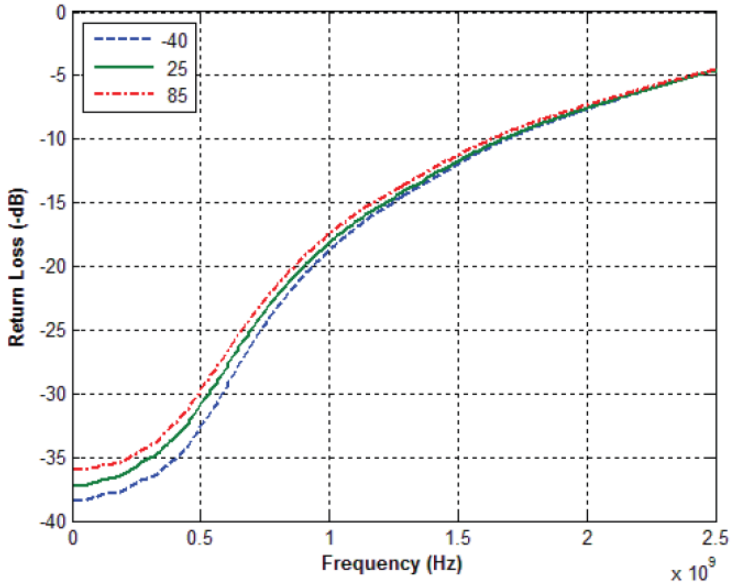


Figure 11. Return loss vs. temperature (TX)

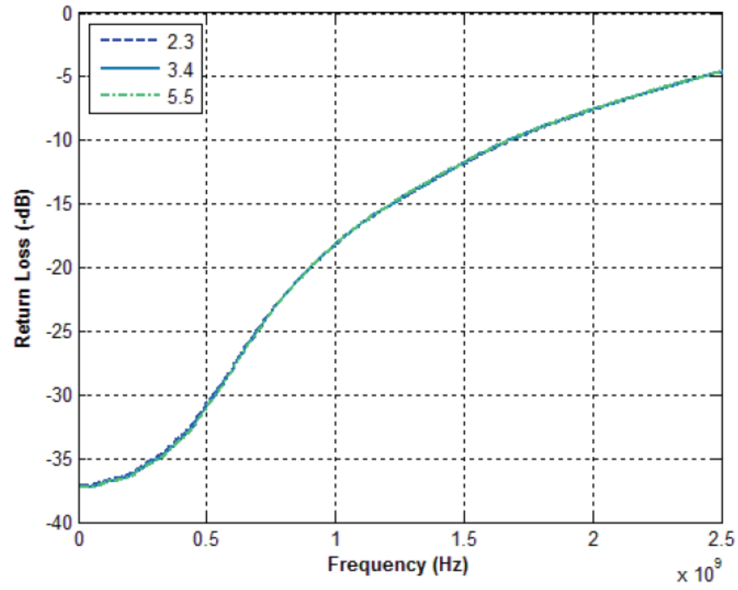


Figure 12. Return loss vs. V_{DD} (TX)

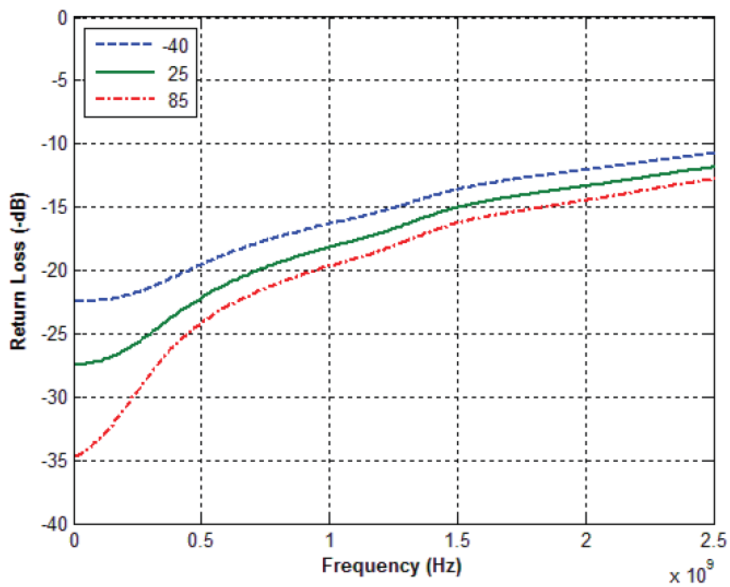


Figure 13. Return loss vs. temperature (RX, attenuated)

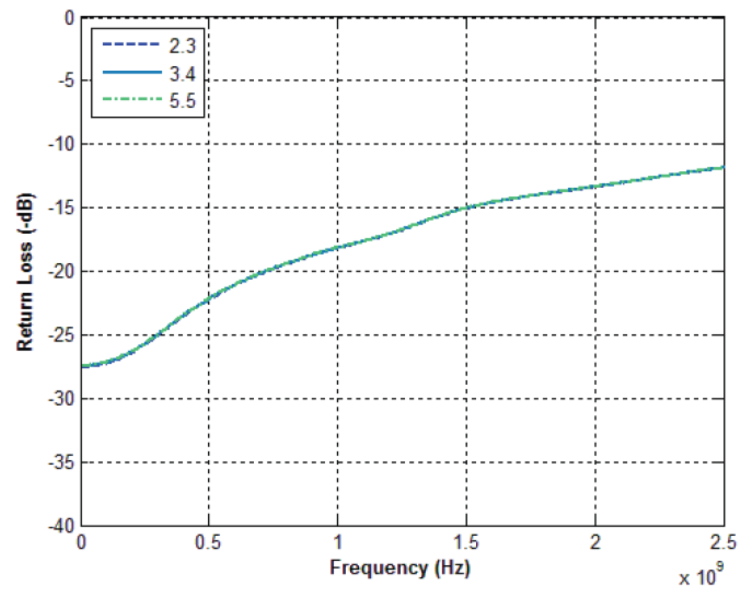


Figure 14. Return loss vs. V_{DD} (RX, attenuated)

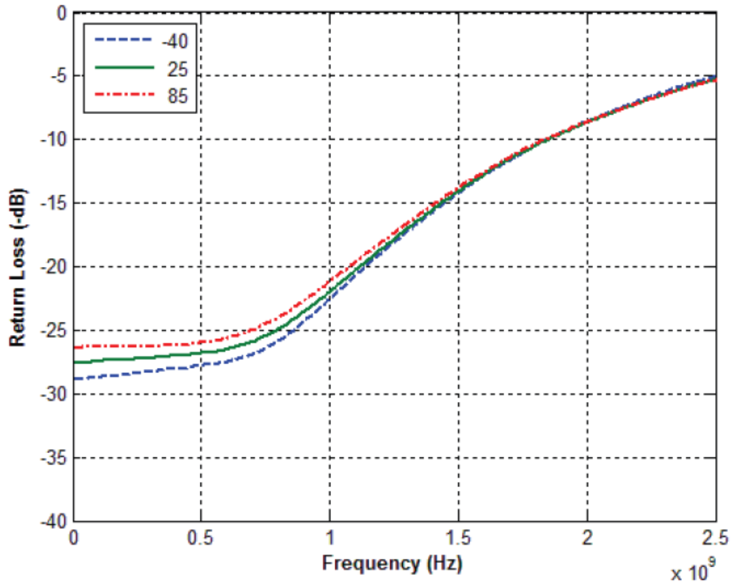


Figure 15. Return loss vs. temperature (RX, un-attenuated)

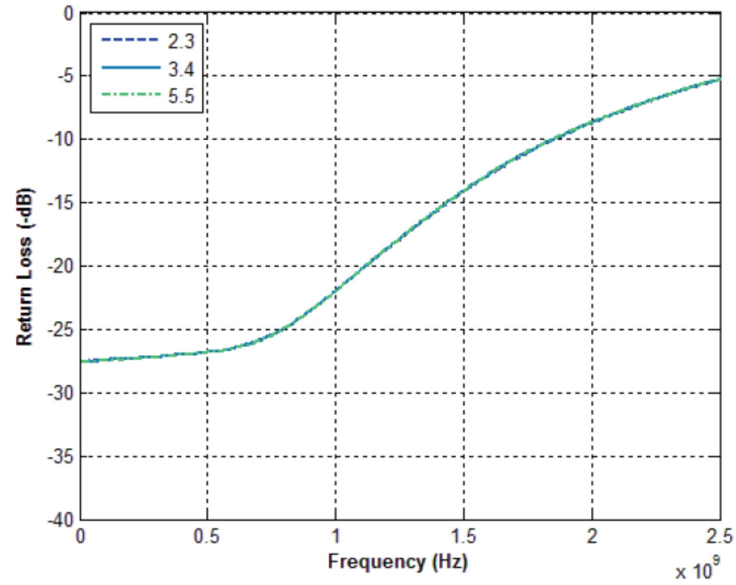


Figure 16. Return loss vs. V_{DD} (RX, un-attenuated)

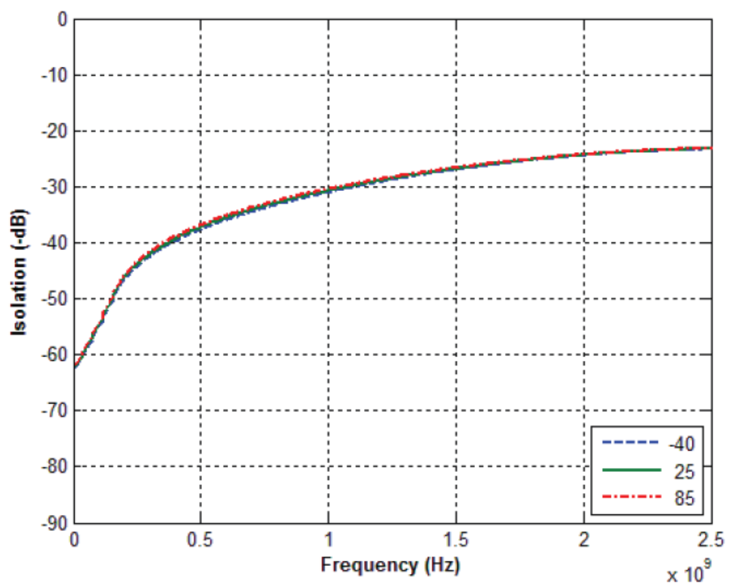


Figure 17. Isolation vs. temperature (TX–TX)

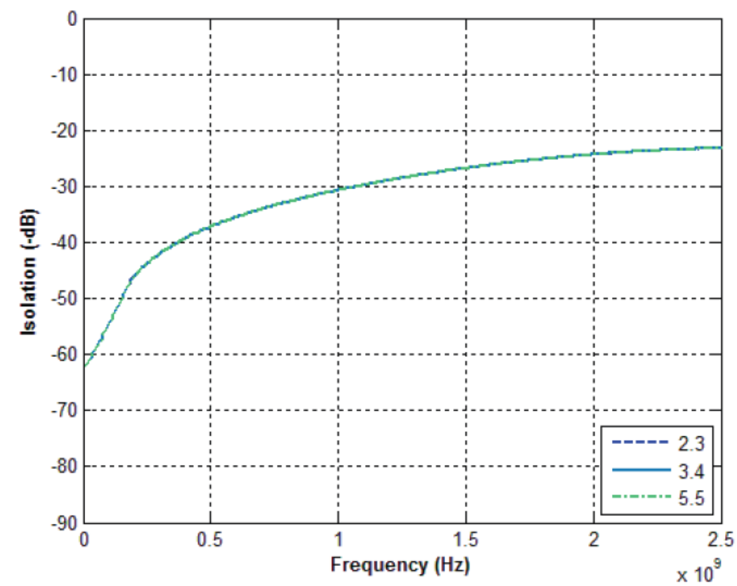


Figure 18. Isolation vs. V_{DD} (TX–TX)

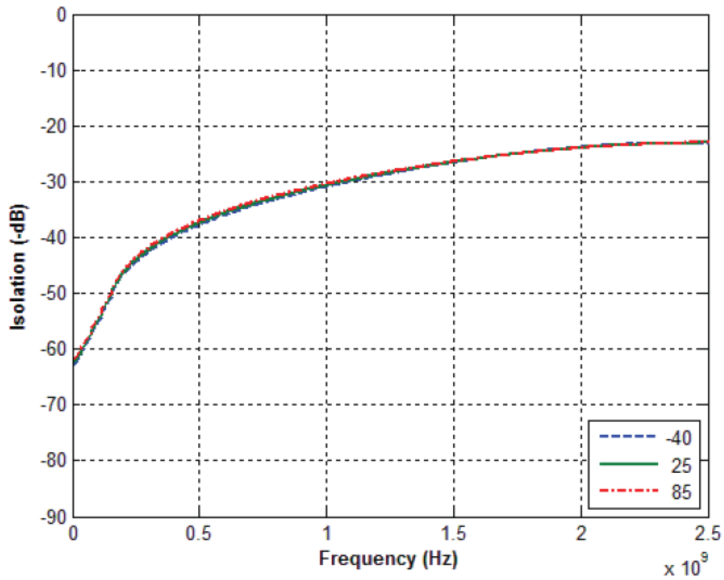


Figure 19. Isolation vs. temperature (TX–RX)

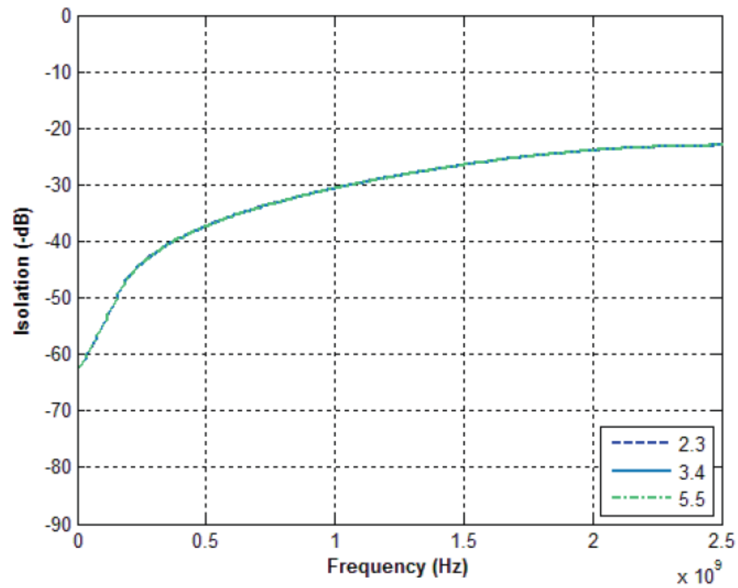


Figure 20. Isolation vs. V_{DD} (TX–RX)

Evaluation kit

pSemi designed the PE42850 evaluation Kit board to ease your evaluation of the PE42850 RF switch.

The evaluation board in Figure 5 was designed to test the PE42850 in the 5T configuration. DC power is supplied through J10, with V_{DD} on pin 9, and GND on the entire lower row of even numbered pins. To evaluate a switch path, add or remove jumpers on V1 (pin 3), V2 (pin 5), and V3 (pin 7) using Table 5. Adding a jumper pulls the CMOS control pin low and removing it allows the on-board pull-up resistor to set the CMOS control pin high. J10 pins 11 and 13 are not connected.

The ANT port connects through a 50Ω transmission line via the top SMA connector, J1. The RX and TX paths also connect through 50Ω transmission lines via SMA connectors. A 50Ω through transmission line is available via SMA connectors J8 and J9. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated. An open-ended 50Ω transmission line is also provided for calibration at J7, if needed.

The narrow trace widths used near each part improve impedance matching.

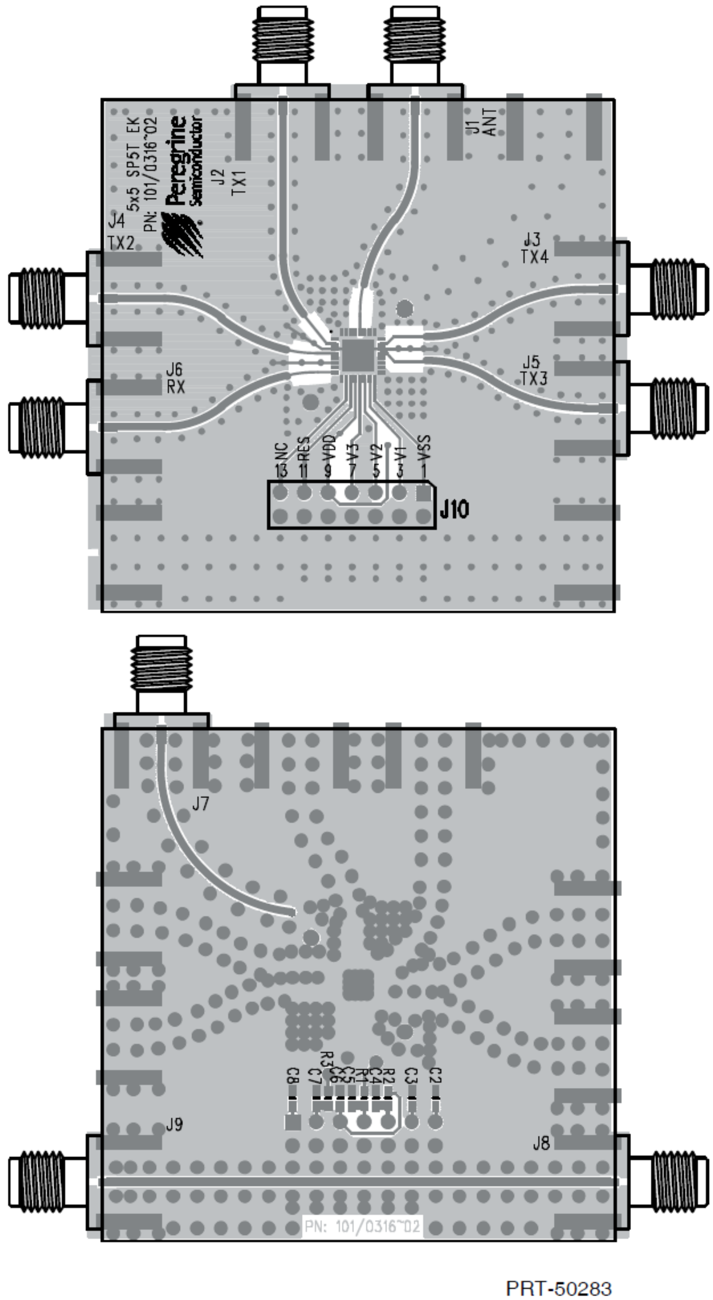
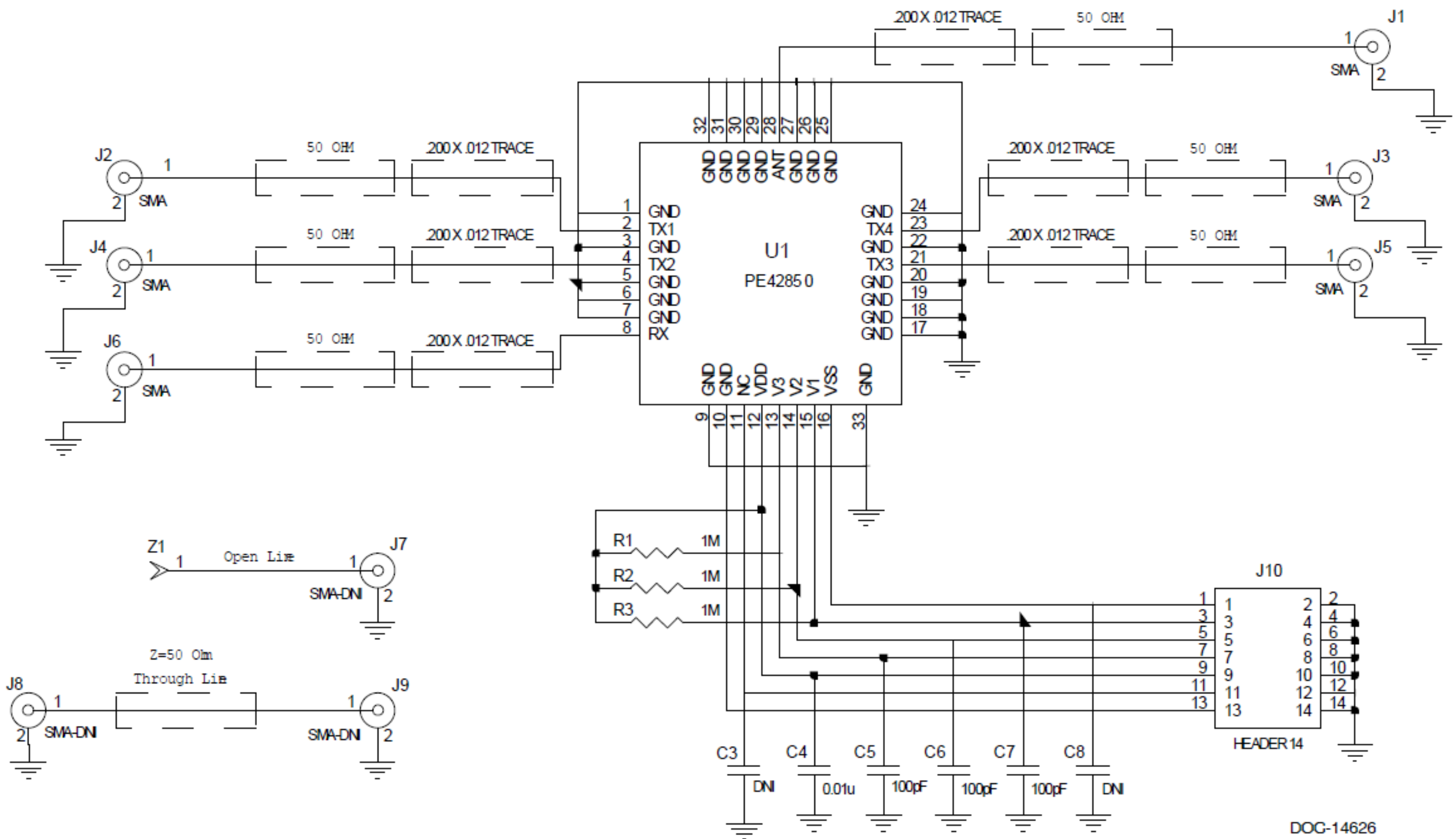


Figure 21. Evaluation board layouts

Evaluation board schematic



Notes: 1. Use 101-0316-02 PCB
2. 32 mil Width, 10 mil Gaps, 28 mil Core, 4.3 Er, and 2.1 mil Cu

Figure 22. Evaluation board schematic

Pin information

Figure 23 shows the PE42850 pin map for the 32-lead 5 × 5 mm QFN package, and Table 5 lists the description for each pin.

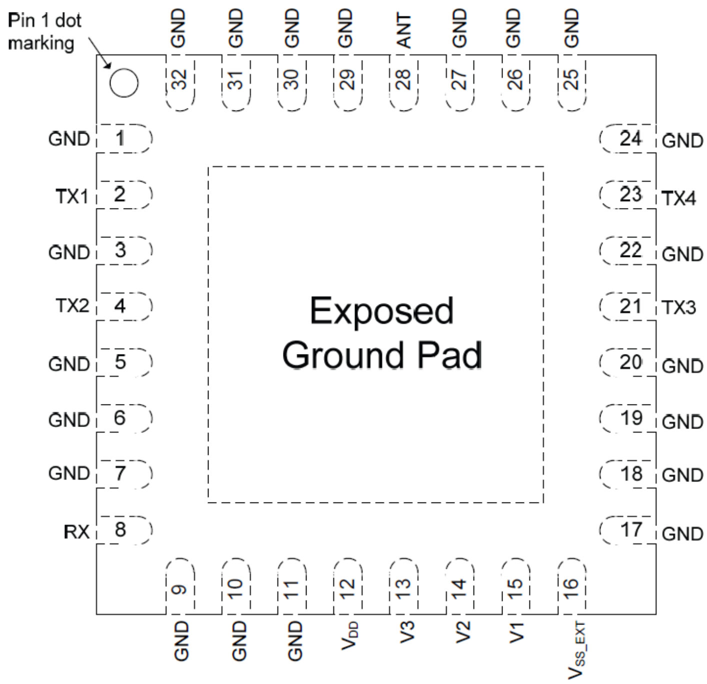


Figure 23. Pin configuration (top view)

Pins 1, 3, 5, 7, 9, 10, 17, 19, 20, 22, 24, 26, 27, 29, 30, and 31 can be N/C if deemed necessary.

Table 5. PE42850 pin descriptions

Pin no.	Pin name	Description
1, 3, 5–7, 9–11, 17–20, 22, 24–27, 29–32	GND	Ground
2(1)	TX1	Transmit pin 1
4(1)(2)	TX2	Transmit pin 2
8(1)	RX	Receive pin
12	V_{DD}	Supply voltage (nominal 3.3V)
13	V3	Digital control logic input 3
14	V2	Digital control logic input 2
15	V1	Digital control logic input 1
16(3)	V_{SS_EXT}	External V_{SS} negative voltage control
21(1)	TX3	Transmit pin 3
23(1)(2)	TX4	Transmit pin 4
28(1)	ANT	Antenna pin
Pad	GND	Exposed pad. Ground for proper operation.

1. RF pins 2, 4, 8, 21, 23, and 28 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2. To operate the PE42850 as a 2TX–1RX SP3T, tie TX1 to TX2 and TX3 to TX4, respectively. For the SP3T performance data, see *Application Note 35: Configuring the PE42850 as an SP3T or SP5T*.
3. Use V_{SS_EXT} (pin 16, $V_{SS\_EXT} = –V_{DD}$) to bypass and disable the internal negative voltage generator. Connect V_{SS_EXT} (pin 16) to GND (V_{SS_EXT} = 0V) to enable the internal negative voltage generator.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42850 moisture sensitivity level rating for the 32-lead 5 × 5 mm QFN package is MSL3.

Package drawing

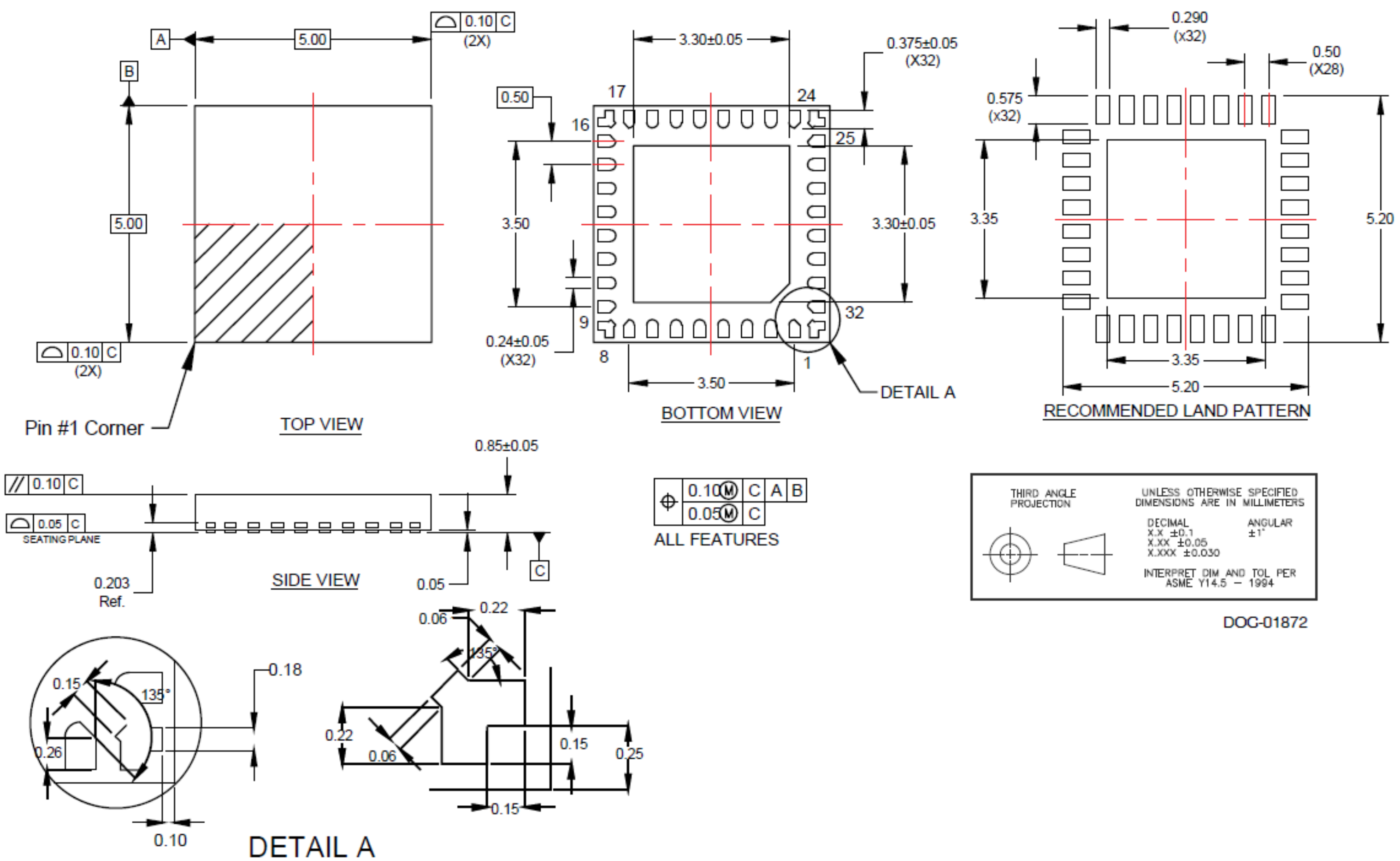


Figure 24. Package mechanical drawing for the 32-lead 5 × 5 mm QFN package

Top-marking specification

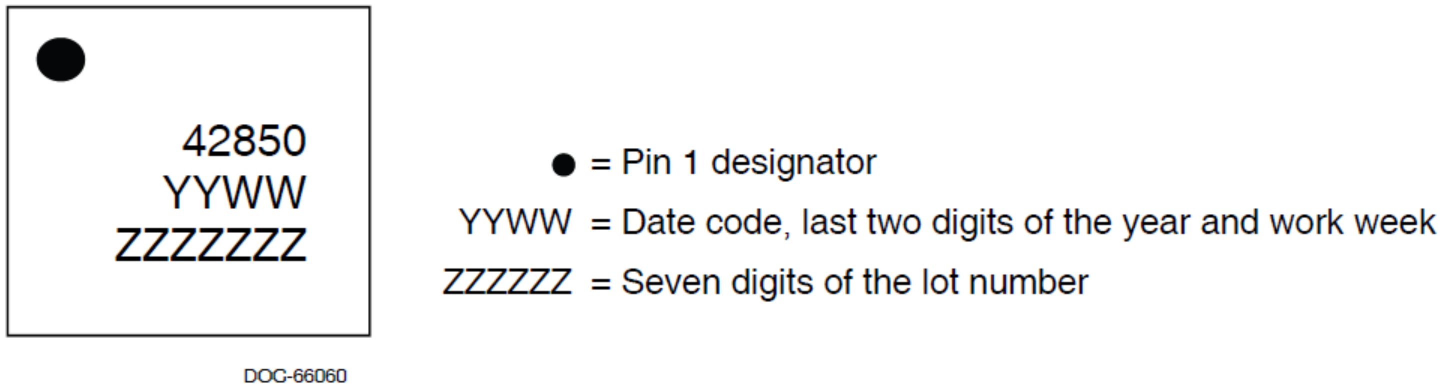


Figure 25. PE42850 package marking specification

Tape and reel specification

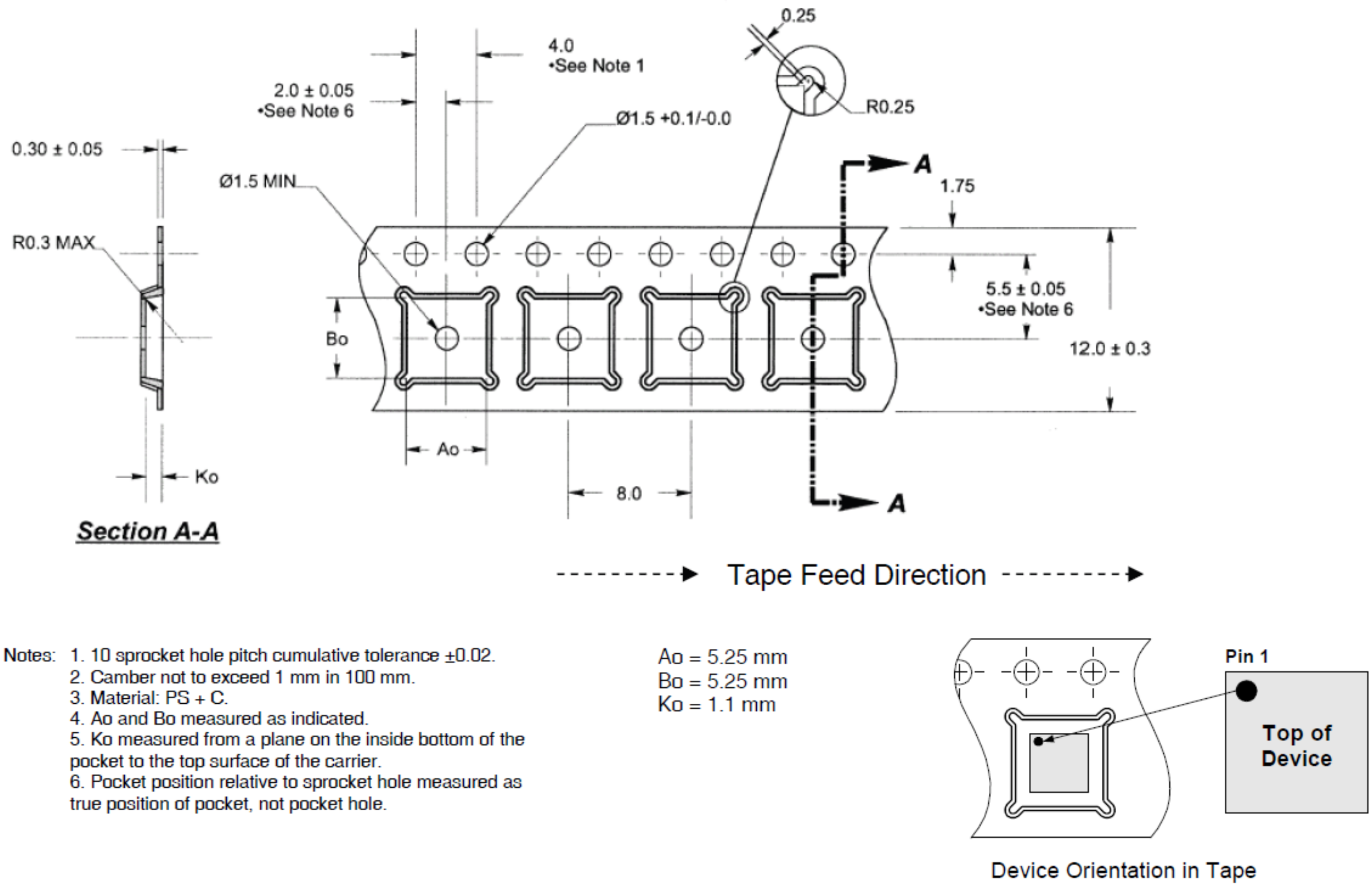


Figure 26. Tape and reel specification for the 32-lead 5 × 5 mm QFN package

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE42850B-X	PE42850 SP5T RF switch	Green 32-lead 5 × 5 mm QFN	500 units/T&R
EK42850-04	PE42850 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

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