PE42441

Document category: Product Specification

UltraCMOS® SP4T RF Switch, 10 MHz–8 GHz

Features

- Four symmetric 50Ω absorptive ports
- High isolation:
  - 45 dB @ 3 GHz
  - 39 dB @ 6 GHz
  - 31 dB @ 8 GHz
- Low insertion loss:
  - 0.8 dB @ 3 GHz
  - 1.0 dB @ 6 GHz
  - 1.2 dB @ 8 GHz
- High linearity:
  - 58 dBm IIP3 @ 8 GHz
  - 110 dBm IIP2 @ 8 GHz
- 1.8V control logic compatible
- ESD performance:
  - 2000V HBM on all pins
  - 100V MM on all pins
  - 1000V CDM on all pins
- Packaging: 32-lead 5 × 5 mm LGA

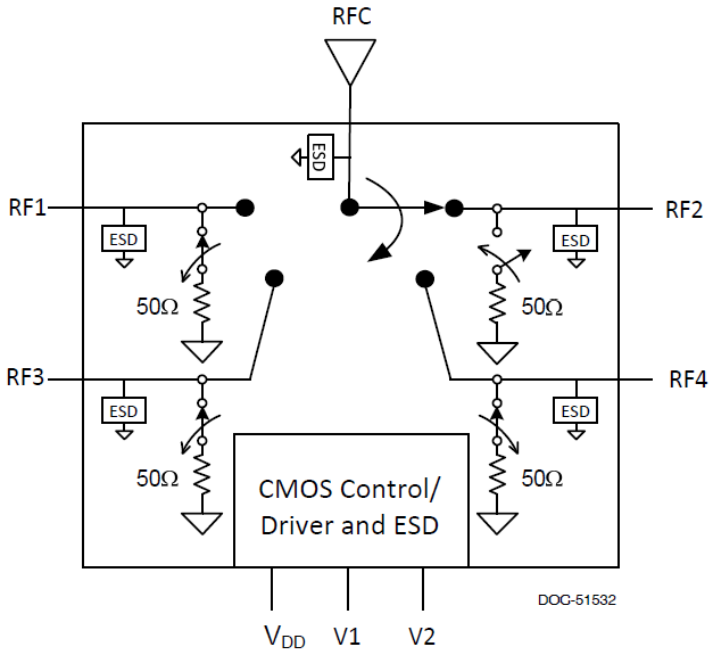


Figure 1. PE42441 functional block diagram

Product description

The PE42441 is a HaRP™ technology-enhanced absorptive SP4T RF switch designed for use in various switching applications spanning multiple markets including wireless infrastructure, broadband, and wireless connectivity.

This switch has four symmetric RF ports and delivers low insertion loss and exceptional isolation. The on-chip CMOS decode logic facilitates a two-pin low-voltage CMOS control interface. In addition, no external blocking capacitors are required if 0 VDC is present on RF ports.

The PE42441 is manufactured using pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS® process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Headquarters: 9369 Carroll Park Dr, San Diego, CA 92121

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42441 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	4.0	V
Digital input voltage (V1, V2)	V_{CTRL}	-0.3	4.0	V
Maximum input power (10–8000 MHZ)	$P_{MAX,ABS}$	–	See Figure 2	dBm
Storage temperature range	T_{ST}	-50	+150	°C
ESD voltage HBM, all pins[1]	$V_{ESD,HBM}$	–	2000	V
ESD voltage MM, all pins[2]	$V_{ESD,MM}$	–	100	V
ESD voltage CDM, all pins[3]	$V_{ESD,CDM}$	–	1000	V

1. Human Body Model (MIL-STD 883 Method 3015.7)
2. Machine Model (JEDEC JESD22-A115-A)
3. Charged Device Model (JEDEC JESD22-C101)

Recommended operating conditions

Table 2 lists the PE42441 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42441 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.55	V
Supply current	I_{DD}	–	90	160	µA
Digital input high (V1, V2)	V_{IH}	1.2	1.5	V_{DD}	V
Digital input low (V1, V2)	V_{IL}	0	0	0.4	V
Digital input current	I_{CTRL}	–	–	1	µA
RF input power, CW (10–8000 MHZ)(*)	$P_{MAX,CW}$	–	–	See Figure 2	dBm
RF input power into terminated ports, CW (10–8000 MHZ)	$P_{MAX,TERM}$	–	–	+20	dBm
Operating temperature range	T_{OP}	-40	–	+85	°C

* 100% duty cycle (–40 to +85 °C, 1:1 VSWR).

Electrical specifications

Table 3 lists the PE42441 key electrical specifications at +25 °C and V_{DD} = 3.3V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. PE42441 electrical specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operating frequency	–	–	10	–	8000	MHz
Insertion loss	RFC–RFx	10 MHz–3000 MHz 3000 MHz–6000 MHz 6000 MHz–7500 MHz 7500 MHz–8000 MHz	–	0.8 1.0 1.1 1.2	1.1 1.3 1.5 1.6	dB
Isolation (active port to terminated port)	RFx–RFx	10 MHz–3000 MHz 3000 MHz–6000 MHz 6000 MHz–7500 MHz 7500 MHz–8000 MHz	40 34 27 25	45 39 32 31	–	dB
Isolation (common port to active port)	RFC–RFx	10 MHz–3000 MHz 3000 MHz–6000 MHz 6000 MHz–7500 MHz 7500 MHz–8000 MHz	40 28 24 21	45 33 29 27	–	dB
Return loss (common port)	RFx	10 MHz–3000 MHz 3000 MHz–6000 MHz 6000 MHz–7500 MHz 7500 MHz–8000 MHz	–	23 18 14 13	–	dB
Return loss (active port)	RFx	10 MHz–3000 MHz 3000 MHz–6000 MHz 6000 MHz–7500 MHz 7500 MHz–8000 MHz	–	23 18 17 16	–	dB
Return loss (terminated port)	RFx	10 MHz–3000 MHz 3000 MHz–6000 MHz 6000 MHz–7500 MHz 7500 MHz–8000 MHz	–	18 13 11 10	–	dB
Input 0.1 dB compression point[1]	RFC–RFx	10 MHz–8000 MHz	–	31	–	dBm
Input IP3	RFC–RFx	8000 MHz	–	58	–	dBm
Input IP2	RFC–RFx	8000 MHz	–	110	–	dBm
Switching time[2]	–	50% CTRL to 90% or 10% RF	–	5	8	µs
Settling time	–	50% CTRL to 0.05 dB final value (–40 to +85°C) rising edge 50% CTRL to 0.05 dB final value (–40 to +85°C) falling edge	–	14 15	18 45	µs

Parameter	Path	Condition	Min	Typ	Max	Unit

1. The input 0.1 dB compression point is a linearity figure of merit. For the operating RF input power (50Ω), see Table 2.
2. The PE42441 has a maximum 25 kHz switching rate. The switching frequency describes the time duration between switching events. The switching time is the time duration between the point that the control signal reaches 50% of the final value and the point that the output signal reaches within 10% or 90% of its target value.

Spurious performance

The PE42441 spurious performance is -159 dBm/Hz.

SP4T control logic

Table 4. PE42441 truth table

State	V1	V2
RF1 on	0	0
RF2 on	1	0
RF3 on	0	1
RF4 on	1	1

Power de-rating curve

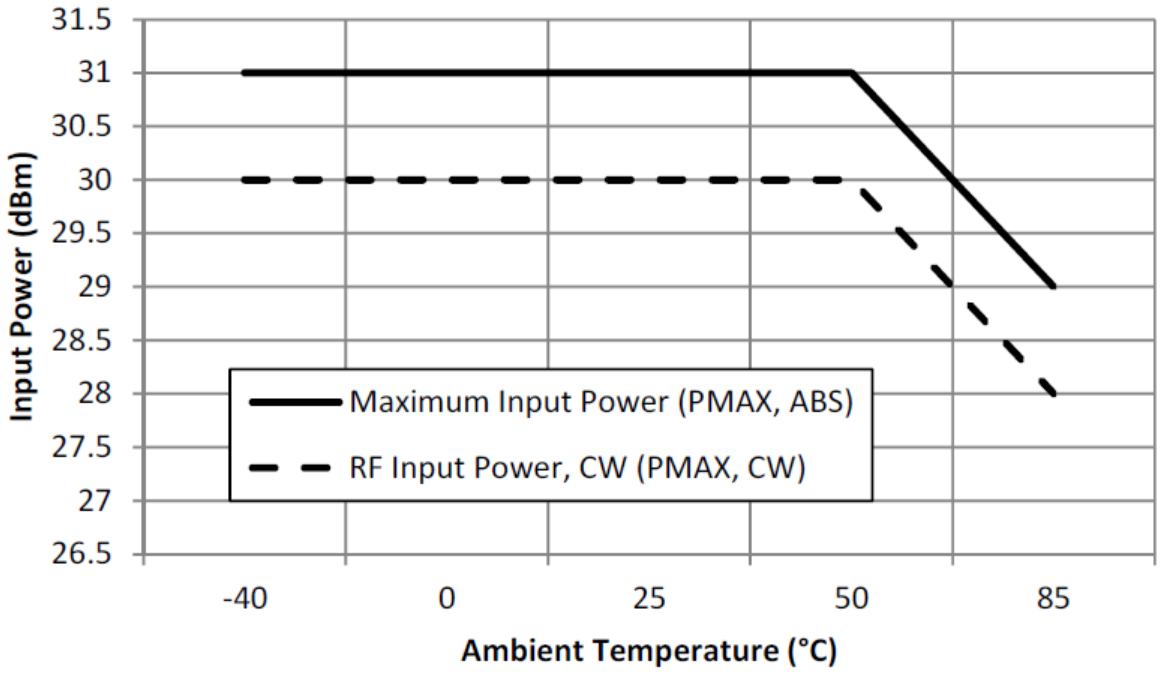


Figure 2. Power de-rating curve vs. temperature

Typical performance data

Figure 3–Figure 16 show the typical performance data at +25 °C and V_{DD} = 3.3V, unless otherwise specified.

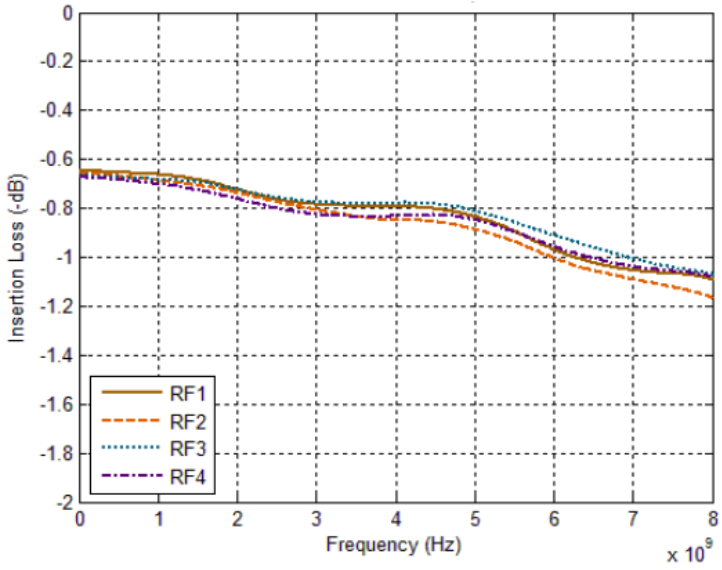


Figure 3. Insertion loss (RFC–RFx)

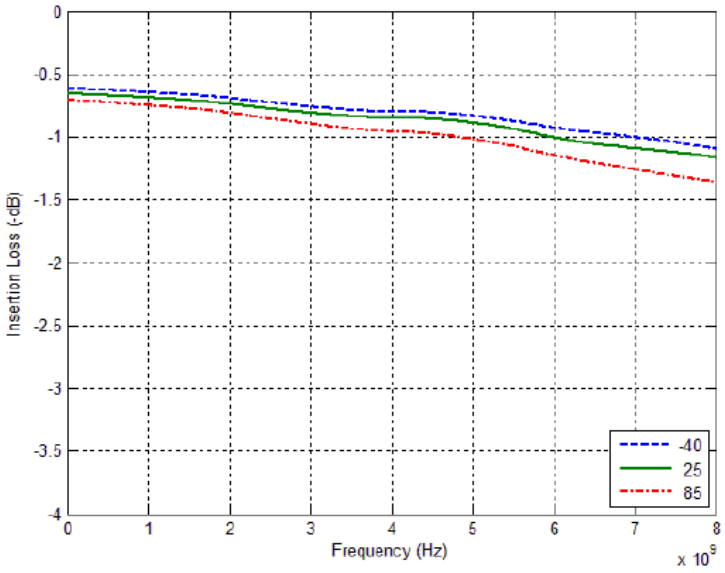


Figure 4. Insertion loss vs. temperature (RFC–RFx)

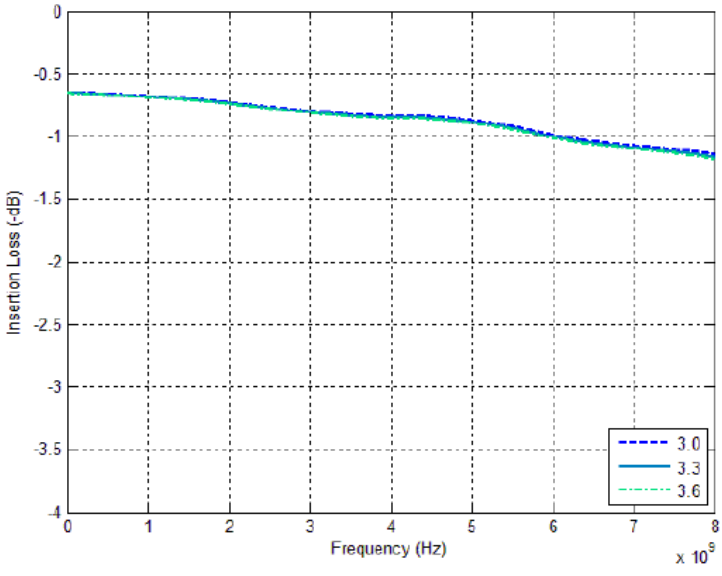


Figure 5. Insertion loss vs. V_{DD} (RFC–RFx)

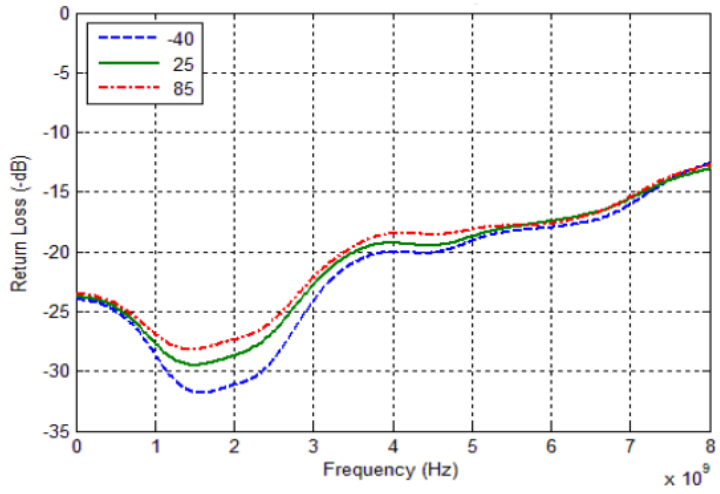


Figure 6. RFC port return loss vs. temperature

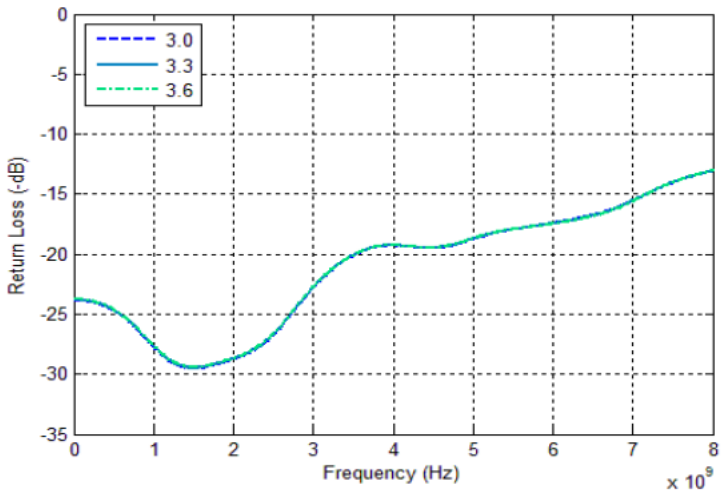


Figure 7. RFC port return loss vs. V_{DD}

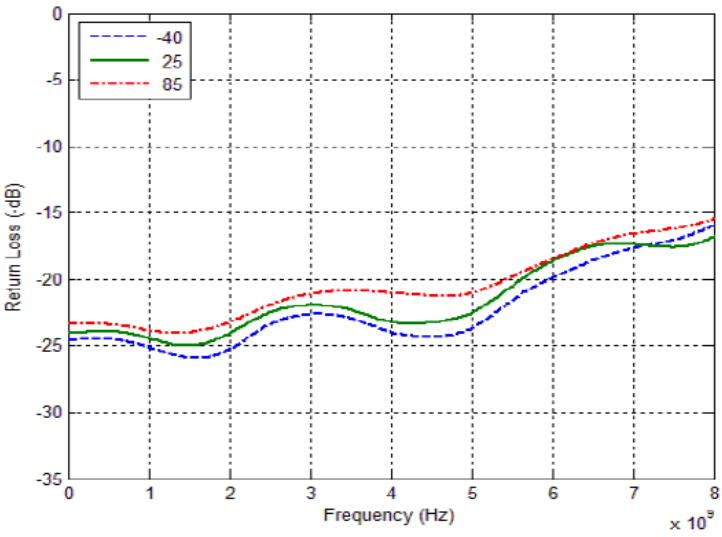


Figure 8. Active port return loss vs. temperature

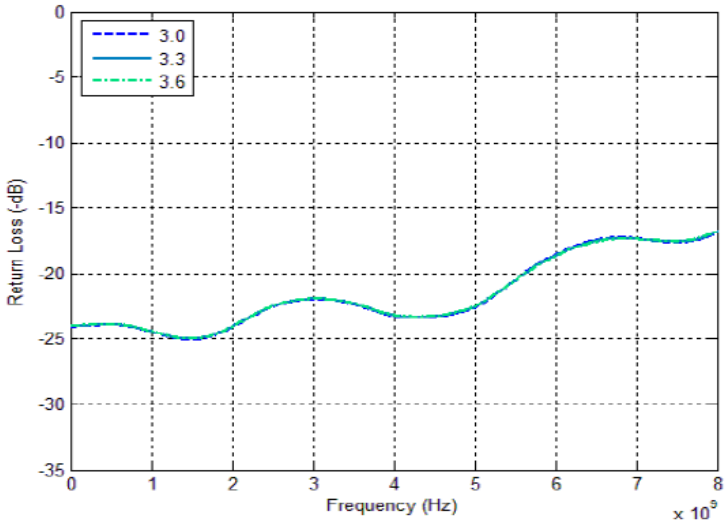


Figure 9. Active port return loss vs. V_{DD}

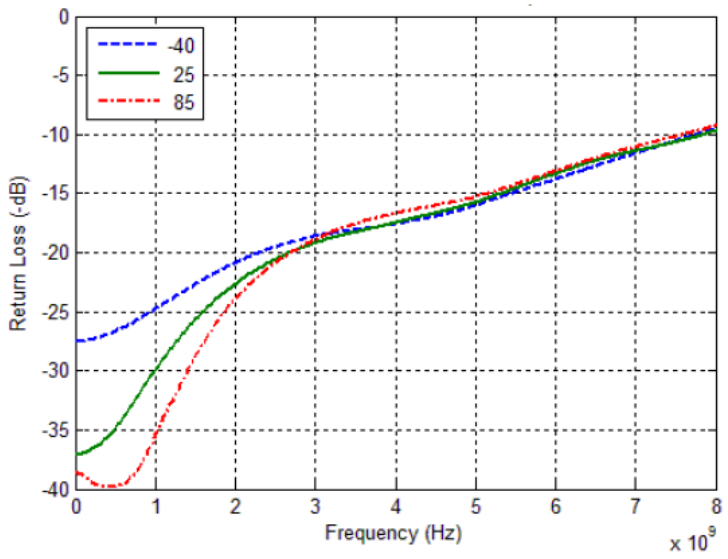


Figure 10. Terminated port return loss vs. temperature

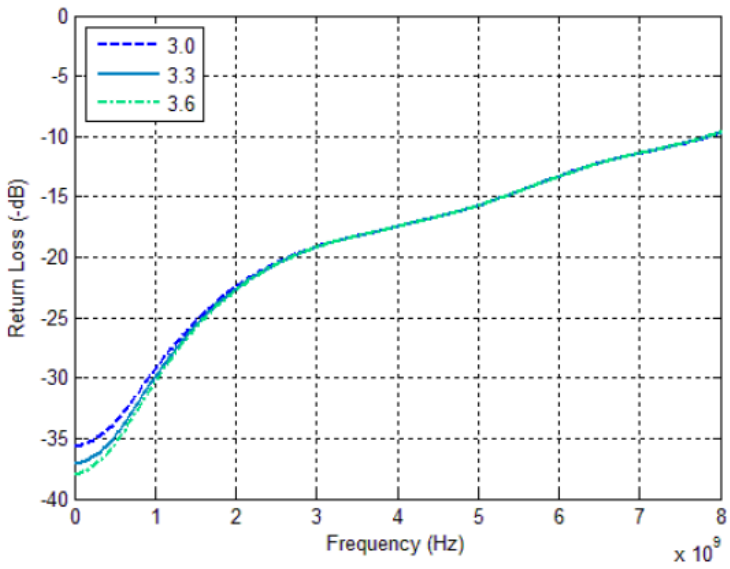


Figure 11. Terminated port return loss vs. V_{DD}

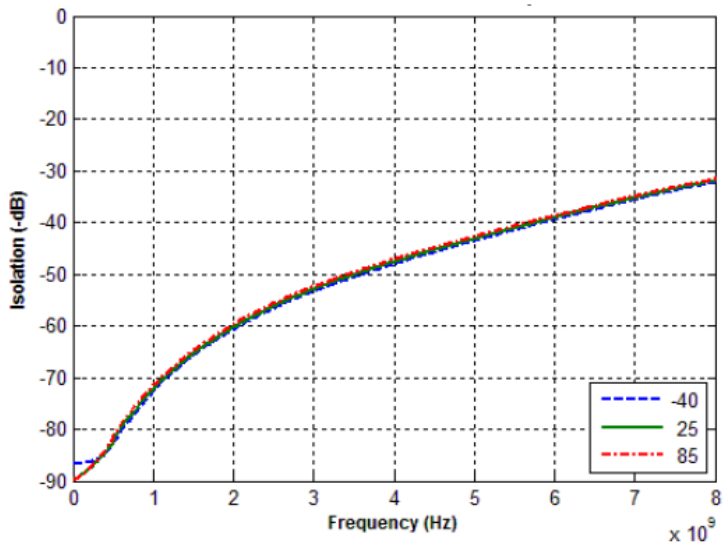


Figure 12. Isolation vs. temperature (RFx–RFx)

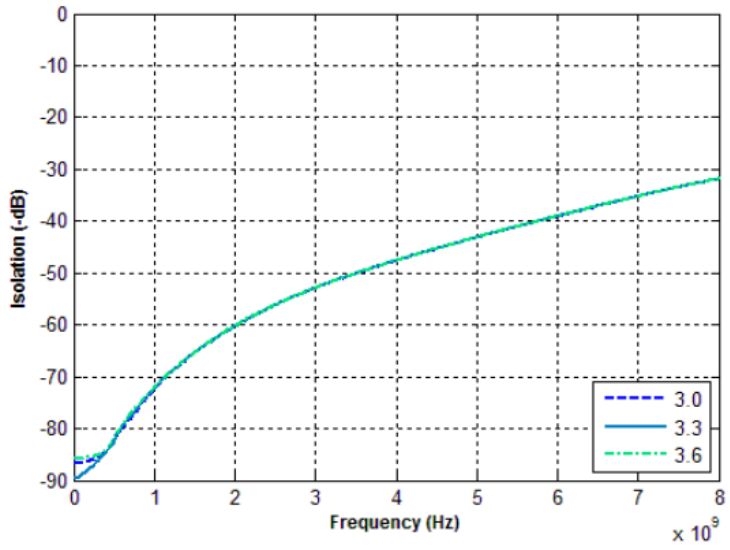


Figure 13. Isolation vs. V_{DD} (RFx–RFx)

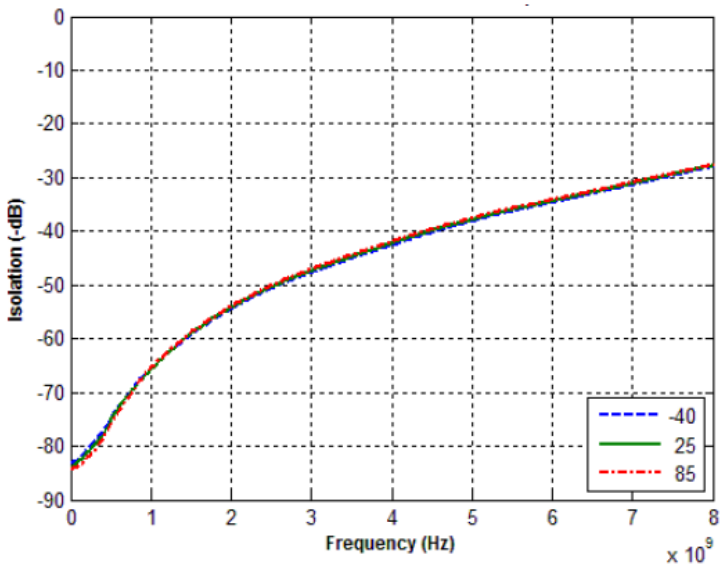


Figure 14. Isolation vs. temperature (RFC–RFx)

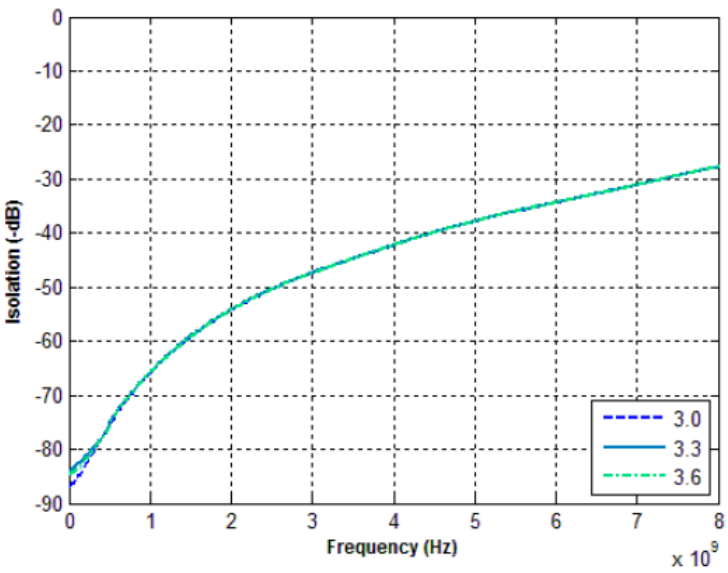


Figure 15. Isolation vs. V_{DD} (RFC–RFx)

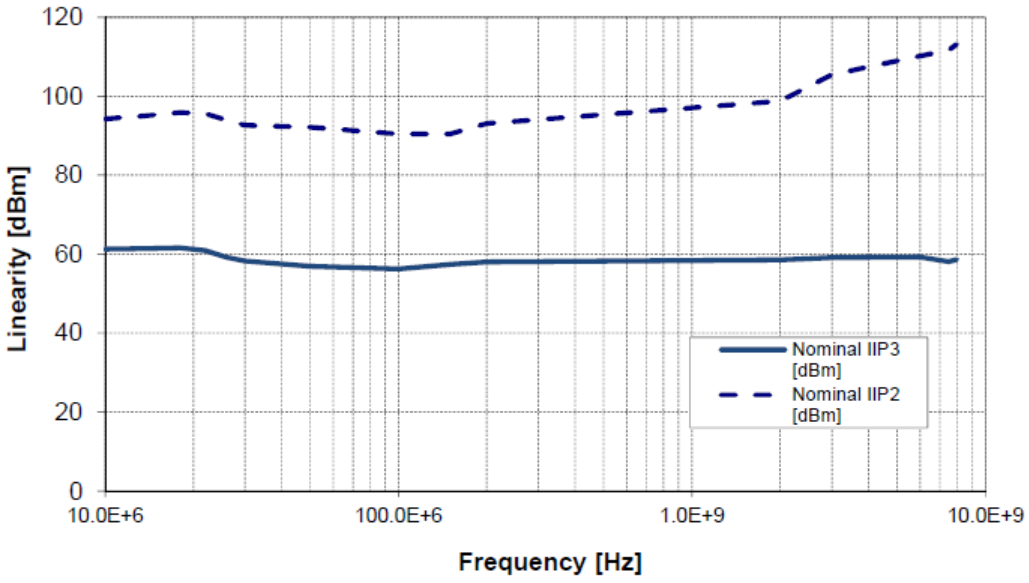


Figure 16. Linearity performance

Evaluation kit

pSemi designed the SP4T switch evaluation board to ease your evaluation of the pSemi PE42441. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1, RF2, RF3, and RF4 are connected through 50Ω transmission lines via SMA connectors J2, J4, J3, and J5, respectively. A through 50Ω transmission is available via SMA connectors J6 and J7. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a four metal layer material with a total thickness of 62 mils. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and er = 3.55. The middle layers provide ground for the transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 15 mils, trace gaps of 10 mils, and metal thickness of 2.1 mils.

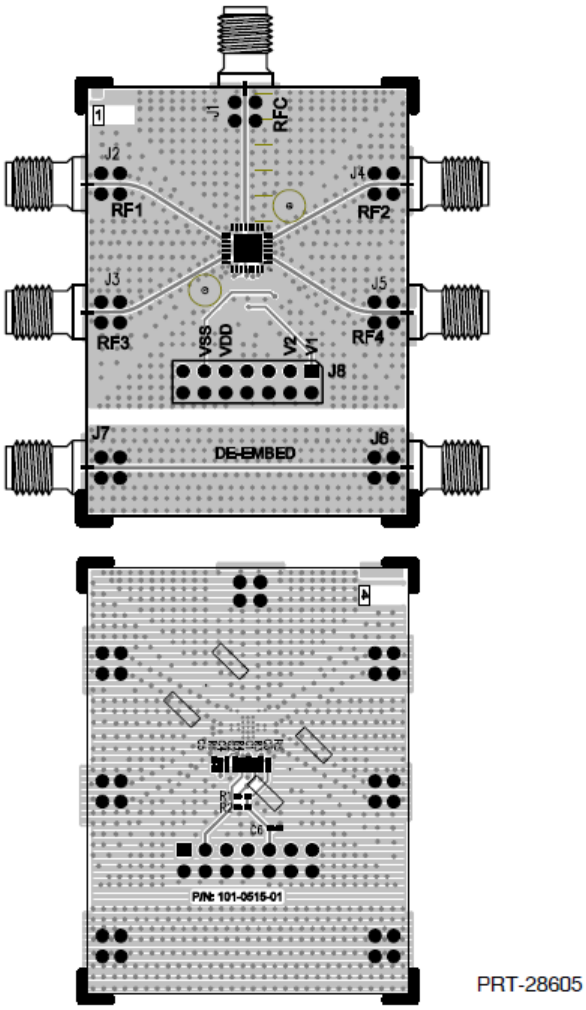


Figure 17. Evaluation board layout

Evaluation board schematic

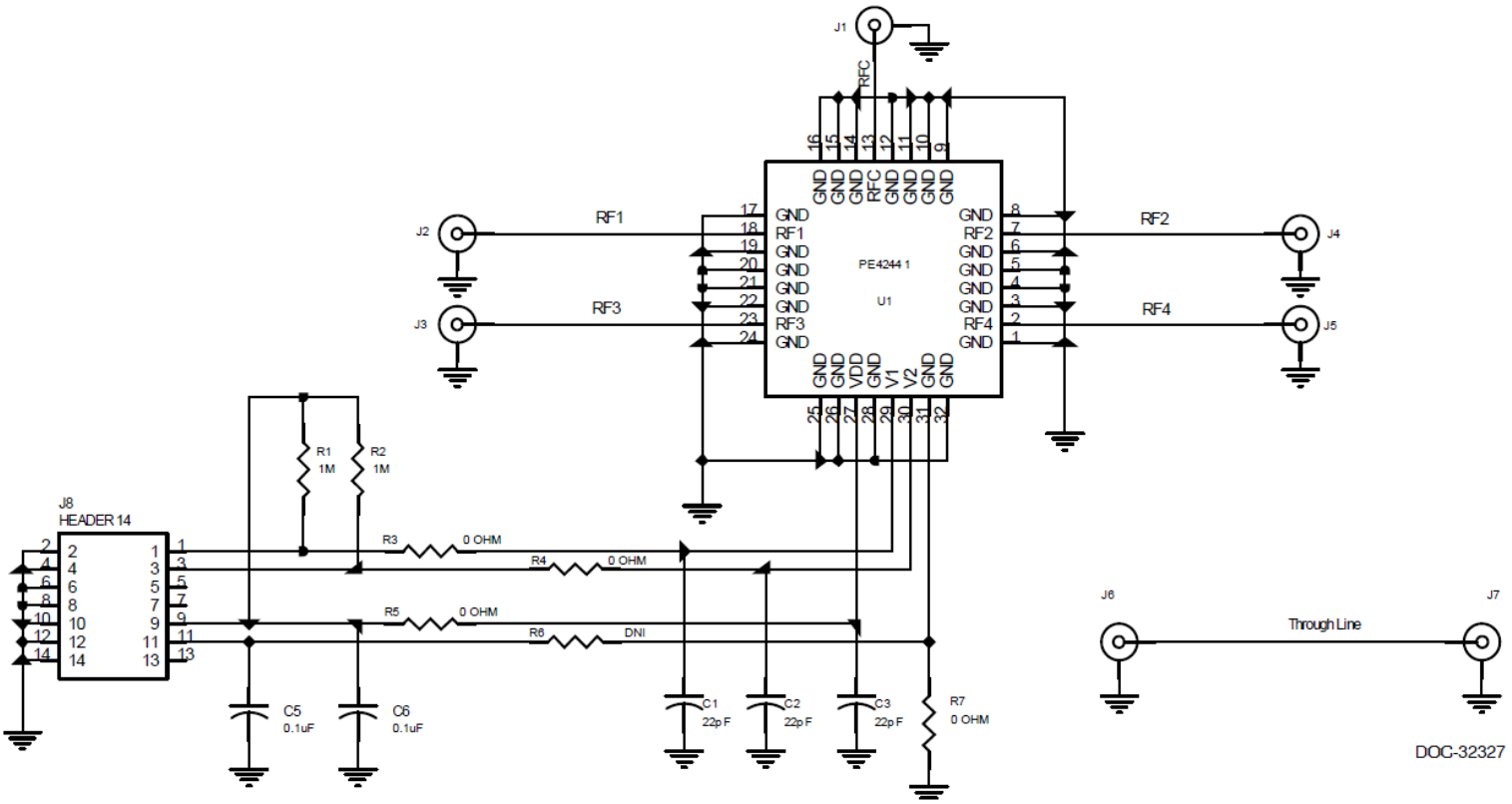


Figure 18. Evaluation board schematic

Pin information

Figure 19 shows the PE42441 pin map for the 32-lead 5 × 5 mm LGA package, and Table 5 lists the description for each pin.

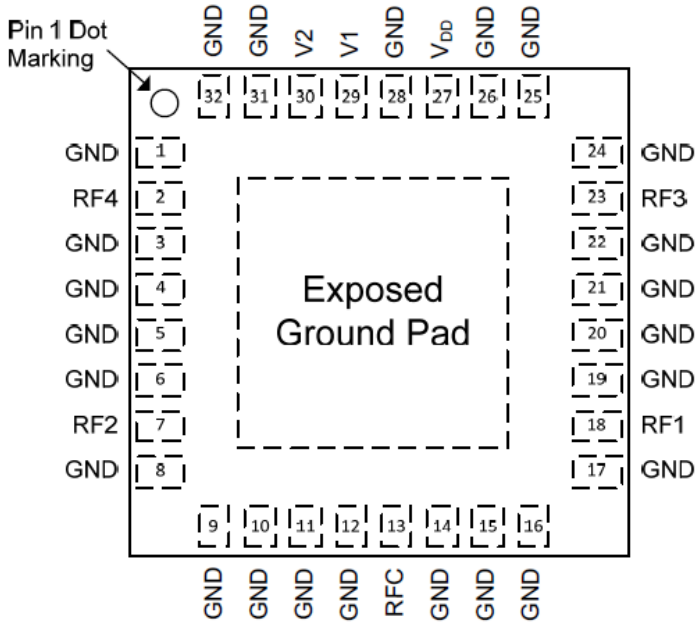


Figure xx. Pin configuration (top view)

Table 5. PE42441 pin descriptions

Pin no.	Pin name	Description
1, 3–6, 8, 9–12, 14–17, 19–22, 24–26, 28, 31, 32	GND	Ground
2(*)	RF4	RF port 4
7(*)	RF2	RF port 2
13(*)	RFC	RF common
18(*)	RF1	RF port 1
23(*)	RF3	RF port 2
27	V_{DD}	Supply voltage
29	V1	Digital control logic input 1
30	V2	Digital control logic input 2
Pad	GND	Exposed pad. Ground for proper operation.

* RF pins 2, 7, 13, 18, and 23 must be at 0 VDC. These RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE42441 moisture sensitivity level rating for the 32-lead 5 × 5 mm LGA package is MSL3.

Package drawing

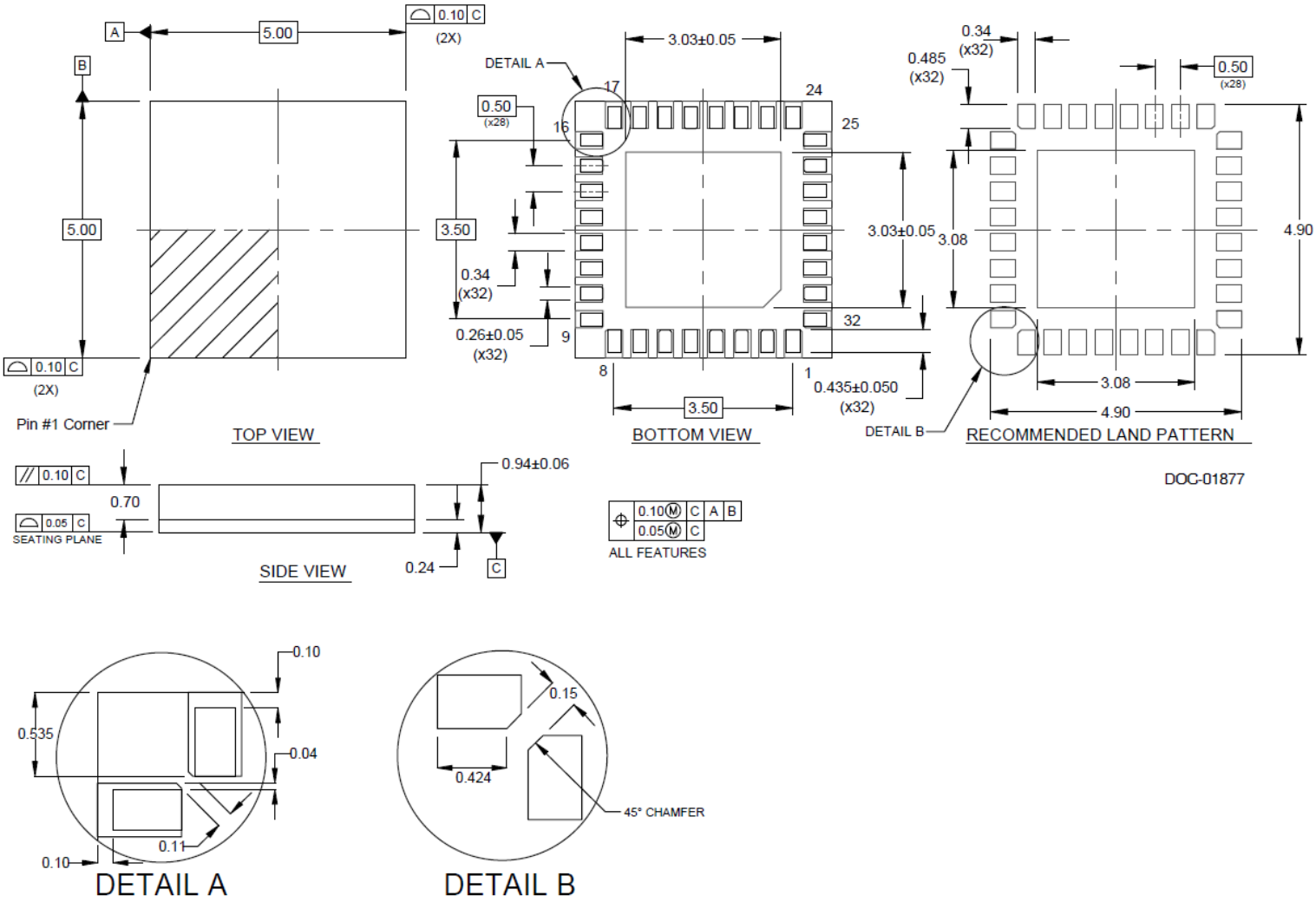


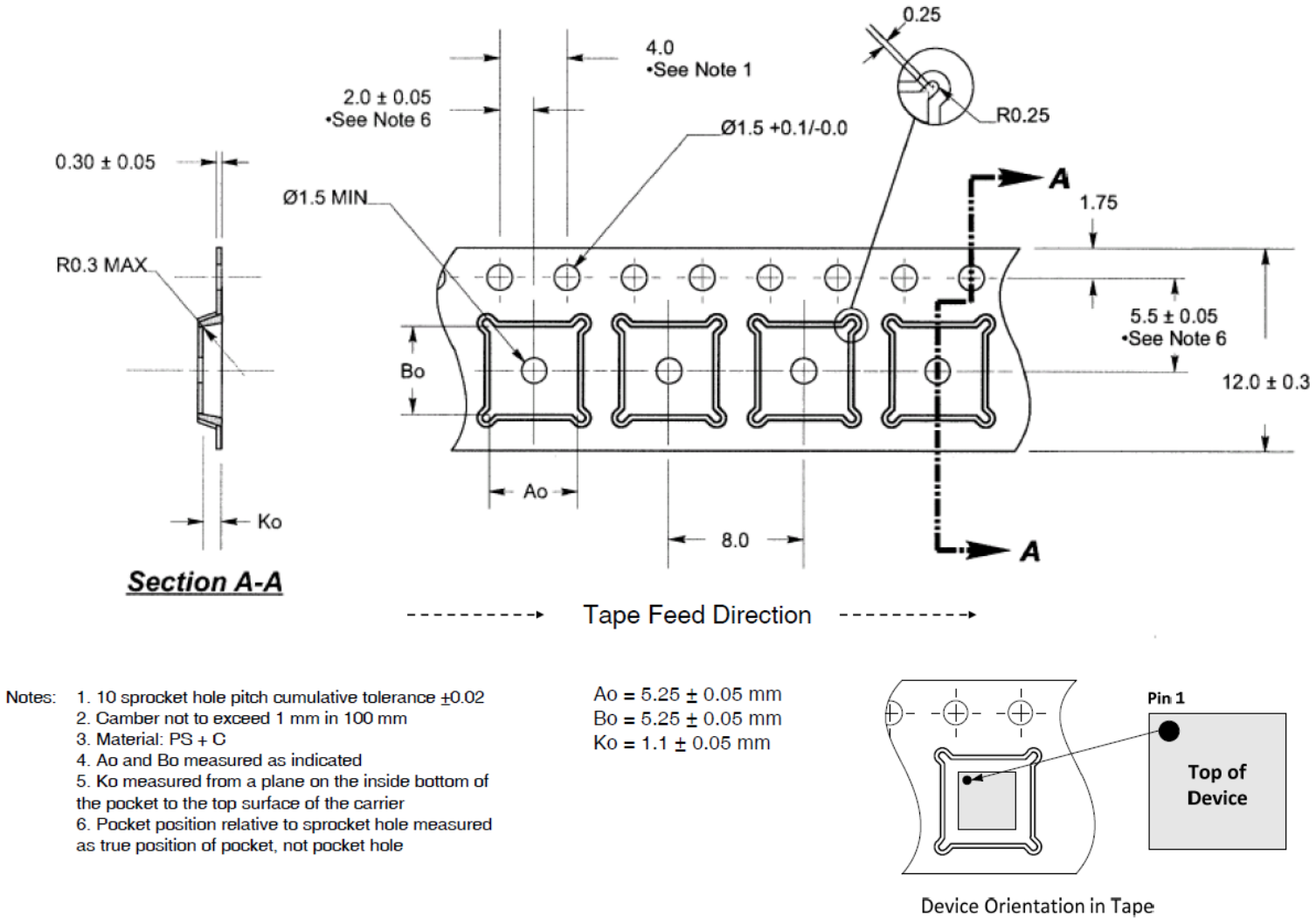
Figure 20. Package mechanical drawing for the 32-lead 5 × 5 mm LGA package

Top-marking specification

● = Pin 1 indicator
YYWW = Date code, last two digits of the year and work week
ZZZZZZ = Six digits of the lot number

Figure 21. PE42441 package marking specification

Tape and reel specification



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.02
2. Camber not to exceed 1 mm in 100 mm
3. Material: PS + C
4. Ao and Bo measured as indicated
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 5.25 ± 0.05 mm
Bo = 5.25 ± 0.05 mm
Ko = 1.1 ± 0.05 mm

Device Orientation in Tape

Figure 22. Tape and reel specification for the 32-lead 5 × 5 mm LGA package

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE42441E-Z	PE42441 SP4T RF switch	Green 32-lead 5 × 5 mm LGA	3000 units/T&R
EK42441-04	PE42441 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
Preliminary Specification	The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product.
Product Specification	The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF).
Product Brief	This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com.

Contact and legal information

Sales contact	For additional information, contact Sales at sales@psemi.com.
Disclaimers	The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.
Patent statement	pSemi products are protected under one or more of the following U.S. patents: http://patents.psemi.com

Copyright and trademarks