# PE42359

## Document category: Product Specification

*UltraCMOS® SPDT RF Switch, 10 MHz–3 GHz*

## Features

- AEC-Q100 Grade 2 certified
- Supports operating temperature up to +105 °C
- Single-pin or complementary CMOS logic control inputs
- Low insertion loss:
  - 0.35 dB @ 1000 MHz
  - 0.50 dB @ 2000 MHz
- High isolation: 30 dB @ 1000 MHz
- High ESD tolerance: 2 kV HBM
- Typical input 1-dB compression point of +33.5 dBm
- 1.8V minimum power supply voltage
- Packaging: 6-lead SC-70

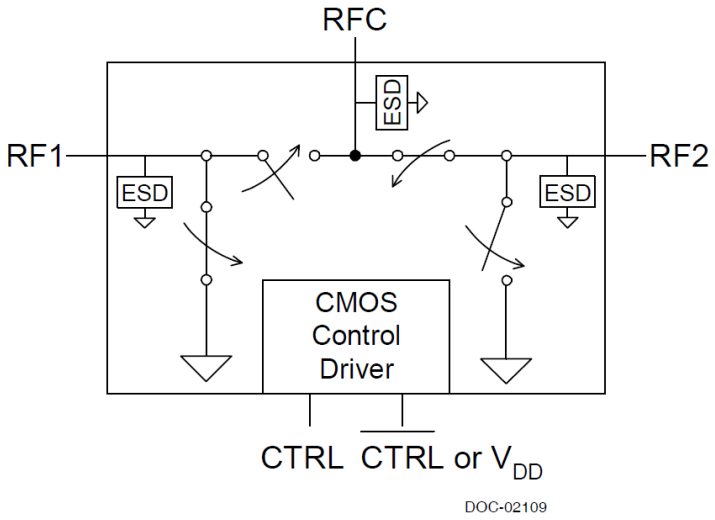



*Figure 1. PE42359 functional diagram*

## Product description

The pSemi PE42359 UltraCMOS® RF switch is designed to cover a broad range of applications from 10 MHz through 3 GHz. This reflective switch integrates on-board CMOS control logic with a low-voltage CMOS-compatible control interface and can be controlled using either single-pin or complementary control inputs. Using a nominal +3V power supply voltage, a typical input 1-dB compression point of +33.5 dBm can be achieved. The PE42359 also meets the quality and performance standards for automotive applications and has received AEC-Q100 Grade 2 certification.

The PE42359 is manufactured using the pSemi UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

# Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

## ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

## Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE42359 absolute maximum ratings

| Parameter or condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | -0.3 | 4.0 | V |
| Voltage on any DC input | $V_I$ | -0.3 | $V_{DD}$ + 0.3 | V |
| Storage temperature range | $T_{ST}$ | -65 | 150 | °C |
| Operating temperature range | $T_{OP}$ | -40 | 105 | °C |
| Input power (50Ω)[1] | $P_{IN}$ | – | See Figure 2 | dBm |
| ESD voltage HBM, all pins[2] | $V_{ESD,HBM}$ | – | 2000 | V |
| ESD voltage CDM, all pins[3] | $V_{ESD,CDM}$ | – | 1000 | V |

1. To maintain the optimum device performance, do not exceed the maximum input power ($P_{IN}$) at the preferred operating frequency. For more information, see Figure 2.
2. Human body model (MIL–STD 883 Method 3015).
3. Charged device model (JEDEC JESD22–C101).

## Recommended operating conditions

Table 2 lists the PE42359 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE42359 operating conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 1.8 | 3.0 | 3.3 | V |
| Power supply current | $I_{DD}$ | – | 9 | 20 | µA |
| Control voltage high | $V_{IH}$ | 0.7 × $V_{DD}$ | – | – | V |
| Control voltage low | $V_{IL}$ | – | – | 0.3 × $V_{DD}$ | V |

# Electrical specifications

Table 3 lists the PE42359 key electrical specifications at +25 °C and $V_{DD}$ = 3.0V ($Z_S$ = $Z_L$ = 50Ω), unless otherwise specified.

Table 3. PE42359 electrical specifications at +25 °C

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating frequency(1) | – | – | 10 | – | 3000 | MHz |
| Insertion loss(2) | – | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | – | 0.35<br>0.5<br>1.1 | 0.45<br>0.6<br>1.3 | dB |
| Isolation | RFx–RFx | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | 32<br>20<br>13 | 35<br>21<br>14 | – | dB |
| Isolation | RFC–RFx | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | 28<br>19<br>12 | 29<br>20<br>13 | – | dB |
| Return loss(2) | RFx–RFC | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | 21<br>15<br>9 | 25<br>18<br>11 | – | dB |
| Switching time(3) | – | 50% CTRL to 90% or 10% RF | – | 2 | – | µs |
| Video feedthrough(4) | – | – | – | 15 | – | $mV_{PP}$ |
| Input 1-dB compression point | – | 1000 MHz @ 2.3–3.3V<br>1000 MHz @ 1.8–2.3V<br>2500 MHz @ 2.3–3.3V<br>2500 MHz @ 1.8–2.3V | 31.5<br>29.5<br>28.5<br>28 | 33.5<br>30.5<br>30.5<br>29 | – | dBm |
| Input IP3 | – | 2500 MHz, 20 dBm input power | – | 55 | – | dBm |

1. Device linearity can degrade below 10 MHz.
2. To improve high-frequency performance, use external matching. For more information, see Figure 18–Figure 23, and Figure 26.
3. The PE42359 has a maximum 25 kHz switching rate.
4. The DC transient at the output of any port of the switch when the control voltage is switched from low-to-high or high-to-low in a 50Ω test set-up, measured with 1 ns rise time pulses and 500 MHz bandwidth.

Table 4 lists the PE42359 key electrical specifications at -40 °C to +105 °C and $V_{DD}$ = 3.0V ($Z_S$ = $Z_L$ = 50Ω), unless otherwise specified.

Table 4. PE42359 electrical specifications at -40 °C to +105 °C

| Parameter | Path | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | – | – | 10 | – | 3000 | MHz |
| Insertion loss | – | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | – | 0.35<br>0.5<br>1.1 | 0.6<br>0.75<br>1.4 | dB |
| Isolation | RFx–RFx | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | 31<br>19<br>12 | 35<br>21<br>14 | – | dB |
| Isolation | RFC–RFx | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | 27<br>18<br>11 | 29<br>20<br>13 | – | dB |
| Return loss | RFx–RFC | 10–1000 MHz<br>1000–2000 MHz<br>2000–3000 MHz | 20<br>14<br>9 | 25<br>18<br>11 | – | dB |
| Switching time | – | 50% CTRL to 90% or 10% RF | – | 3.6 | – | µs |
| Video feedthrough | – | – | – | 15 | – | $mV_{PP}$ |
| Input 1-dB compression point | – | 1000 MHz @ 2.3–3.3V<br>1000 MHz @ 1.8–2.3V<br>2500 MHz @ 2.3–3.3V<br>2500 MHz @ 1.8–2.3V | 30.5<br>28.5<br>27.5<br>27 | 33.5<br>30.5<br>30.5<br>29 | – | dBm |
| Input IP3 | – | 2500 MHz, 20 dBm input power | – | 54 | – | dBm |

# SPDT control logic

Table 5. Single-pin control logic truth table

| Control voltages | Signal path |
|---|---|
| Pin 6 ($V_{DD}$) = $V_{DD}$<br>Pin 4 (CTRL) = High | RFC–RF1 |
| Pin 6 ($V_{DD}$) = $V_{DD}$<br>Pin 4 (CTRL) = Low | RFC–RF2 |

Table 6. Complementary-pin control logic truth table

| Control voltages | Signal path |
|---|---|
| Pin 6 (CTRL or $V_{DD}$) = Low<br>Pin 4 (CTRL) = High | RFC–RF1 |
| Pin 6 (CTRL or $V_{DD}$) = High<br>Pin 4 (CTRL) = Low | RFC–RF2 |

## Control logic input

The PE42359 is a versatile RF CMOS switch that supports two operating control modes: single-pin control mode and complementary-pin control mode:

- In single-pin control mode, the switch operates with a single control pin (pin 4) supporting a +3V CMOS logic input and requires a dedicated +3V power supply connection on pin 6 ($V_{DD}$). This mode reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- In complementary-pin control mode, the switch operates using complementary control pins CTRL and ~~CTRL~~ (pins 4 and 6, respectively), that can be directly driven by +3V CMOS logic or a suitable microprocessor I/O port. This enables the PE42359 to serve as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE42359 operating limits.

## Maximum power handling

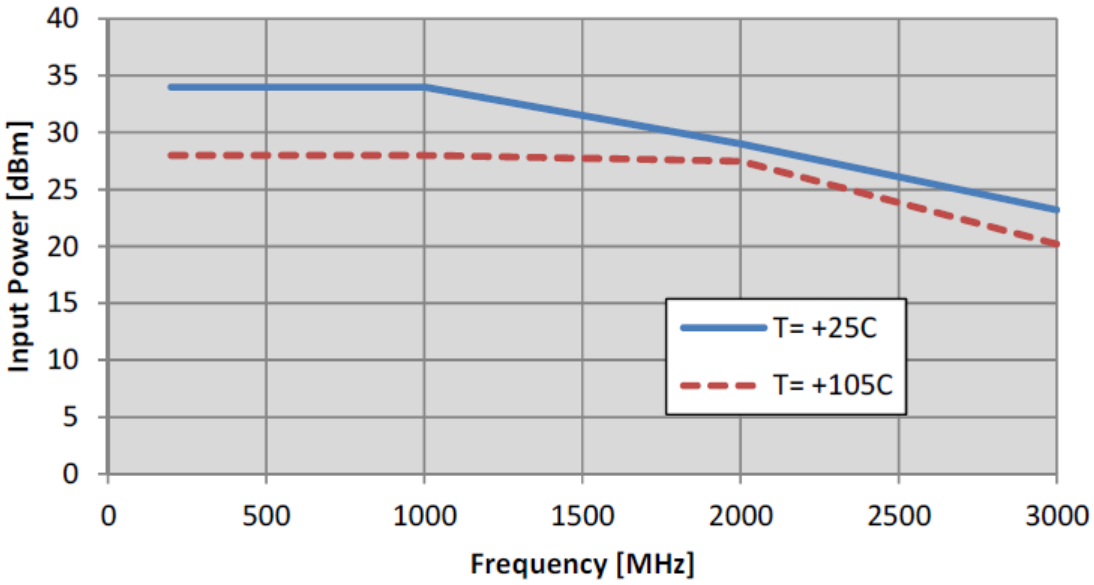



*Figure 2. Maximum power handling at $V_{DD}$ = 3.3V*

# Typical performance data

Figure 3–Figure 17 show the typical performance data at +25 °C and $V_{DD}$ = 3.0V, unless otherwise specified.

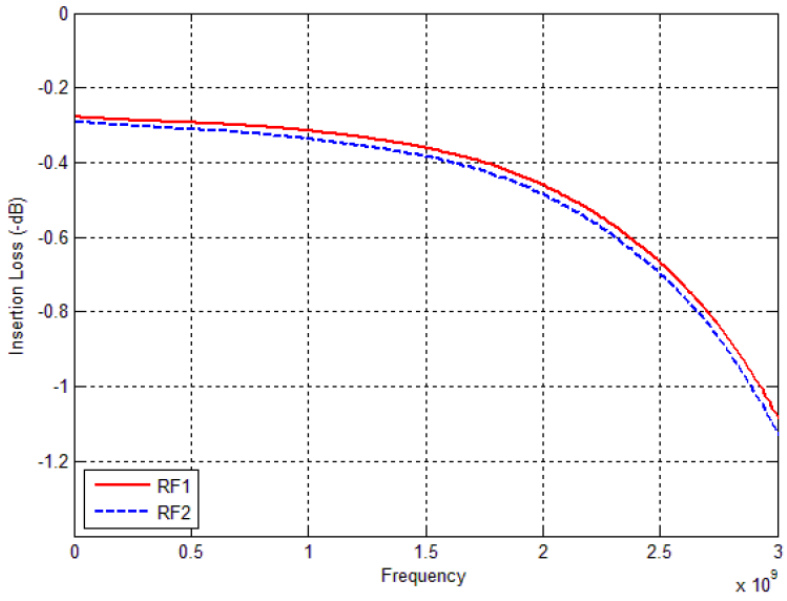



*Figure 3. Insertion loss (RFx nominal condition(*)*

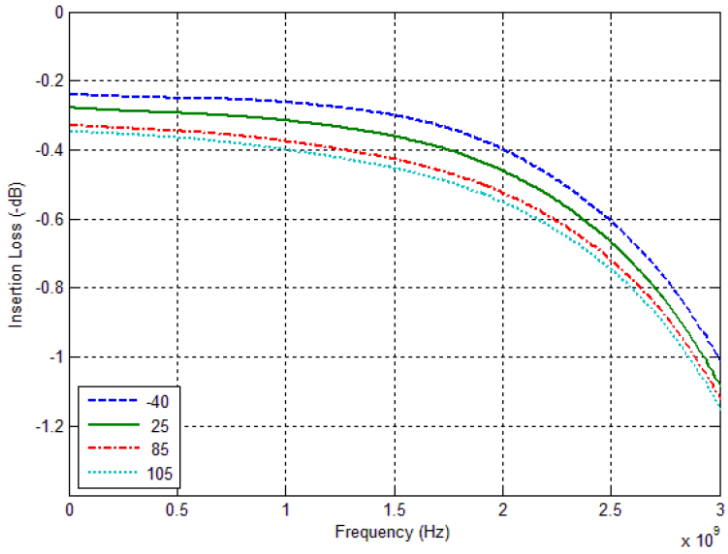



*Figure 4. Insertion loss vs. temperature (RF1–RFC)(*)*

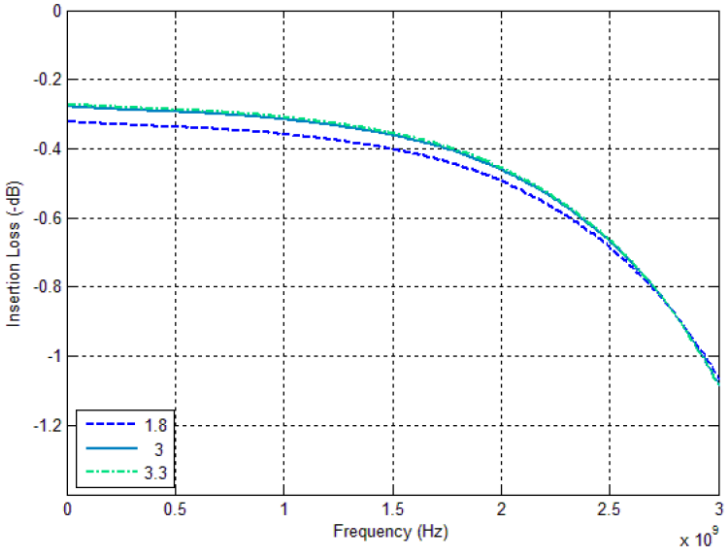



*Figure 5. Insertion loss vs. $V_{DD}$ (RF1–RFC)(*)*

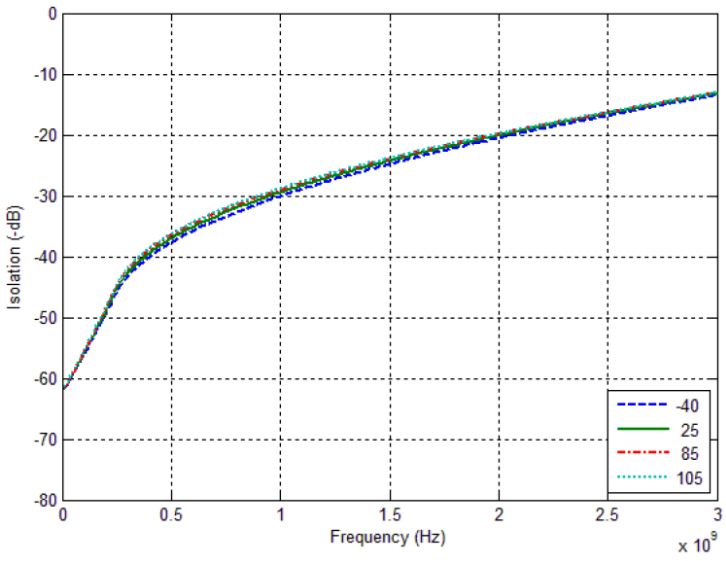



*Figure 6. RFC–RFx isolation vs. temperature*

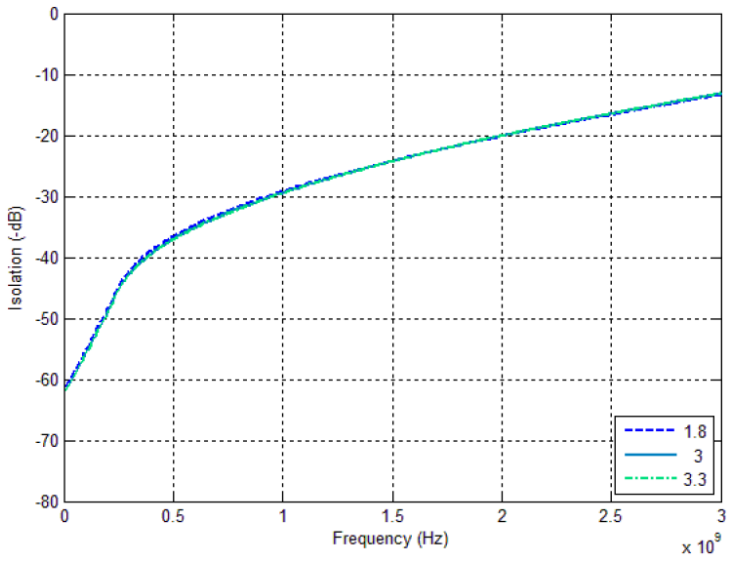



*Figure 7. RFC–RFx isolation vs. $V_{DD}$*

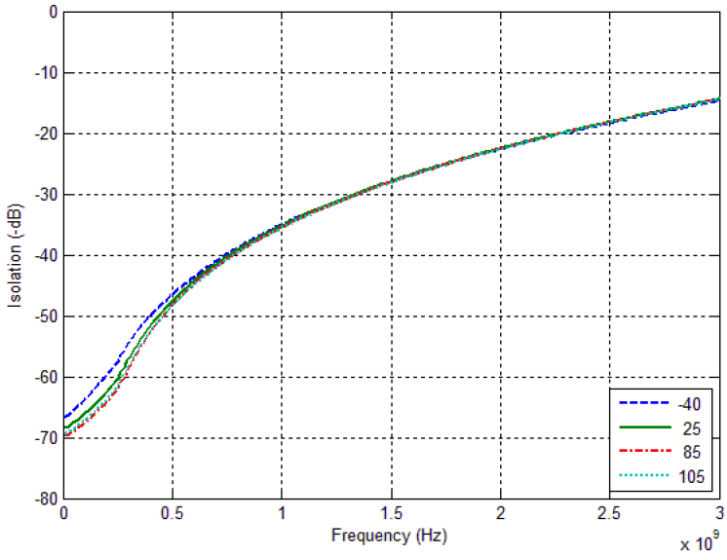



*Figure 8. RFx–RFx isolation vs. temperature*

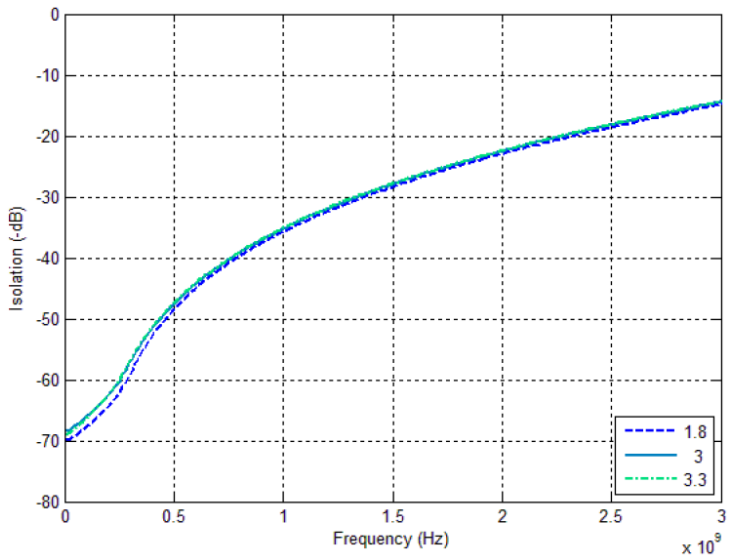



*Figure 9. RFx–RFx isolation vs. $V_{DD}$*

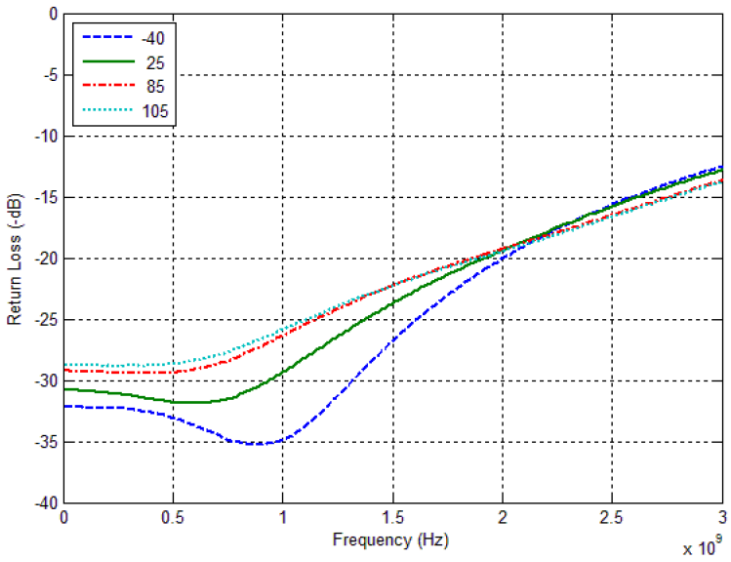



*Figure 10. RFC port return loss vs. temperature (RF1 active)(*)*

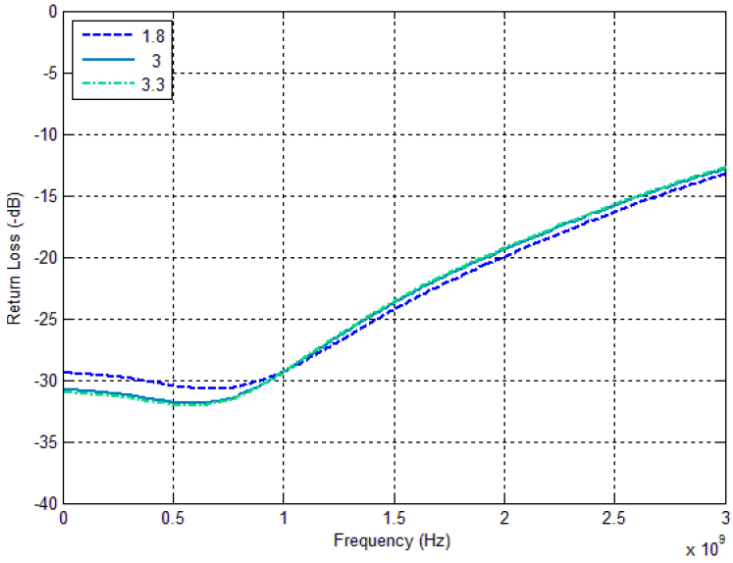



*Figure 11. RFC port return loss vs. $V_{DD}$ (RF1 active)(*)*

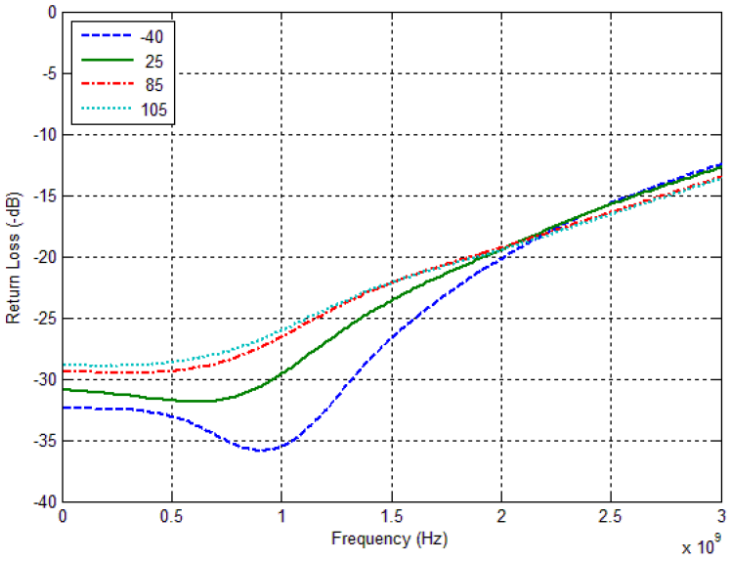



*Figure 12. RFC port return loss vs. temperature (RF2 active)(*)*

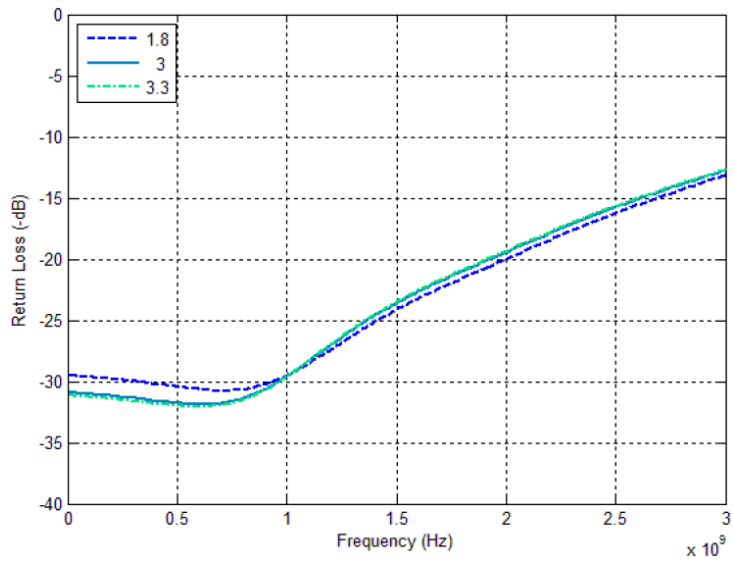



*Figure 13. RFC port return loss vs. $V_{DD}$ (RF2 active)(*)*

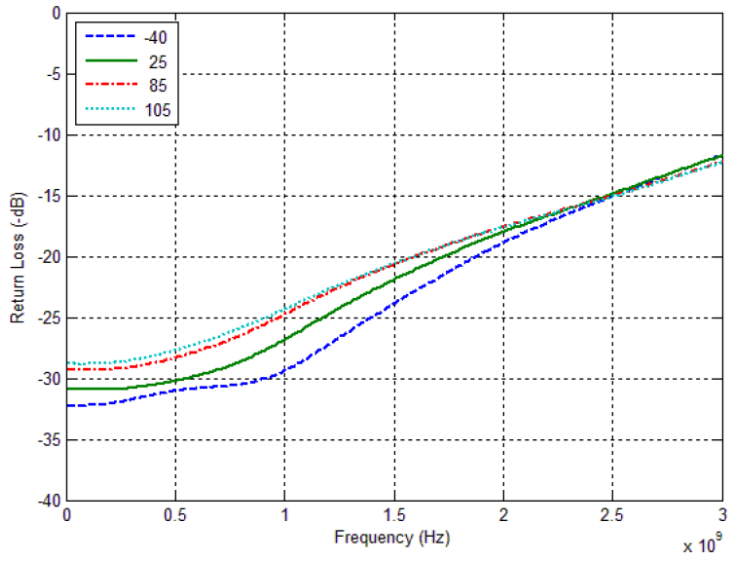



*Figure 14. Active port return loss vs. temperature (RF1 active)(*)*

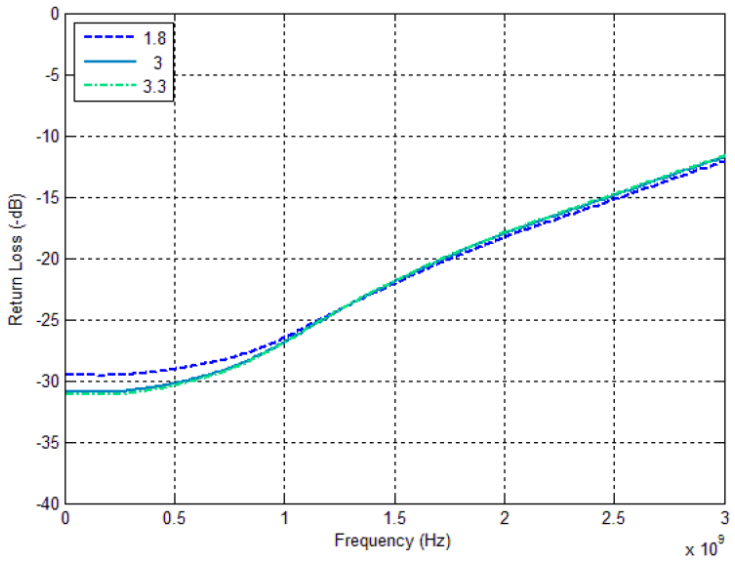



*Figure 15. Active port return loss vs. $V_{DD}$ (RF1 active)(*)*

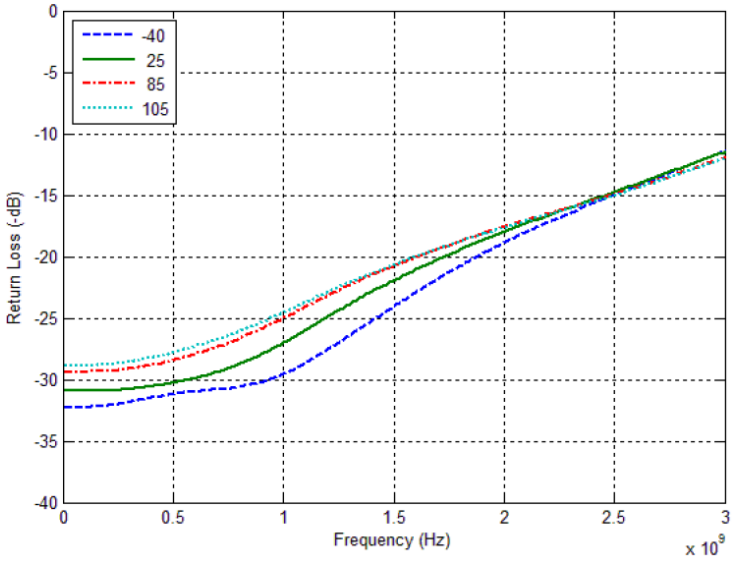



*Figure 16. Active port return loss vs. temperature (RF2 active)(*)*

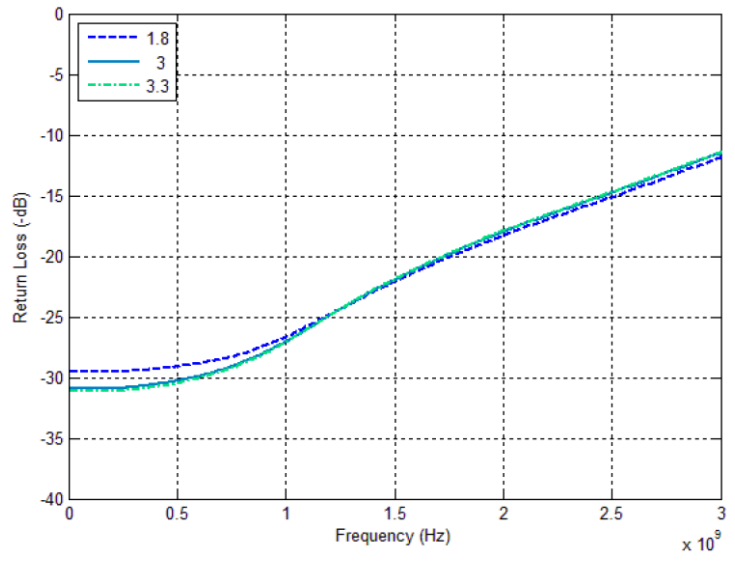



*Figure 17. Active port return loss vs. $V_{DD}$ (RF2 active)(*)*

* To improve high-frequency performance, use external matching. For more information, see Figure 18–Figure 23, and Figure 26.

Figure 18–Figure 23 show the performance comparison data at +25 °C and $V_{DD}$ = 3.0V, with or without matching.

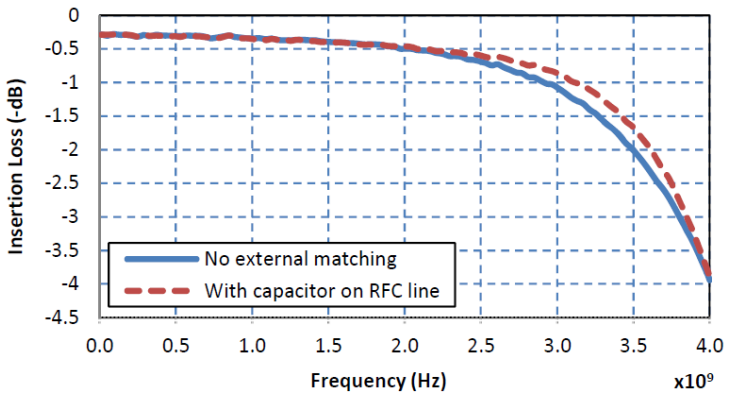



*Figure 18. Insertion loss RF1(*)*

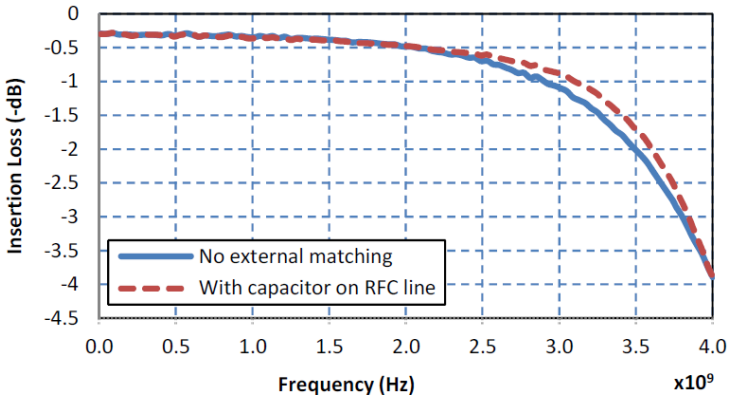



*Figure 19. Insertion loss RF2(*)*

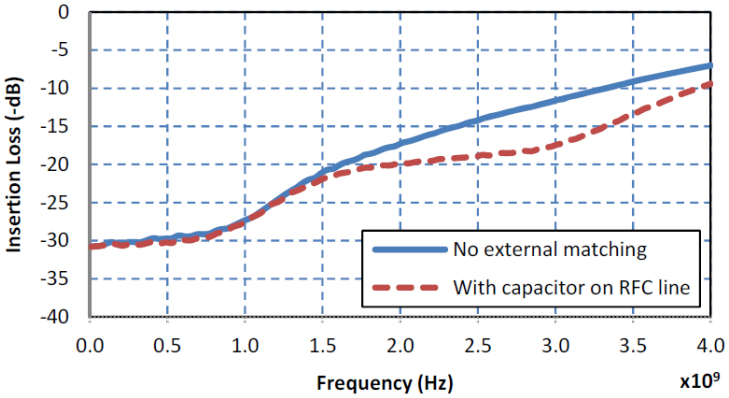



*Figure 20. Active port return loss (RF1 active)(*)*

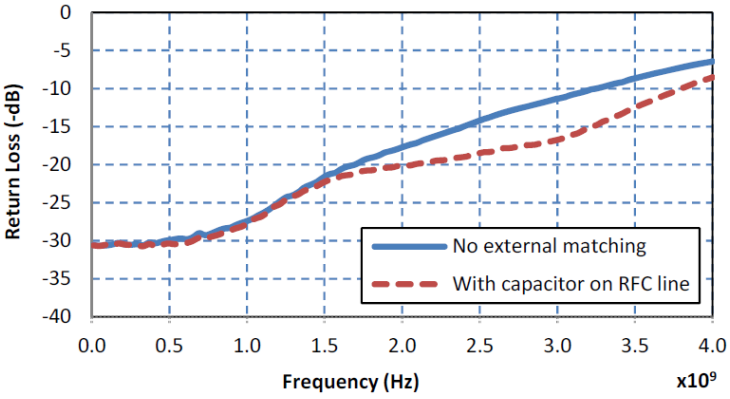



*Figure 21. Active port return loss (RF2 active)(*)*

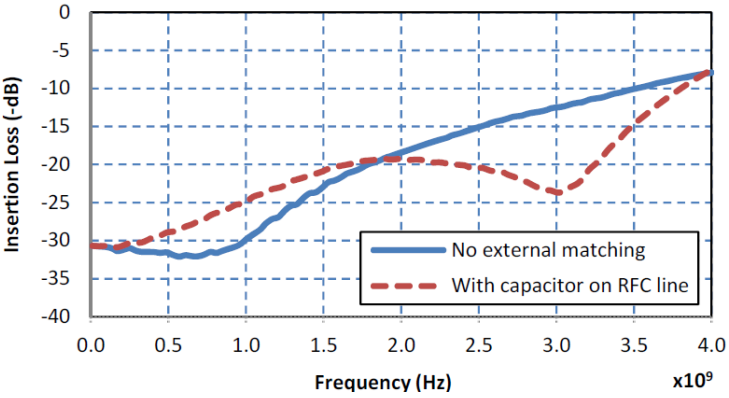



*Figure 22. RFC port return loss (RF1 active)(*)*

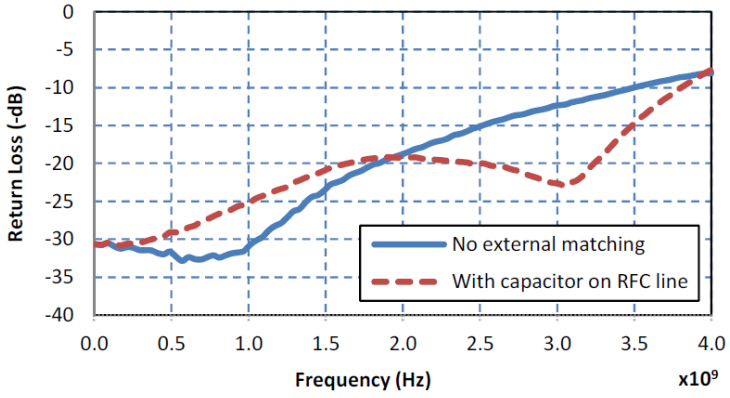



*Figure 23. RFC port return loss (RF2 active)(*)*

- To improve high-frequency performance, use external matching. For more information, see Figure 26.

# Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the pSemi PE42359. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two-metal-layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with a ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and εr of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device $V_{DD}$ or CTRL input. J7-1 is connected to the device CTRL input.

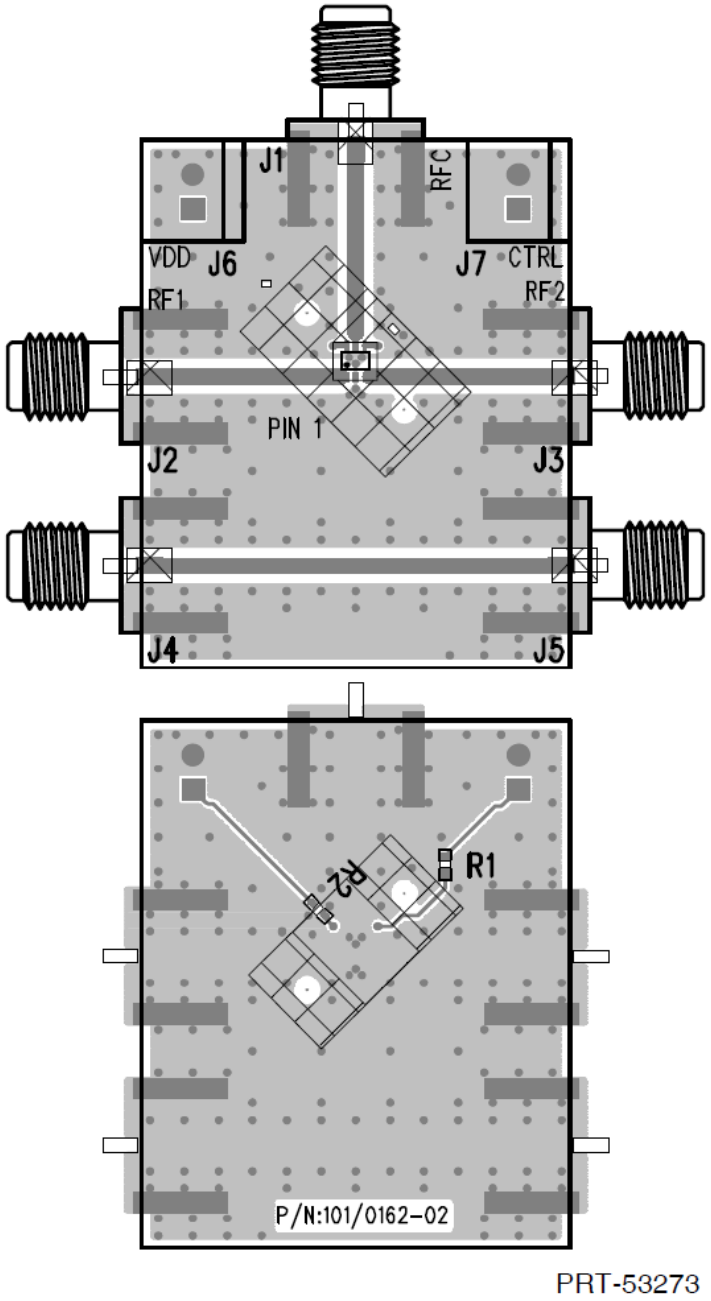



*Figure 24. Evaluation board layout*

# Evaluation board schematic

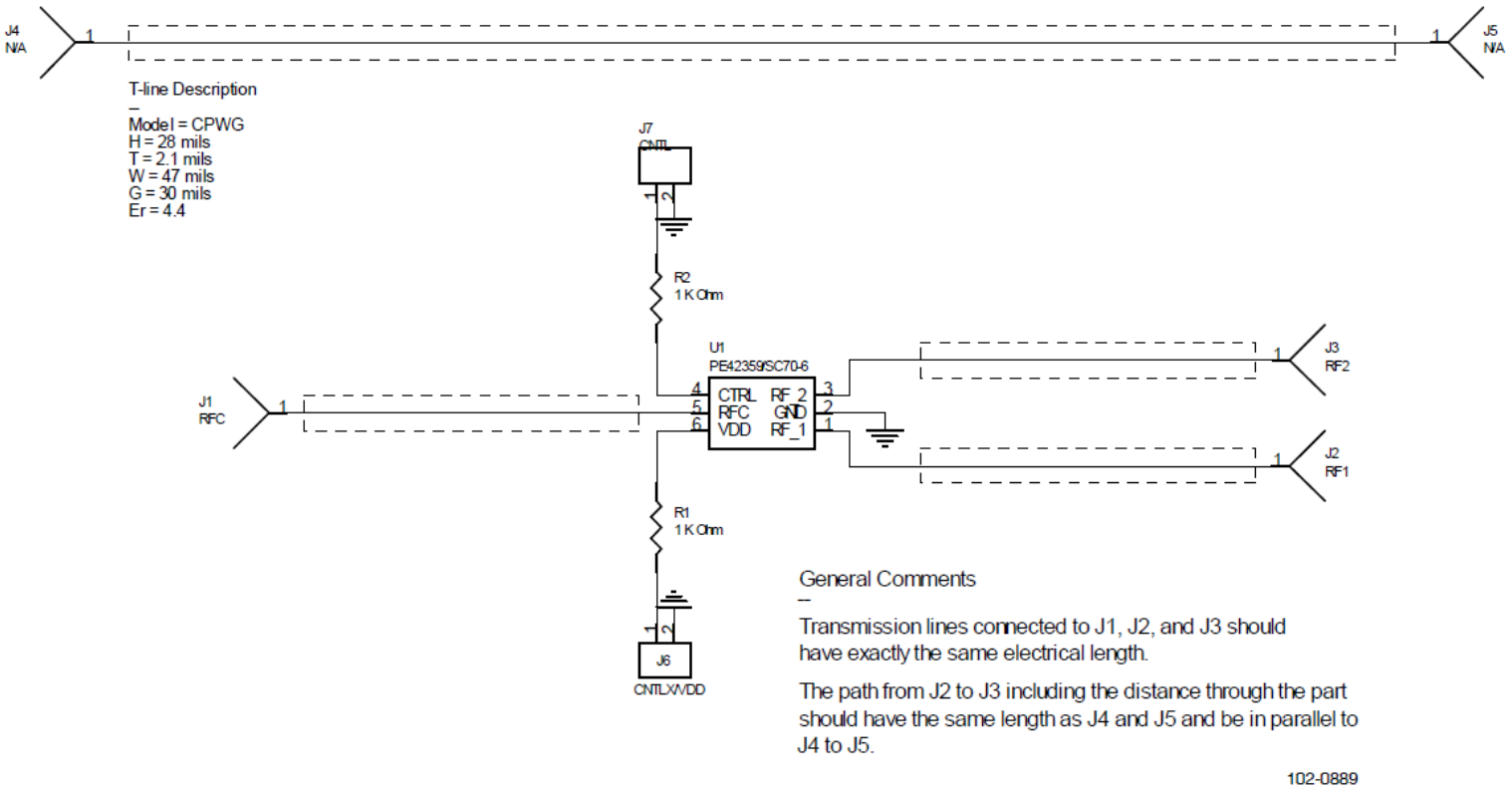



*Figure 25. Evaluation board schematic*

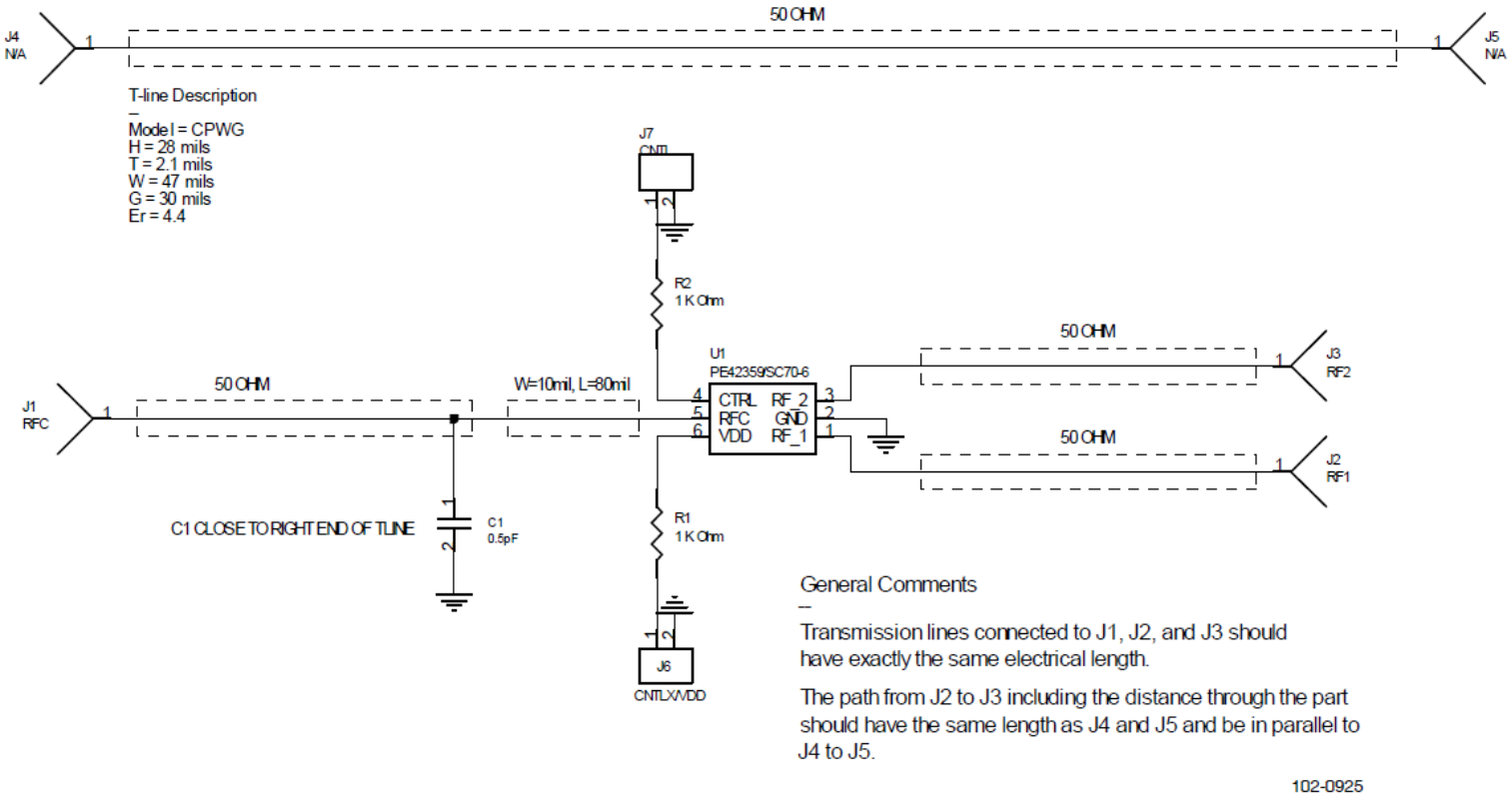



*Figure 26. Evaluation board schematic with matching*

# Pin information

Figure 27 shows the PE42359 pin map for the 6-lead SC-70 package, and Table 7 lists the description for each pin.

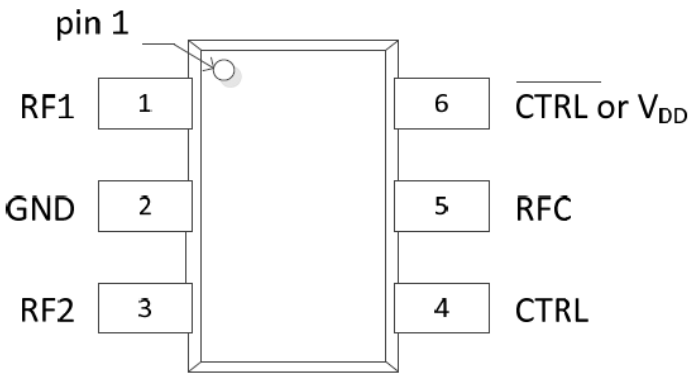



*Figure 27. Pin configuration (top view)*

Table 7. PE42359 pin descriptions

| Pin no. | Pin name | Description |
|---|---|---|
| 1(*) | RF1 | RF port 1 |
| 2 | GND | Ground connecttion. For the best performance, traces must be short and connected to the ground plane. |
| 3(*) | RF2 | RF port 2 |
| 4 | CTRL | Switch control input, CMOS logic level |
| 5(*) | RFC | RF common |
| 6 | ~~CTRL~~ or $V_{DD}$ | This pin supports two interface options:<br>• Single-pin control mode: A nominal 3V supply connection is required.<br>• Complementary-pin control mode: A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode. |

* RF pins 1, 3, and 5 must be blocked with an external series capacitor or held at 0 VDC.

# Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

## Moisture sensitivity level

The PE42359 moisture sensitivity level rating for the 6-lead SC-70 package is MSL1.

## Package drawing

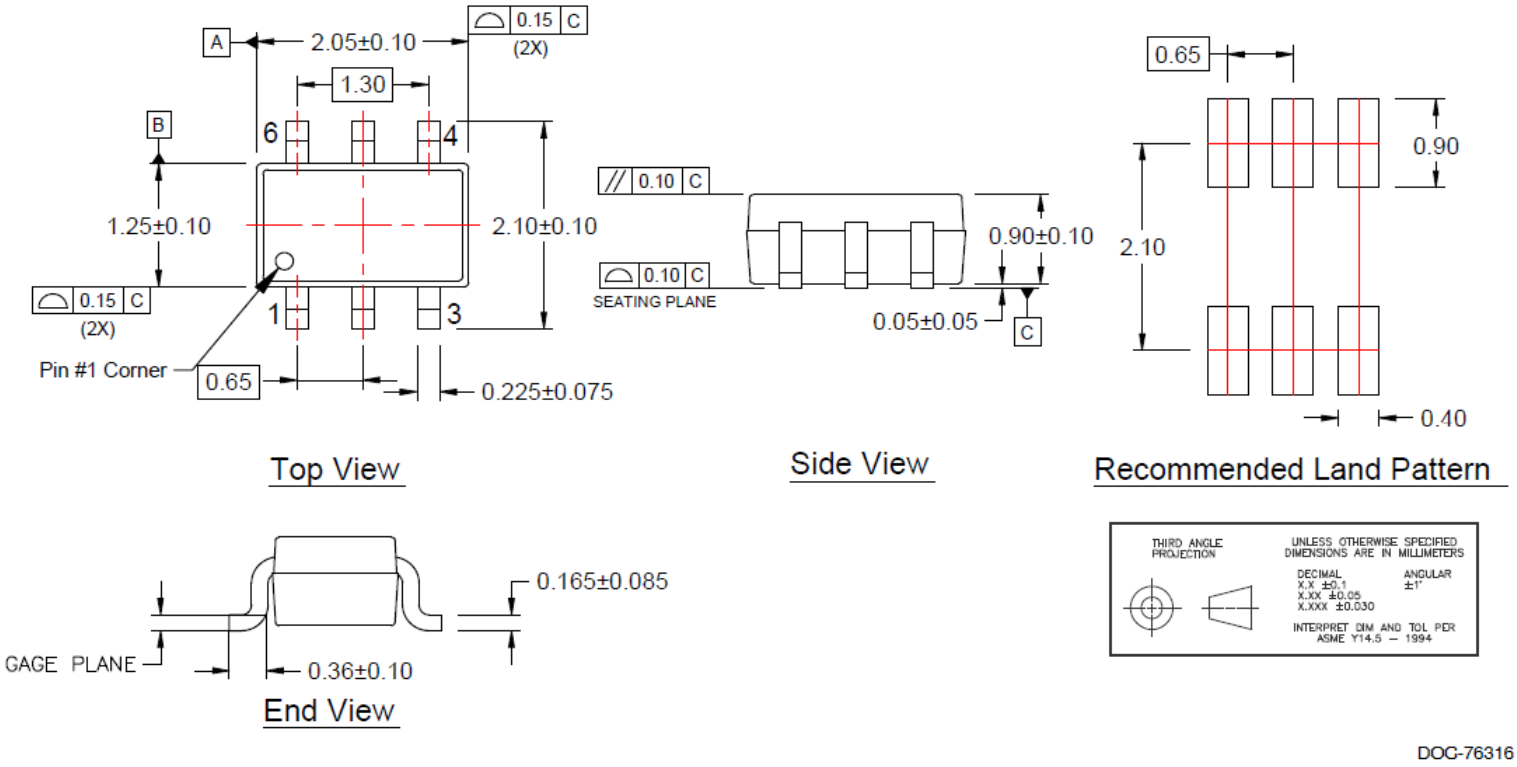



*Figure 28. Package mechanical drawing for the 6-lead SC-70 package*

## Top-marking specification

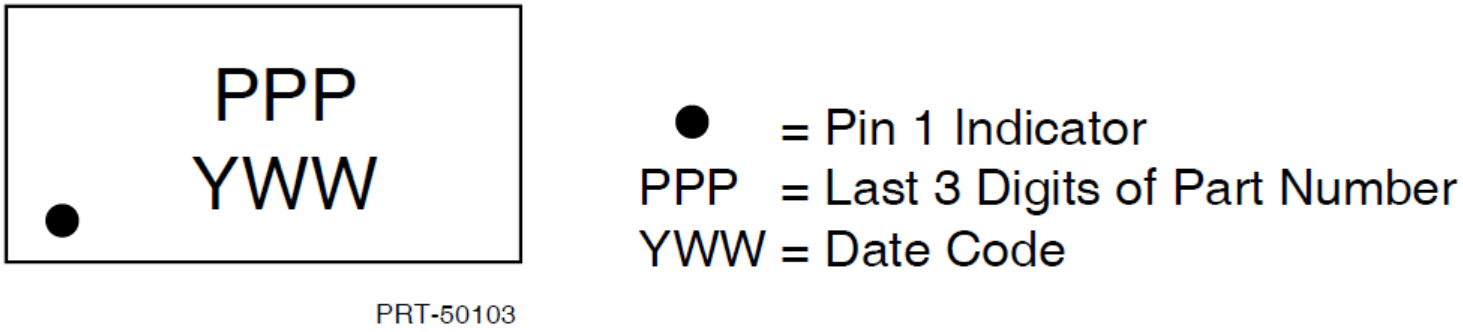
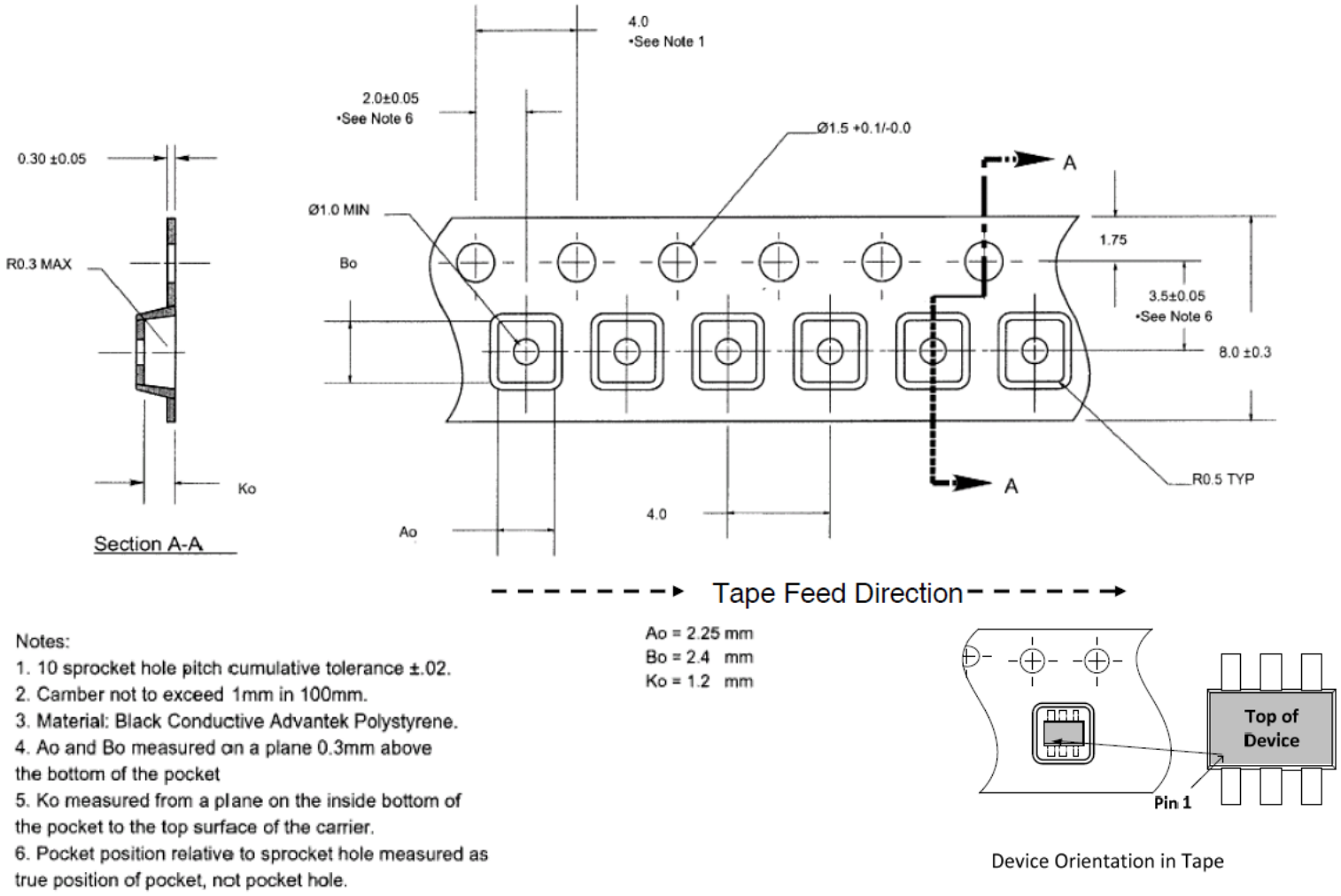



*Figure 29. PE42359 package marking specification*

## Tape and reel specification




Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

*Figure 30. Tape and reel specification for the 6-lead SC-70 package*

# Ordering information

| Order code | Description | Packaging | Shipping method |
|---|---|---|---|
| PE42359SCAA-Z | PE42359 SPDT RF switch | 6-lead SC-70 | 3000 units/T&R |
| EK42359-01 | PE42359 evaluation kit | Evaluation kit | 1/box |

# Document categories

| | |
|---|---|
| **Advance Information** | The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice. |
| **Preliminary Specification** | The data sheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice to supply the best possible product. |
| **Product Specification** | The data sheet contains final data. In the event that pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a Customer Notification Form (CNF). |
| **Product Brief** | This document contains a shortened version of the data sheet. For the full data sheet, contact sales@psemi.com. |

# Contact and legal information

| | |
|---|---|
| **Sales contact** | For additional information, contact Sales at sales@psemi.com. |
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