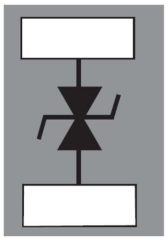
ESDZX168B-1BF4

Datasheet

Ultra-low capacitance single line ESD protection



Product status link
ESDZX168B-1BF4

Features

- Stand-off voltage : 16 V
- Ultra-low clamping voltage: 32 V at 16 A I_{pp} TLP
- Bidirectional protection
- Ultra-low capacitance: 0.12 pF
- Very high bandwidth: > 40 GHz
- Very low harmonic : H3 < -55 dBm at 25 dBm power
- Very low dynamic resistance : 0.8 Ω
- 0201 package
- ECOPACK2 compliant component
- Exceeds IEC 61000-4-2 level 4 standard:
  - ±12 kV (contact discharge)
  - ±30 kV (air discharge)

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- USB4, USB 3.1 Gen 1 and Gen 2
- HDMI 2.1
- Ethernet 1G, 10G
- DisplayPort
- LVDS

Description

The ESDZX168B-1BF4 is a bidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients. Thanks to extra low capacitance, ESDZX168B-1BF4 can protect high-speed differential lines with no impact on signal integrity.

With an extremely low clamping voltage, ESDZX168B-1BF4 is able to protect the most sensitive, submicron technology circuits.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	±12 ±30	kV
I_{pp}	Peak pulse current (8/20 µs)		2.2	A
T_j	Operating junction temperature range		-55 to +150	°C
T_{stg}	Storage junction temperature range		-65 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics (definitions)

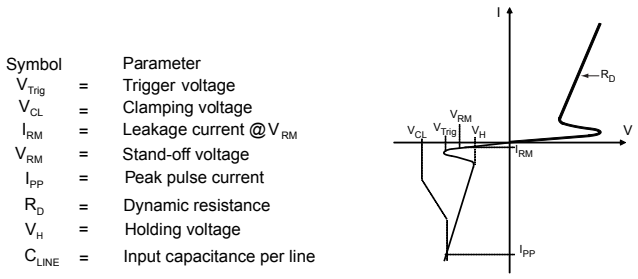


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{trig}	Trigger voltage		18	23	25	V
V_H	Holding voltage		16			V
V_{RM}	Reverse working voltage				16	V
I_{RM}	Leakage current	V_{RM} = 16 V			50	nA
I_R	Leakage current	V_R = 5 V			10	nA
V_{CL}(1)	Clamping voltage	IEC 61000-4-2, 8 kV contact discharge measured after 30 ns		32		V
V_{CL}(1)	Clamping voltage	8/20 µs waveform, I_{PP} = 2 A			24	V
V_{CL}(1)	TLP measurement (pulse duration 100ns)	I_{PP} = 16 A		32		V
		I_{PP} = 4 A		23		
R_D(1)	Dynamic resistance	TLP - Pulse duration 100 ns - I_{PP} [1 A – 16 A]		0.8		Ω
C_{LINE}	Line capacitance	V_{LINE} = 0 V, F = 1 MHz		0.7		pF
C_{LINE}(1)	Line capacitance	V_{LINE} = 0 V, F = 2.5 GHz		0.11	0.17	pF
		V_{LINE} = 0 V, F = 5 GHz		0.10	0.15	
F_C(1)	-3dB			> 40		GHz

1. *Evaluated by characterization – Not tested in production.*

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature (typical values)

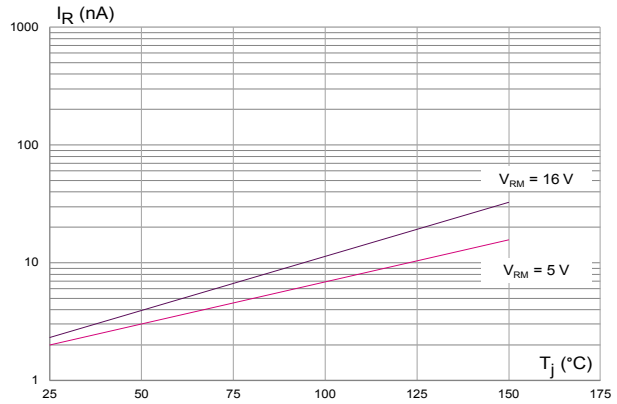


Figure 3. Junction capacitance versus frequency (typical values)

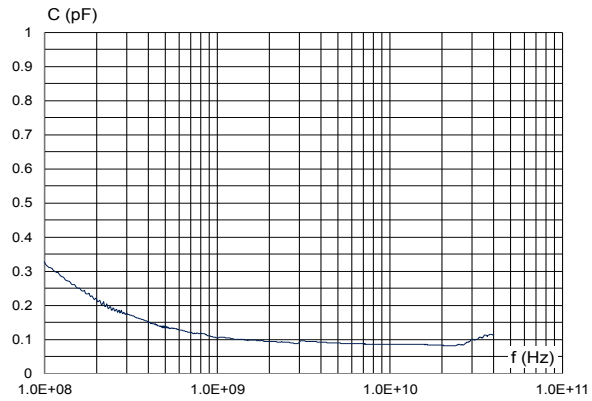


Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

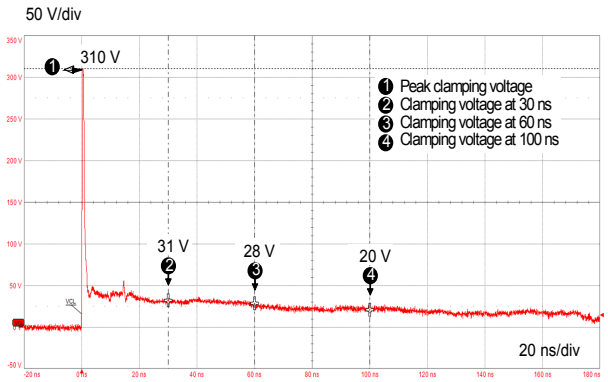


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

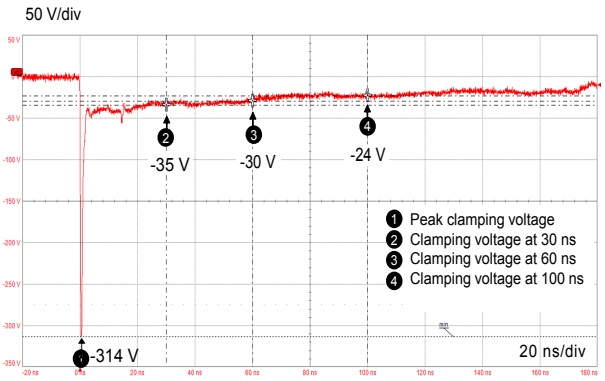


Figure 6. S21 attenuation measurement result

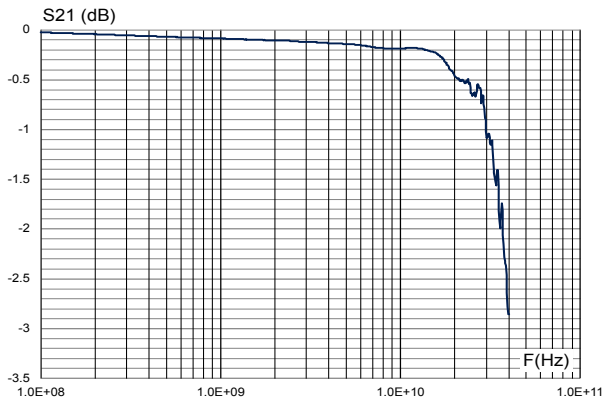


Figure 7. TLP measurement

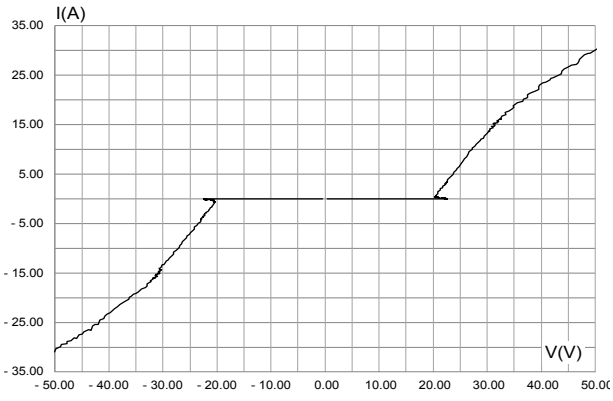


Figure 8. H2 harmonic measurements

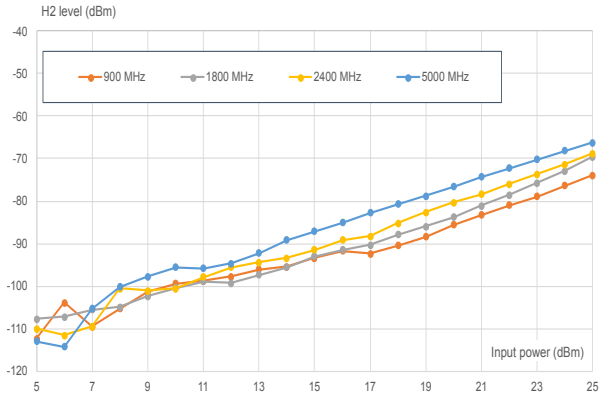
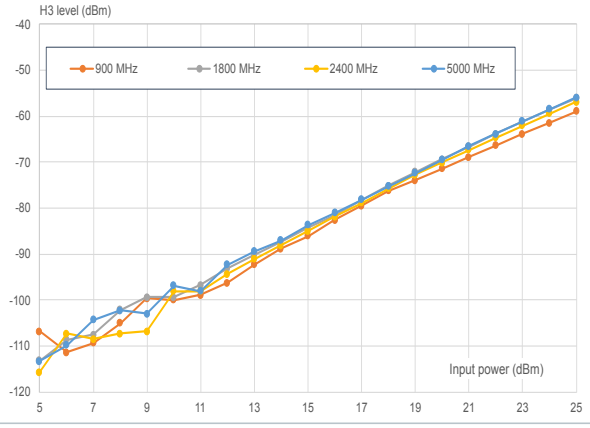


Figure 9. H3 harmonic measurements



2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 0201 package information

Figure 10. Package outline

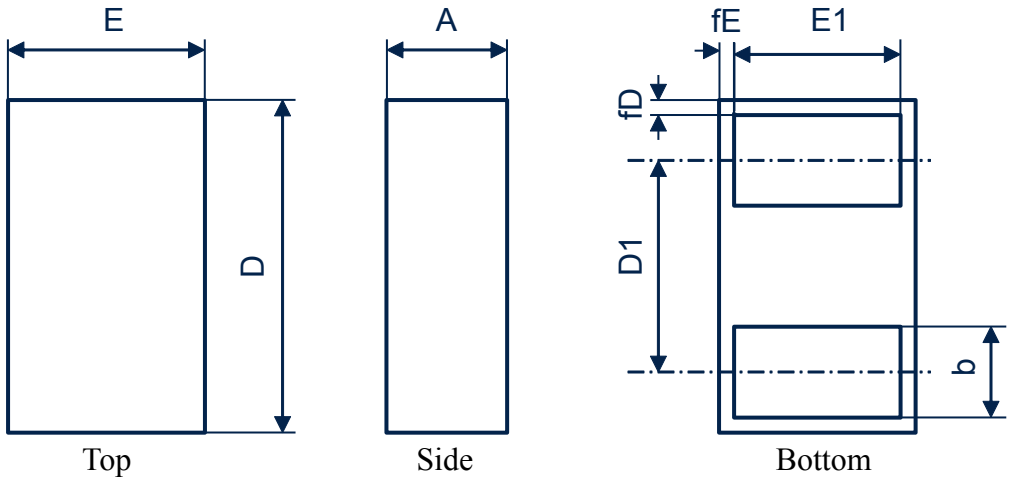


Table 3. Package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.180	0.200	0.220
b	0.1475	0.1675	0.1875
D	0.560	0.580	0.600
D1		0.3375	
E	0.260	0.280	0.300
E1	0.185	0.205	0.225
fD		0.0375	
fE		0.0375	

2.2 Packing and marking information

Figure 11. Marking layout

The marking « U » can be rotated by a multiple of 90° to differentiate assembly location.

Figure 12. Package orientation in reel

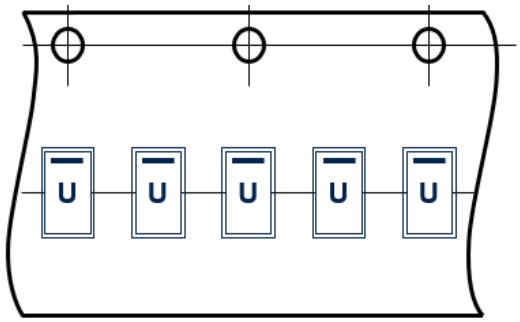


Figure 13. Tape outline

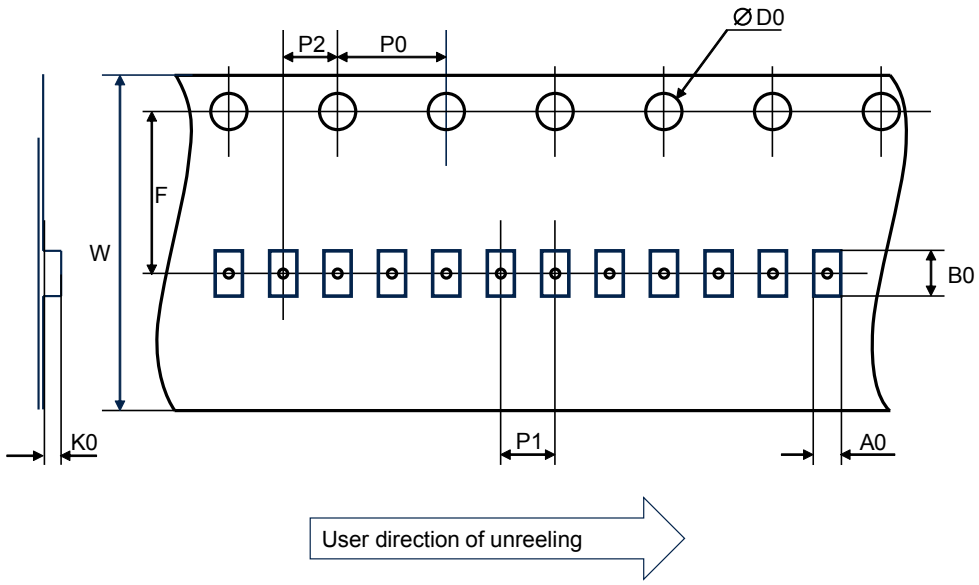


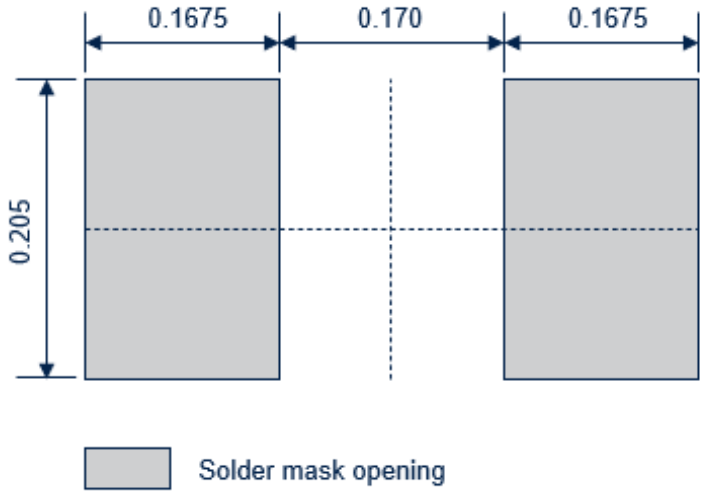
Table 4. Tape and reel mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A0	0.31	0.34	0.37
B0	0.61	0.64	0.67
D0	1.40	1.50	1.60
F	3.45	3.50	3.55
K0	0.21	0.24	0.27
P0	3.90	4.00	4.10
P1	1.95	2.00	2.05
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

3 Recommendation on PCB assembly

3.1 Footprint

Figure 14. **Recommended footprint in mm**

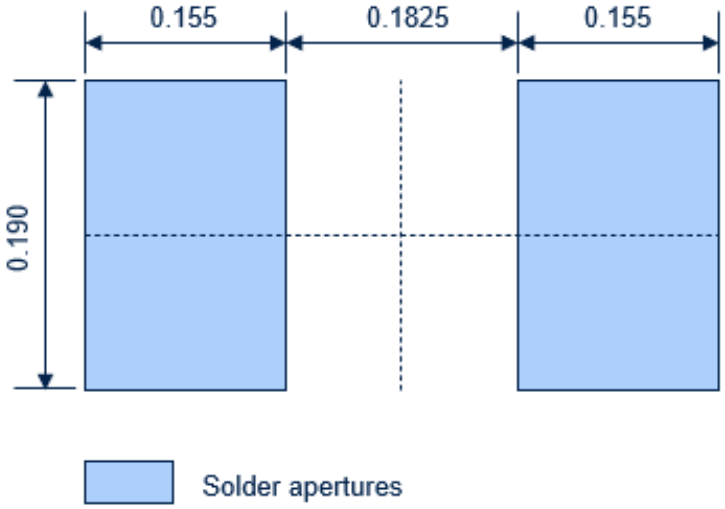


Note: Solder mask defined (SMD) recommended.

3.2 Stencil opening design

Stencil opening thickness: 75 µm / 3 mils

Figure 15. **Stencil opening recommendations**



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

3.4 Placement

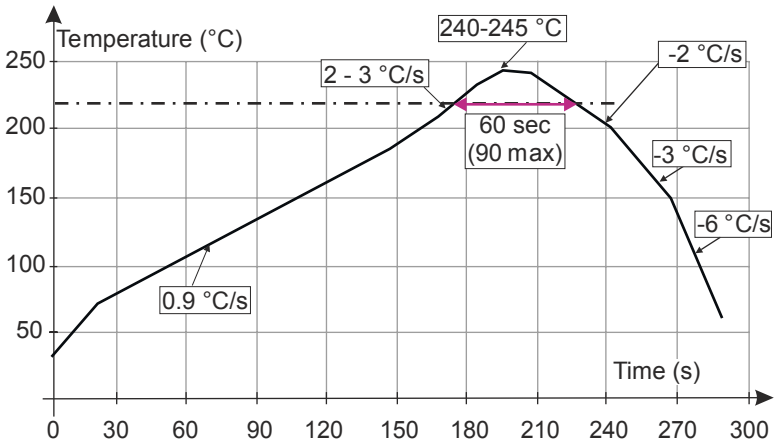
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 16. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDZX168B-1BF4	U[1]	ST0201	0.100 mg	17000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
21-Sep-2023	1	Initial release.
10-Jul-2024	2	Updated *Table 2*, *Figure 3*, *Figure 4*, *Figure 5*, and *Figure 6*.
16-Sep-2024	3	Updated *Product status link* on cover page.
26-Jun-2025	4	Updated Section Features. Added Figure 8, and Figure 9.