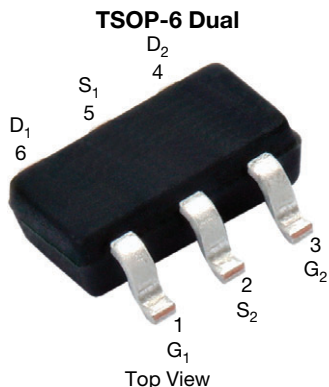


Automotive N- and P-Channel 20 V (D-S) MOSFET

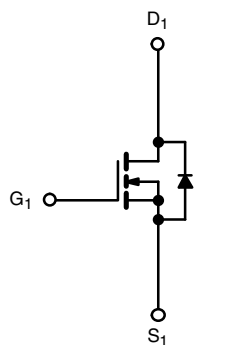


FEATURES

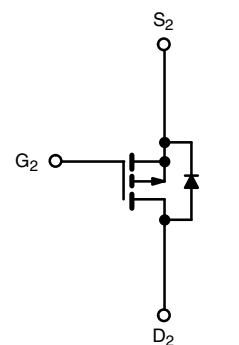
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE



N-Channel MOSFET



P-Channel MOSFET

PRODUCT SUMMARY

	N-CHANNEL	P-CHANNEL
V _{DS} (V)	20	-20
R _{DS(on)} (Ω) at V _{GS} = ± 4.5 V	0.077	0.166
R _{DS(on)} (Ω) at V _{GS} = ± 2.5 V	0.120	0.318
I _D (A)	3.57	-2.5
Configuration	N- and p-pair	

ORDERING INFORMATION

Package	TSOP-6 Dual
Lead (Pb)-free and halogen-free	SQ3585EV (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage	V _{DS}	20	-20	V
Gate-source voltage	V _{GS}	± 12	± 12	
Continuous drain current	I _D	3.57	-2.5	A
		2	-1.45	
Pulsed drain current	I _{DM}	12	-10	
Continuous source current (diode conduction)	I _S	2.1	-2.1	W
Maximum power dissipation	P _D	1.67	1.67	
		0.56	0.56	
Unclamped inductive surge UIS	I _{AV}	3.3	3	A
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175		°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	N-CHANNEL MAX.	P-CHANNEL MAX.	UNIT
Maximum junction-to-ambient ^a	R _{thJA}	150	150	°C/W
Maximum junction-to-foot (drain)	R _{thJF}	90	90	

Note

a. Surface mounted on 1" x 1" FR4 board

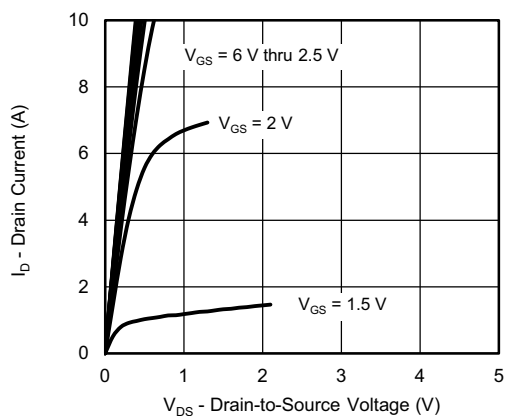
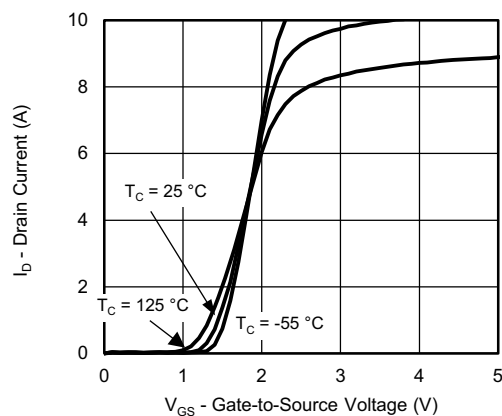
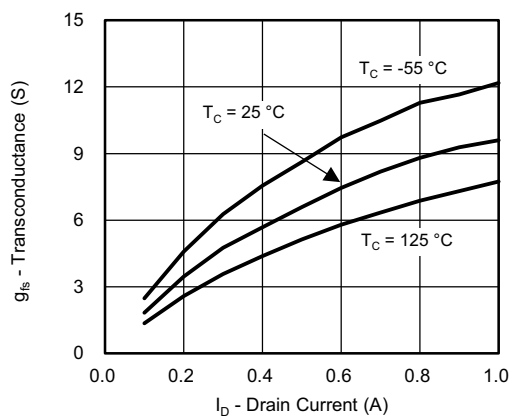
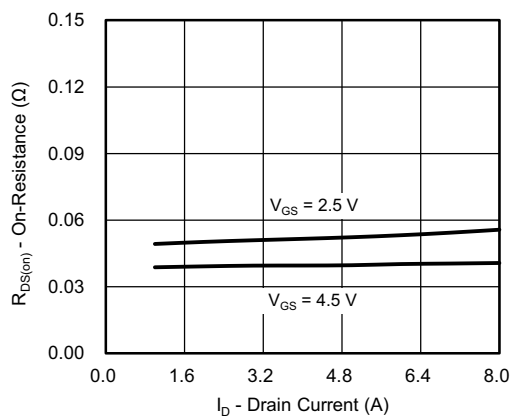
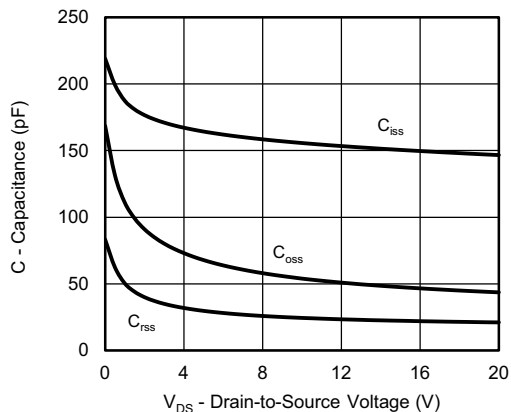
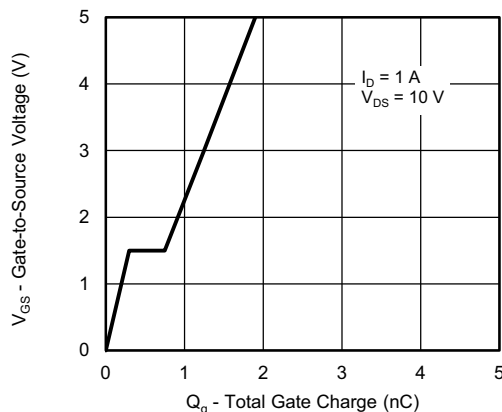


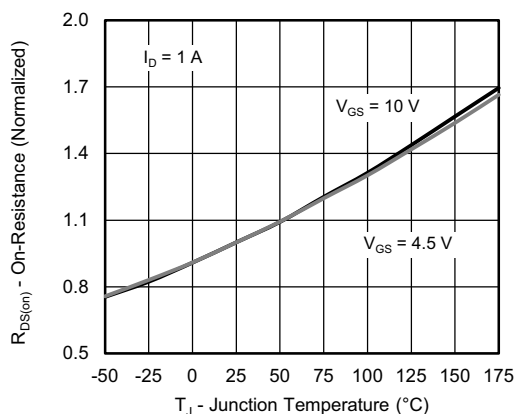
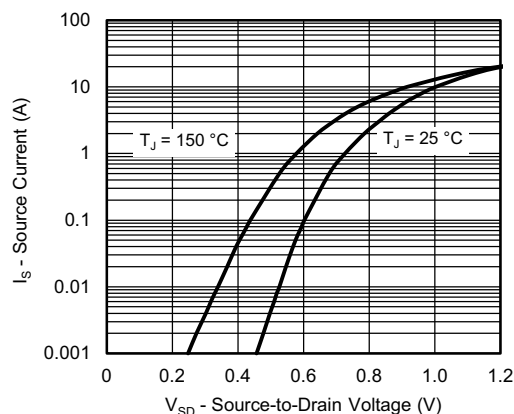
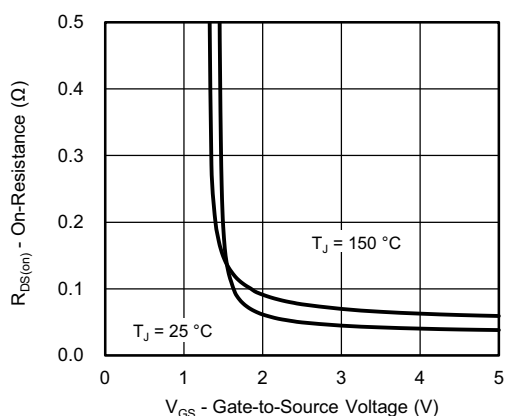
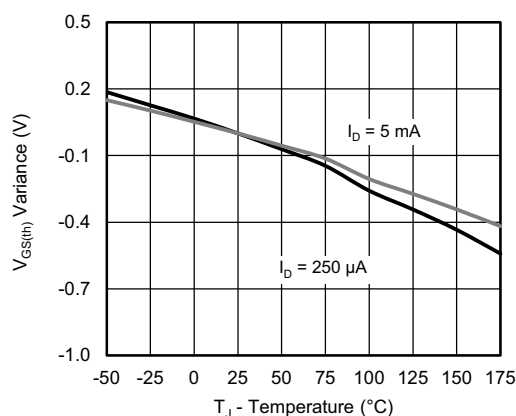
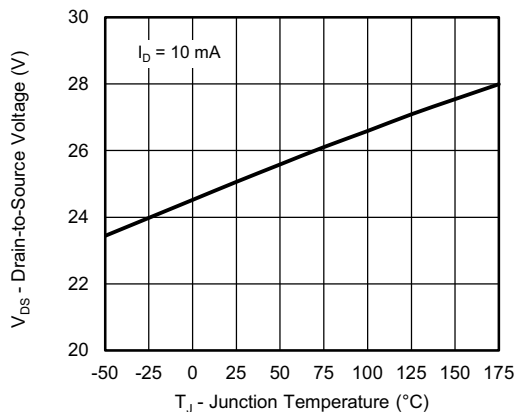
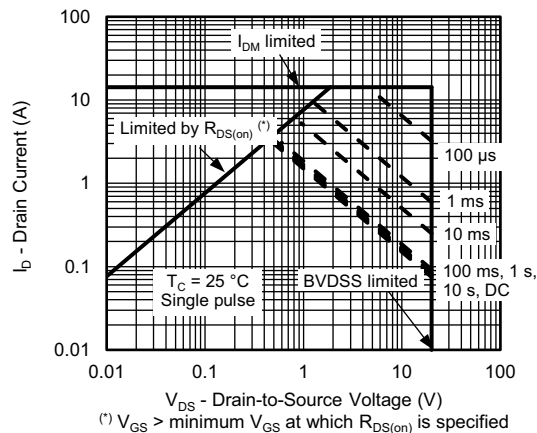
SPECIFICATIONS (T _J = 25°C, unless otherwise noted)									
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT	
Static									
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch	0.6	-	1.5	V	
		V _{DS} = V _{GS} , I _D = -250 μA		P-Ch	-0.6	-	-1.5		
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V		N-Ch	-	-	± 100	nA	
				P-Ch	-	-	± 100		
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 20 V	N-Ch	-	-	1	μA	
		V _{GS} = 0 V	V _{DS} = -20 V	P-Ch	-	-	-1		
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 55 °C	N-Ch	-	-	5		
		V _{GS} = 0 V	V _{DS} = -20 V, T _J = 55 °C	P-Ch	-	-	-5		
On-state drain current ^a	I _{D(on)}	V _{GS} = 4.5 V	V _{DS} ≥ 5 V	N-Ch	5	-	-	A	
		V _{GS} = -4.5 V	V _{DS} ≤ -5 V	P-Ch	-5	-	-		
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 1 A	N-Ch	-	0.049	0.077	Ω	
		V _{GS} = -4.5 V	I _D = -1 A	P-Ch	-	0.140	0.166		
		V _{GS} = 2.5 V	I _D = 1 A	N-Ch	-	0.066	0.120		
		V _{GS} = -2.5 V	I _D = -1 A	P-Ch	-	0.265	0.318		
Forward transconductance ^a	g _{fs}	V _{DS} = 5 V, I _D = 1 A		N-Ch	-	10	-	S	
		V _{DS} = -5 V, I _D = -1 A		P-Ch	-	3	-		
Diode forward voltage ^a	V _{SD}	I _S = 1.05 A, V _{GS} = 0 V		N-Ch	-	0.80	1.10	V	
		I _S = -1.05 A, V _{GS} = 0 V		P-Ch	-	-0.83	-1.10		
Dynamic ^b									
Total gate charge	Q _g	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 1 A	N-Ch	-	1.8	2.5	nC	
		V _{GS} = -4.5 V	V _{DS} = -10 V, I _D = -1 A	P-Ch	-	2.4	3.5		
Gate-source charge	Q _{gs}	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 1 A	N-Ch	-	0.3	-		
		V _{GS} = -4.5 V	V _{DS} = -10 V, I _D = -1 A	P-Ch	-	0.4	-		
Gate-drain charge	Q _{gd}	V _{GS} = 4.5 V	V _{DS} = 10 V, I _D = 1 A	N-Ch	-	0.4	-		
		V _{GS} = -4.5 V	V _{DS} = -10 V, I _D = -1 A	P-Ch	-	0.7	-		
Gate resistance	R _g	f = 1 MHz		N-Ch	3.4	-	9.1	Ω	
				P-Ch	3.4	-	9.1		
Turn-on delay time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 10 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 kΩ		N-Ch	-	9	12	ns	
Rise time	t _r			P-Ch	-	7	11		
				N-Ch	-	15	19		
				P-Ch	-	16	22		
Turn-off delay time	t _{d(off)}	P-Channel V _{DD} = -10 V, R _L = 10 Ω I _D ≡ -1 A, V _{GEN} = -10 V, R _g = 1 kΩ		N-Ch	-	22	28		
				P-Ch	-	29	40		
Fall time	t _f			N-Ch	-	8	12		
				P-Ch	-	14	24		

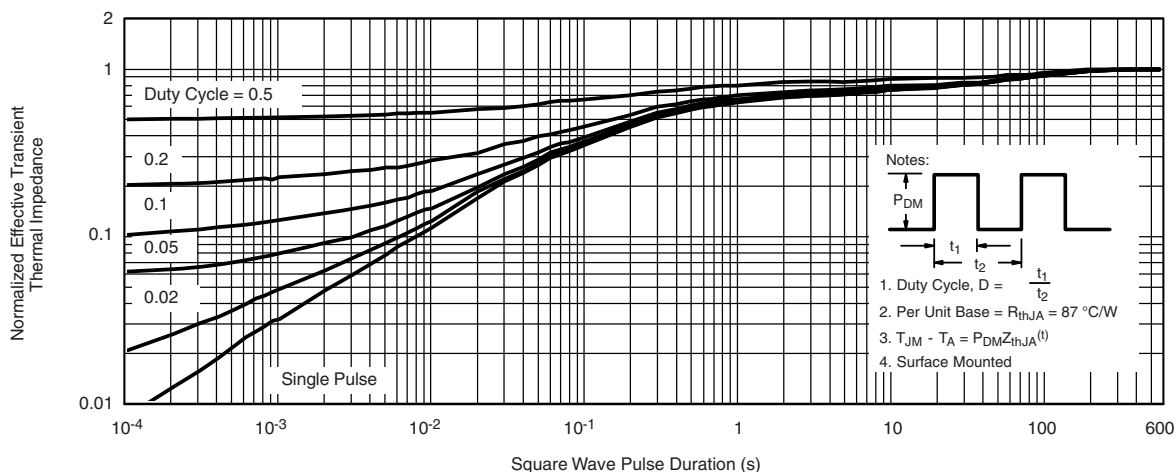
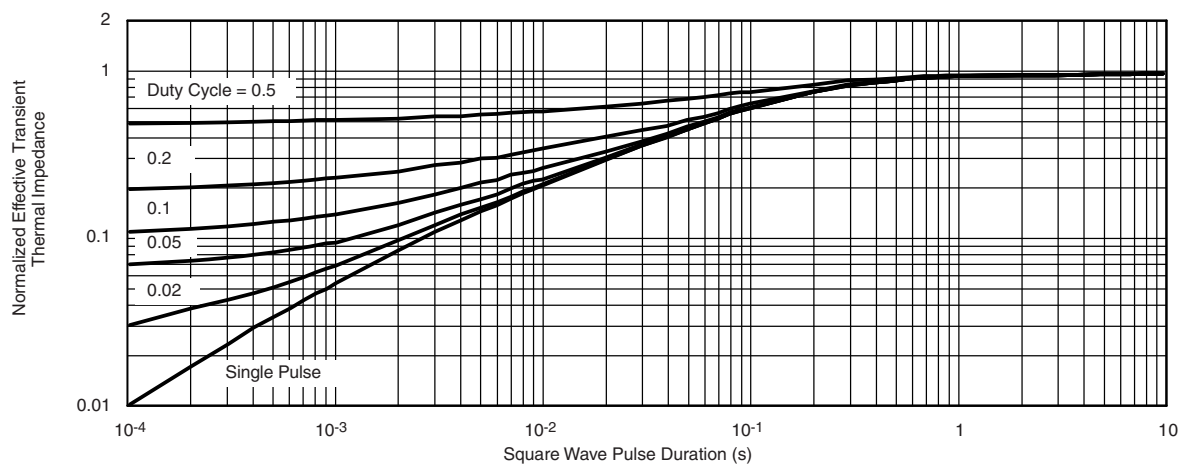
Notes

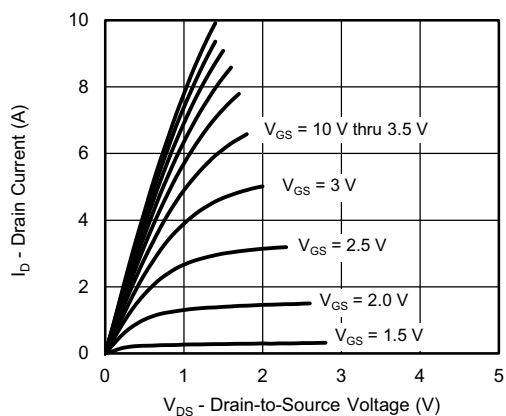
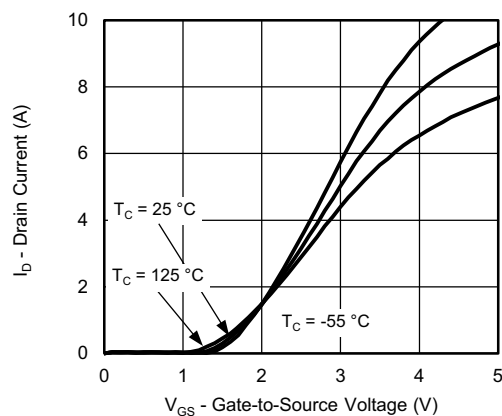
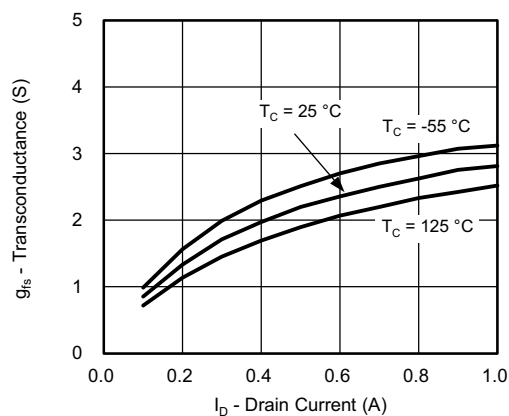
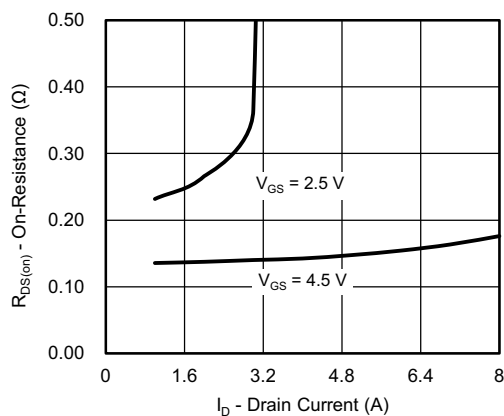
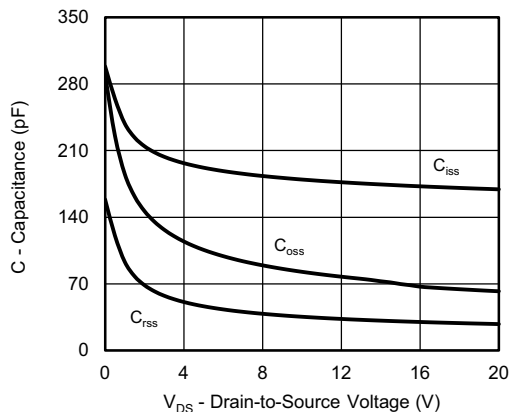
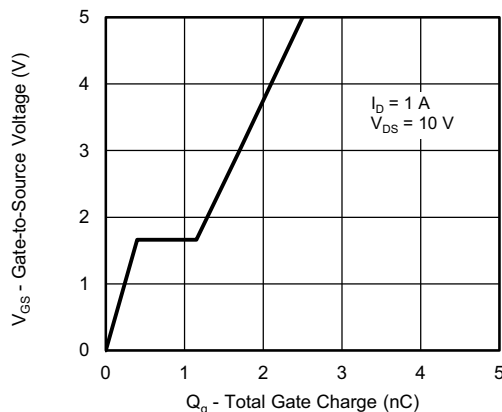
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

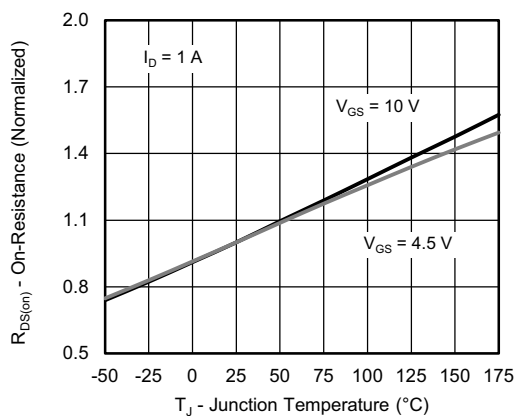
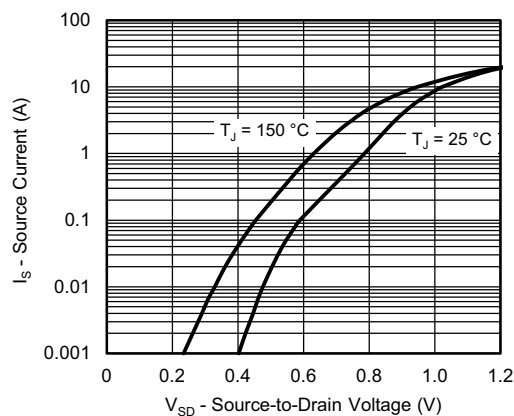
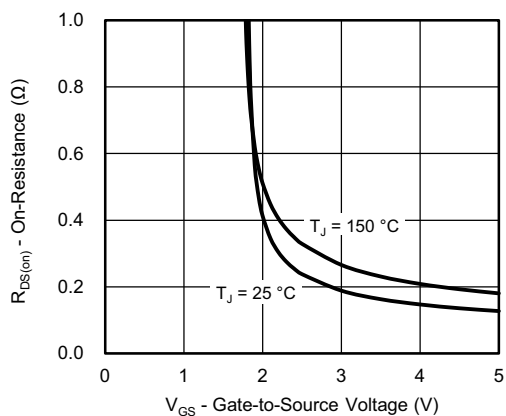
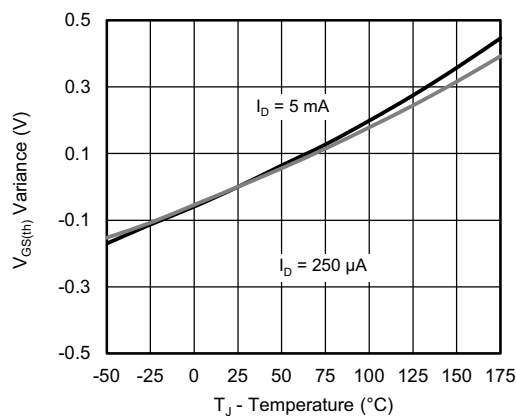
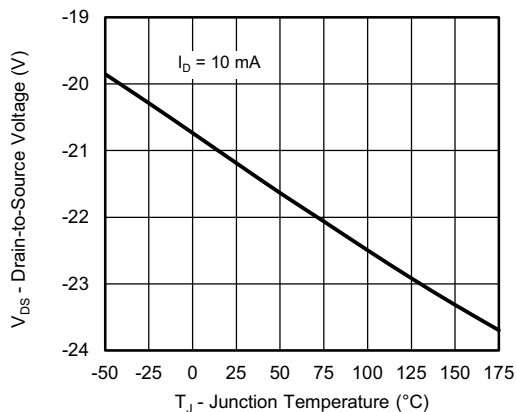
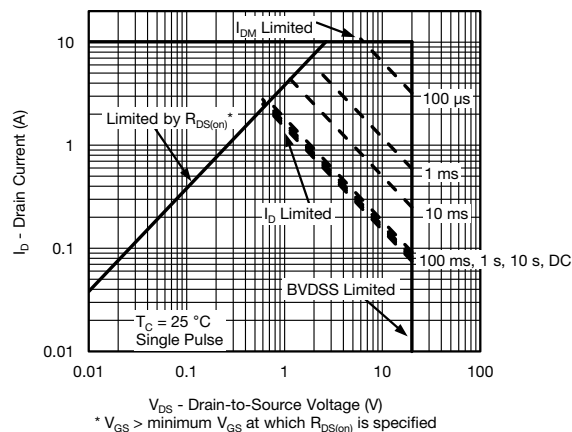
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area

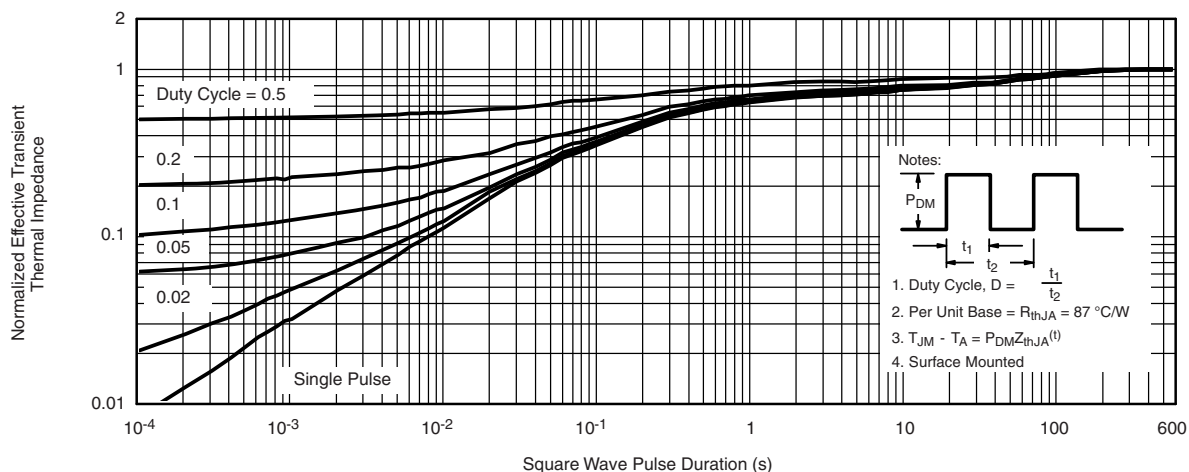
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

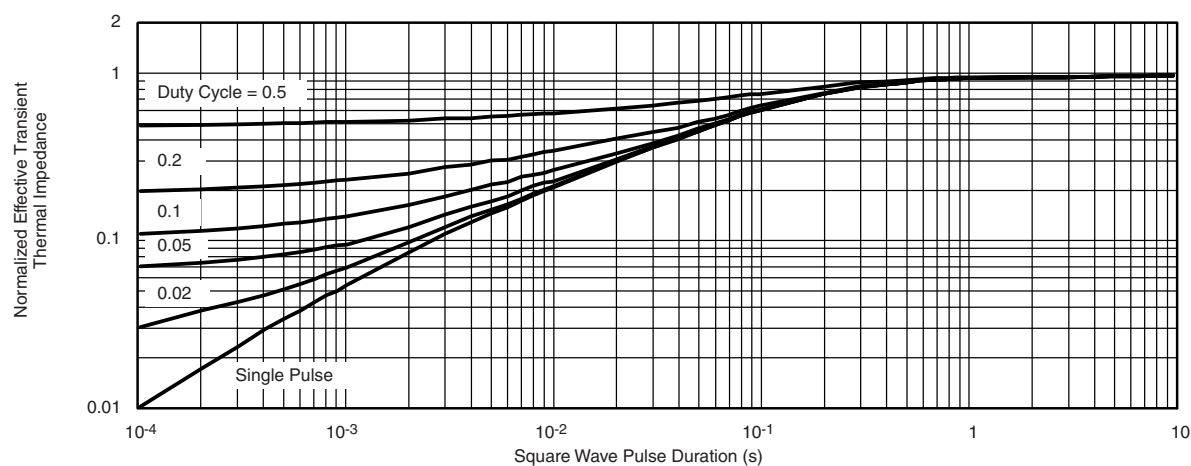
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



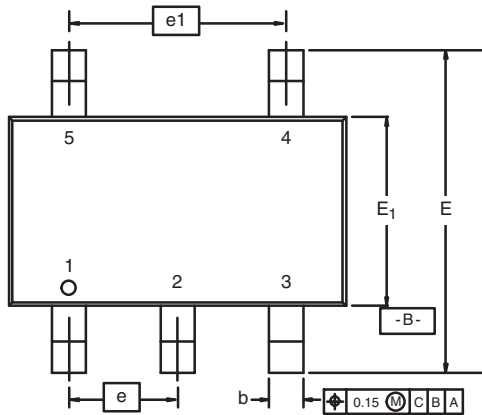
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75126.

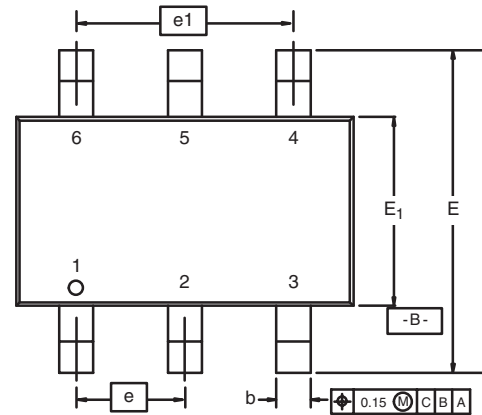


TSOP: 5/6-LEAD

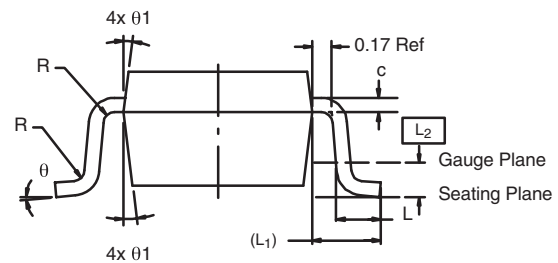
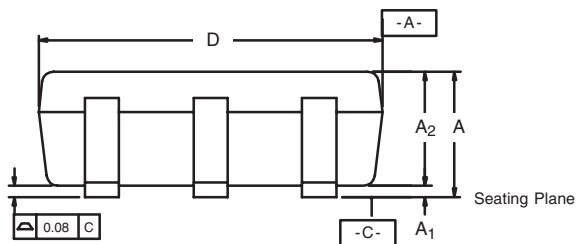
JEDEC Part Number: MO-193C



5-LEAD TSOP

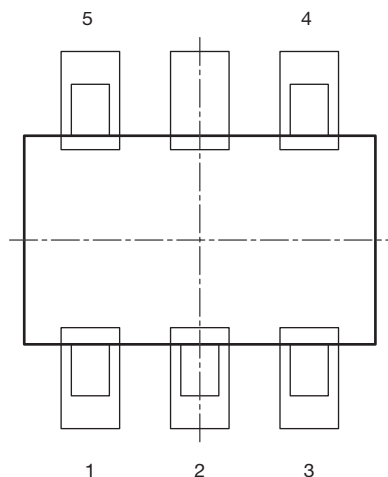


6-LEAD TSOP

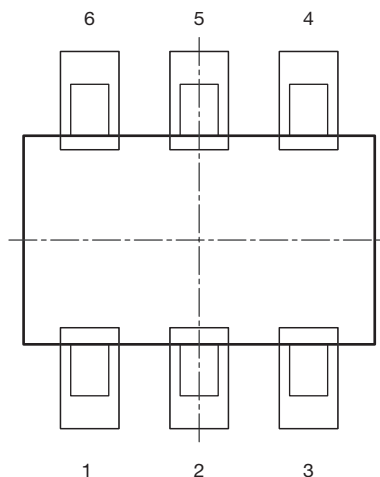


	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

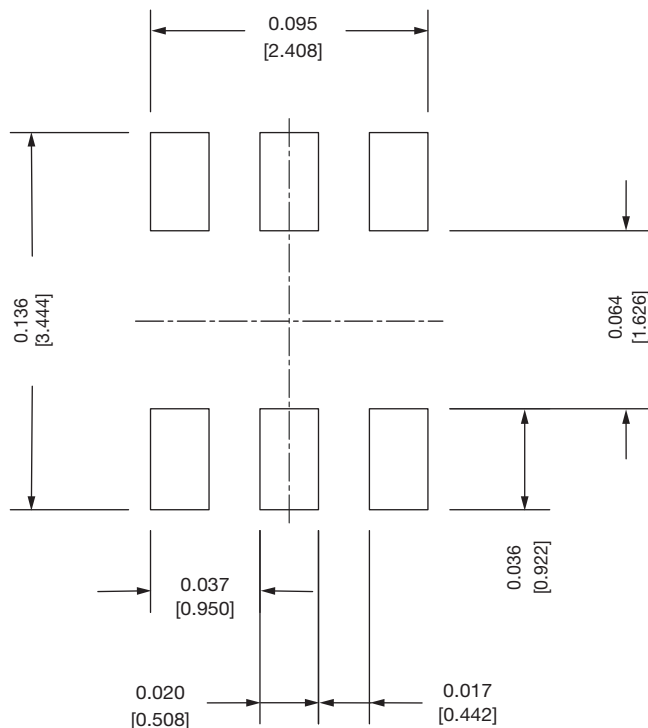
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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