

# MOSFET – Power, Single N-Channel

**40 V, 7.3 mΩ, 52 A**

## NVMYS7D3N04CL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- LFAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Value	Unit	
$V_{DSS}$	Drain-to-Source Voltage		40	V	
$V_{GS}$	Gate-to-Source Voltage		$\pm 20$	V	
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	52	A
			$T_C = 100\text{ }^\circ\text{C}$	29	
$P_D$	Power Dissipation $R_{\theta JC}$ (Notes 1, 2, 3)		$T_C = 25\text{ }^\circ\text{C}$	38	W
			$T_C = 100\text{ }^\circ\text{C}$	12	
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3, 4)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	17	A
			$T_A = 100\text{ }^\circ\text{C}$	12	
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1, 3)		$T_A = 25\text{ }^\circ\text{C}$	3.8	W
			$T_A = 100\text{ }^\circ\text{C}$	1.9	
$I_{DM}$	Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, t_p = 10\text{ }\mu\text{s}$	269	A	
$T_J, T_{stg}$	Operating Junction and Storage Temperature		-55 to +175	$^\circ\text{C}$	
$I_S$	Source Current (Body Diode)		31	A	
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 2.9\text{ A}$ )		65	mJ	
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case - Steady State (Note 3)	4.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 3)	39	

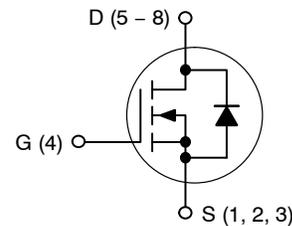
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Psi ( $\Psi$ ) is used as required per JE51-12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
40 V	7.3 mΩ @ 10 V	52 A
	12 mΩ @ 4.5 V	

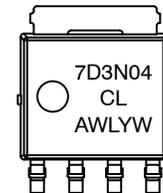


LFAK4  
CASE 760AB

### N-Channel



### MARKING DIAGRAM



7D3N04CL = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
W = Work Week

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMYS7D3N04CL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

### OFF CHARACTERISTICS

V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
V <sub>(BR)DSS</sub> /T <sub>J</sub>	Drain-to-Source Breakdown Voltage Temperature Coefficient			25		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 40 V			10	μA
					250	
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 5)

V <sub>GS(TH)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 30 μA	1.2		2.0	V
R <sub>DS(on)</sub>	Drain-to-Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		6.1	7.3	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		9.7	12	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		33		S

### CHARGES AND CAPACITANCES

C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		860		pF
C <sub>oss</sub>	Output Capacitance			360		
C <sub>riss</sub>	Reverse Transfer Capacitance			15		
Q <sub>G(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 10 A		7.0		nC
Q <sub>G(TH)</sub>	Threshold Gate Charge	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 10 A		1.8		nC
Q <sub>GS</sub>	Gate-to-Source Charge			3.3		
Q <sub>GD</sub>	Gate-to-Drain Charge			2.5		
Q <sub>G(TOT)</sub>	Total Gate Charge		V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 10 A		16	

### SWITCHING CHARACTERISTICS (Note 6)

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 32 V, I <sub>D</sub> = 10 A, R <sub>G</sub> = 1 Ω		8.0		ns
t <sub>r</sub>	Rise Time			24		
t <sub>d(off)</sub>	Turn-Off Delay Time			29		
t <sub>f</sub>	Fall Time			6.0		

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Forward Diode Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A	T <sub>J</sub> = 25 °C		0.84	1.2	V
			T <sub>J</sub> = 125 °C		0.71		
t <sub>RR</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 10 A		24		ns	
t <sub>a</sub>	Charge Time			11			
t <sub>b</sub>	Discharge Time			12			
Q <sub>RR</sub>	Reverse Recovery Charge			11			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

# NVMYS7D3N04CL

## TYPICAL CHARACTERISTICS

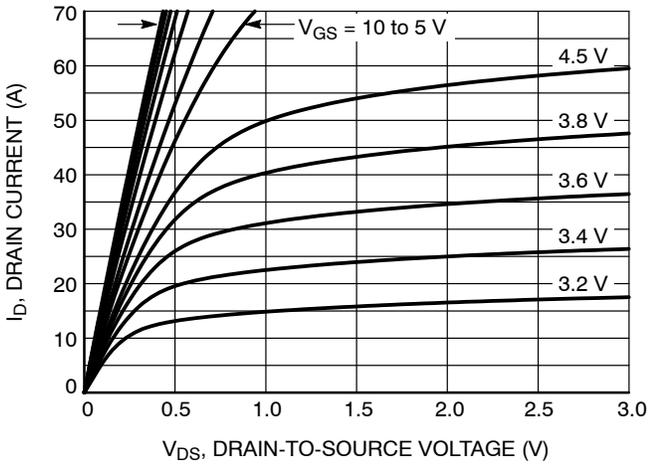


Figure 1. On-Region Characteristics

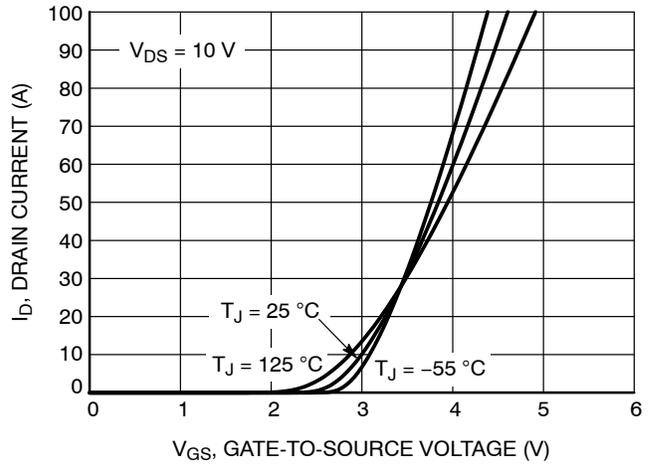


Figure 2. Transfer Characteristics

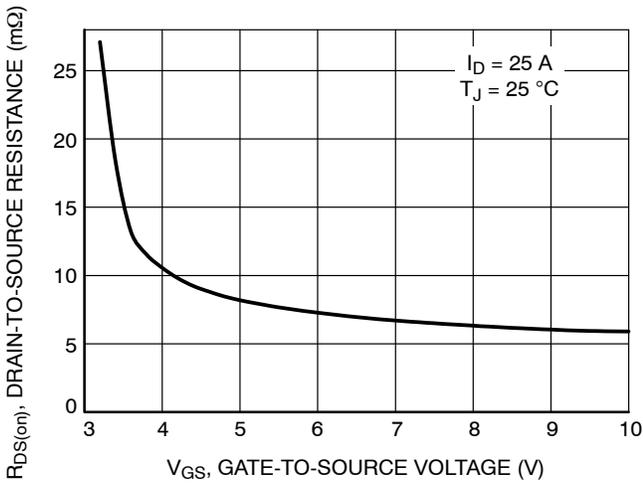


Figure 3. On-Resistance vs. Gate-to-Source Voltage

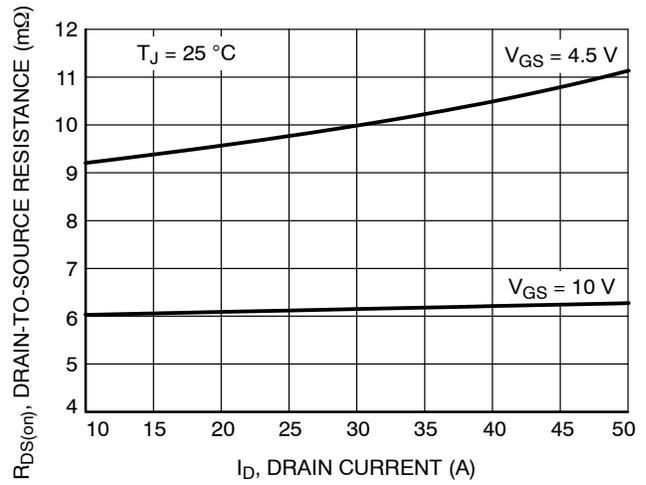


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

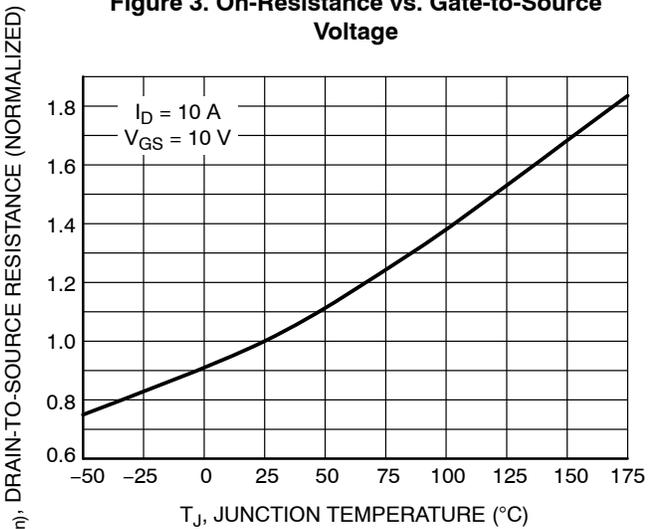


Figure 5. On-Resistance Variation with Temperature

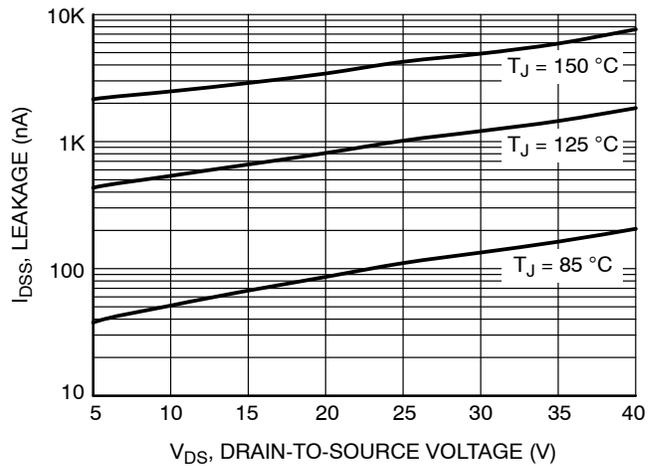


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

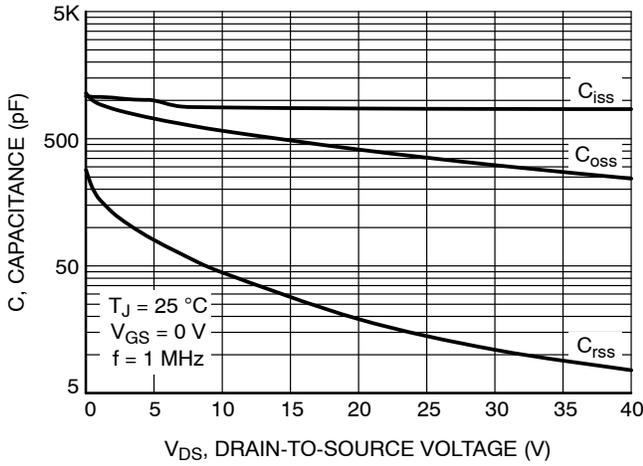


Figure 7. Capacitance Variation

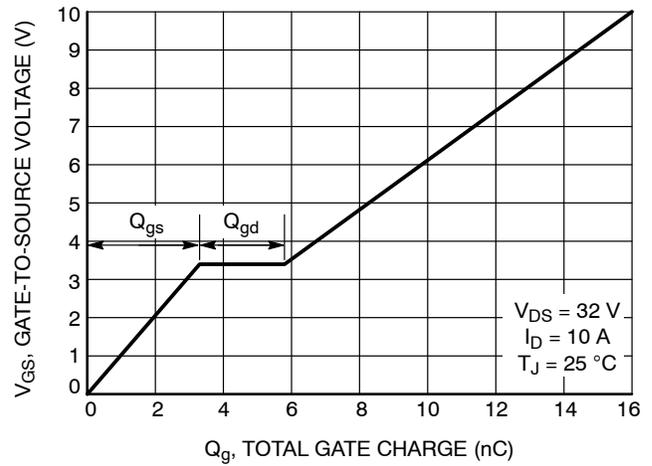


Figure 8. Gate-to-Source vs. Total Charge

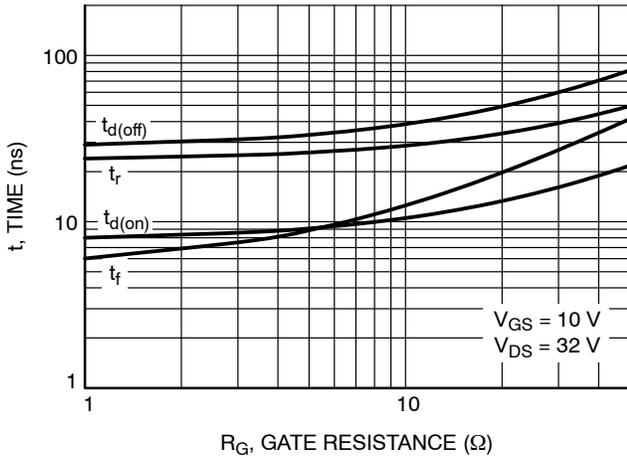


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

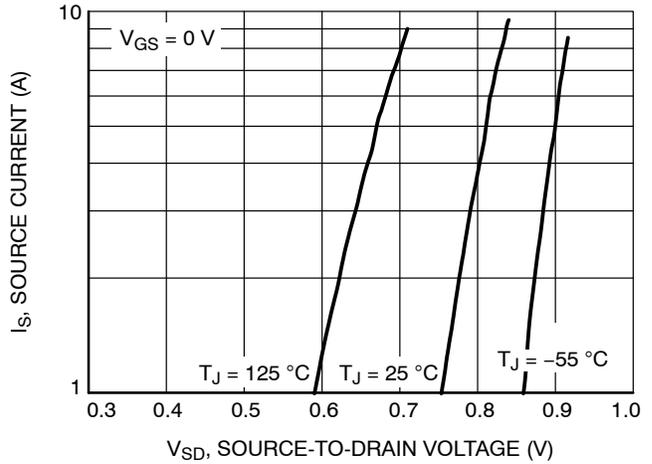


Figure 10. Diode Forward Voltage vs. Current

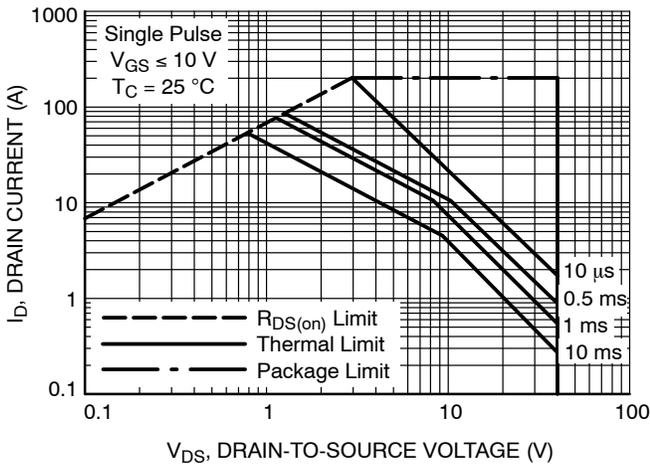


Figure 11. Maximum Rated Forward Biased Safe Operating Area

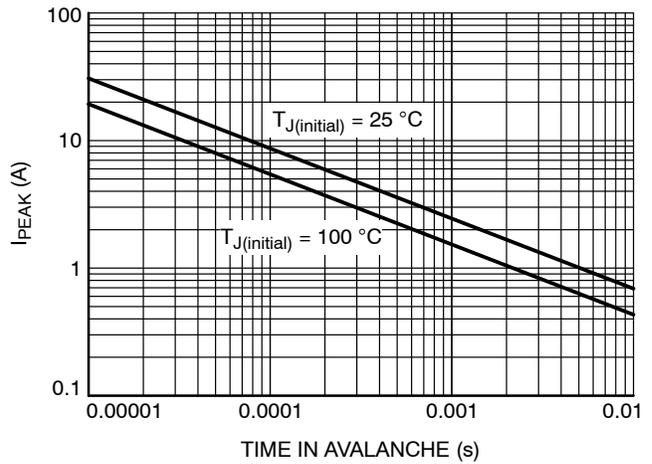


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMYS7D3N04CL

## TYPICAL CHARACTERISTICS (continued)

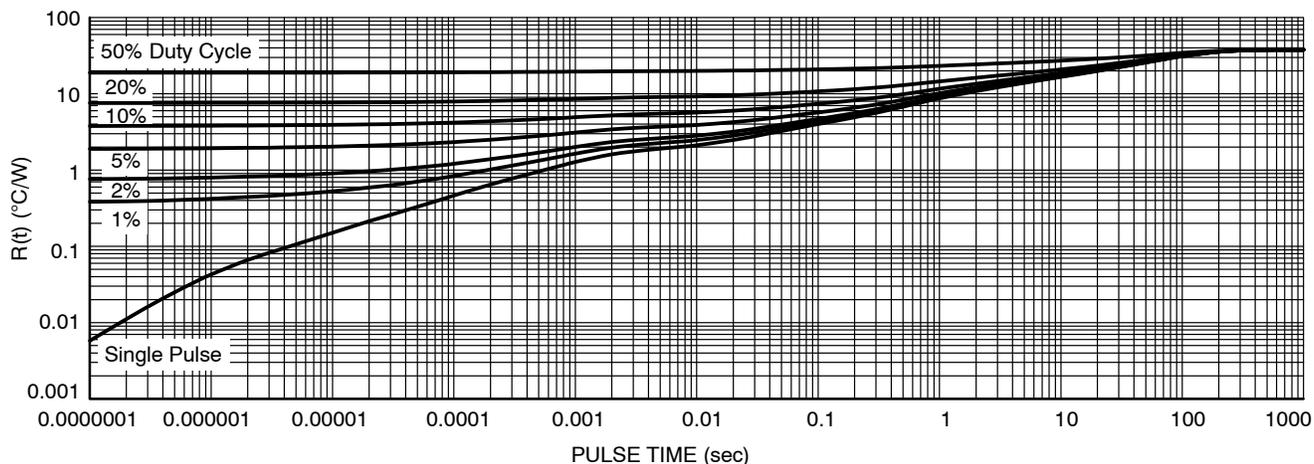


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMYS7D3N04CLTWG	7D3N04CL	LFPAK4 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

**NVMYS7D3N04CL**

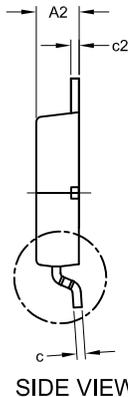
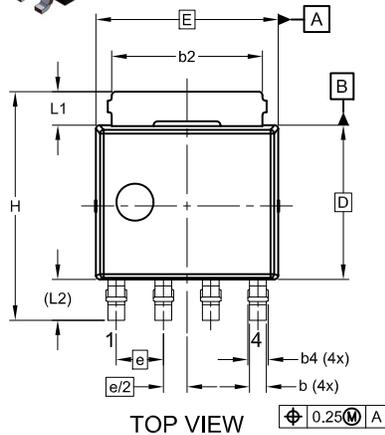
**REVISION HISTORY**

<b>Revision</b>	<b>Description of Changes</b>	<b>Date</b>
1	Rebranded the Data Sheet to <b>onsemi</b> format.	12/1/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

LFLPAK4 4.90x4.15x1.15MM, 1.27P  
CASE 760AB  
ISSUE D

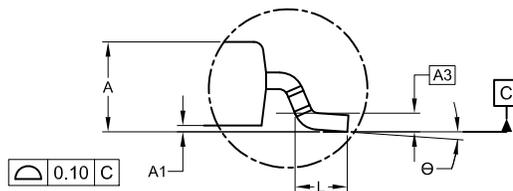
DATE 22 MAY 2024



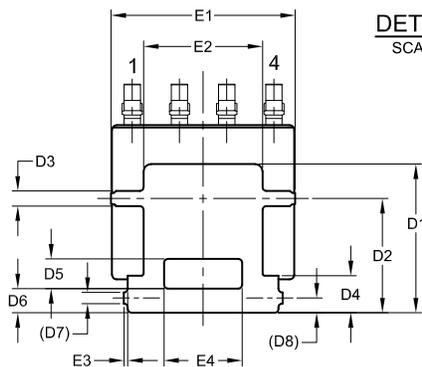
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
  4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

TOP VIEW  $\text{M} \begin{matrix} \text{A} \\ 0.25 \end{matrix}$

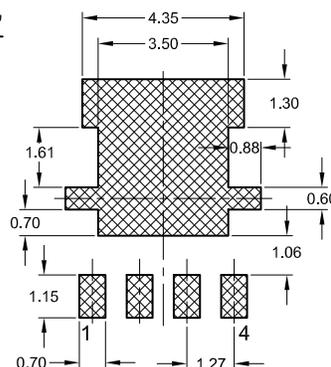
SIDE VIEW



DETAIL 'A'  
SCALE: 2:1



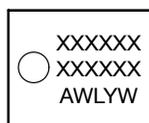
BOTTOM VIEW



RECOMMENDED LAND PATTERN

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- W = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
Θ	0°	4°	8°

DOCUMENT NUMBER:	98AON82777G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	LFLPAK4 4.90x4.15x1.15MM, 1.27P	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)