

# MOSFET - Power, Single N-Channel, STD Gate, SO8-FL

## 40 V, 0.7 mΩ, 323 A

### NVMFWS0D7N04XM

#### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Applications

- Motor Drive
- Battery Protection
- Synchronous Rectification

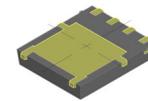
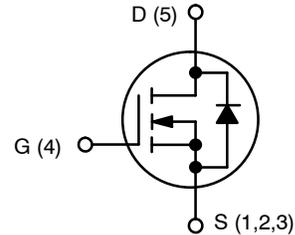
#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	40	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	$T_C = 25^\circ\text{C}$	323
		$T_C = 100^\circ\text{C}$	229
Power Dissipation	$P_D$	134	W
Continuous Drain Current	$I_{DA}$	$T_A = 25^\circ\text{C}$	9.18
		$T_A = 100^\circ\text{C}$	6.49
Pulsed Drain Current	$I_{DM}$	900	A
Pulsed Source Current (Body Diode)	$I_{SM}$	900	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	202	A
Single Pulse Avalanche Energy ( $I_{PK} = 21\text{ A}$ )	$E_{AS}$	987	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

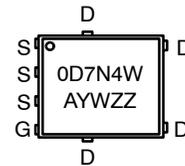
$V_{(BR)DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
40 V	0.7 mΩ	323 A

#### N-CHANNEL MOSFET



DFNW5 (SO-8FL)  
CASE 507BA

#### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFWS0D7N04XM

## THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.11	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	39.3	

- Surface-mounted on FR4 board using 650 mm<sup>2</sup> pad, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 250\ \mu\text{A}$ , Referenced to 25°C		14.9		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, T_J = 25^\circ\text{C}$			1	μA
		$V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$			40	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

### ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		0.59	0.7	mΩ
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 180\ \mu\text{A}$	2.5	3.0	3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 180\ \mu\text{A}$		-7.2		mV/°C
Forward Trans-conductance	$g_{FS}$	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		244		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		4595		pF
Output Capacitance	$C_{OSS}$			2980		
Reverse Transfer Capacitance	$C_{RSS}$			41.8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 32\text{ V}; I_D = 50\text{ A}$		71.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			13.5		
Gate-to-Source Charge	$Q_{GS}$			20.6		
Gate-to-Drain Charge	$Q_{GD}$			13		
Gate Resistance	$R_G$		$f = 1\text{ MHz}$		0.69	

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 32\text{ V}, I_D = 50\text{ A}, R_G = 0\ \Omega$		7.33		ns
Rise Time	$t_r$			5.39		
Turn-Off Delay Time	$t_{d(OFF)}$			11.1		
Fall Time	$t_f$			4.48		

### SOURCE TO DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.81	1.2	V
			$T_J = 125^\circ\text{C}$		0.66		
Reverse Recovery Time	$t_{RR}$	$V_{DD} = 32\text{ V}, I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$			94.4		ns
Charge Time	$t_a$				55.6		
Discharge Time	$t_b$				38.8		
Reverse Recovery Charge	$Q_{RR}$				269		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

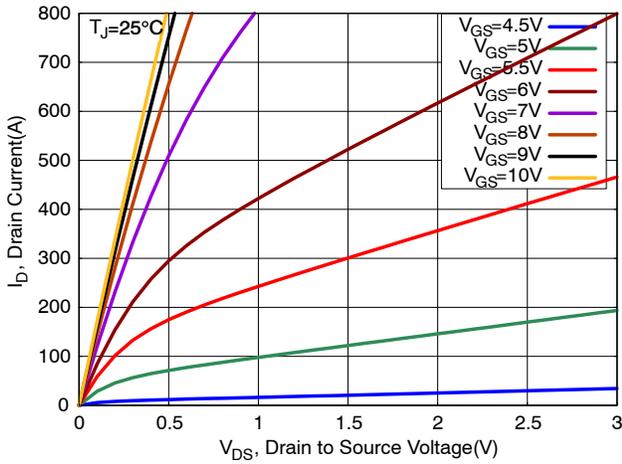


Figure 1. On-Region Characteristics

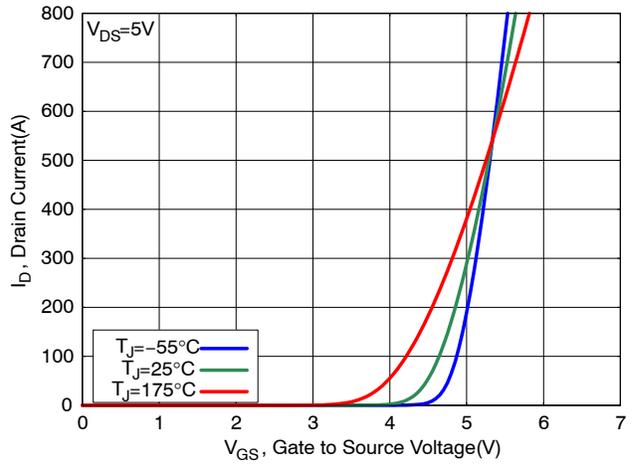


Figure 2. Transfer Characteristics

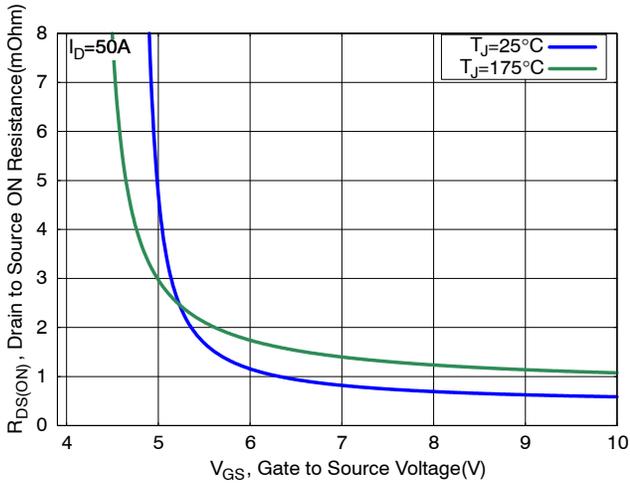


Figure 3. On-Resistance vs. Gate Voltage

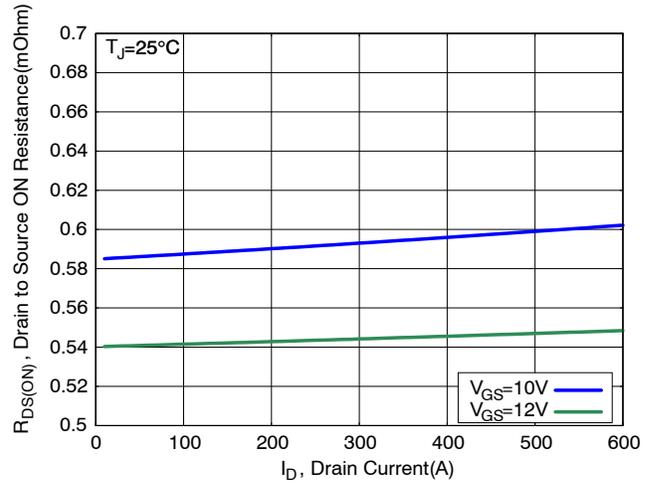


Figure 4. On-Resistance vs. Drain Current

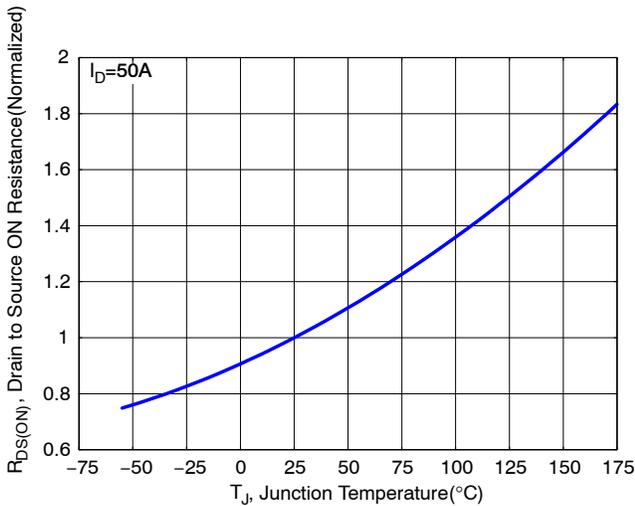


Figure 5. Normalized ON Resistance vs. Junction Temperature

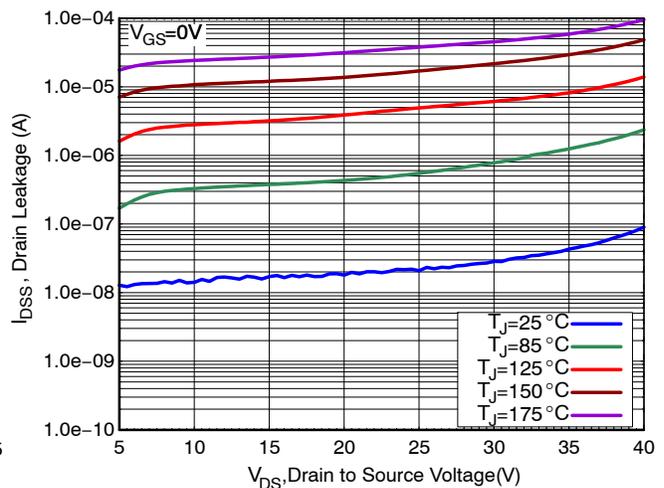


Figure 6. Drain Leakage vs. Drain-to-Source Voltage

# NVMFWS0D7N04XM

## TYPICAL CHARACTERISTICS

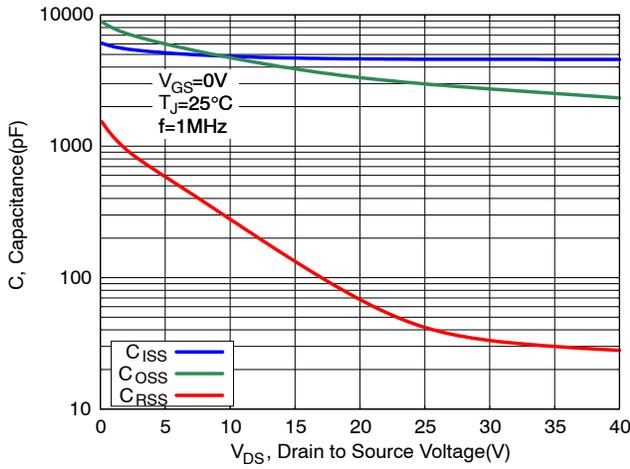


Figure 7. Capacitance Characteristics

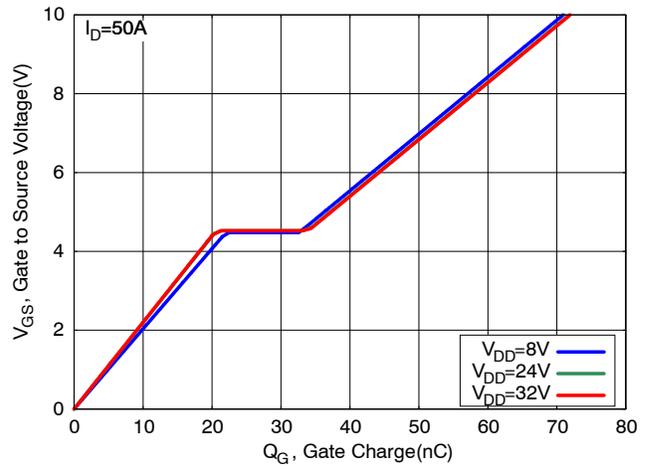


Figure 8. Gate Charge Characteristics

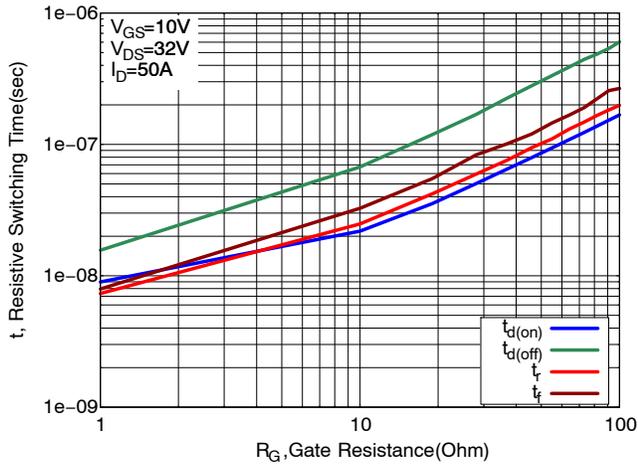


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

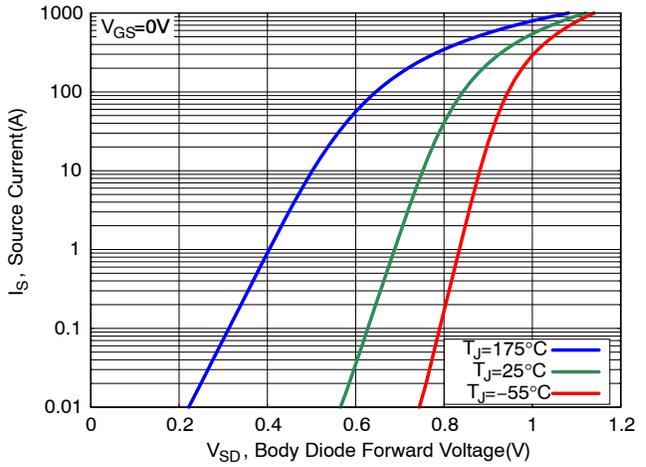


Figure 10. Diode Forward Characteristics

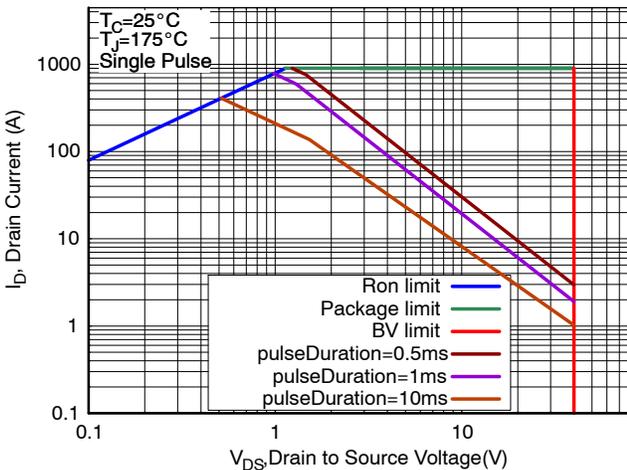


Figure 11. Maximum Rated Forward Biased Safe Operating Area

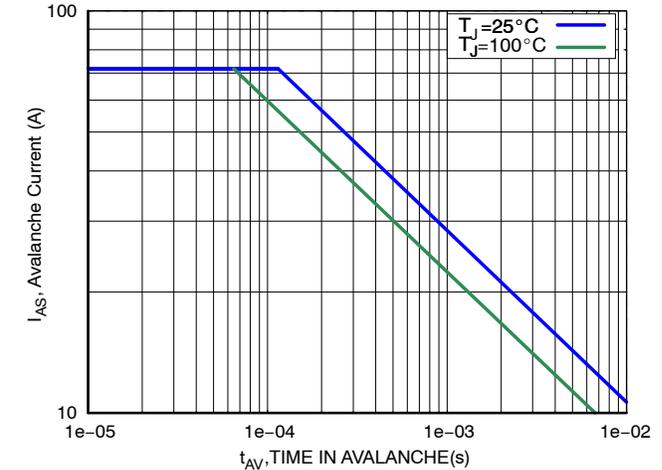


Figure 12.  $I_{peak}$  vs. Time in Avalanche

# NVMFWS0D7N04XM

## TYPICAL CHARACTERISTICS

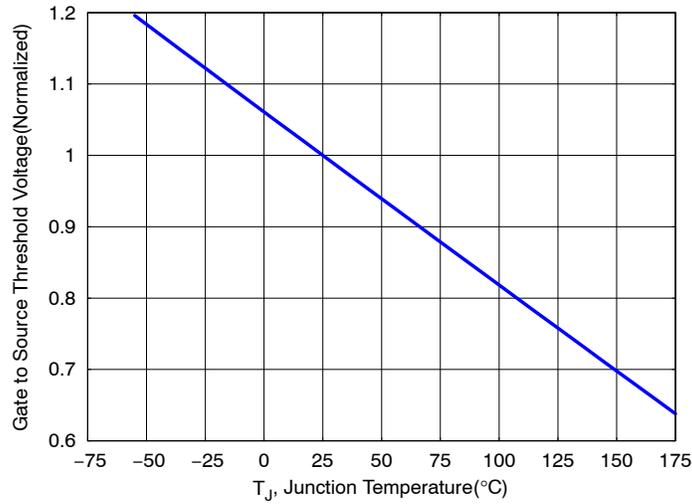


Figure 13. Gate Threshold Voltage vs. Junction Temperature

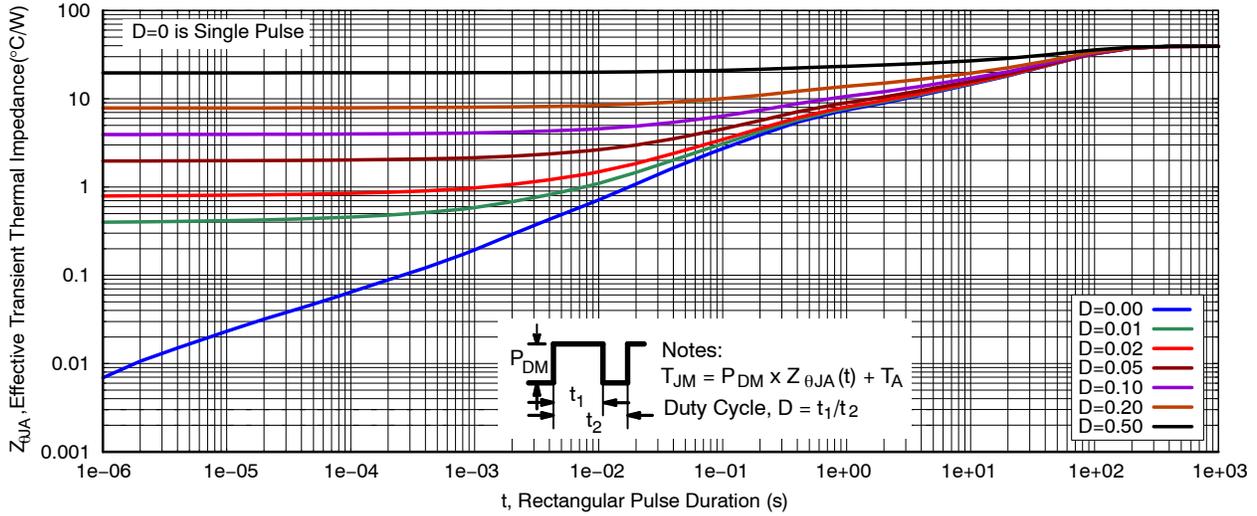
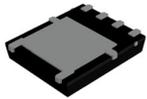


Figure 14. Thermal Response

### ORDERING INFORMATION

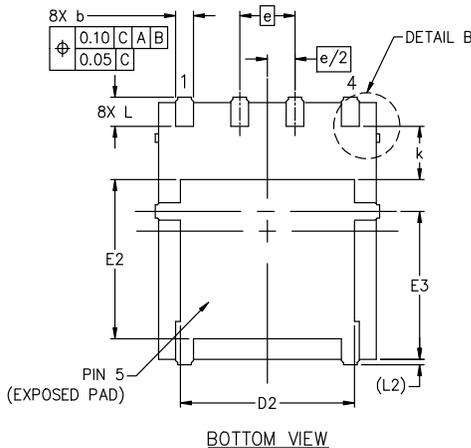
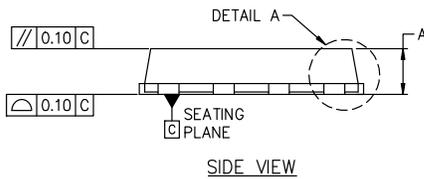
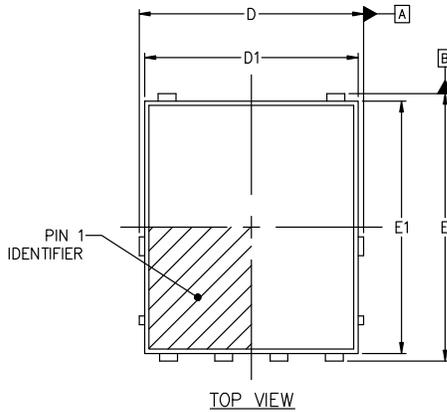
Device	Marking	Package	Shipping <sup>†</sup>
NVMFWS0D7N04XMT1G	0D7N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel
NVMFWS0D7N04XMET1G	0D7N4W	DFNW5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



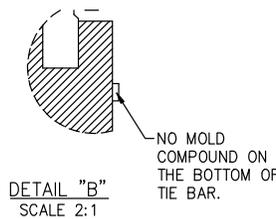
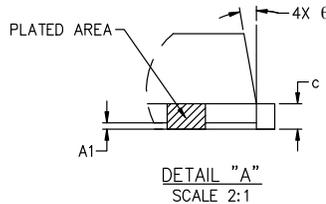
DFNW5 4.90x5.90x1.00, 1.27P  
CASE 507BA  
ISSUE C

DATE 19 SEP 2024

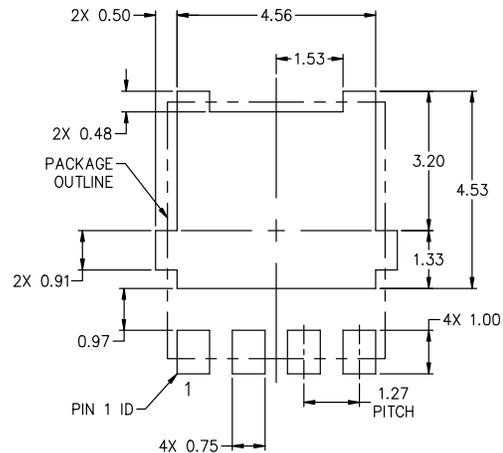


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
theta	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT\*  
\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON26450H	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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