

# MOSFET – N-Channel Shielded Gate POWERTRENCH®

150 V, 15 mΩ, 61.3 A

## NVDS015N15MC

### Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)}$  = 15 mΩ at  $V_{GS} = 10$  V,  $I_D = 29$  A
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Primary Side for 48 V Isolated Bus
- SR for MV Secondary Applications

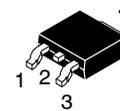
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
$V_{DSS}$	Drain-to-Source Voltage	150	V	
$V_{GS}$	Gate-to-Source Voltage	±20	V	
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State		
		$T_C = 25^\circ\text{C}$	61.3	A
		$T_C = 100^\circ\text{C}$	43.4	
$P_D$	Power Dissipation $R_{\theta JC}$ (Note 2)	Steady State		
		$T_C = 25^\circ\text{C}$	107.1	W
		$T_C = 100^\circ\text{C}$	53.6	
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State		
		$T_A = 25^\circ\text{C}$	10.5	A
		$T_A = 100^\circ\text{C}$	7.4	
$P_D$	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State		
		$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 100^\circ\text{C}$	1.6	
$I_{DM}$	Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$	382	A
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to +175	°C	
$I_S$	Source Current (Body Diode)	89.3	A	
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 4.4$ A)	1301	mJ	
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	°C	

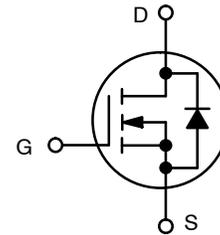
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
150 V	15 mΩ @ 10 V	61.3 A

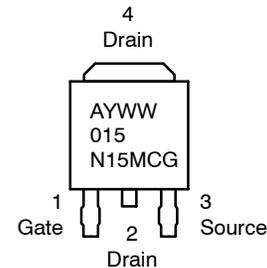


DPAK  
CASE 369C



N-CHANNEL MOSFET

### MARKING DIAGRAM



015N15MCG = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping†
NVDS015N15MCT4G	DPAK (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# NVDS015N15MC

## THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Notes 1, 2)	47.9	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	150			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , ref to $25^\circ\text{C}$		83		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 120\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		1.1	
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 162\ \mu\text{A}$	2.5		4.5	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient	$I_D = 162\ \mu\text{A}$ , ref to $25^\circ\text{C}$		-8.2		mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 29\text{ A}$		11.8	15	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 29\text{ A}$		58		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2120		pF
$C_{OSS}$	Output Capacitance			595		
$C_{RSS}$	Reverse Transfer Capacitance			10.5		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}; I_D = 29\text{ A}$		27		nC
$Q_{G(TH)}$	Threshold Gate Charge			7		
$Q_{GS}$	Gate-to-Source Charge			11		
$Q_{GD}$	Gate-to-Drain Charge			4		
$V_{GP}$	Plateau Voltage			5.5		

### SWITCHING CHARACTERISTICS (Note 3)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DD} = 75\text{ V}, I_D = 29\text{ A}, R_G = 6\ \Omega$		16		ns
$t_r$	Rise Time			5		
$t_{d(OFF)}$	Turn-Off Delay Time			21		
$t_f$	Fall Time			4		

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 29\text{ A}$	$T_J = 25^\circ\text{C}$		0.89	1.2	V
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 300\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			49		ns
$Q_{RR}$	Reverse Recovery Charge					197	
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 75\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 29\text{ A}$			34		ns
$Q_{RR}$	Reverse Recovery Charge					345	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures.

# NVDS015N15MC

## TYPICAL CHARACTERISTICS

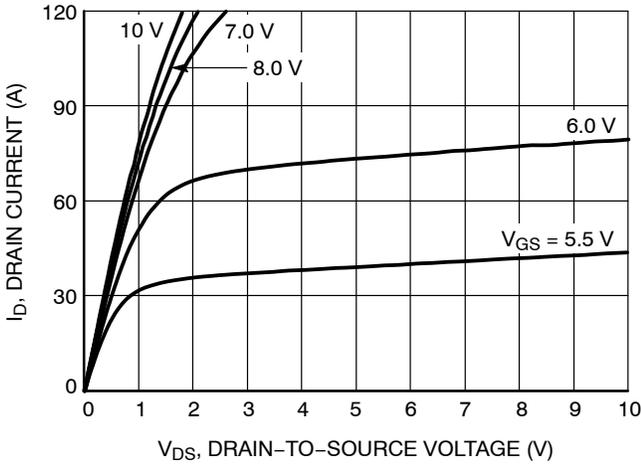


Figure 1. On-Region Characteristics

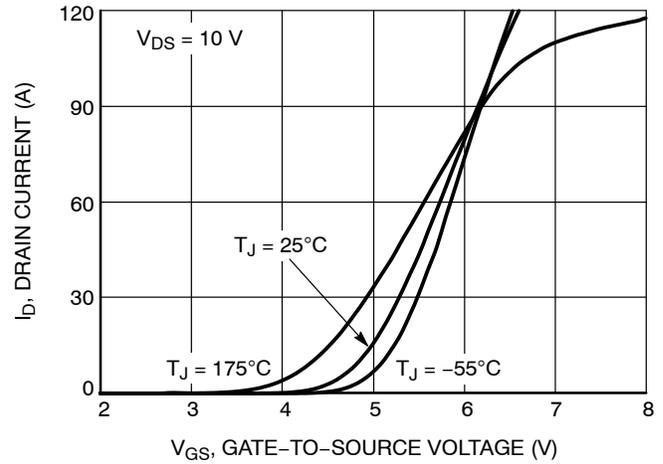


Figure 2. Transfer Characteristics

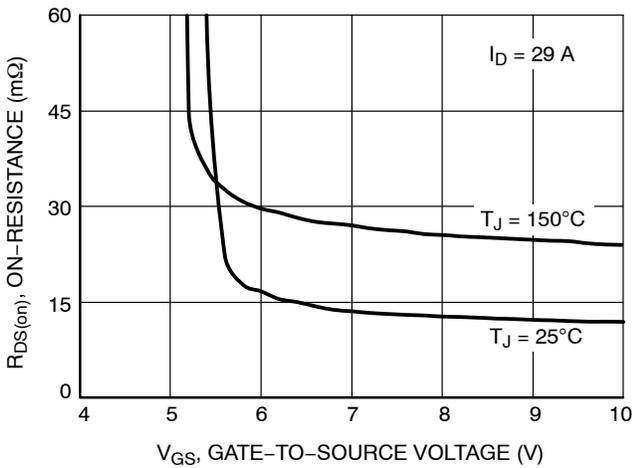


Figure 3. On-Resistance vs. Gate-to-Source Voltage

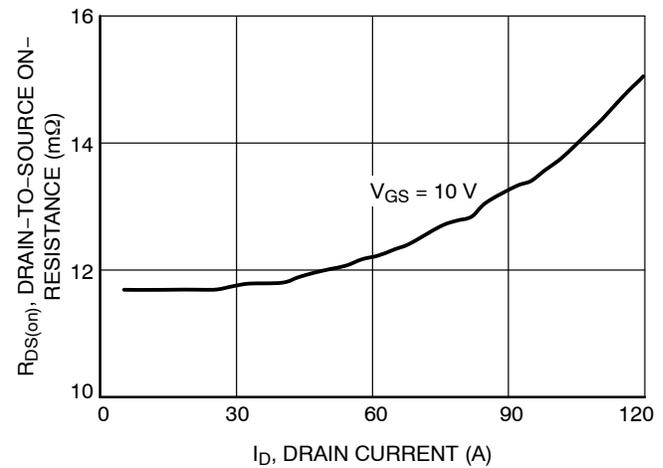


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

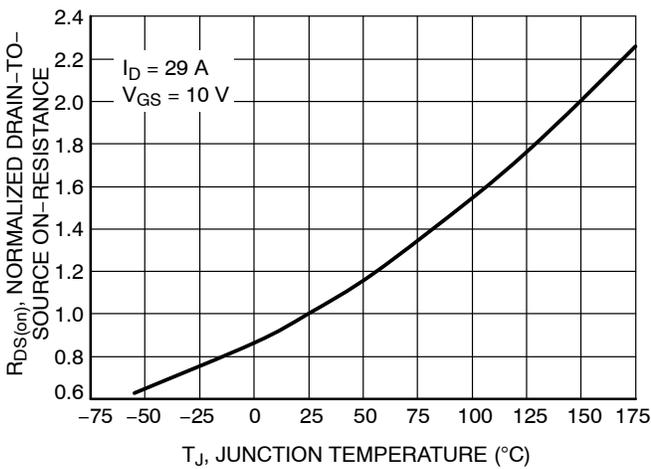


Figure 5. Normalized On-Resistance vs. Junction Temperature

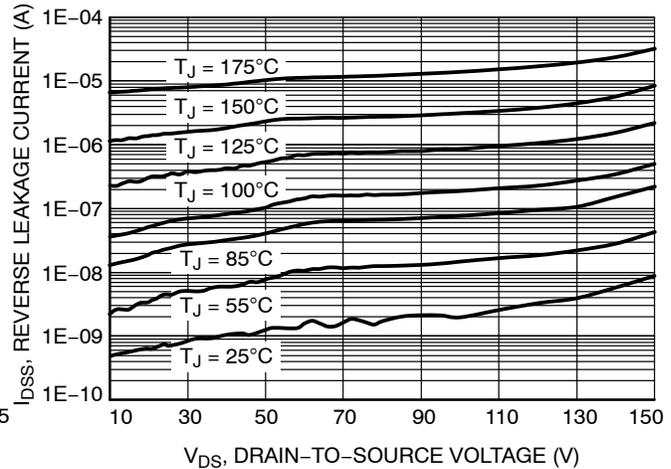
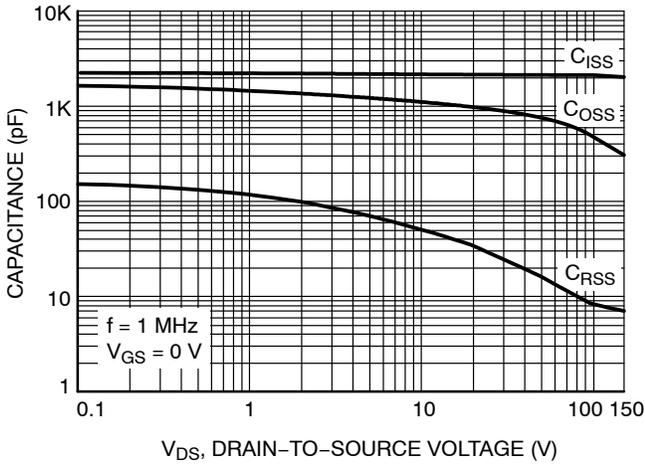


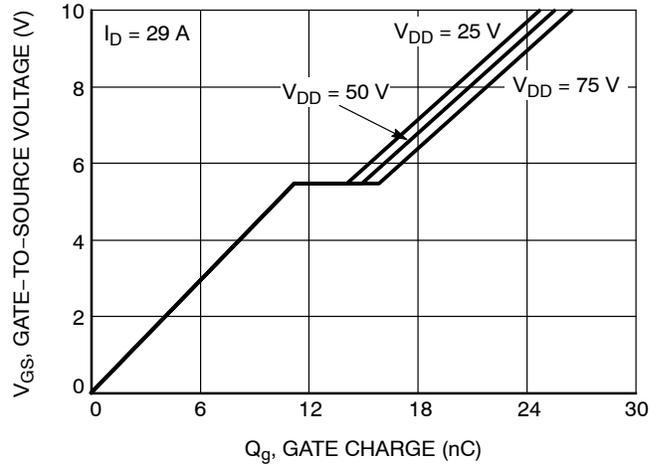
Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVDS015N15MC

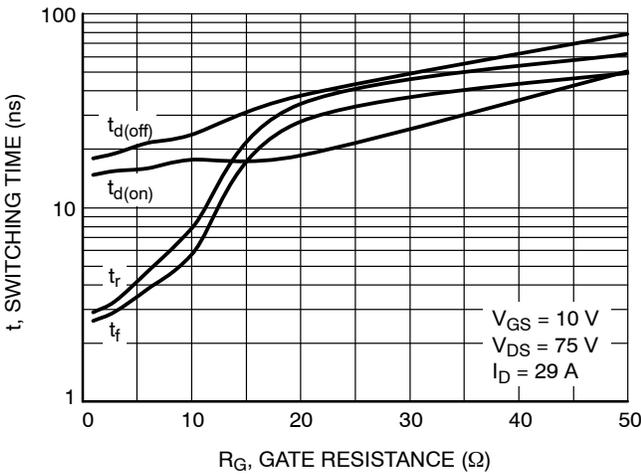
## TYPICAL CHARACTERISTICS (continue)



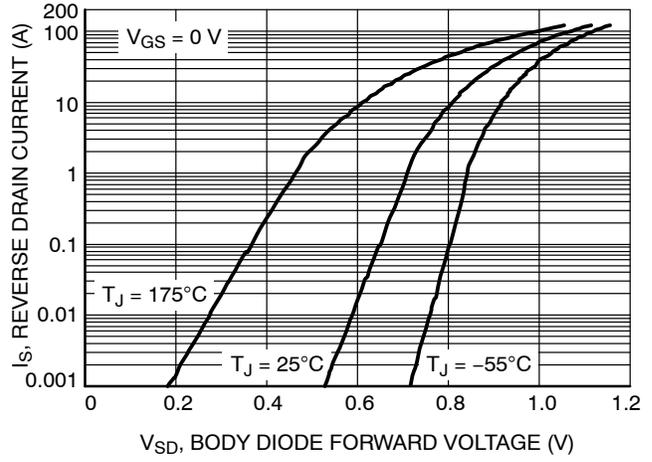
**Figure 7. Capacitance vs. Drain-to-Source Voltage**



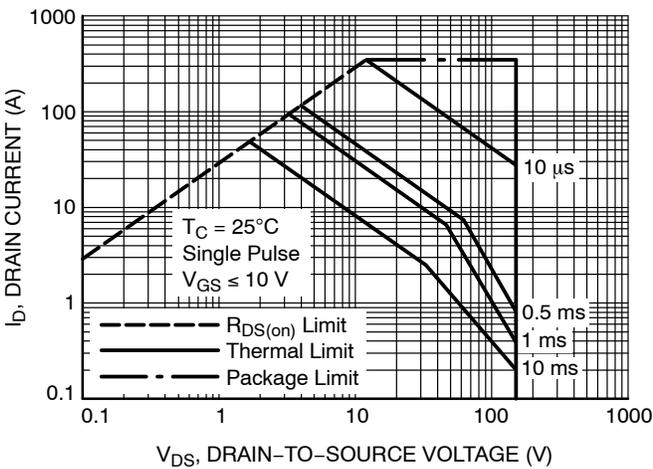
**Figure 8. Gate Charge Characteristics**



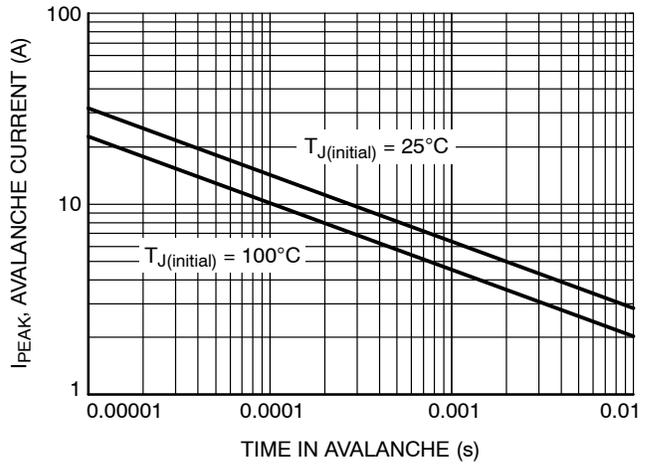
**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 10. Source-to-Drain Diode Forward Voltage vs. Source Current**



**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Unclamped Inductive Switching Capability**

# NVDS015N15MC

## TYPICAL CHARACTERISTICS (continue)

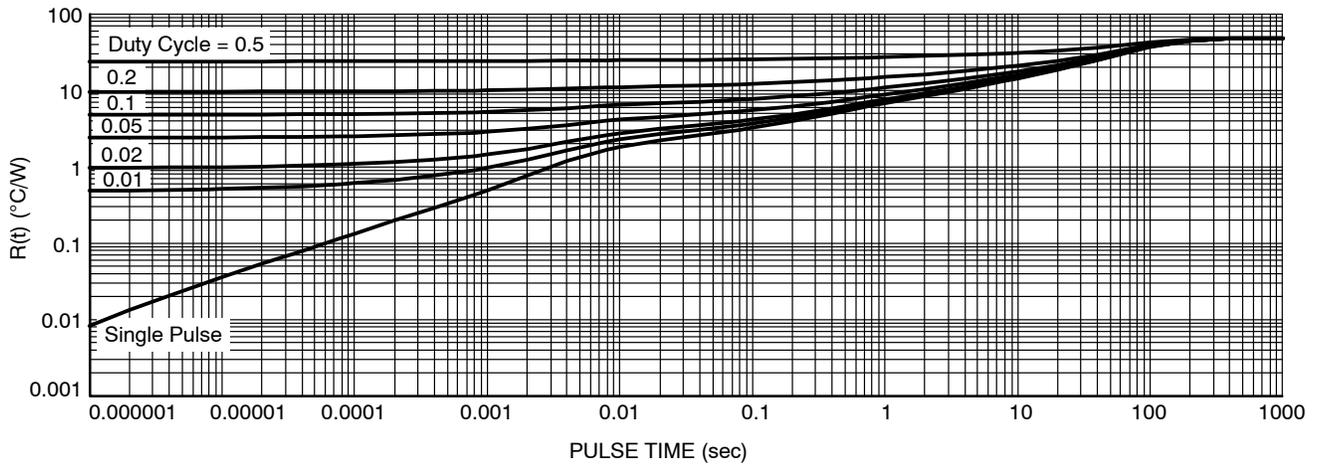
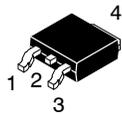


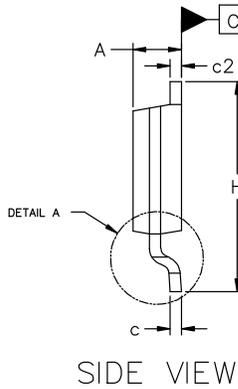
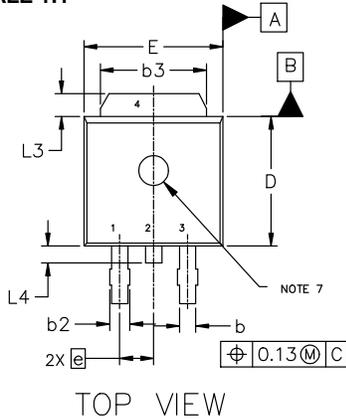
Figure 13. Transient Thermal Impedance



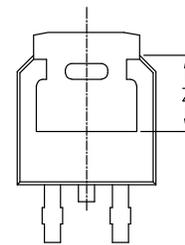
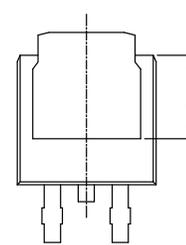
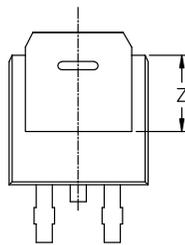
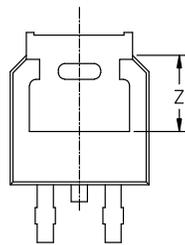
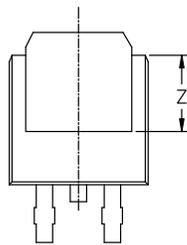
DPAK3 6.10x6.54x2.28, 2.29P  
CASE 369C  
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



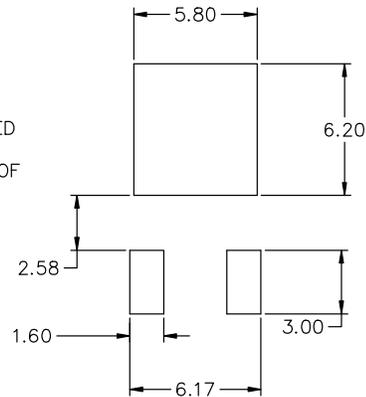
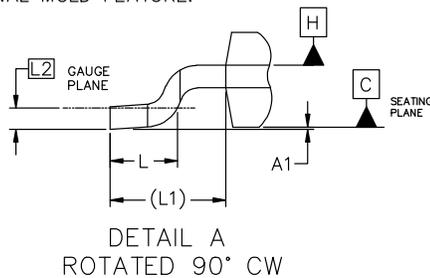
MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

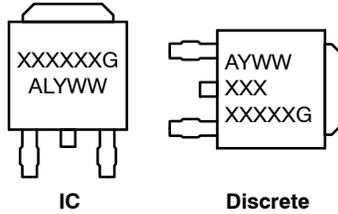
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**DPAK3 6.10x6.54x2.28, 2.29P**  
**CASE 369C**  
**ISSUE J**

DATE 12 AUG 2025

**GENERIC  
MARKING DIAGRAM\***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/> PIN 1. BASE<br/> 2. COLLECTOR<br/> 3. EMITTER<br/> 4. COLLECTOR</p> | <p>STYLE 2:<br/> PIN 1. GATE<br/> 2. DRAIN<br/> 3. SOURCE<br/> 4. DRAIN</p>          | <p>STYLE 3:<br/> PIN 1. ANODE<br/> 2. CATHODE<br/> 3. ANODE<br/> 4. CATHODE</p> | <p>STYLE 4:<br/> PIN 1. CATHODE<br/> 2. ANODE<br/> 3. GATE<br/> 4. ANODE</p>              | <p>STYLE 5:<br/> PIN 1. GATE<br/> 2. ANODE<br/> 3. CATHODE<br/> 4. ANODE</p>     |
| <p>STYLE 6:<br/> PIN 1. MT1<br/> 2. MT2<br/> 3. GATE<br/> 4. MT2</p>                 | <p>STYLE 7:<br/> PIN 1. GATE<br/> 2. COLLECTOR<br/> 3. EMITTER<br/> 4. COLLECTOR</p> | <p>STYLE 8:<br/> PIN 1. N/C<br/> 2. CATHODE<br/> 3. ANODE<br/> 4. CATHODE</p>   | <p>STYLE 9:<br/> PIN 1. ANODE<br/> 2. CATHODE<br/> 3. RESISTOR ADJUST<br/> 4. CATHODE</p> | <p>STYLE 10:<br/> PIN 1. CATHODE<br/> 2. ANODE<br/> 3. CATHODE<br/> 4. ANODE</p> |

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