

MOSFET – Power, Single, P-Channel

-60 V, -61 A, 16 mΩ

NVD5117PL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			-60	V
V_{GS}	Gate-to-Source Voltage			± 20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	-61	A
			$T_C = 100^\circ\text{C}$	-43	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	118	W
			$T_C = 100^\circ\text{C}$	59	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	-11	A
			$T_A = 100^\circ\text{C}$	-8	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	4.1	W
			$T_A = 100^\circ\text{C}$	2.1	
I_{DM}	Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$		-419	A
I_{Dmaxpk}	Current Limited by Package (Note 3)	$T_A = 25^\circ\text{C}$		60	A
T_J , T_{stg}	Operating Junction and Storage Temperature			-55 to 175	$^\circ\text{C}$
I_S	Source Current (Body Diode)			-118	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_{L(pk)} = 40 \text{ A}$, $L = 0.3 \text{ mH}$, $R_G = 25 \Omega$)			240	mJ
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	$^\circ\text{C}$

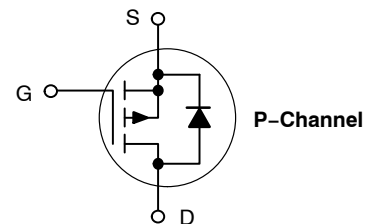
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

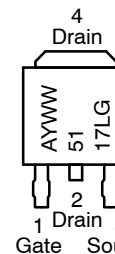
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Drain)	1.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	37	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
-60 V	16 mΩ @ -10 V	-61 A
	22 mΩ @ -4.5 V	



MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5117L = Device Code
G = Pb-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NVD5117PL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = -250 μA	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = -60 V	T _J = 25°C T _J = 125°C		-1.0 -100	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 4)

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-1.5		-2.5	V
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = -10 V, I _D = -29 A V _{GS} = -4.5 V, I _D = -29 A		12 16	16 22	mΩ
g _{FS}	Froward Transconductance	V _{DS} = -15 V, I _D = -15 A		30		S

CHARGES AND CAPACITANCES

C _{iss}	Input Capacitance	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -25 V		4800		pF
C _{oss}	Output Capacitance			480		
C _{rss}	Reverse Transfer Capacitance			320		
Q _{G(TOT)}	Total Gate Charge	V _{DS} = -48 V, I _D = -29 A	V _{GS} = -4.5 V V _{GS} = -10 V	49 85		nC
Q _{G(TH)}	Threshold Gate Charge	V _{GS} = -4.5 V, V _{DS} = -48 V, I _D = -29 A		3		
Q _{GS}	Gate-to-Source Charge			13		
Q _{GD}	Gate-to-Drain Charge			28		
V _{GP}	Plateau Voltage			3.2		V

SWITCHING CHARACTERISTICS (Notes 4)

t _{d(on)}	Turn-On Delay Time	V _{GS} = -4.5 V, V _{DS} = -48 V, I _D = -29 A, R _G = 2.5 Ω		22		ns
t _r	Rise Time			195		
t _{d(off)}	Turn-Off Delay Time			50		
t _f	Fall Time			132		

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = -29 A	T _J = 25°C T _J = 125°C	-0.86 -0.74	-1.0	V
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -29 A		36		ns
t _a	Charge Time			19		
t _b	Discharge Time			17		
Q _{RR}	Reverse Recovery Charge			44		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

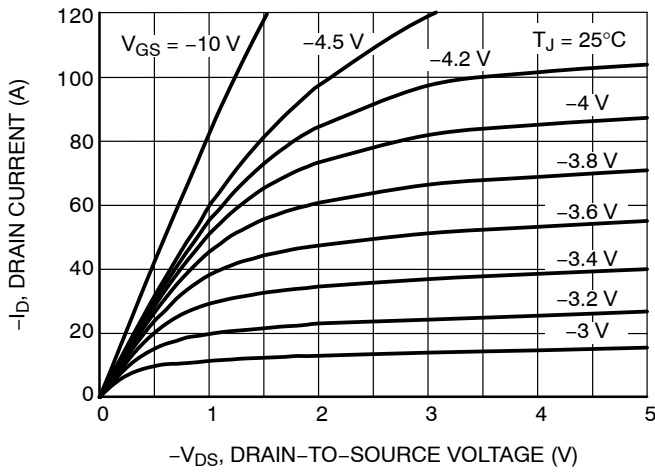


Figure 1. On-Region Characteristics

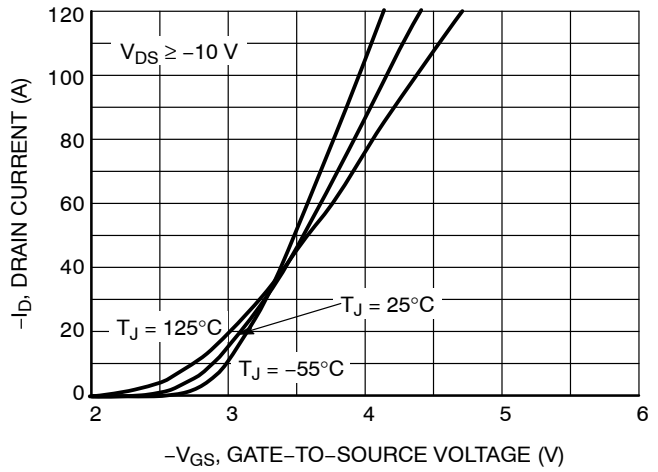


Figure 2. Transfer Characteristics

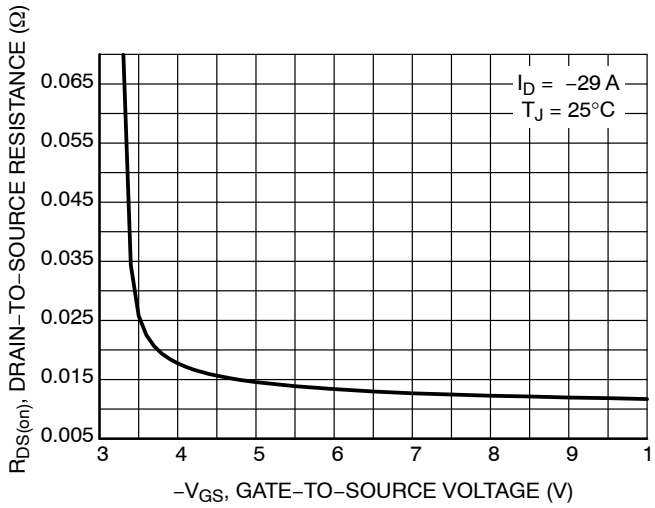


Figure 3. On-Resistance vs. Gate-to-Source Voltage

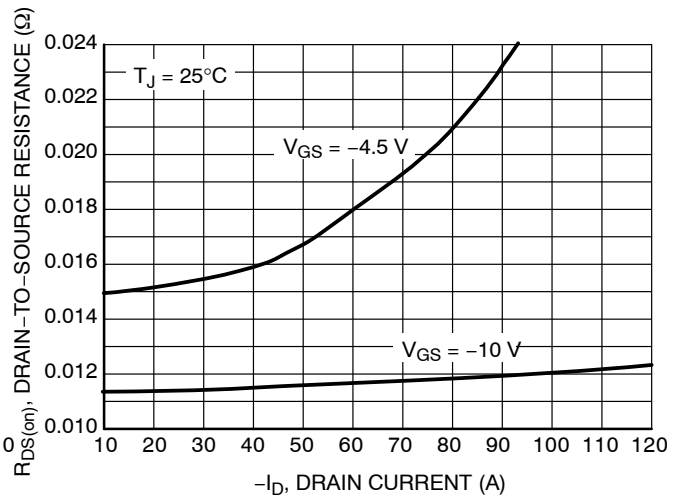


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

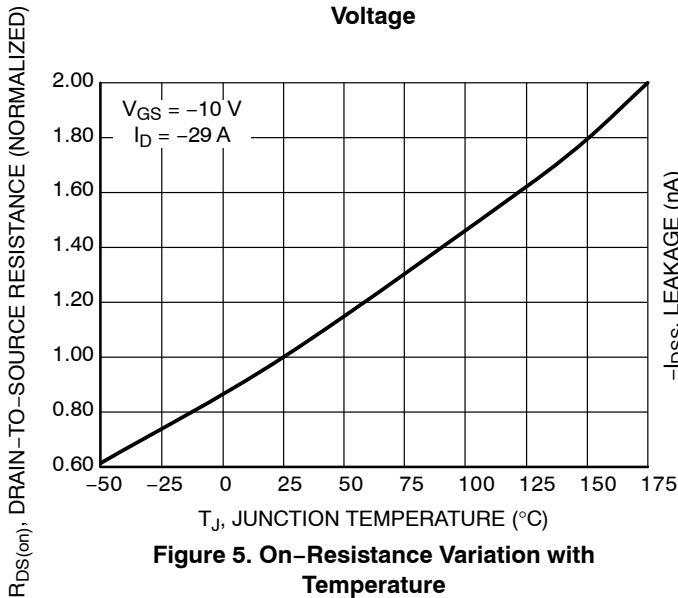


Figure 5. On-Resistance Variation with Temperature

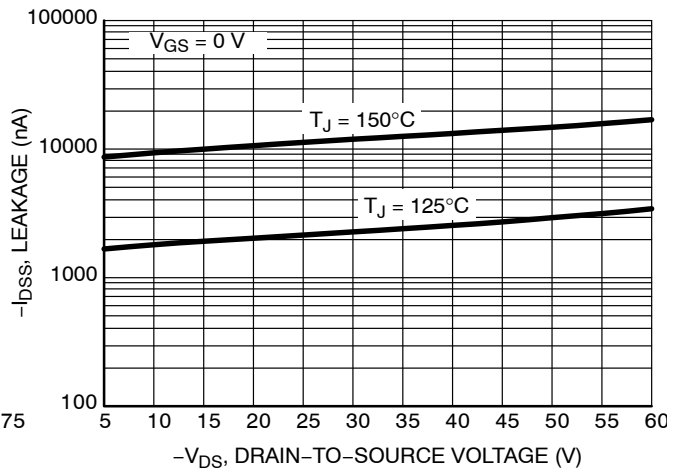


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

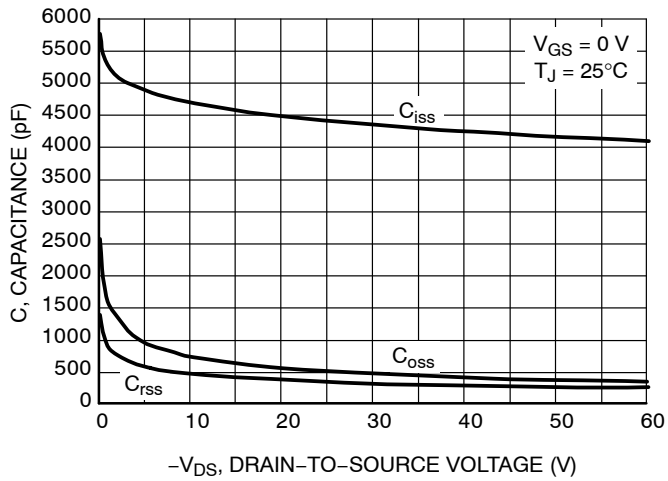


Figure 7. Capacitance Variation

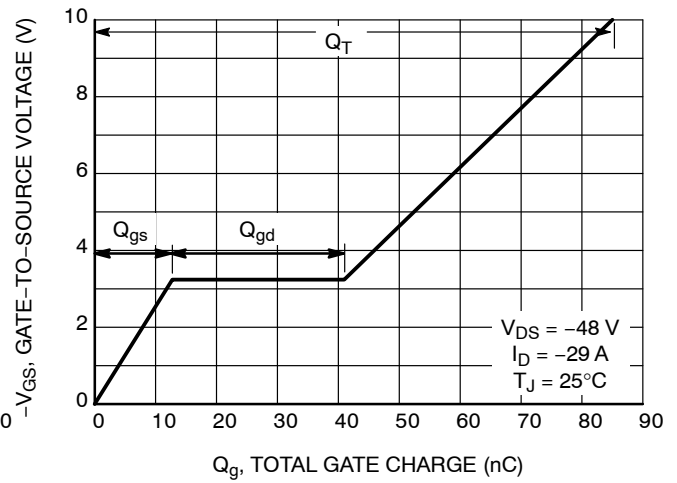


Figure 8. Gate-to-Source vs. Total Charge

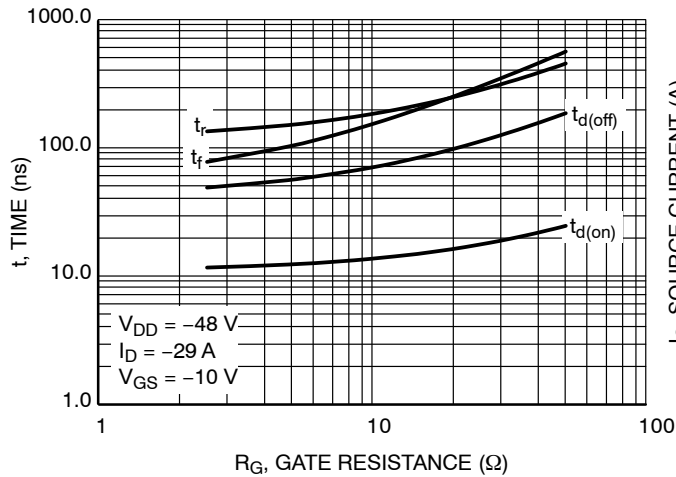


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

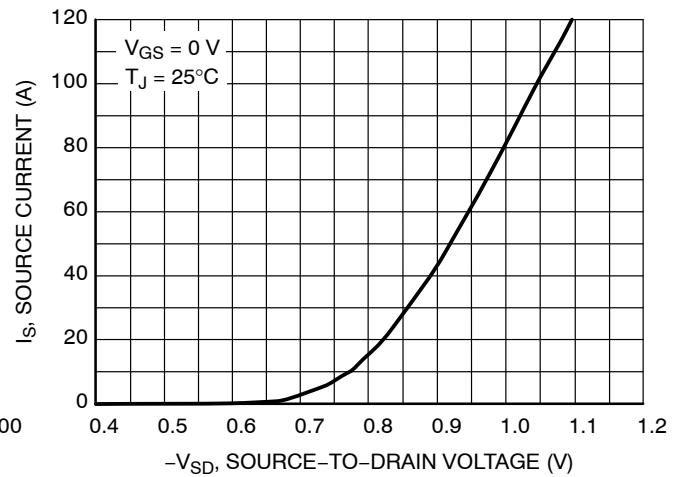


Figure 10. Diode Forward Voltage vs. Current

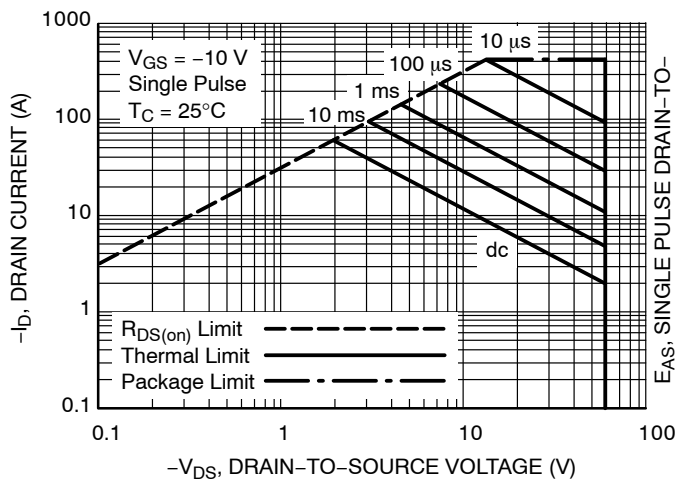


Figure 11. Maximum Rated Forward Biased Safe Operating Area

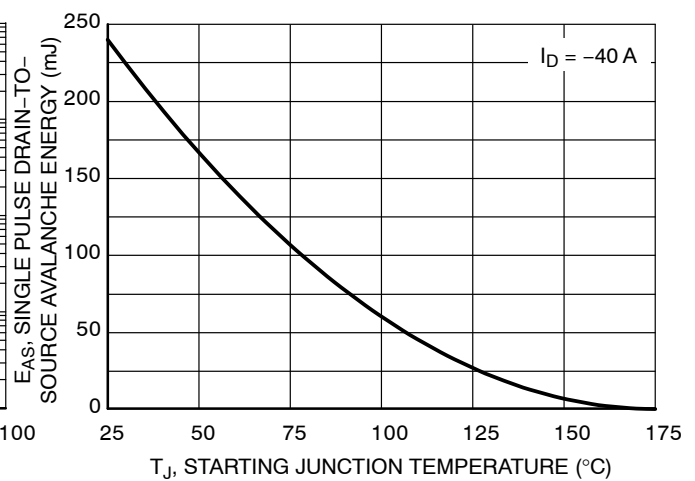


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NVD5117PL

TYPICAL CHARACTERISTICS (continued)

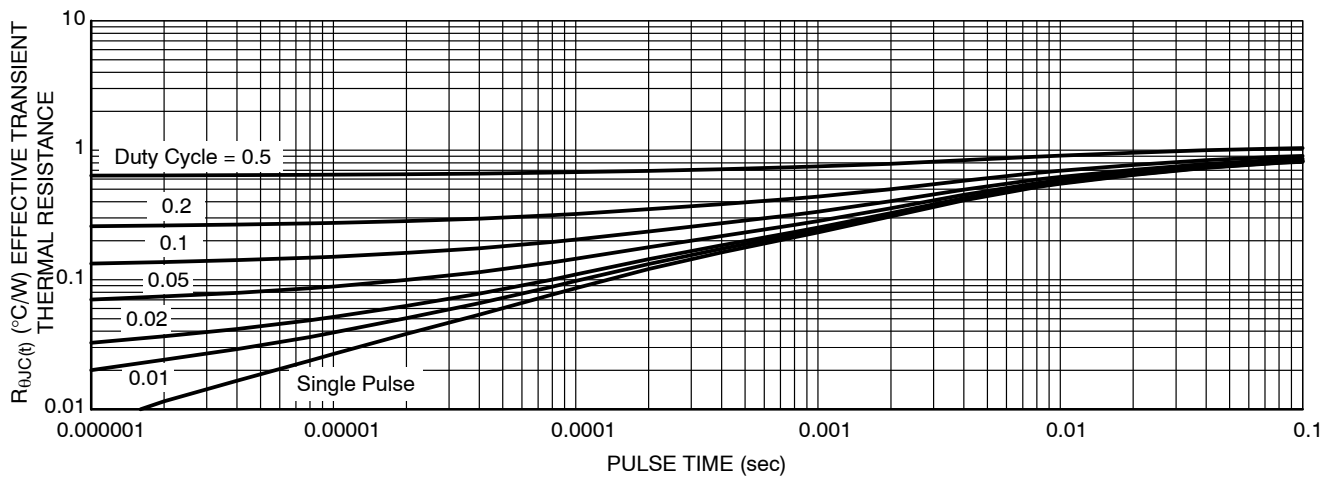


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

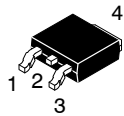
Device	Package	Shipping [†]
NVD5117PLT4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

DISCONTINUED (Note 5)

NVD5117PLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
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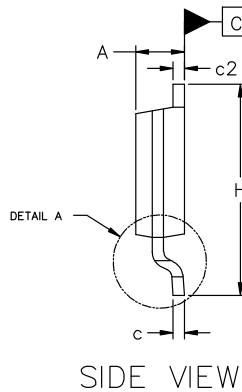
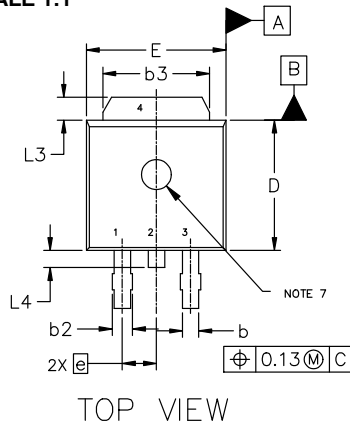
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

5. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

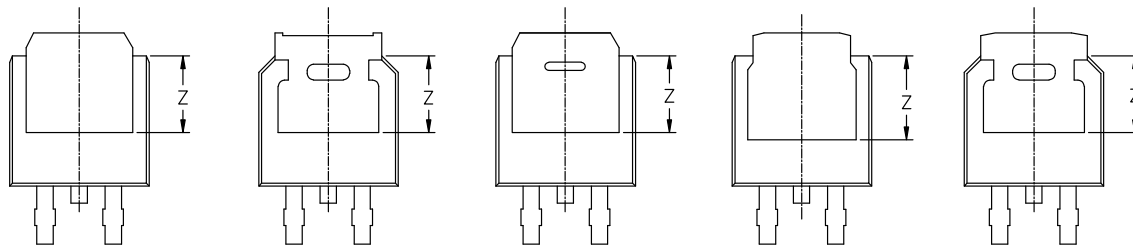

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1

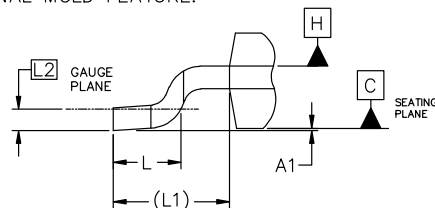


MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

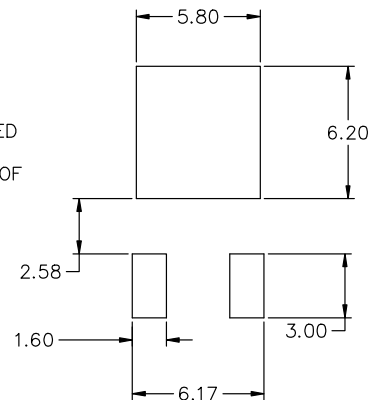


NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

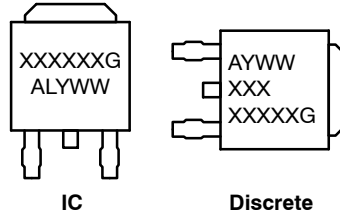
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DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

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