

# NTMD6N02R2

## MOSFET – Power, Dual, N-Channel Enhancement Mode, SO-8

6.0 A, 20 V

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SOIC-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SOIC-8 Mounting Information Provided
- Pb-Free Package is Available

### Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery-Powered Products, for example, Computers, Printers, Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating                                                  | Symbol          | Value    | Unit               |
|---------------------------------------------------------|-----------------|----------|--------------------|
| Drain-to-Source Voltage                                 | $V_{DSS}$       | 20       | V                  |
| Drain-to-Gate Voltage ( $R_{GS} = 1.0\text{ M}\Omega$ ) | $V_{DGR}$       | 20       | V                  |
| Gate-to-Source Voltage – Continuous                     | $V_{GS}$        | $\pm 12$ | V                  |
| Thermal Resistance,<br>Junction-to-Ambient (Note 1)     | $R_{\theta JA}$ | 62.5     | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$      | $P_D$           | 2.0      | W                  |
| Continuous Drain Current @ $T_A = 25^\circ\text{C}$     | $I_D$           | 6.5      | A                  |
| Continuous Drain Current @ $T_A = 70^\circ\text{C}$     | $I_D$           | 5.5      | A                  |
| Pulsed Drain Current (Note 4)                           | $I_{DM}$        | 50       | A                  |
| Thermal Resistance,<br>Junction-to-Ambient (Note 2)     | $R_{\theta JA}$ | 102      | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$      | $P_D$           | 1.22     | W                  |
| Continuous Drain Current @ $T_A = 25^\circ\text{C}$     | $I_D$           | 5.07     | A                  |
| Continuous Drain Current @ $T_A = 70^\circ\text{C}$     | $I_D$           | 4.07     | A                  |
| Pulsed Drain Current (Note 4)                           | $I_{DM}$        | 40       | A                  |
| Thermal Resistance<br>Junction-to-Ambient (Note 3)      | $R_{\theta JA}$ | 172      | $^\circ\text{C/W}$ |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$      | $P_D$           | 0.73     | W                  |
| Continuous Drain Current @ $T_A = 25^\circ\text{C}$     | $I_D$           | 3.92     | A                  |
| Continuous Drain Current @ $T_A = 70^\circ\text{C}$     | $I_D$           | 3.14     | A                  |
| Pulsed Drain Current (Note 4)                           | $I_{DM}$        | 30       | A                  |

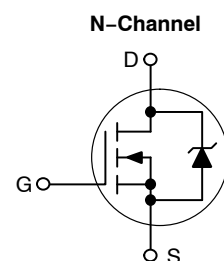
1. Mounted onto a 2 in square FR-4 Board (1 in sq. 2 oz. Cu 0.06 in thick single sided),  $t < 10$  seconds.
2. Mounted onto a 2 in square FR-4 Board (1 in sq. 2 oz. Cu 0.06 in thick single sided),  $t = \text{steady state}$ .
3. Minimum FR-4 or G-10 PCB,  $t = \text{steady state}$ .
4. Pulse Test: Pulse Width = 10  $\mu\text{s}$ , Duty Cycle = 2%.



ON Semiconductor®

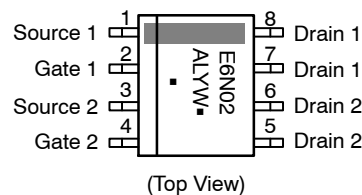
<http://onsemi.com>

| $V_{DSS}$ | $R_{DS(on)}$ TYP                        | $I_D$ MAX |
|-----------|-----------------------------------------|-----------|
| 20 V      | 35 m $\Omega$ @ $V_{GS} = 4.5\text{ V}$ | 6.0 A     |



SOIC-8  
CASE 751  
STYLE 11

### MARKING DIAGRAM & PIN ASSIGNMENT



E6N02 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
■ = Pb-Free Package  
(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device      | Package          | Shipping†        |
|-------------|------------------|------------------|
| NTMD6N02R2  | SOIC-8           | 2500/Tape & Reel |
| NTMD6N02R2G | SOIC-8 (Pb-Free) | 2500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMD6N02R2

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted) (continued)

| Rating                                                                                                                                                                                                   | Symbol                            | Value       | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|-------------|------|
| Operating and Storage Temperature Range                                                                                                                                                                  | T <sub>J</sub> , T <sub>stg</sub> | –55 to +150 | °C   |
| Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C<br>(V <sub>DD</sub> = 20 Vdc, V <sub>GS</sub> = 5.0 Vdc, Peak I <sub>L</sub> = 6.0 Apk, L = 20 mH, R <sub>G</sub> = 25 Ω) | E <sub>AS</sub>                   | 360         | mJ   |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds                                                                                                                                           | T <sub>L</sub>                    | 260         | °C   |

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted) (Note 5)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                                                                                                                                                                              |                      |         |           |           |              |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|---------|-----------|-----------|--------------|
| Drain-to-Source Breakdown Voltage<br>(V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc)<br>Temperature Coefficient (Positive)                                                              | V <sub>(BR)DSS</sub> | 20<br>– | –<br>19.2 | –<br>–    | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>(V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C)<br>(V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C) | I <sub>DSS</sub>     | –<br>–  | –<br>–    | 1.0<br>10 | μAdc         |
| Gate-Body Leakage Current (V <sub>GS</sub> = +12 Vdc, V <sub>DS</sub> = 0 Vdc)                                                                                                               | I <sub>GSS</sub>     | –       | –         | 100       | nAdc         |
| Gate-Body Leakage Current (V <sub>GS</sub> = –12 Vdc, V <sub>DS</sub> = 0 Vdc)                                                                                                               | I <sub>GSS</sub>     | –       | –         | –100      | nAdc         |

### ON CHARACTERISTICS

|                                                                                                                                                                                                                                                                                |                     |                  |                                  |                                  |              |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------------------|----------------------------------|----------------------------------|--------------|
| Gate Threshold Voltage<br>(V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = –250 μAdc)<br>Temperature Coefficient (Negative)                                                                                                                                               | V <sub>GS(th)</sub> | 0.6<br>–         | 0.9<br>–3.0                      | 1.2<br>–                         | Vdc<br>mV/°C |
| Static Drain-to-Source On-State Resistance<br>(V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 6.0 Adc)<br>(V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 4.0 Adc)<br>(V <sub>GS</sub> = 2.7 Vdc, I <sub>D</sub> = 2.0 Adc)<br>(V <sub>GS</sub> = 2.5 Vdc, I <sub>D</sub> = 3.0 Adc) | R <sub>DS(on)</sub> | –<br>–<br>–<br>– | 0.028<br>0.028<br>0.033<br>0.035 | 0.035<br>0.043<br>0.048<br>0.049 | Ω            |
| Forward Transconductance (V <sub>DS</sub> = 12 Vdc, I <sub>D</sub> = 3.0 Adc)                                                                                                                                                                                                  | g <sub>FS</sub>     | –                | 10                               | –                                | Mhos         |

### DYNAMIC CHARACTERISTICS

|                              |                                                                     |                  |   |     |      |    |
|------------------------------|---------------------------------------------------------------------|------------------|---|-----|------|----|
| Input Capacitance            | (V <sub>DS</sub> = 16 Vdc, V <sub>GS</sub> = 0 Vdc,<br>f = 1.0 MHz) | C <sub>iss</sub> | – | 785 | 1100 | pF |
| Output Capacitance           |                                                                     | C <sub>oss</sub> | – | 260 | 450  |    |
| Reverse Transfer Capacitance |                                                                     | C <sub>rss</sub> | – | 75  | 180  |    |

### SWITCHING CHARACTERISTICS (Notes 6 and 7)

|                     |                                                                                                               |                     |   |     |     |    |
|---------------------|---------------------------------------------------------------------------------------------------------------|---------------------|---|-----|-----|----|
| Turn-On Delay Time  | (V <sub>DD</sub> = 16 Vdc, I <sub>D</sub> = 6.0 Adc,<br>V <sub>GS</sub> = 4.5 Vdc,<br>R <sub>G</sub> = 6.0 Ω) | t <sub>d(on)</sub>  | – | 12  | 20  | ns |
| Rise Time           |                                                                                                               | t <sub>r</sub>      | – | 50  | 90  |    |
| Turn-Off Delay Time |                                                                                                               | t <sub>d(off)</sub> | – | 45  | 75  |    |
| Fall Time           |                                                                                                               | t <sub>f</sub>      | – | 80  | 130 |    |
| Turn-On Delay Time  | (V <sub>DD</sub> = 16 Vdc, I <sub>D</sub> = 4.0 Adc,<br>V <sub>GS</sub> = 4.5 Vdc,<br>R <sub>G</sub> = 6.0 Ω) | t <sub>d(on)</sub>  | – | 11  | 18  | ns |
| Rise Time           |                                                                                                               | t <sub>r</sub>      | – | 35  | 65  |    |
| Turn-Off Delay Time |                                                                                                               | t <sub>d(off)</sub> | – | 45  | 75  |    |
| Fall Time           |                                                                                                               | t <sub>f</sub>      | – | 60  | 110 |    |
| Total Gate Charge   | (V <sub>DS</sub> = 16 Vdc,<br>V <sub>GS</sub> = 4.5 Vdc,<br>I <sub>D</sub> = 6.0 Adc)                         | Q <sub>tot</sub>    | – | 12  | 20  | nC |
| Gate-Source Charge  |                                                                                                               | Q <sub>gs</sub>     | – | 1.5 | –   |    |
| Gate-Drain Charge   |                                                                                                               | Q <sub>gd</sub>     | – | 4.0 | –   |    |

5. Handling precautions to protect against electrostatic discharge is mandatory

6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

# NTMD6N02R2

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (continued) (Note 8)

| Characteristic                           |                                                                                                                                                                                                        | Symbol   | Min | Typ                  | Max             | Unit          |
|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|----------------------|-----------------|---------------|
| <b>BODY-DRAIN DIODE RATINGS</b> (Note 9) |                                                                                                                                                                                                        |          |     |                      |                 |               |
| Diode Forward On-Voltage                 | ( $I_S = 4.0 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ )<br>( $I_S = 6.0 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ )<br>( $I_S = 6.0 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ , $T_J = 125^\circ\text{C}$ ) | $V_{SD}$ | –   | 0.83<br>0.88<br>0.75 | 1.1<br>1.2<br>– | Vdc           |
| Reverse Recovery Time                    | ( $I_S = 6.0 \text{ Adc}$ , $V_{GS} = 0 \text{ Vdc}$ ,<br>$dI_S/dt = 100 \text{ A}/\mu\text{s}$ )                                                                                                      | $t_{rr}$ | –   | 30                   | –               | ns            |
|                                          |                                                                                                                                                                                                        | $t_a$    | –   | 15                   | –               |               |
|                                          |                                                                                                                                                                                                        | $t_b$    | –   | 15                   | –               |               |
| Reverse Recovery Stored Charge           |                                                                                                                                                                                                        | $Q_{RR}$ | –   | 0.02                 | –               | $\mu\text{C}$ |

8. Handling precautions to protect against electrostatic discharge is mandatory.

9. Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  max, Duty Cycle = 2%.

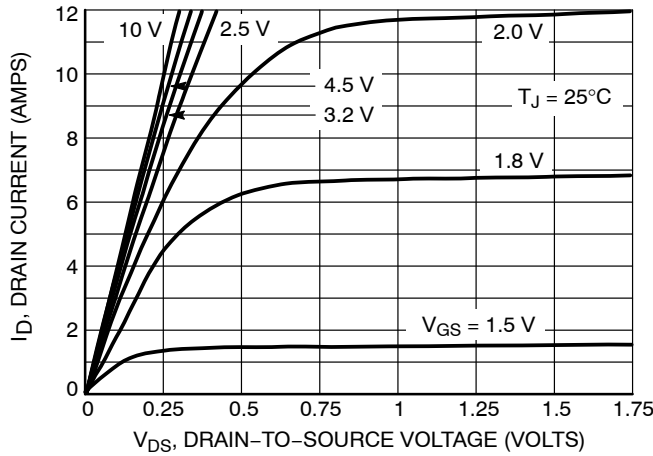


Figure 1. On-Region Characteristics

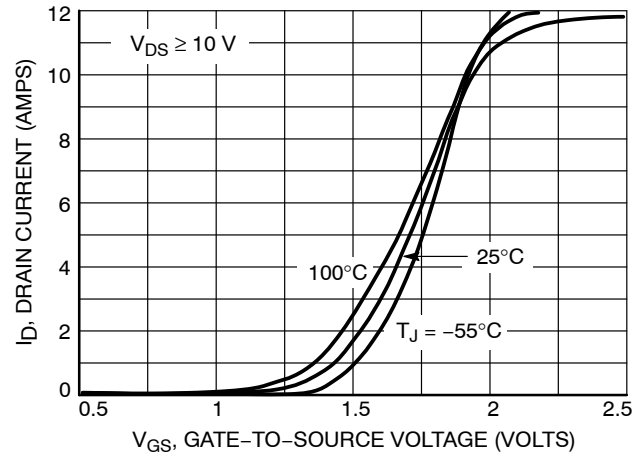


Figure 2. Transfer Characteristics

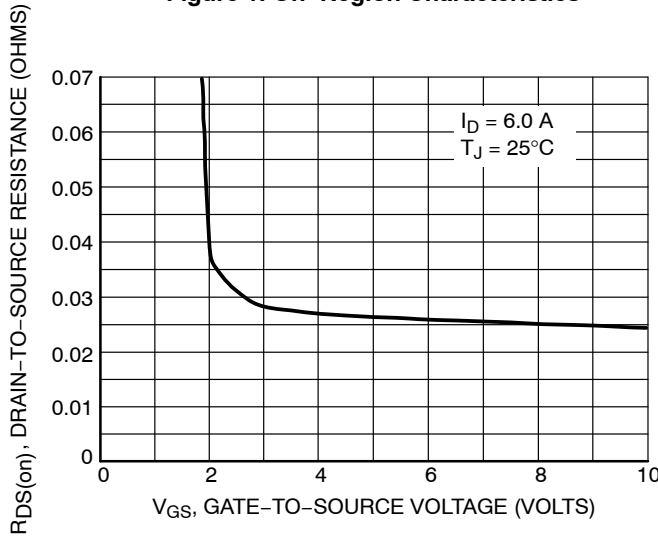


Figure 3. On-Resistance versus Gate-To-Source Voltage

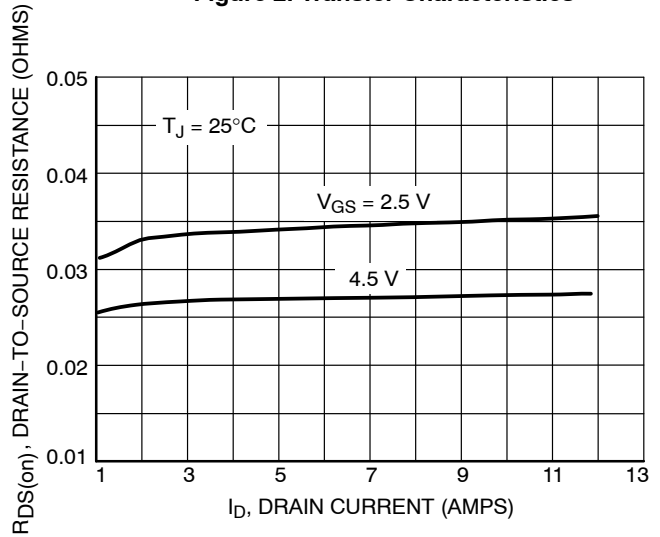
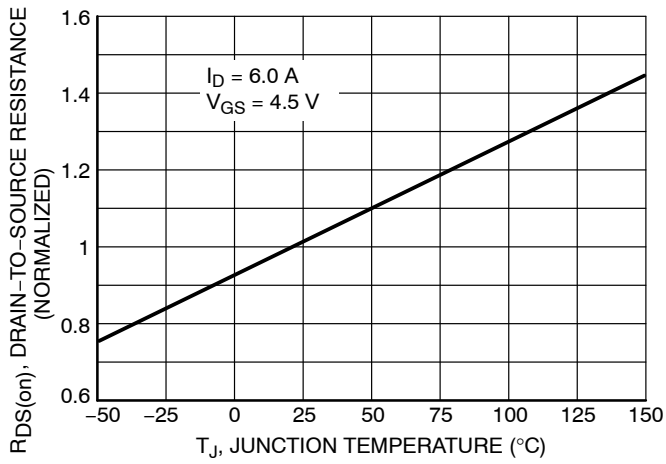
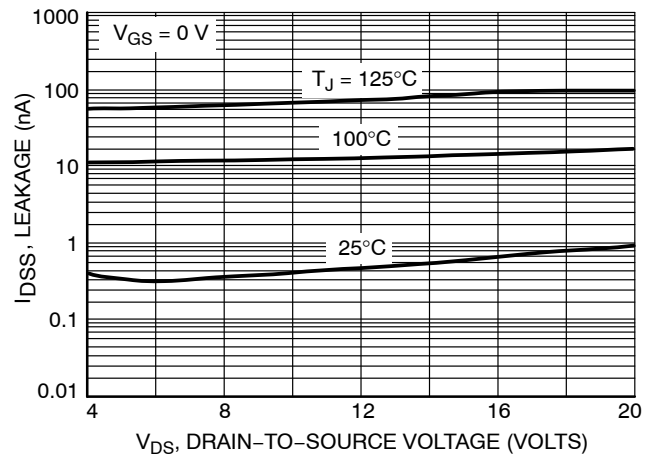


Figure 4. On-Resistance versus Drain Current and Gate Voltage

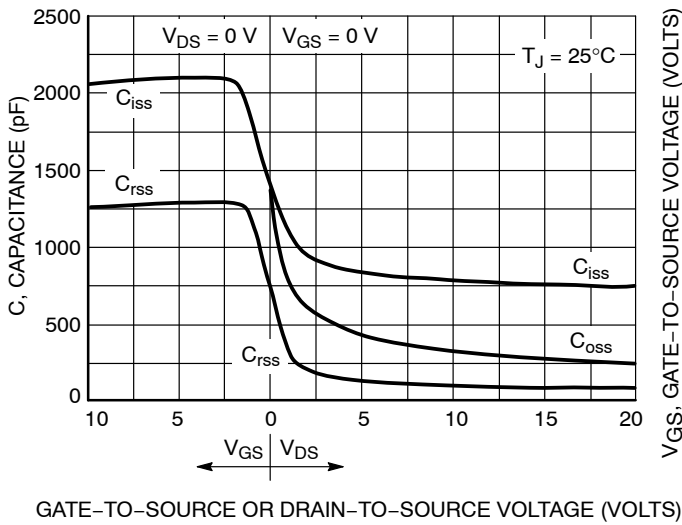
# NTMD6N02R2



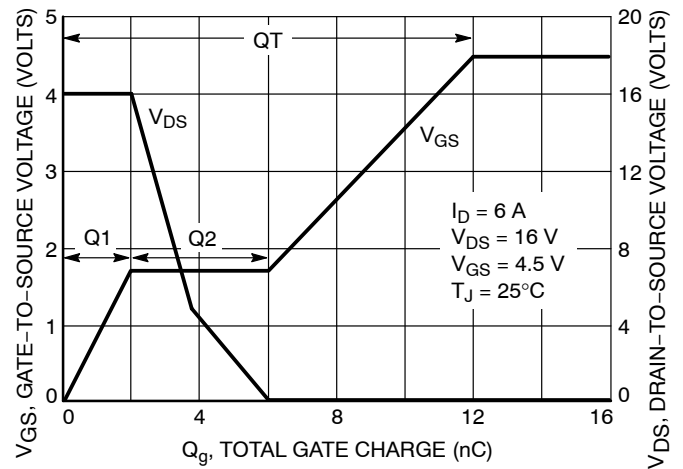
**Figure 5. On-Resistance Variation with Temperature**



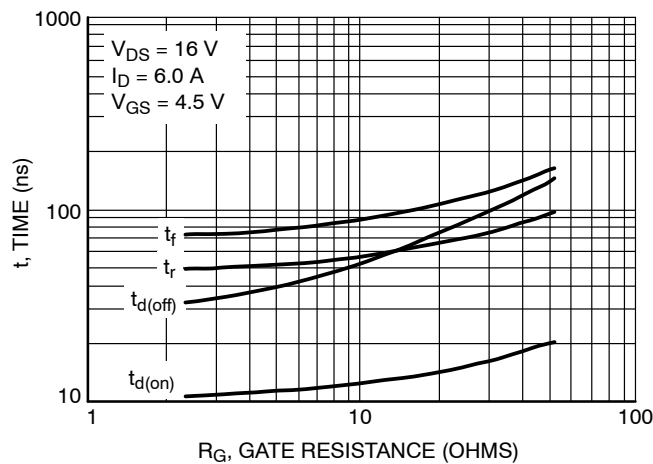
**Figure 6. Drain-To-Source Leakage Current versus Voltage**



**Figure 7. Capacitance Variation**



**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

# DRAIN-TO-SOURCE DIODE CHARACTERISTICS

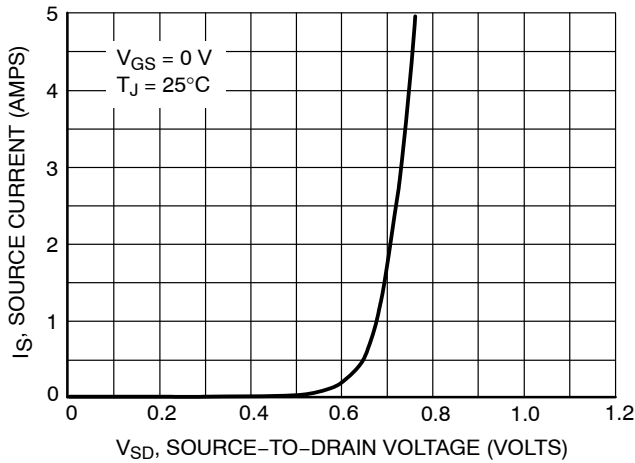


Figure 10. Diode Forward Voltage versus Current

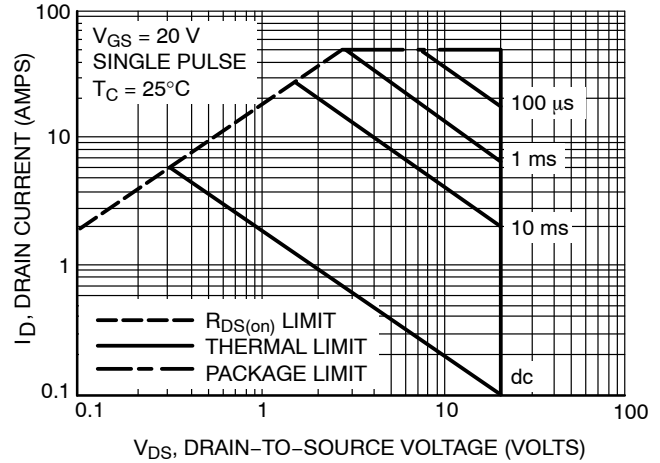


Figure 11. Maximum Rated Forward Biased Safe Operating Area

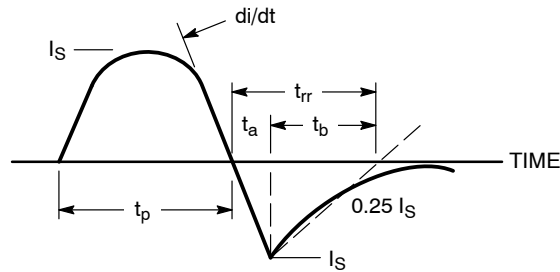


Figure 12. Diode Reverse Recovery Waveform

## TYPICAL ELECTRICAL CHARACTERISTICS

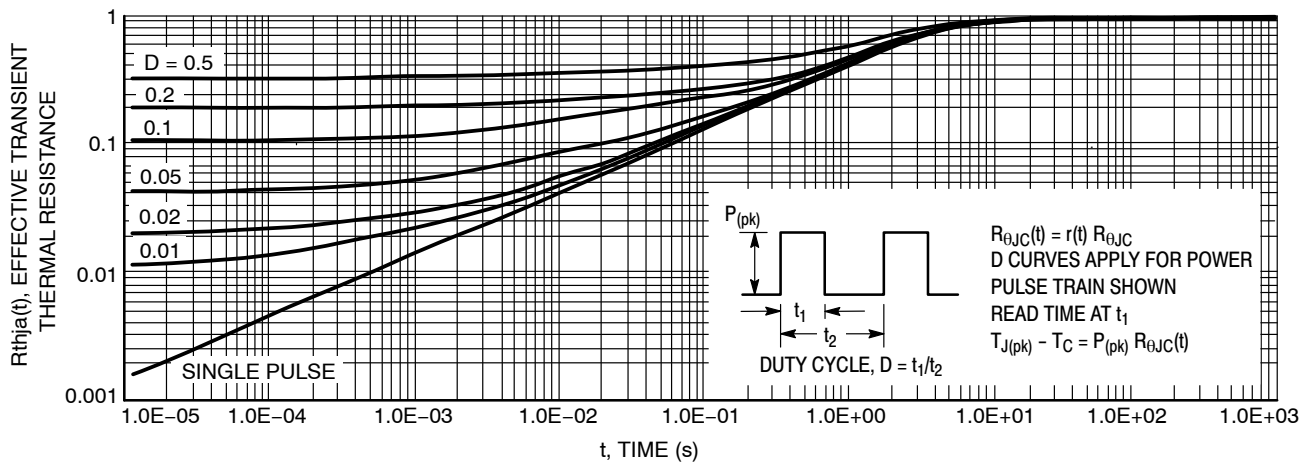


Figure 13. Thermal Response



SCALE 1:1

SOIC-8 NB  
CASE 751-07  
ISSUE AK

DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

GENERIC  
MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | SOIC-8 NB   | PAGE 1 OF 2                                                                                                                                                                         |

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**SOIC-8 NB**  
**CASE 751-07**  
**ISSUE AK**

DATE 16 FEB 2011

|                                                                                                                                                                                                   |                                                                                                                                                                                          |                                                                                                                                                                                    |                                                                                                                                                                                                        |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. COLLECTOR<br>4. EMITTER<br>5. EMITTER<br>6. BASE<br>7. BASE<br>8. EMITTER                                                                 | <b>STYLE 2:</b><br>PIN 1. COLLECTOR, DIE, #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. BASE, #2<br>6. EMITTER, #2<br>7. BASE, #1<br>8. EMITTER, #1               | <b>STYLE 3:</b><br>PIN 1. DRAIN, DIE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. GATE, #2<br>6. SOURCE, #2<br>7. GATE, #1<br>8. SOURCE, #1                            | <b>STYLE 4:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE<br>4. ANODE<br>5. ANODE<br>6. ANODE<br>7. ANODE<br>8. COMMON CATHODE                                                                           |
| <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. DRAIN<br>3. DRAIN<br>4. DRAIN<br>5. GATE<br>6. GATE<br>7. SOURCE<br>8. SOURCE                                                                               | <b>STYLE 6:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. DRAIN<br>4. SOURCE<br>5. SOURCE<br>6. GATE<br>7. GATE<br>8. SOURCE                                                                    | <b>STYLE 7:</b><br>PIN 1. INPUT<br>2. EXTERNAL BYPASS<br>3. THIRD STAGE SOURCE<br>4. GROUND<br>5. DRAIN<br>6. GATE 3<br>7. SECOND STAGE Vd<br>8. FIRST STAGE Vd                    | <b>STYLE 8:</b><br>PIN 1. COLLECTOR, DIE #1<br>2. BASE, #1<br>3. BASE, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #2<br>6. EMITTER, #2<br>7. EMITTER, #1<br>8. COLLECTOR, #1                              |
| <b>STYLE 9:</b><br>PIN 1. EMITTER, COMMON<br>2. COLLECTOR, DIE #1<br>3. COLLECTOR, DIE #2<br>4. EMITTER, COMMON<br>5. EMITTER, COMMON<br>6. BASE, DIE #2<br>7. BASE, DIE #1<br>8. EMITTER, COMMON | <b>STYLE 10:</b><br>PIN 1. GROUND<br>2. BIAS 1<br>3. OUTPUT<br>4. GROUND<br>5. GROUND<br>6. BIAS 2<br>7. INPUT<br>8. GROUND                                                              | <b>STYLE 11:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. DRAIN 2<br>7. DRAIN 1<br>8. DRAIN 1                                               | <b>STYLE 12:</b><br>PIN 1. SOURCE<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                                 |
| <b>STYLE 13:</b><br>PIN 1. N.C.<br>2. SOURCE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                              | <b>STYLE 14:</b><br>PIN 1. N-SOURCE<br>2. N-GATE<br>3. P-SOURCE<br>4. P-GATE<br>5. P-DRAIN<br>6. P-DRAIN<br>7. N-DRAIN<br>8. N-DRAIN                                                     | <b>STYLE 15:</b><br>PIN 1. ANODE 1<br>2. ANODE 1<br>3. ANODE 1<br>4. ANODE 1<br>5. CATHODE, COMMON<br>6. CATHODE, COMMON<br>7. CATHODE, COMMON<br>8. CATHODE, COMMON               | <b>STYLE 16:</b><br>PIN 1. EMITTER, DIE #1<br>2. BASE, DIE #1<br>3. EMITTER, DIE #2<br>4. BASE, DIE #2<br>5. COLLECTOR, DIE #2<br>6. COLLECTOR, DIE #2<br>7. COLLECTOR, DIE #1<br>8. COLLECTOR, DIE #1 |
| <b>STYLE 17:</b><br>PIN 1. VCC<br>2. V2OUT<br>3. V1OUT<br>4. TXE<br>5. RXE<br>6. VEE<br>7. GND<br>8. ACC                                                                                          | <b>STYLE 18:</b><br>PIN 1. ANODE<br>2. ANODE<br>3. SOURCE<br>4. GATE<br>5. DRAIN<br>6. DRAIN<br>7. CATHODE<br>8. CATHODE                                                                 | <b>STYLE 19:</b><br>PIN 1. SOURCE 1<br>2. GATE 1<br>3. SOURCE 2<br>4. GATE 2<br>5. DRAIN 2<br>6. MIRROR 2<br>7. DRAIN 1<br>8. MIRROR 1                                             | <b>STYLE 20:</b><br>PIN 1. SOURCE (N)<br>2. GATE (N)<br>3. SOURCE (P)<br>4. GATE (P)<br>5. DRAIN<br>6. DRAIN<br>7. DRAIN<br>8. DRAIN                                                                   |
| <b>STYLE 21:</b><br>PIN 1. CATHODE 1<br>2. CATHODE 2<br>3. CATHODE 3<br>4. CATHODE 4<br>5. CATHODE 5<br>6. COMMON ANODE<br>7. COMMON ANODE<br>8. CATHODE 6                                        | <b>STYLE 22:</b><br>PIN 1. I/O LINE 1<br>2. COMMON CATHODE/VCC<br>3. COMMON CATHODE/VCC<br>4. I/O LINE 3<br>5. COMMON ANODE/GND<br>6. I/O LINE 4<br>7. I/O LINE 5<br>8. COMMON ANODE/GND | <b>STYLE 23:</b><br>PIN 1. LINE 1 IN<br>2. COMMON ANODE/GND<br>3. COMMON ANODE/GND<br>4. LINE 2 IN<br>5. LINE 2 OUT<br>6. COMMON ANODE/GND<br>7. COMMON ANODE/GND<br>8. LINE 1 OUT | <b>STYLE 24:</b><br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR/ANODE<br>4. COLLECTOR/ANODE<br>5. CATHODE<br>6. CATHODE<br>7. COLLECTOR/ANODE<br>8. COLLECTOR/ANODE                                      |
| <b>STYLE 25:</b><br>PIN 1. VIN<br>2. N/C<br>3. REXT<br>4. GND<br>5. IOUT<br>6. IOUT<br>7. IOUT<br>8. IOUT                                                                                         | <b>STYLE 26:</b><br>PIN 1. GND<br>2. dv/dt<br>3. ENABLE<br>4. ILIMIT<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. VCC                                                                    | <b>STYLE 27:</b><br>PIN 1. ILIMIT<br>2. OVLO<br>3. UVLO<br>4. INPUT+<br>5. SOURCE<br>6. SOURCE<br>7. SOURCE<br>8. DRAIN                                                            | <b>STYLE 28:</b><br>PIN 1. SW_TO_GND<br>2. DASIC_OFF<br>3. DASIC_SW_DET<br>4. GND<br>5. V_MON<br>6. VBULK<br>7. VBULK<br>8. VIN                                                                        |
| <b>STYLE 29:</b><br>PIN 1. BASE, DIE #1<br>2. EMITTER, #1<br>3. BASE, #2<br>4. EMITTER, #2<br>5. COLLECTOR, #2<br>6. COLLECTOR, #2<br>7. COLLECTOR, #1<br>8. COLLECTOR, #1                        | <b>STYLE 30:</b><br>PIN 1. DRAIN 1<br>2. DRAIN 1<br>3. GATE 2<br>4. SOURCE 2<br>5. SOURCE 1/DRAIN 2<br>6. SOURCE 1/DRAIN 2<br>7. SOURCE 1/DRAIN 2<br>8. GATE 1                           |                                                                                                                                                                                    |                                                                                                                                                                                                        |

|                         |                    |                                                                                                                                                                                     |
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