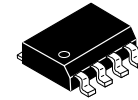


MOSFET – Dual, N-Channel, POWERTRENCH[®], 80 V

FDS3890



SOIC8
CASE 751EB

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC-DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC-DC power supply designs with higher overall efficiency.

Features

- 4.7 A, 80 V:
 - ◆ $R_{DS(ON)} = 44\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 - ◆ $R_{DS(ON)} = 50\text{ m}\Omega @ V_{GS} = 6\text{ V}$
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- Pb-Free and Halide Free

ABSOLUTE MAXIMUM RATINGS

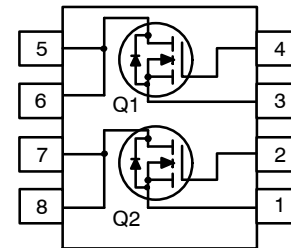
($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-Source Voltage	80	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current		A
	Continuous (Note 1a)	4.7	
	Pulsed	20	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation		
	(Note 1a)	1.6	
	(Note 1b)	1.0	
	(Note 1c)	0.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

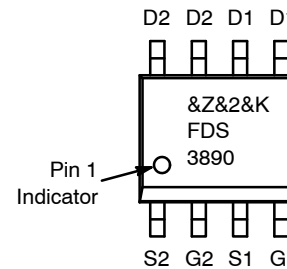
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C}/\text{W}$



MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = Date Code (Year & Week)
- &K = Lot Traceability Code
- FDS3890 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDS3890	SOIC8 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FDS3890

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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DRAIN-SOURCE AVALANCHE RATINGS (Note 2)

W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 40 V, I _D = 4.7 A	-	-	175	mJ
I _{AR}	Maximum Drain-Source Avalanche Current		-	-	4.7	A

OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	80	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	86	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 64 V, V _{GS} = 0 V	-	-	1	μA
I _{GSSF}	Gate-Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V	-	-	100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	-	-	-100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	2.3	4	V
ΔV _{GS(th)} / ΔT _J	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	-6	-	mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 4.7 A V _{GS} = 6 V, I _D = 4.4 A V _{GS} = 10 V, I _D = 4.7 A, T _J = 125°C	-	34 37 60	44 50 82	mΩ
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	20	-	-	A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 4.7 A	-	24	-	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 40 V, V _{GS} = 0 V, f = 1.0 MHz	-	1180	-	pF
C _{oss}	Output Capacitance		-	171	-	pF
C _{rss}	Reverse Transfer Capacitance		-	50	-	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn-On Delay Time	V _{DD} = 40 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	-	11	20	ns
t _r	Turn-On Rise Time		-	8	16	ns
t _{d(off)}	Turn-Off Delay Time		-	26	50	ns
t _f	Turn-Off Fall Time		-	12	25	ns
Q _g	Total Gate Charge	V _{DS} = 40 V, I _D = 4.7 A, V _{GS} = 10 V	-	25	35	nC
Q _{gs}	Gate-Source Charge		-	4.5	-	nC
Q _{gd}	Gate-Drain Charge		-	5.8	-	nC

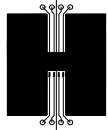
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		-	-	1.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)	-	0.74	1.2	V

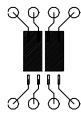
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

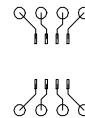
- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 78°C/W when mounted on a 1 in² pad of 2 oz. copper.



b) 125°C/W when mounted on a 0.04 in² pad of 2 oz. copper.



c) 135°C/W when mounted on a minimum pad.

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

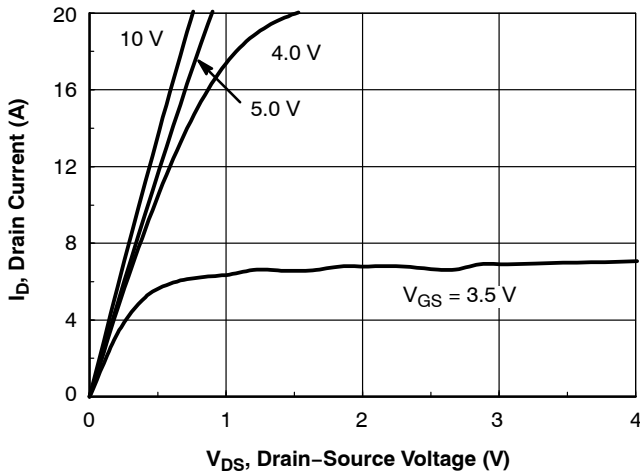


Figure 1. On-Region Characteristic

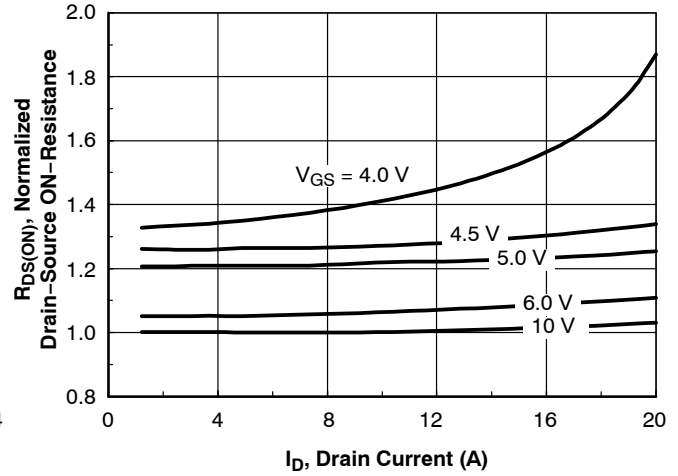


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

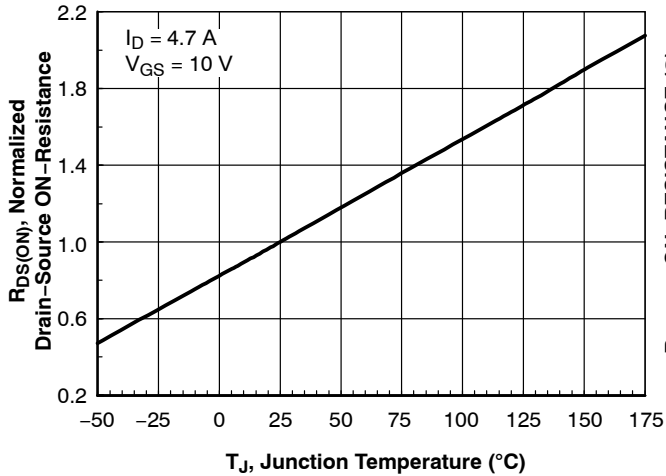


Figure 3. On-Resistance Variation with Temperature

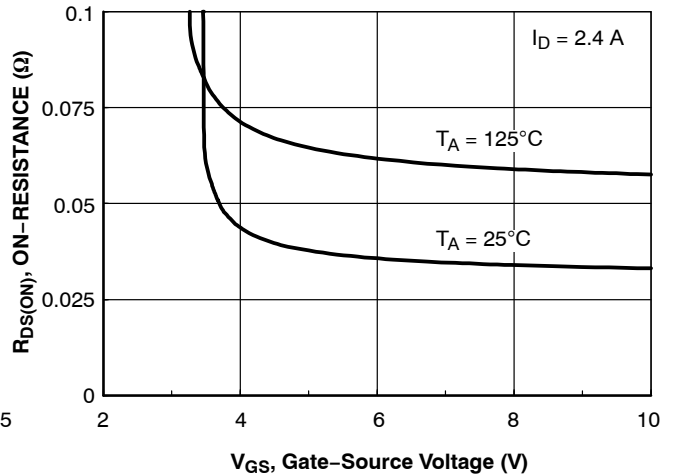


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

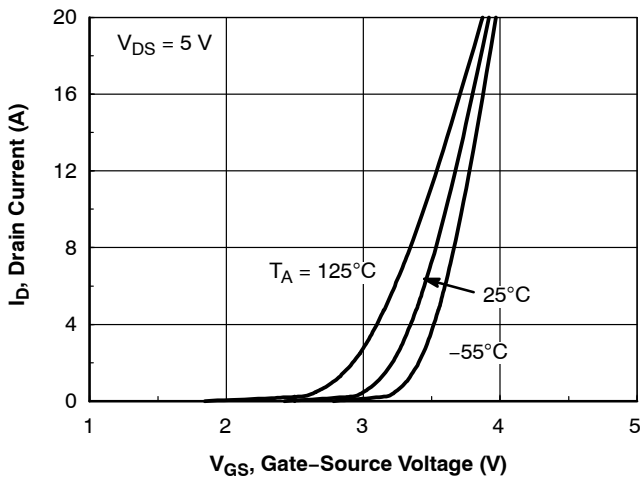


Figure 5. Transfer Characteristics

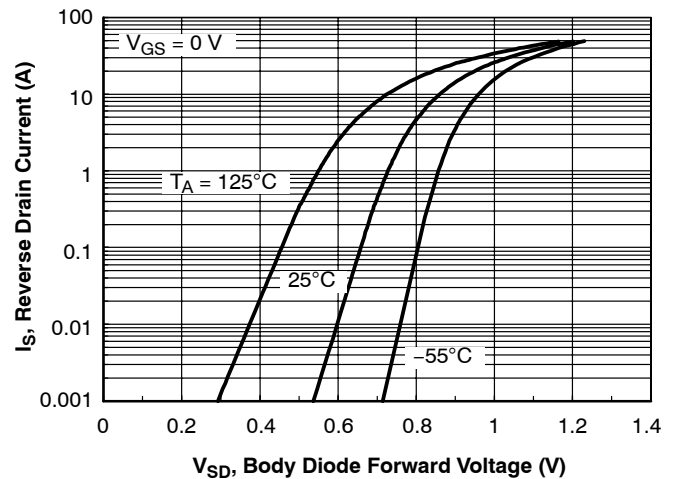


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Continued)

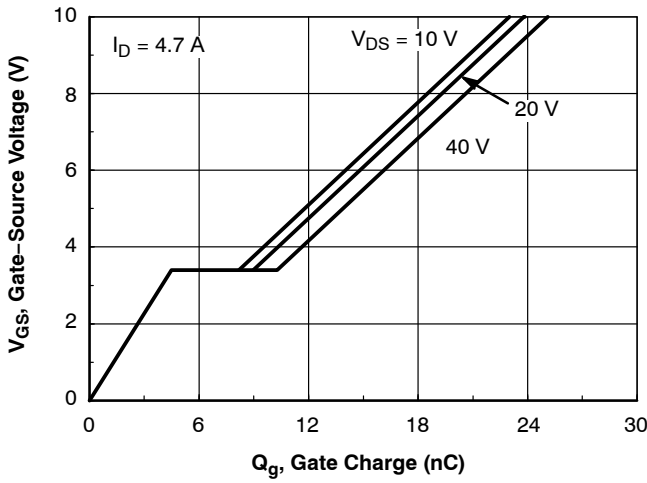


Figure 7. Gate-Charge Characteristics

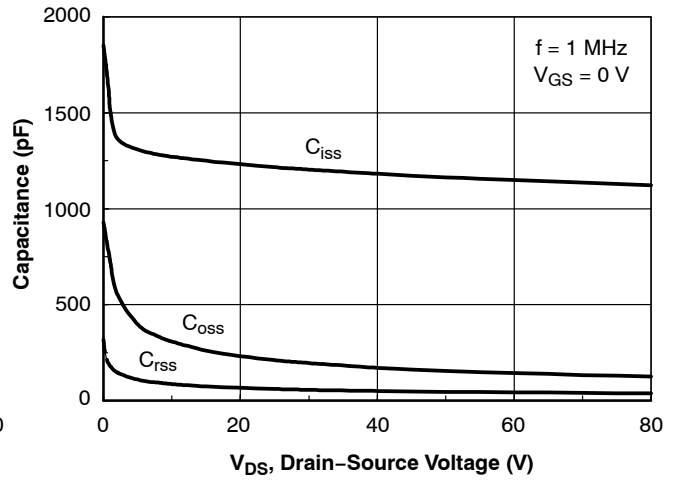


Figure 8. Capacitance Characteristics

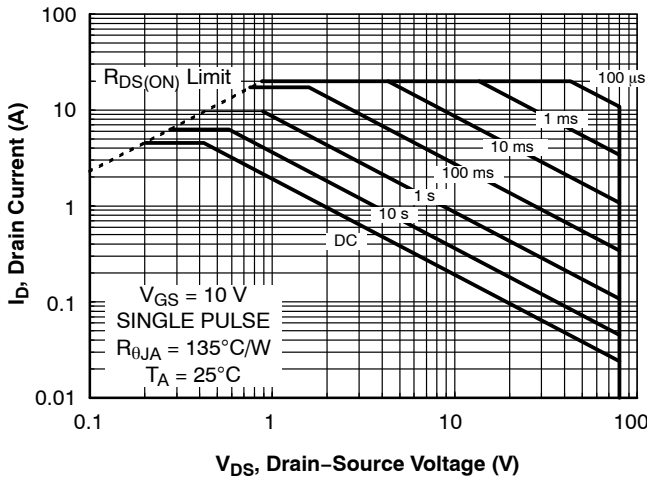


Figure 9. Maximum Safe Operating Area

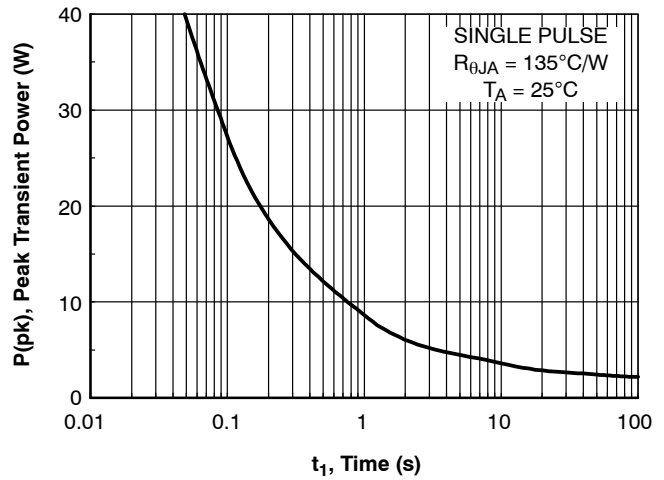


Figure 10. Single Pulse Maximum Power Dissipation

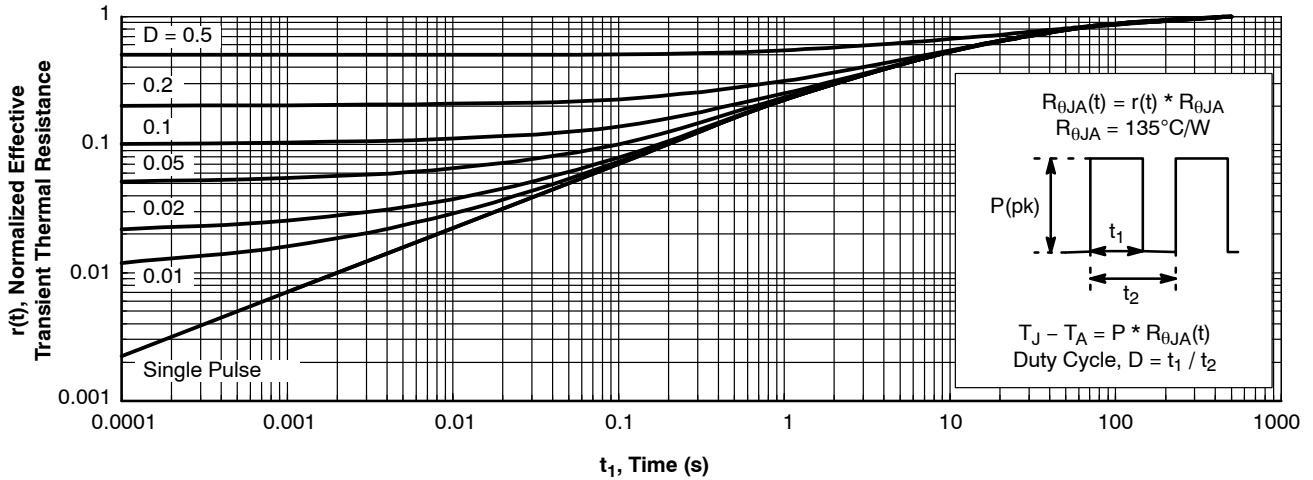
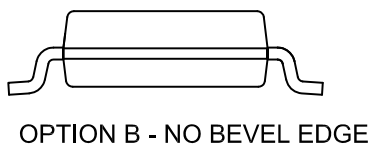
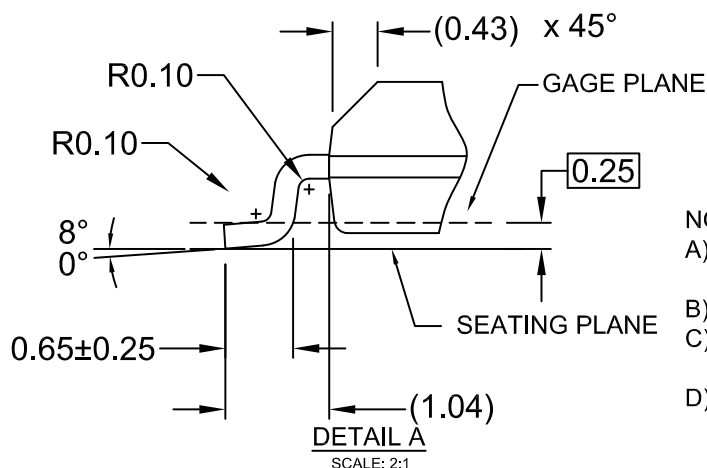
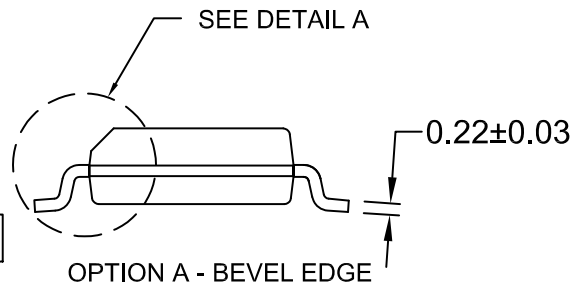
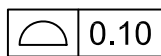
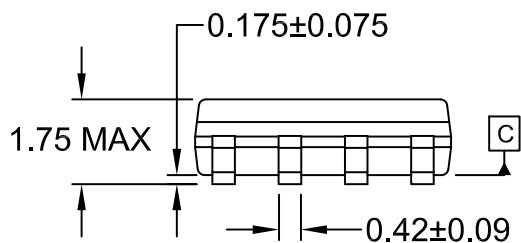
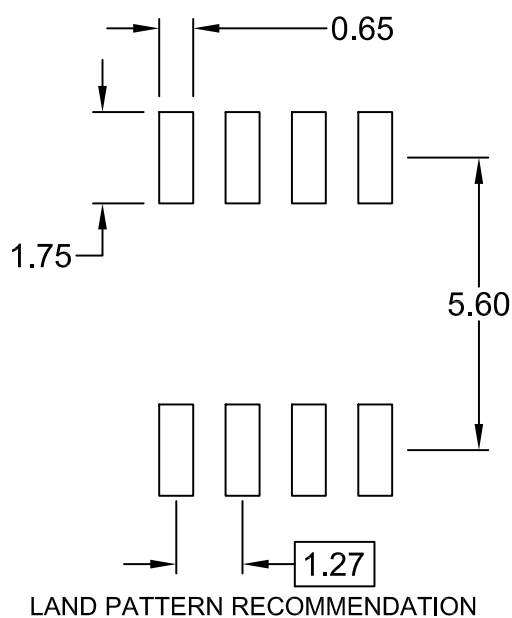
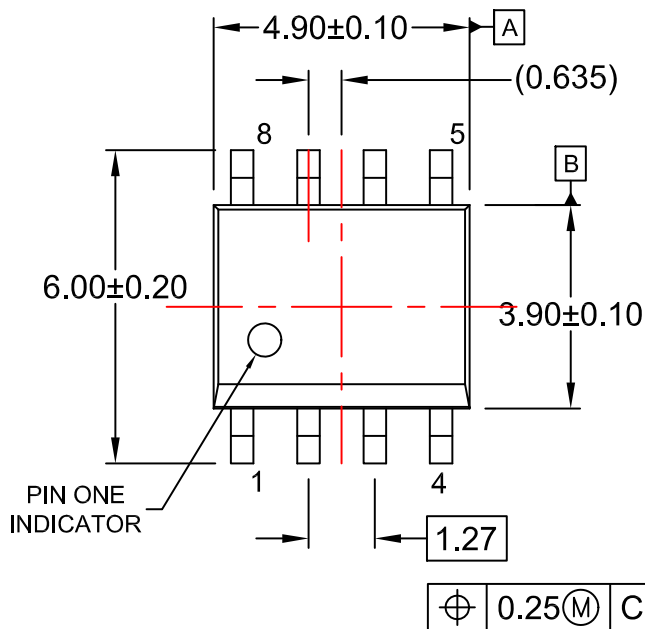


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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ISSUE A

DATE 24 AUG 2017



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