

MOSFET – N-Channel, UniFET™, FRFET®

500 V, 45 A, 120 mΩ

FDH45N50F

Description

UniFET MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100 nsec and the reverse dv/dt immunity is 15 V/ns while normal planar MOSFETs have over 200 nsec and 4.5 V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)} = 105 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 22.5 \text{ A}$
- Low Gate Charge (Typ. 105 nC)
- Low C_{rss} (Typ. 62 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

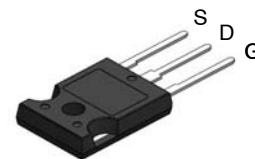
Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
500 V	120 mΩ @ 10 V	45 A

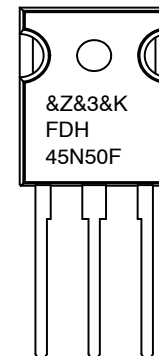


N-CHANNEL MOSFET



TO-247-3LD
CASE 340CK

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3-Digit Date Code (YWW)
&K	= 2-Digit Lot Traceability Code
FDH45N50F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDH45N50F

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FDH45N50F-F133	Unit
V _{DSS}	Drain to Source Voltage	500	V
I _D	Drain Current – –Continuous (T _C = 25°C) –Continuous (T _C = 100°C)	45 28.4	A A
I _{DM}	Drain Current –Pulsed (Note 1)	180	A
V _{GSS}	Gate–Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1868	mJ
I _{AR}	Avalanche Current (Note 1)	45	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	62.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	50	V/ns
P _D	Power Dissipation (T _C = 25°C) –Derate Above 25°C	625 5	W W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Second	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 1.46 mH, I_{AS} = 48 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25 °C.
3. I_{SD} ≤ 45 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Package Method	Reel Size	Tape Width	Quantity
FDH45N50F-F133	FDH45N50F	TO-247-3	Tube	–	–	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FDH45N50F-F133	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.2	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

FDH45N50F

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	500	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.5	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	–	–	25	μA
		V _{DS} = 400 V, T _C = 125°C	–	–	250	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = –30 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	–	5	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 22.5 A	–	0.105	0.12	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 22.5 A	–	49	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	5100	6630	pF
C _{oss}	Output Capacitance		–	790	1030	pF
C _{rss}	Reverse Transfer Capacitance		–	62	–	pF
C _{oss}	Output Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	161	–	pF
C _{oss,eff.}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	342	–	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 48 A, V _{GS} = 10 V, R _G = 25 Ω (Note 4)	–	140	290	ns
t _r	Turn-On Rise Time		–	500	1010	ns
t _{d(off)}	Turn-Off Delay Time		–	215	440	ns
t _f	Turn-Off Fall Time		–	245	500	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 48 A, V _{GS} = 10 V (Note 4)	–	105	137	nC
Q _{gs}	Gate–Source Charge		–	33	–	nC
Q _{gd}	Gate–Drain Charge		–	45	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	45	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	180	A
V _{SD}	Source to Drain Diode Voltage	V _{GS} = 0 V, I _S = 45 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 45 A, dI _F /dt = 100 A/μs	–	188	–	ns
Q _{rr}	Reverse Recovery Charge		–	0.64	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

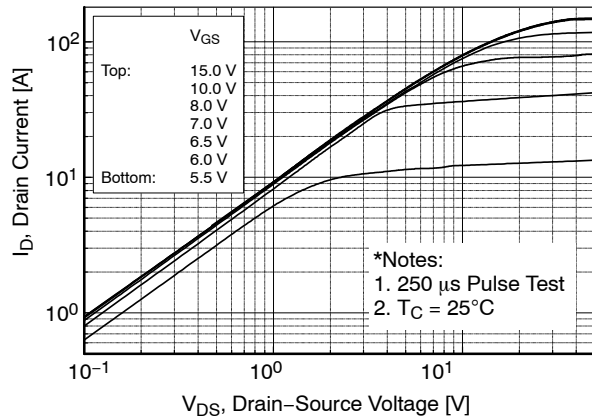


Figure 1. On-Region Characteristics

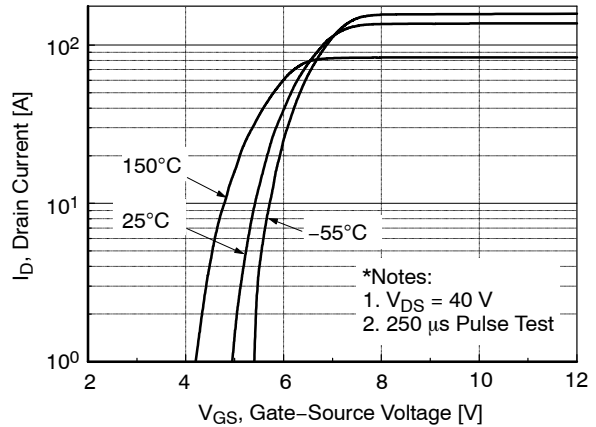


Figure 2. Transfer Characteristics

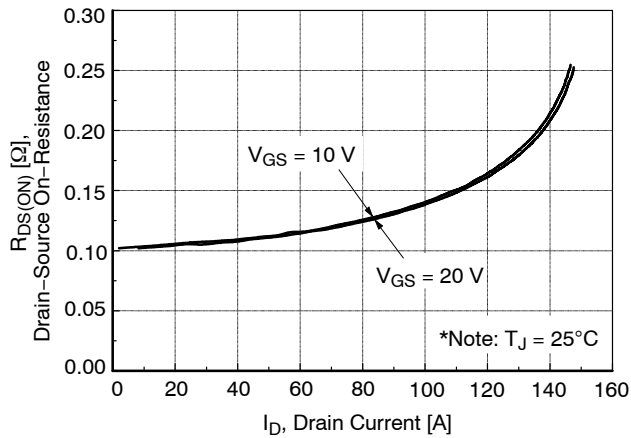


Figure 3. On-Resistance Variation vs. Drain Current and Gate voltage

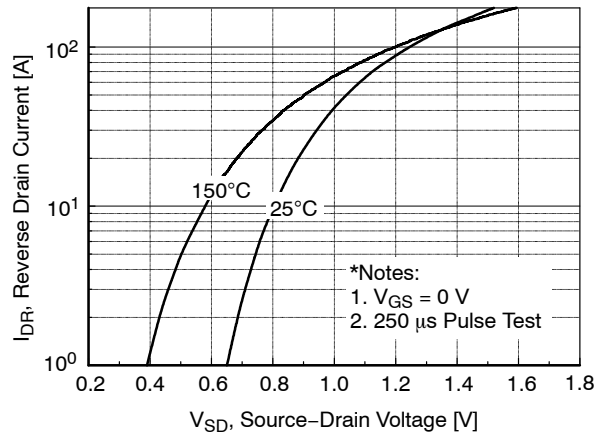


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

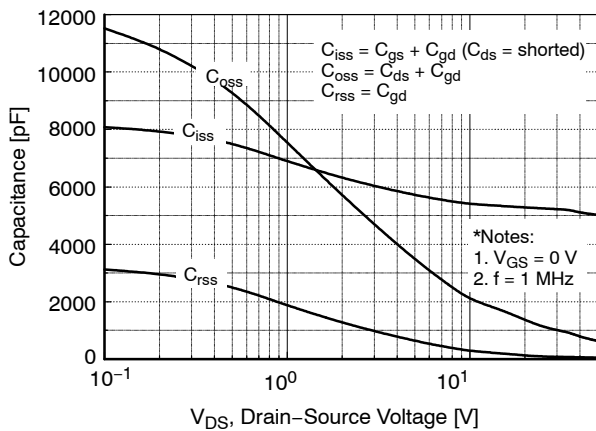


Figure 5. Capacitance Characteristics

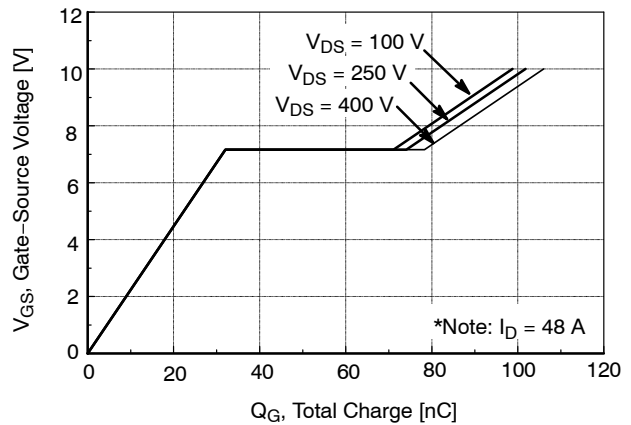


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

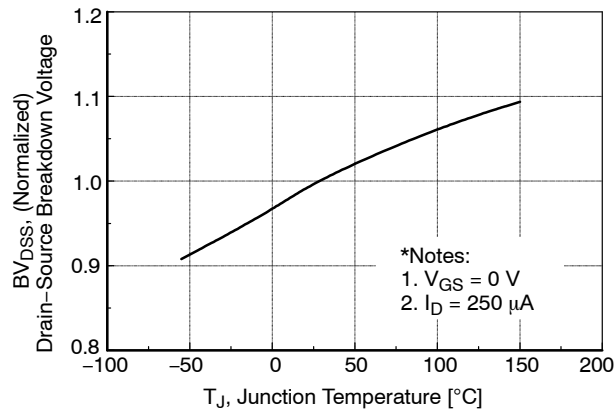


Figure 7. Breakdown Voltage Variation vs. Temperature

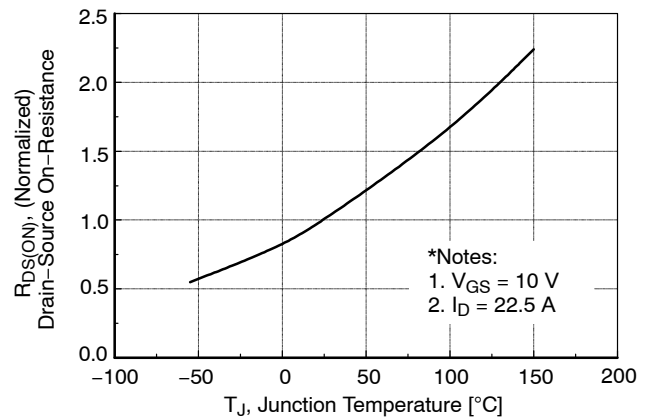


Figure 8. On-Resistance Variation vs. Temperature

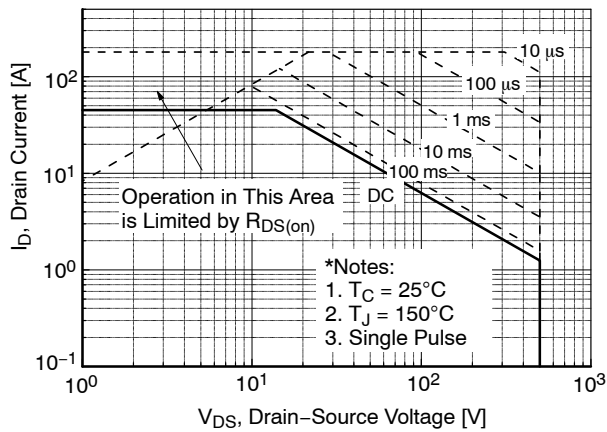


Figure 9. Maximum Safe Operating Area

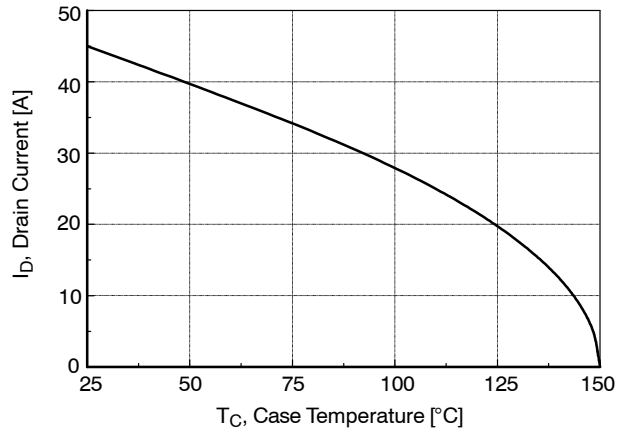


Figure 10. Maximum Drain Current vs. Case Temperature

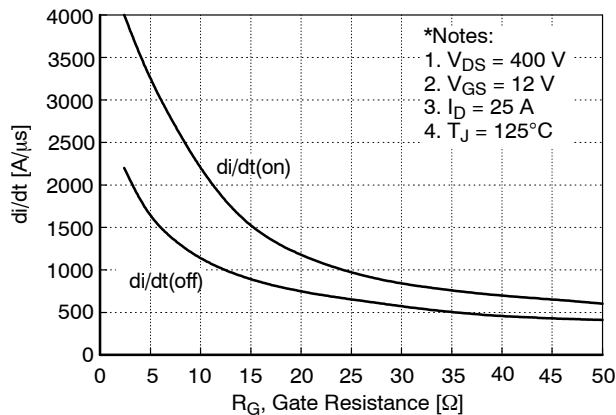


Figure 11. Typical Drain Current Slope vs. Gate Resistance

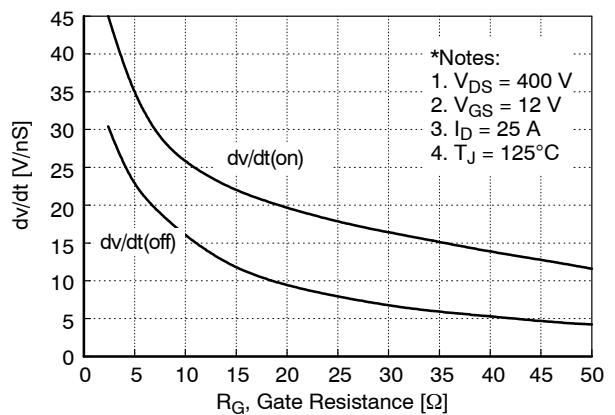


Figure 12. Typical Drain-Source Voltage Slope vs. Gate Resistance

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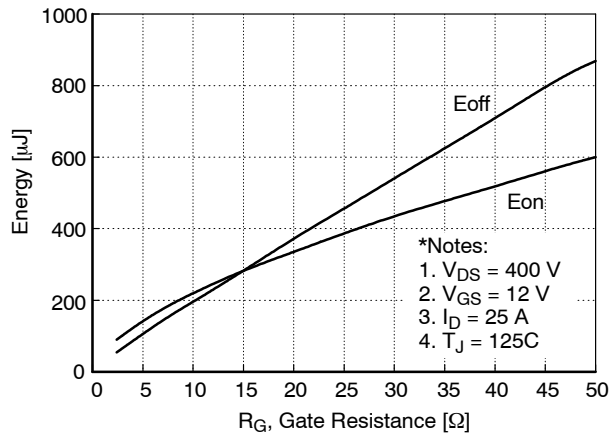


Figure 13. Typical Switching Losses vs. Gate Resistance

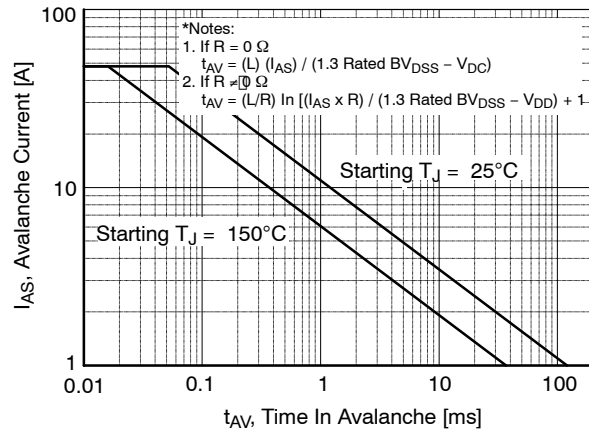


Figure 14. Unclamped Inductive Switching Capability

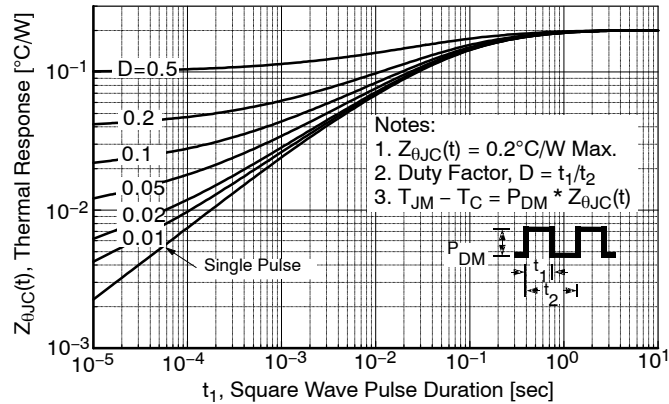
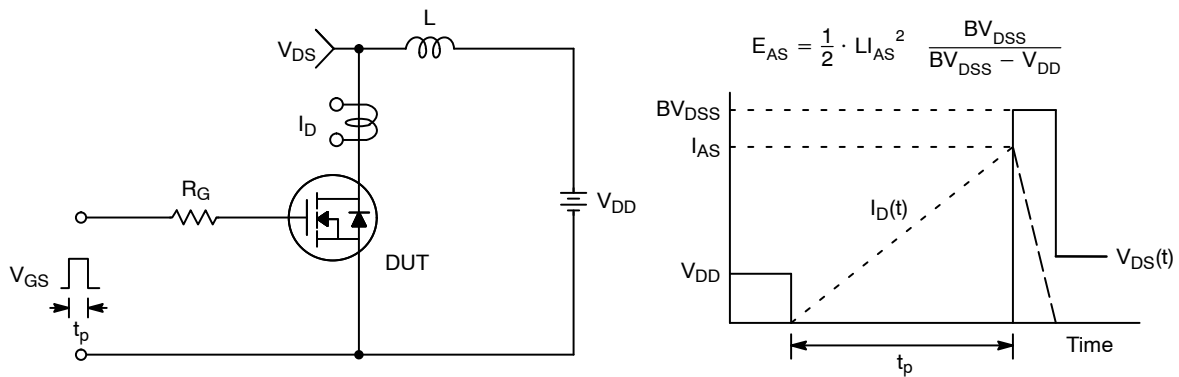
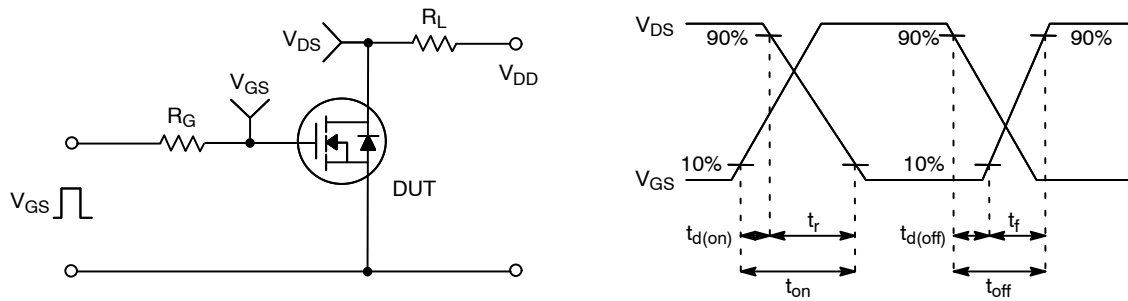
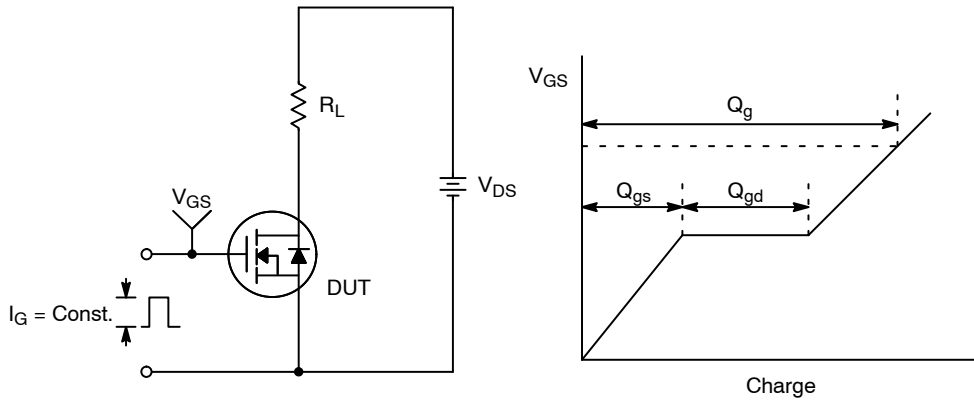


Figure 15. Transient Thermal Resistance Curve



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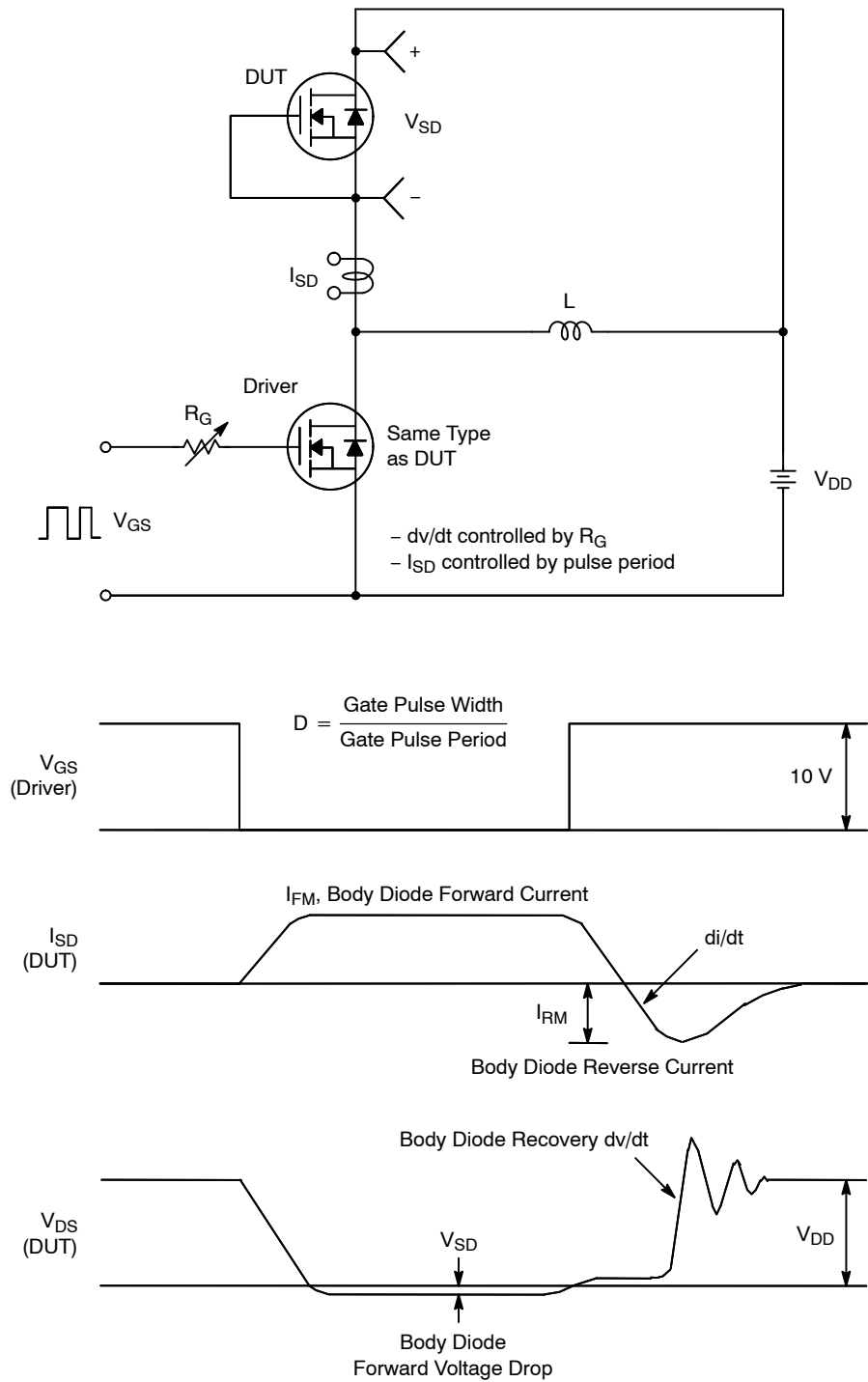


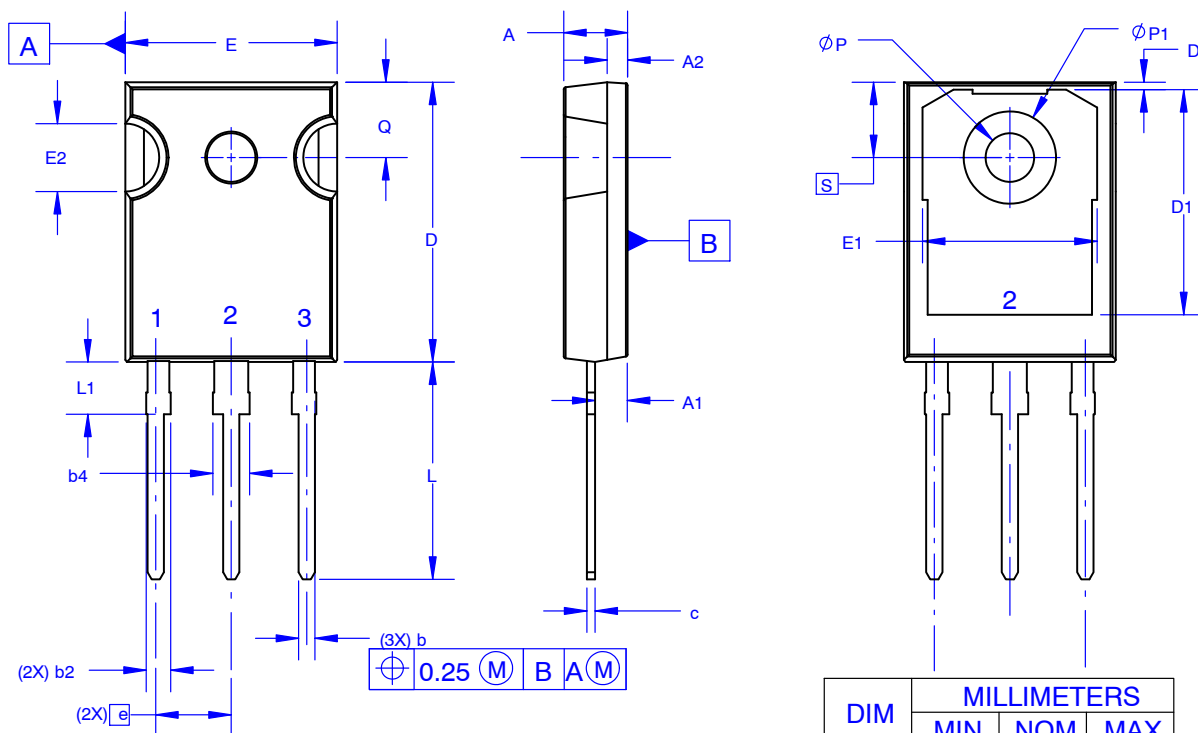
Figure 19. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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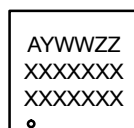
TO-247-3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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