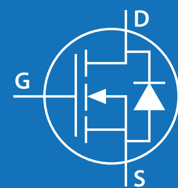
EPC2252 – Enhancement Mode Power Transistor

V_{DS} , 80 V
$R_{DS(on)}$, 11 mΩ max
I_D , 8.2 A
AEC-Q101



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised April 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

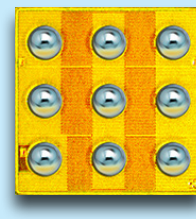
Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	8.2	A
	Pulsed (25 °C, T_{PULSE} = 10 µs)	100	
	Pulsed (125 °C, T_{PULSE} = 10 µs)	80	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case (Case Top)	1.6	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board (Case Bottom)	8.3	
$R_{θJA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	95	
$R_{θJA\_EVB}$	Thermal Resistance, Junction to Ambient (using EPC9093 EVB)	71	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.12 mA	80			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V , V_{DS} = 80 V		25	120	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 6 V		0.02	1.4	mA
	Gate-to-Source Forward Leakage#	V_{GS} = 6 V, T_J = 125°C		0.3	5.0	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.02	0.125	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2.5 mA	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 11 A		8	11	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

Defined by design. Not subject to production test.



Die size: 1.5 x 1.5 mm

EPC2252 eGaN® FETs are supplied in passivated die form with solder bumps.

Applications
- Automotive lidar/TOF
- 48 V servers
- Pulsed power
- Isolated power supplies
- Point of load converters
- Class D audio
- LED lighting
- Low inductance motor drive

Benefits
- Higher switching frequency – Lower switching losses and lower drive power
- Higher efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint – Higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2252

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
C_{ISS}	Input Capacitance	V_{DS} = 50 V , V_{GS} = 0 V		440	576	pF
C_{RSS}	Reverse Transfer Capacitance			1.3		
C_{OSS}	Output Capacitance			190	204	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		233		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			305		
R_G	Gate Resistance			0.6		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 11 A		3.5	4.3	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 11 A		1.0		
Q_{GD}	Gate-to-Drain Charge			0.5		
$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
Q_{OSS}	Output Charge	V_{DS} = 50 V , V_{GS} = 0 V		15	17	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Figure 1: Typical Output Characteristics at 25°C*

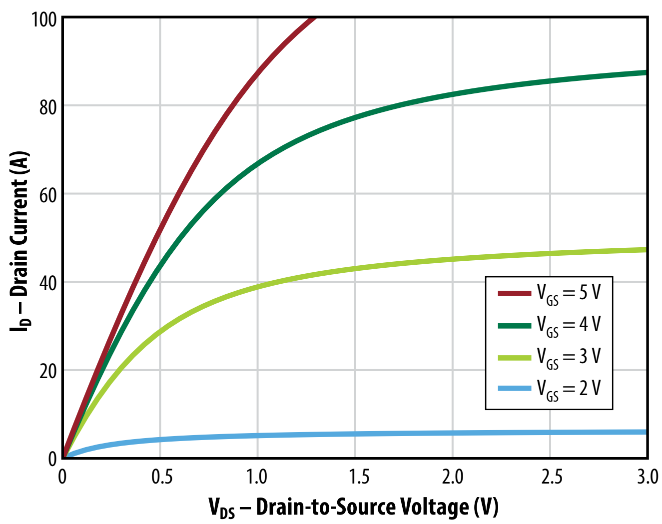


Figure 2: Typical Transfer Characteristics*

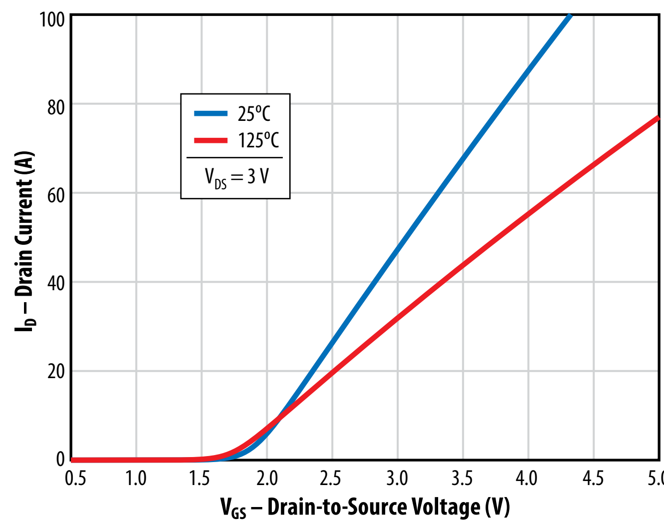


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Currents

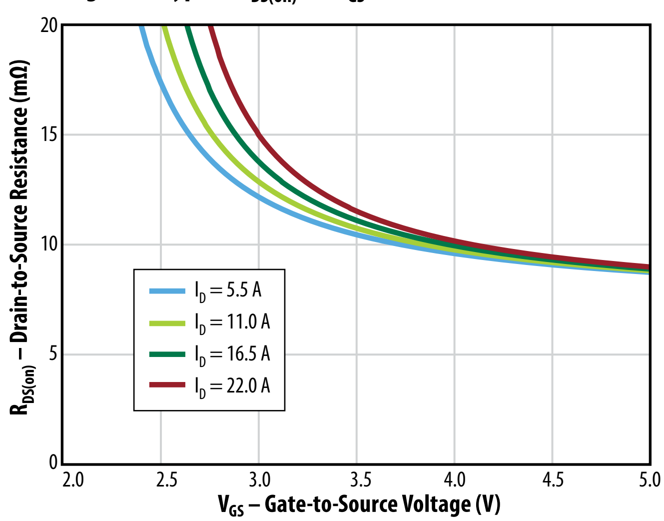
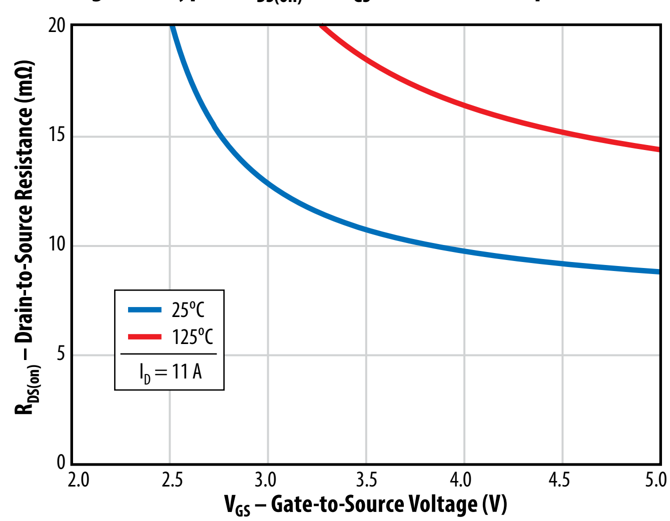


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures



* Generated based on a pulse width of 300 µs.

Figure 5a: Typical Capacitance (Linear Scale)

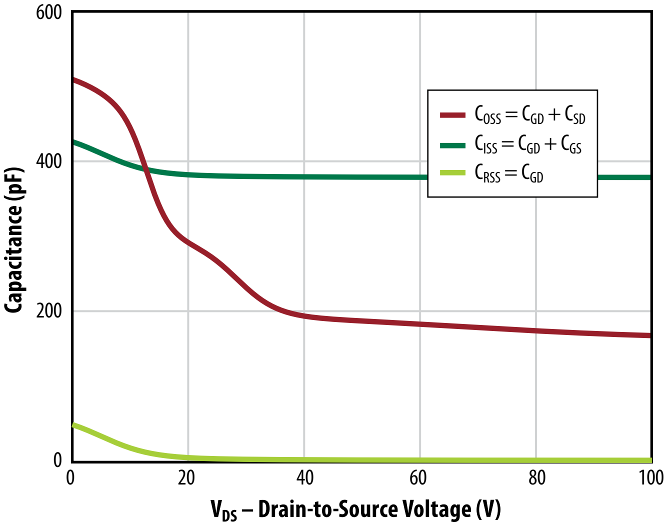


Figure 5b: Typical Capacitance (Log Scale)

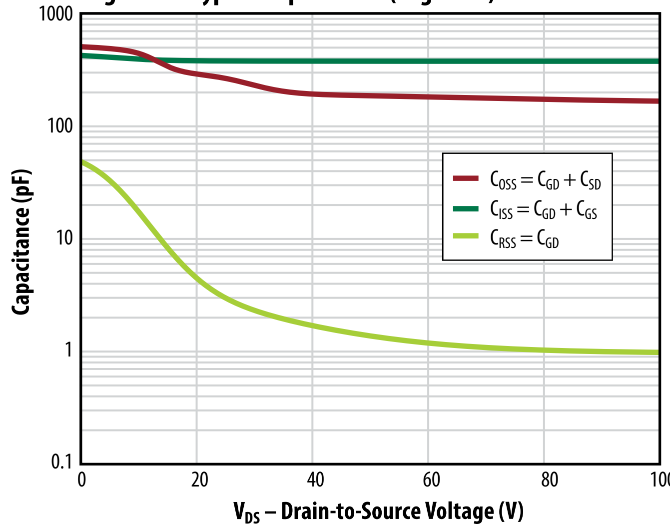


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

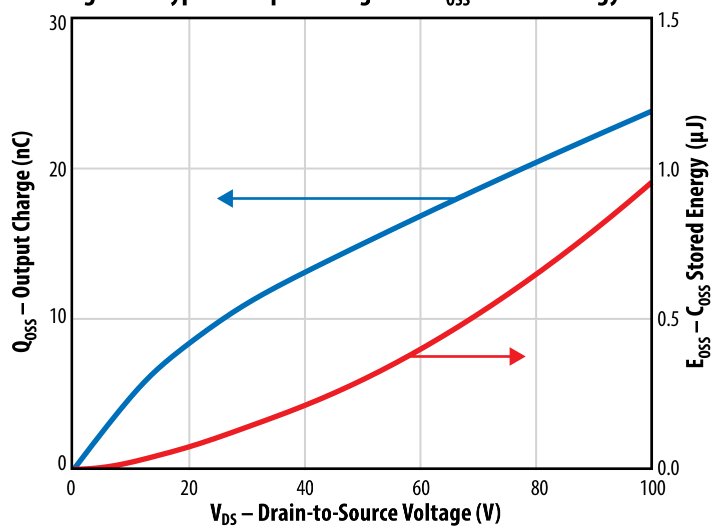


Figure 7: Typical Gate Charge

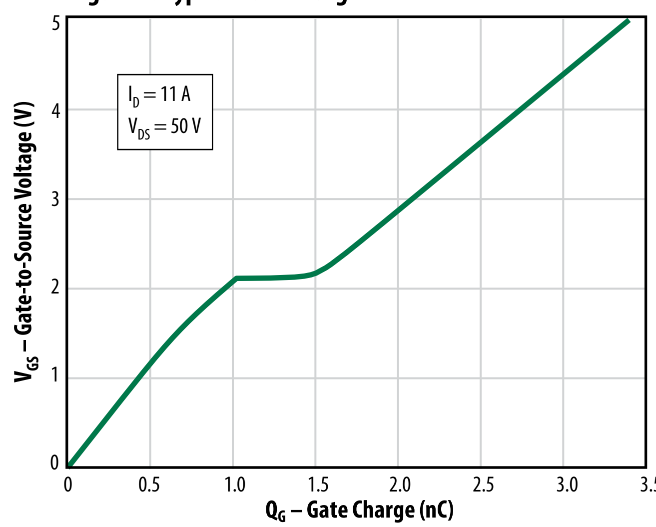
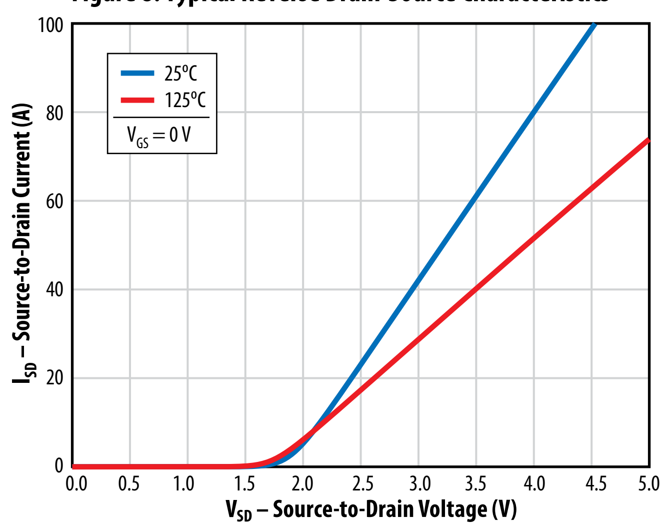


Figure 8: Typical Reverse Drain-Source Characteristics*



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

* Generated based on a pulse width of 300 µs.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

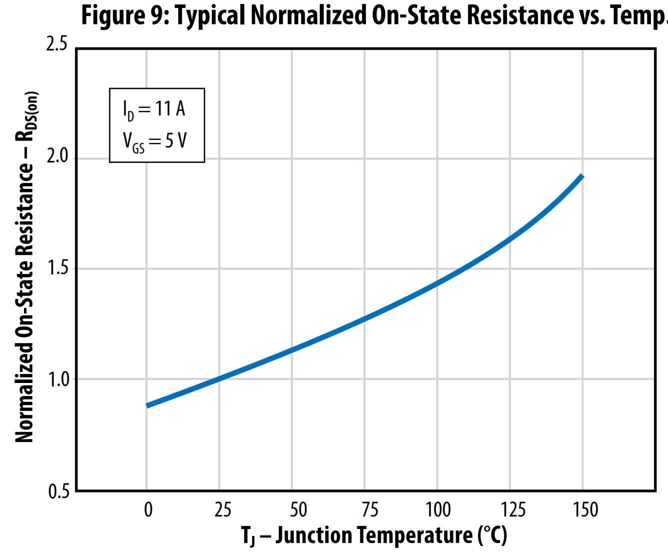


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

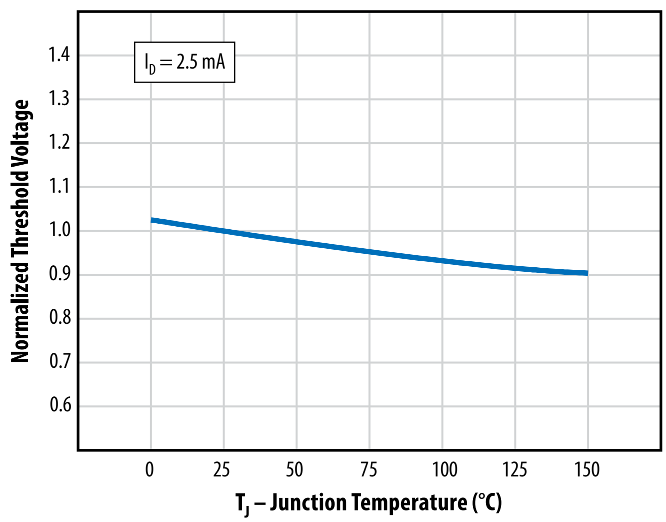
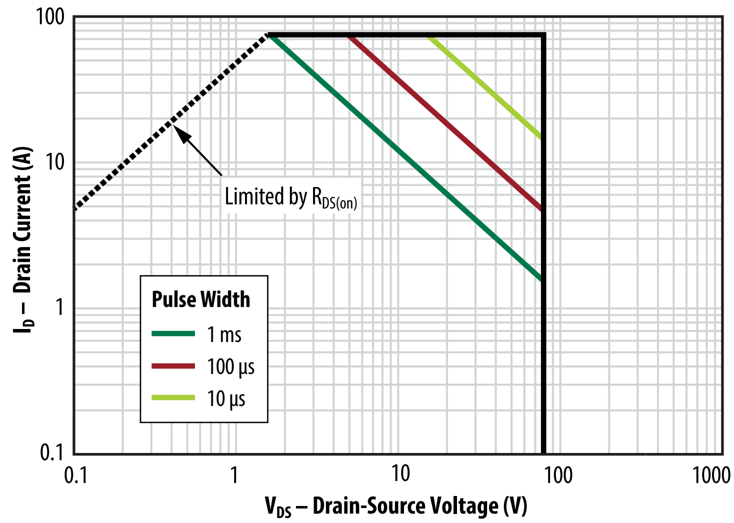
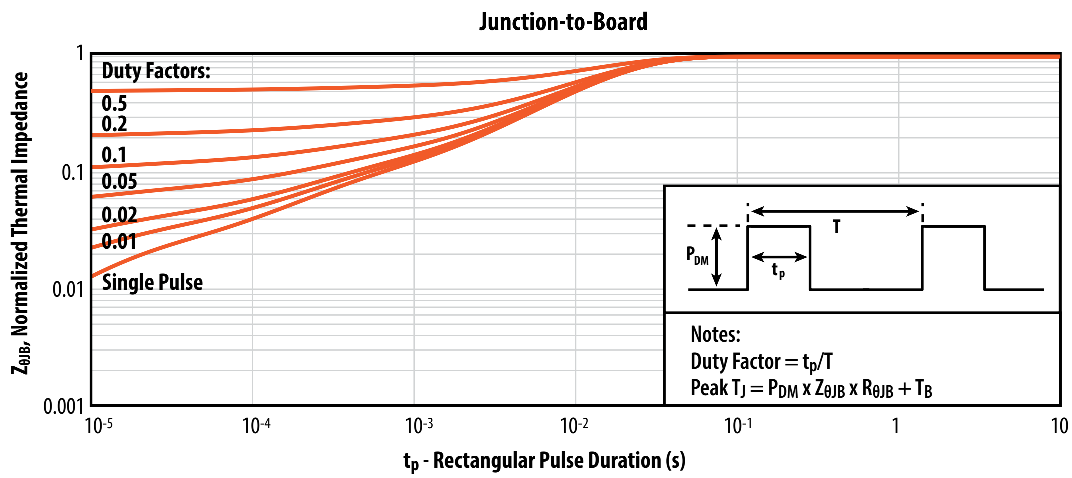


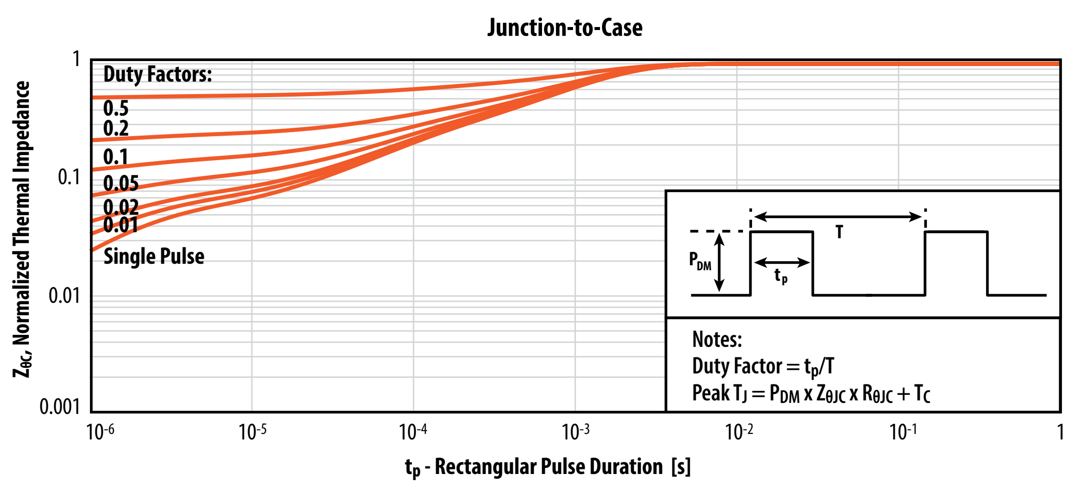
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

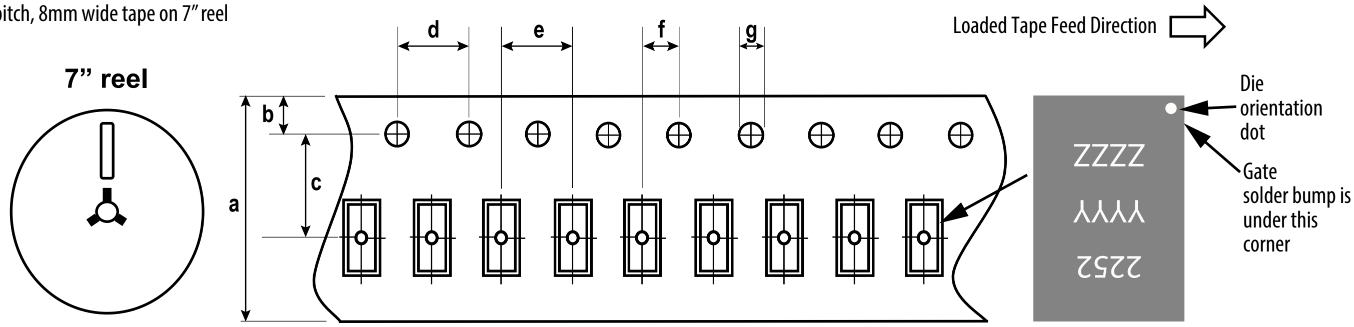
Figure 12: Typical Transient Thermal Response Curves





TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel



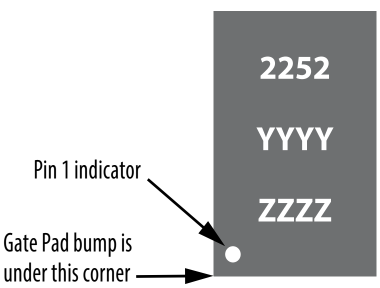
Die is placed into pocket solder bump side down (face side down)

	Dimension (mm)		
EPC2252 (Note 1)	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

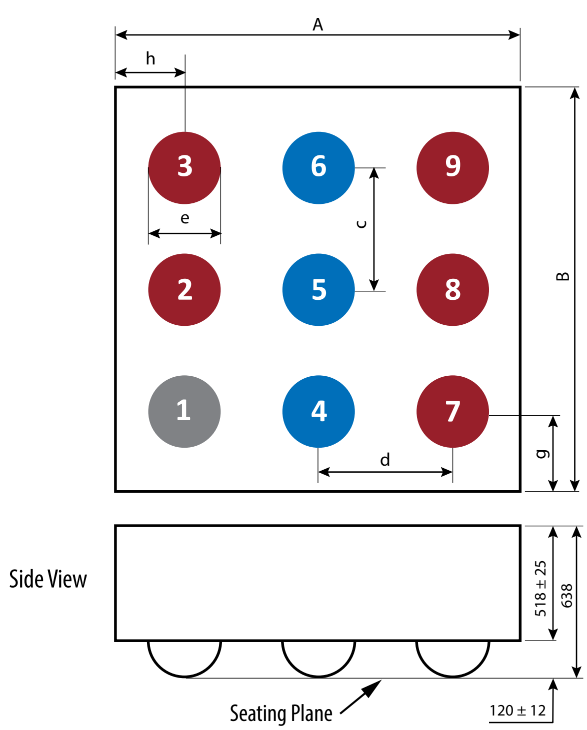
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2252	2252	YYYY	ZZZZ

DIE OUTLINE

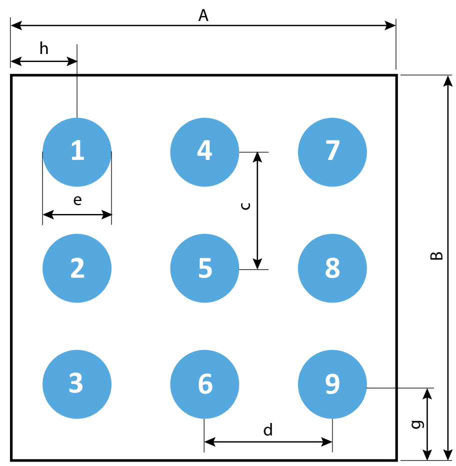
Solder Bump View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1470	1500	1530
B	1470	1500	1530
c		450	
d		500	
e		250	
g		300	
h		250	

Pad 1 is Gate;
Pads 2, 3, 7, 8, 9 are Source;
Pads 4, 5, 6 are Drain

RECOMMENDED LAND PATTERN
(units in µm)

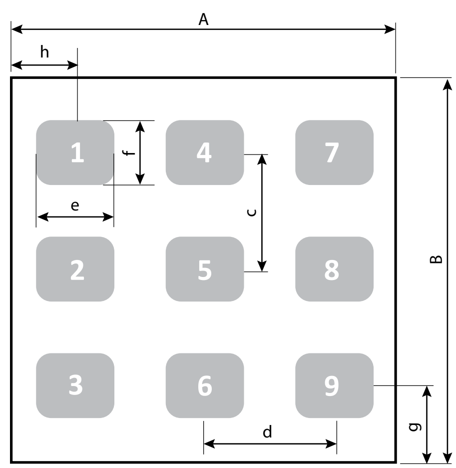


Land pattern is solder mask defined.

DIM	MICROMETERS
A	1500
B	1500
c	450
d	500
e	230
g	300
h	250

Pad 1 is Gate;
Pads 2, 3, 7, 8, 9 are Source;
Pads 4, 5, 6 are Drain

RECOMMENDED STENCIL DRAWING
(measurements in µm)



DIM	MICROMETERS
A	1500
B	1500
c	450
d	500
e	300
f	250
g	300
h	250

Pad 1 is Gate;
Pads 2, 3, 7, 8, 9 are Source;
Pads 4, 5, 6 are Drain

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, opening per drawing.
The corner has a radius of R60. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional resources available:

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip** (for preliminary device Altium footprints, contact EPC)