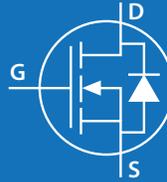# EPC2206 – Automotive 80 V (D-S) Enhancement Mode Power Transistor

V_{DS} , 80 V

$R_{DS(on)}$, 2.2 mΩ

I_D , 90 A

AEC-Q101

EFFICIENT POWER CONVERSION

RoHS | Halogen-Free

Revised April 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source
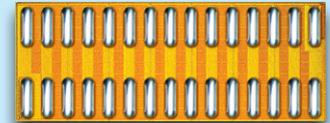
Questions:
Ask a GaN Expert
ASK AN EXPERT GaN

Die Size: 6.05 x 2.3 mm

EPC2206 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications
- 48 V automotive power
- Open rack server architectures
- High power density DC-DC converters
- Isolated power supplies
- Class-D audio
- Low inductance motor drive

Benefits
- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
I_D	Continuous (T_A = 25℃)	90	A
	Pulsed (25℃, T_{PULSE} = 300 µs)	390	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	℃
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{θJC}$	Thermal Resistance, Junction-to-Case	0.4	℃/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

Static Characteristics (T_J = 25℃ unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 500 µA	80			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		20	200	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 6 V, T_J = 25℃		0.02	4	mA
	Gate-to-Source Forward Leakage#	V_{GS} = 6 V, T_J = 125℃		0.1	9	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		20	200	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 13 mA	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 29 A		1.8	2.2	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

Defined by design. Not subject to production test.

https://l.ead.me/EPC2206

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 40\ V, V_{GS} = 0\ V$		1610	1940	pF
C_{RSS}	Reverse Transfer Capacitance			15		
C_{OSS}	Output Capacitance			1100	1650	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\ to\ 40\ V, V_{GS} = 0\ V$		1450		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1790		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	$V_{DS} = 40\ V, V_{GS} = 5\ V, I_D = 29\ A$		15	19	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 40\ V, I_D = 29\ A$		4.1		
Q_{GD}	Gate-to-Drain Charge			3		
$Q_{G(TH)}$	Gate Charge at Threshold			2.7		
Q_{OSS}	Output Charge	$V_{DS} = 40\ V, V_{GS} = 0\ V$		72	108	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
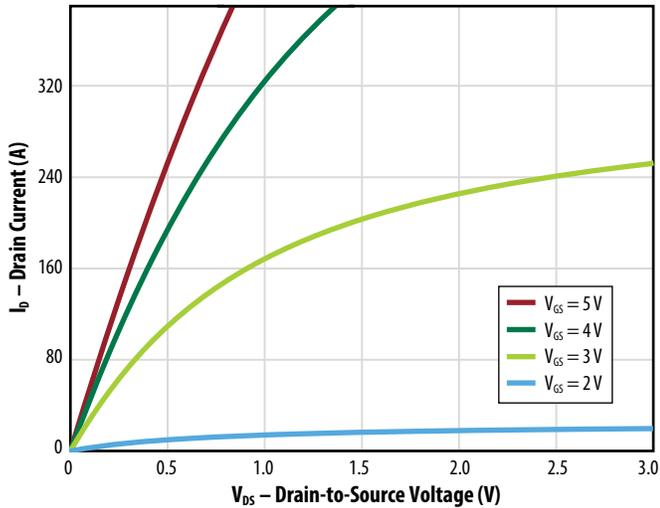
Figure 1: Typical Output Characteristics at 25°C
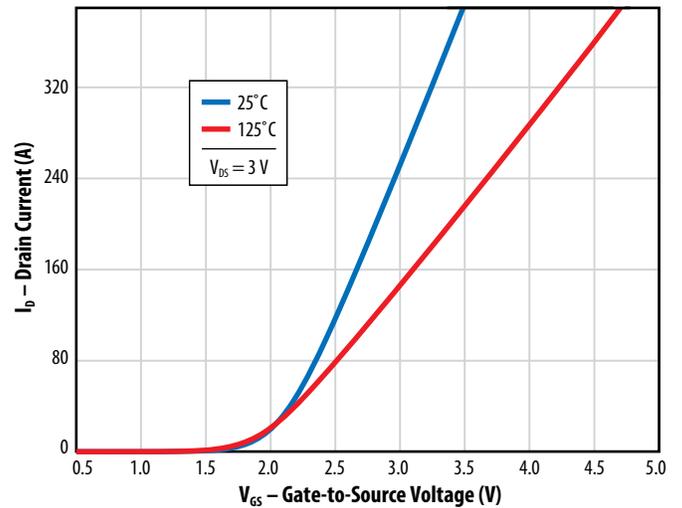

Figure 2: Typical Transfer Characteristics

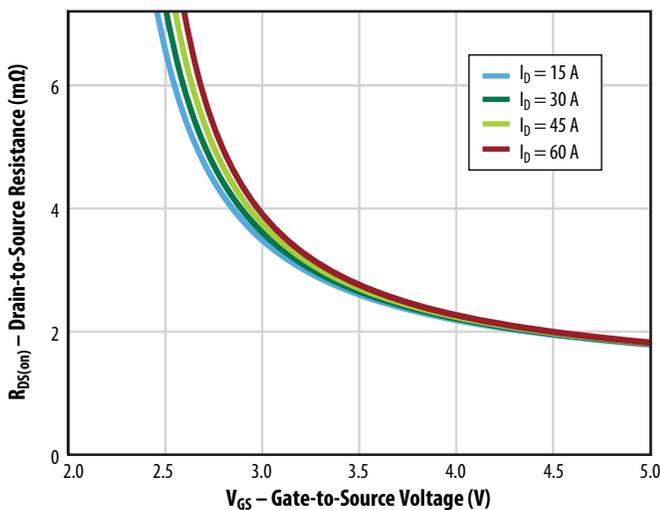### Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures
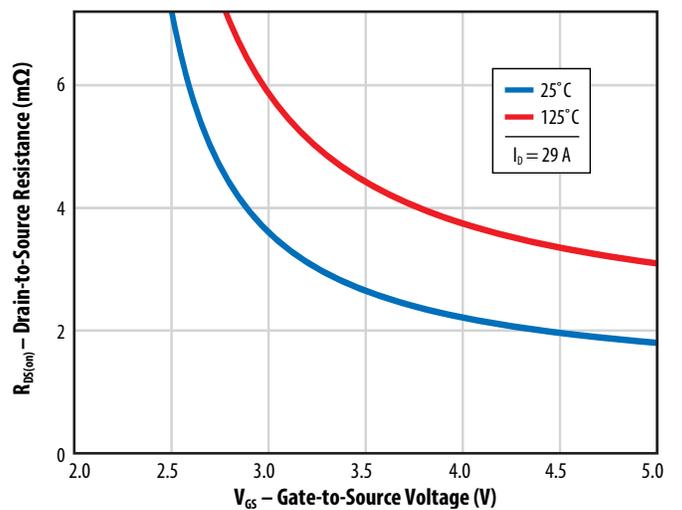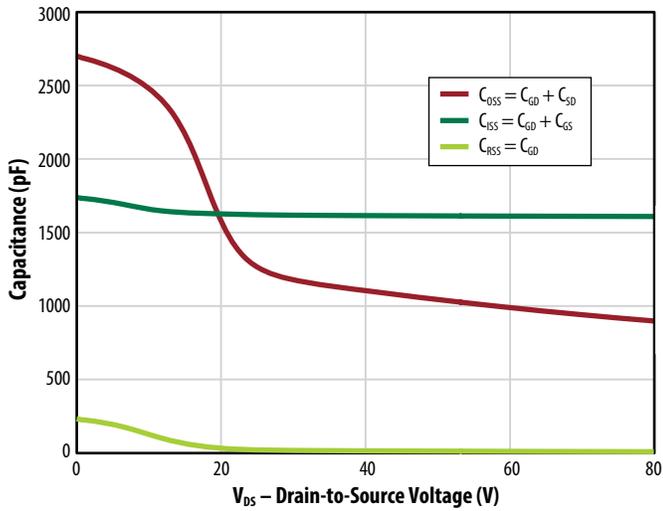
Figure 5a: Typical Capacitance (Linear Scale)

Legend:
$C_{OSS} = C_{GD} + C_{SD}$
$C_{ISS} = C_{GD} + C_{GS}$
$C_{RSS} = C_{GD}$

Y-axis: Capacitance (pF)
X-axis: V_{DS} – Drain-to-Source Voltage (V)

Figure 5b: Typical Capacitance (Log Scale)

Legend:
$C_{OSS} = C_{GD} + C_{SD}$
$C_{ISS} = C_{GD} + C_{GS}$
$C_{RSS} = C_{GD}$

Y-axis: Capacitance (pF)
X-axis: V_{DS} – Drain-to-Source Voltage (V)
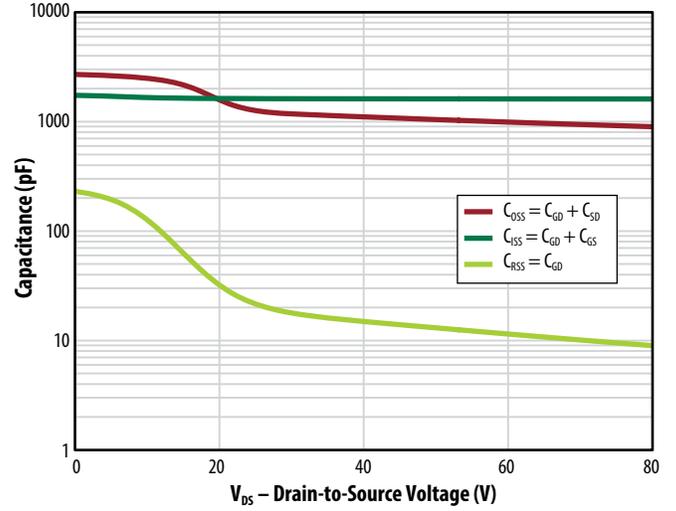
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Y-axis (left): Q_{OSS} – Output Charge (nC)
Y-axis (right): E_{OSS} – C_{OSS} Stored Energy (µJ)
X-axis: V_{DS} – Drain-to-Source Voltage (V)

Figure 7: Typical Gate Charge

$I_D = 29$ A
$V_{DS} = 40$ V
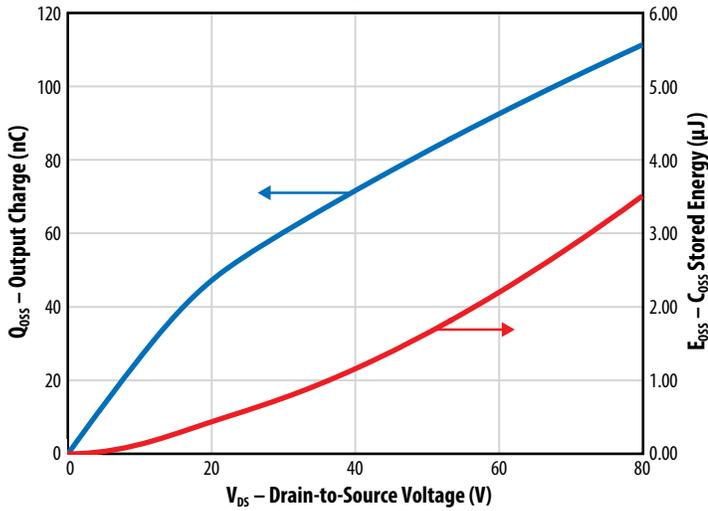
Y-axis: V_{GS} – Gate-to-Source Voltage (V)
X-axis: Q_G – Gate Charge (nC)
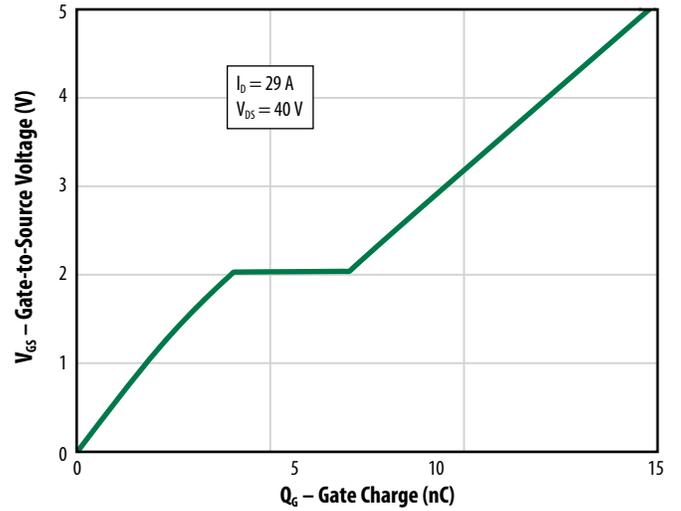
Figure 8: Typical Reverse Drain-Source Characteristics

Legend:
25°C
125°C

Y-axis: I_{SD} – Source-to-Drain Current (A)
X-axis: V_{SD} – Source-to-Drain Voltage (V)
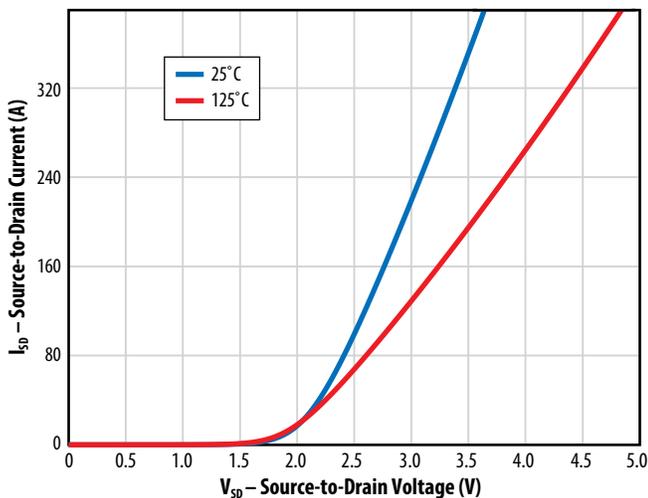
Figure 9: Typical Normalized On-State Resistance vs. Temp.

$I_D = 29$ A
$V_{GS} = 5$ V

Y-axis: Normalized On-State Resistance $R_{DS(on)}$
X-axis: T_J – Junction Temperature (°C)
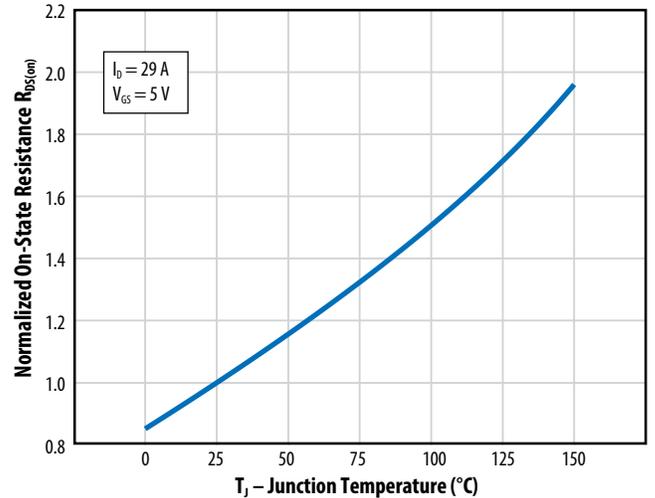
Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

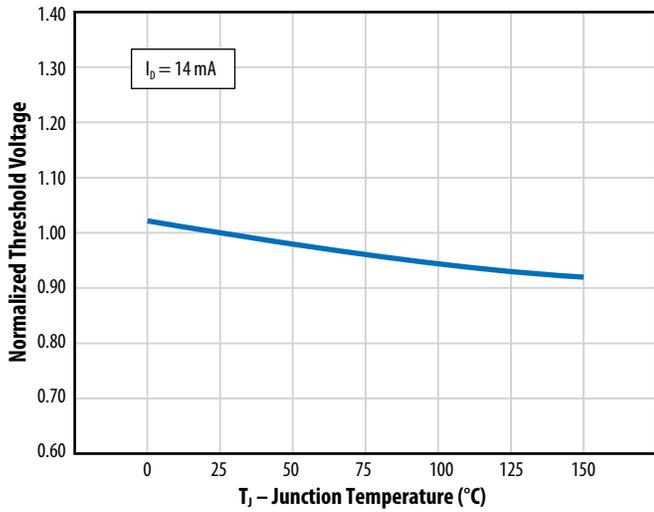## Figure 10: Typical Normalized Threshold Voltage vs. Temp.

$I_D = 14$ mA

X-axis: T_J – Junction Temperature (°C)
Y-axis: Normalized Threshold Voltage

Figure 11: Safe Operating Area

Limited by $R_{DS(on)}$

Pulse Width
1 ms
250 µs
100 µs

X-axis: V_{DS} - Drain-Source Voltage (V)
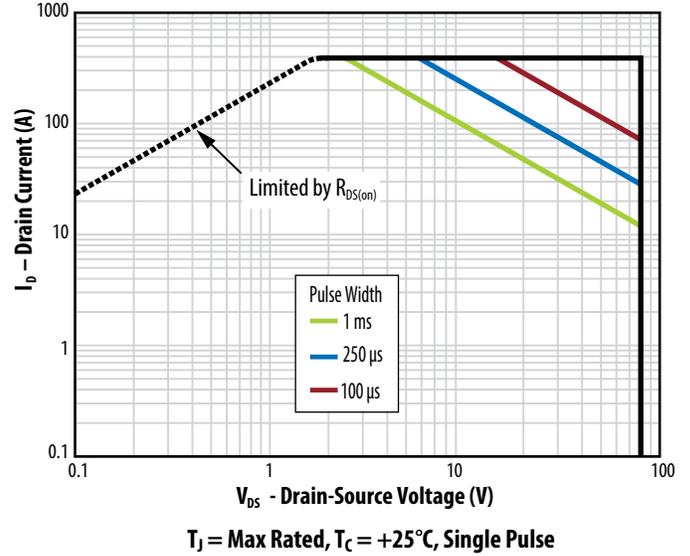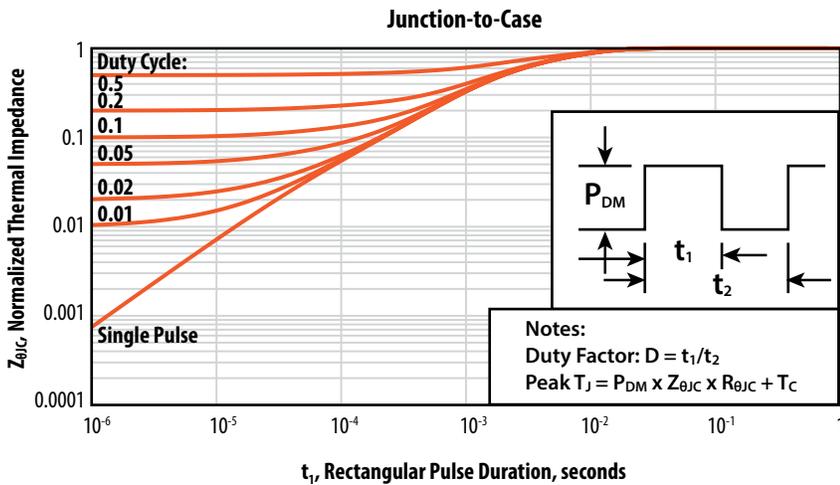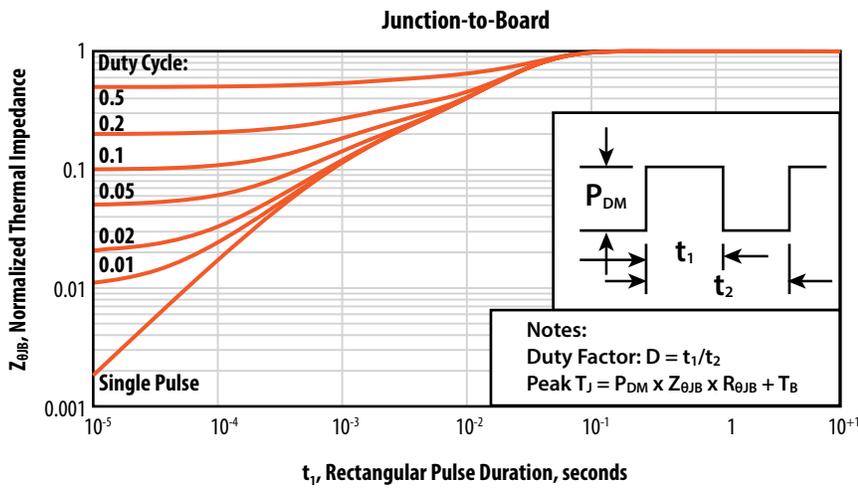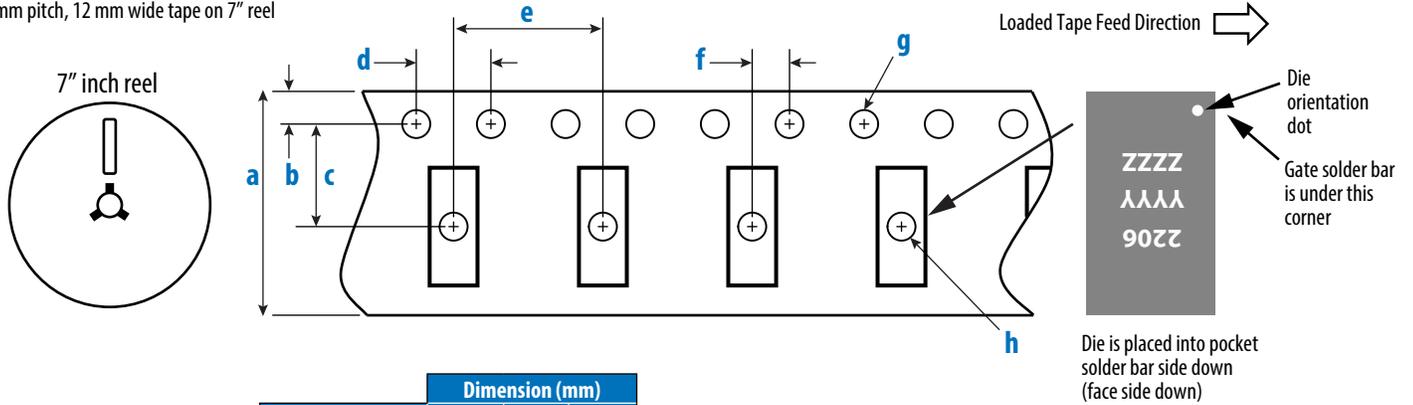Y-axis: I_D – Drain Current (A)

T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Typical Transient Thermal Response Curves

Junction-to-Board

Duty Cycle:
0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

P_{DM}
t_1
t_2

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Y-axis: $Z_{\theta JB}$, Normalized Thermal Impedance
X-axis: t_1, Rectangular Pulse Duration, seconds

Junction-to-Case

Duty Cycle:
0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

P_{DM}
t_1
t_2

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Y-axis: $Z_{\theta JC}$, Normalized Thermal Impedance
X-axis: t_1, Rectangular Pulse Duration, seconds

TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

7" inch reel

Loaded Tape Feed Direction

Die orientation dot

Gate solder bar is under this corner

Die is placed into pocket solder bar side down (face side down)

EPC2206 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS

2206
YYYY
ZZZZ

Die orientation dot

Gate Pad bar is under this corner
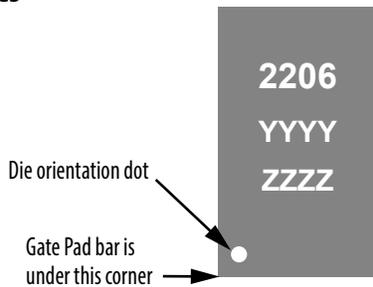
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2206	2206	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View

Side View

Seating plane
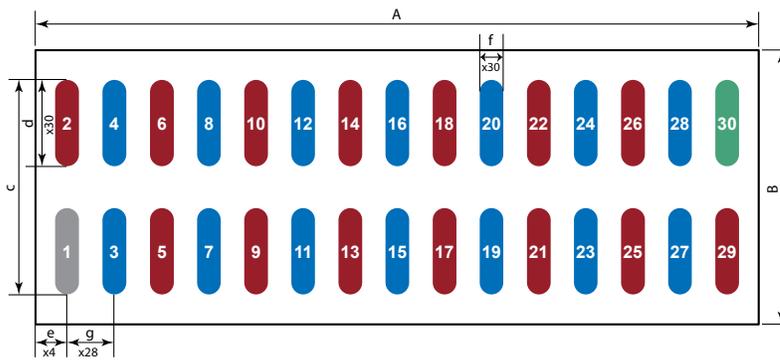
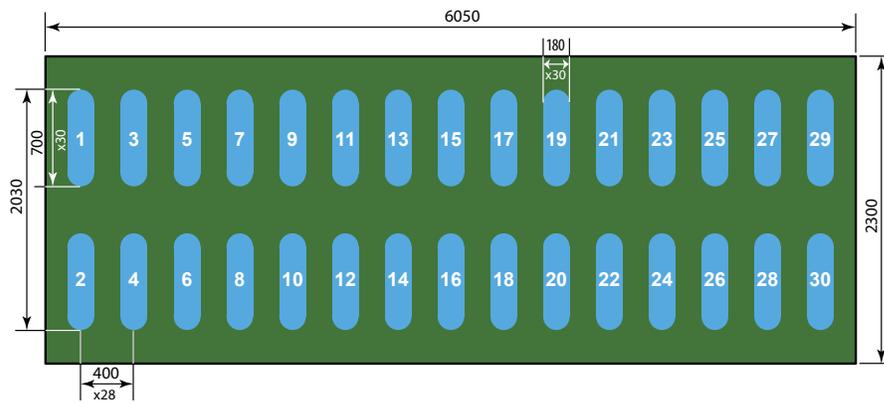| DIM	Micrometers		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400
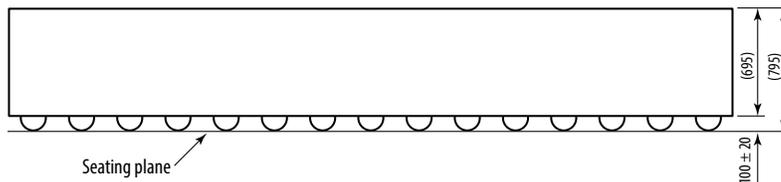
Pad 1 is Gate;

Pads 2 ,5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29 are Source;

Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain;

Pad 30 is Substrate.*

*Substrate pin should be connected to Source
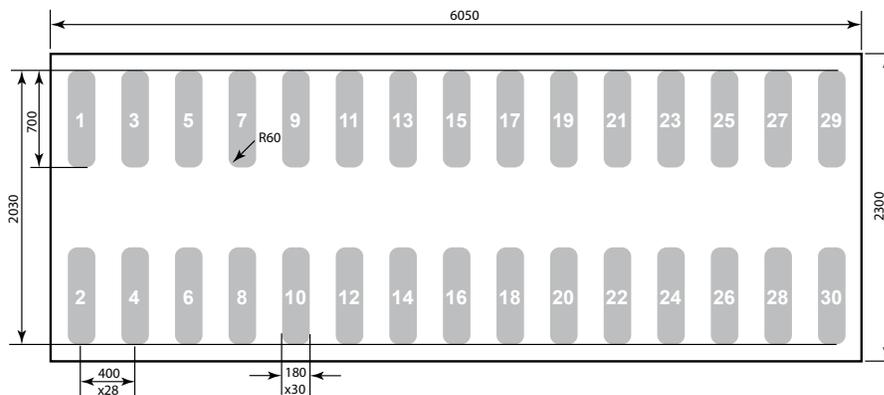
RECOMMENDED LAND PATTERN
(units in µm)

Land pattern is solder mask defined.

Pad 1 is Gate;
Pads 2, 5, 6, 9,10,13,14, 17, 18, 21, 22, 25, 26, 29 are Source;
Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain;
Pad 30 is Substrate.*

*Substrate pin should be connected to Source

Solder mask
(for solder mask defined pads)

RECOMMENDED STENCIL DRAWING
(units in µm)

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

TYPICAL THERMAL CONCEPT

The EPC2206 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs.

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.
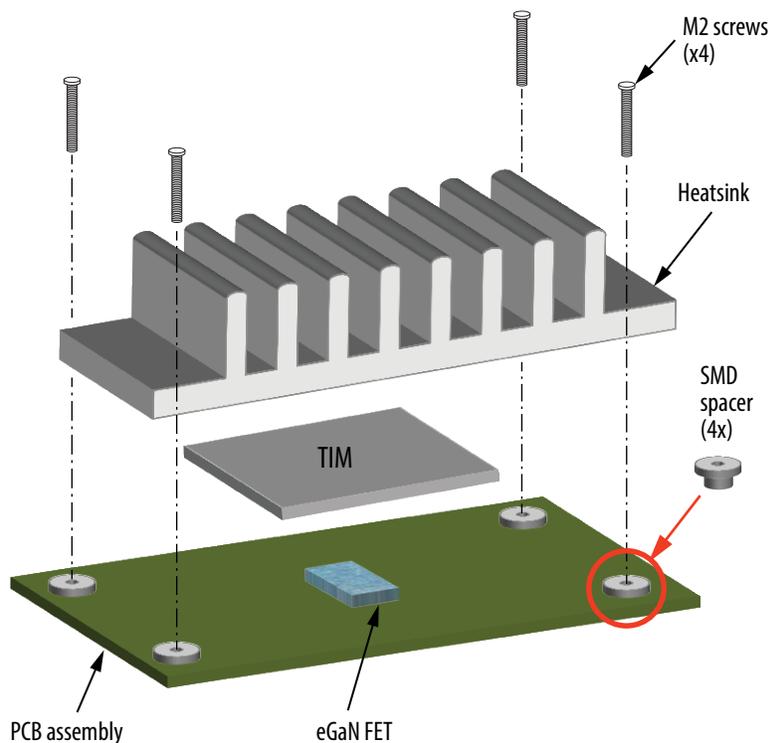

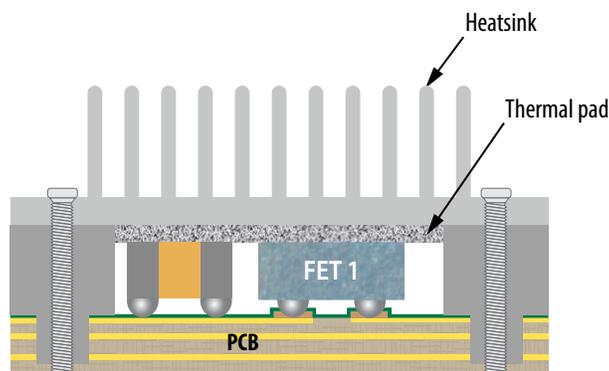*Figure 13: Exploded view of heatsink assembly using screws*

Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the *GaN FET Thermal Calculator* on EPC's website.

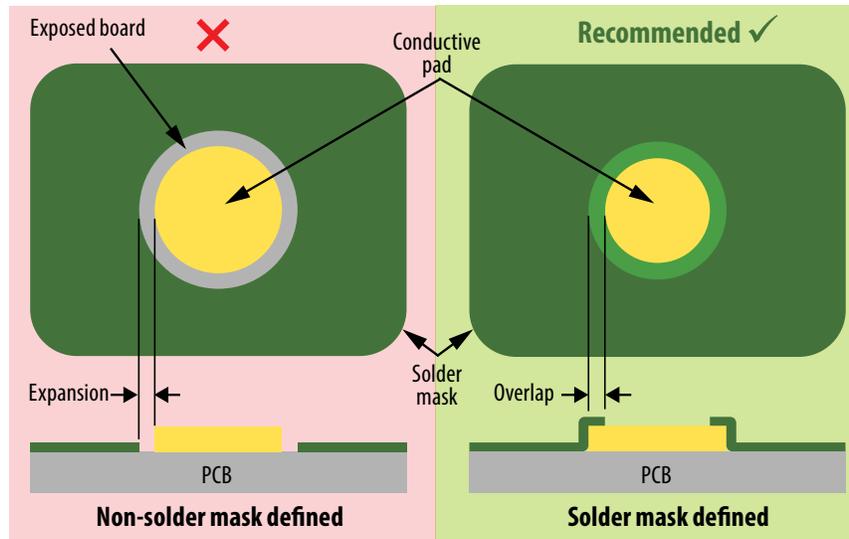Solder mask defined pads are recommended for best reliability.

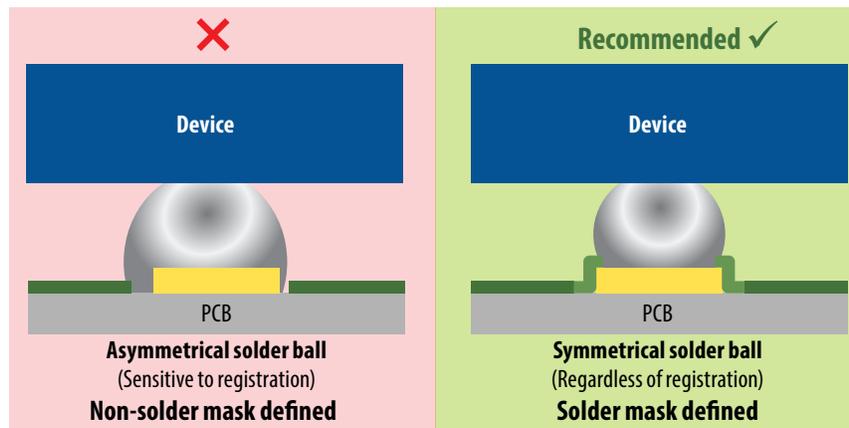*Figure 15: Solder mask defined versus non-solder mask defined pad*

Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip** (for preliminary device Altium footprints, contact EPC)