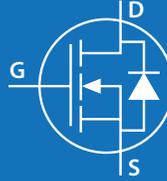


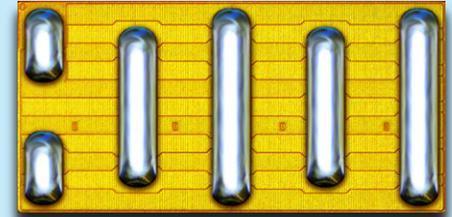
# EPC2059 – Enhancement Mode Power Transistor

 $V_{DS}, 170\text{ V}$ 
 $R_{DS(on)}, 9\text{ m}\Omega$ 
 $I_D, 24\text{ A}$ 


Revised October 28, 2020

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:  
Ask a GaN  
Expert



Die Size: 2.8 x 1.4 mm

EPC2059 eGaN® FETs are supplied only in passivated die form with solder bars.

## Applications

- DC-DC Converters
- Sync rectification for AC/DC & DC-DC
- USB-C PD quick chargers and adaptors
- BLDC motor drives
- Lidar
- Class-D audio

## Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low  $Q_G$
- Small footprint

Maximum Ratings			
PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	170	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	24	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300\ \mu\text{s}$ )	102	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.9	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	3	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	63	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$ , $I_D = 0.15\text{ mA}$	170			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0\text{ V}$ , $V_{DS} = 136\text{ V}$		0.03	0.1	mA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.01	2.4	
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5\text{ V}$ , $T_J = 125^\circ\text{C}$		0.13	5.5	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.03	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 3\text{ mA}$	0.7	1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 10\text{ A}$		6.8	9	$\text{m}\Omega$
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$		1.6		V

<sup>#</sup> Defined by design. Not subject to production test.

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2059>

Dynamic Characteristics<sup>#</sup> (T<sub>j</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 85 V, V <sub>GS</sub> = 0 V		633	836	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			1.6		
C <sub>OSS</sub>	Output Capacitance			267	401	
C <sub>OSS(ER)</sub>	Effective Output Capacitance, Energy Related (Note 2)	V <sub>DS</sub> = 0 to 85 V, V <sub>GS</sub> = 0 V		332		
C <sub>OSS(TR)</sub>	Effective Output Capacitance, Time Related (Note 3)			414		
R <sub>G</sub>	Gate Resistance			0.5		Ω
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 85 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 10 A		5.7	7.4	nC
Q <sub>GS</sub>	Gate-to-Source Charge	V <sub>DS</sub> = 85 V, I <sub>D</sub> = 10 A		1.3		
Q <sub>GD</sub>	Gate-to-Drain Charge			0.9		
Q <sub>G(TH)</sub>	Gate Charge at Threshold			1.0		
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 85 V, V <sub>GS</sub> = 0 V		35	53	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

# Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C<sub>OSS(ER)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Note 3: C<sub>OSS(TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Figure 1: Typical Output Characteristics at 25°C

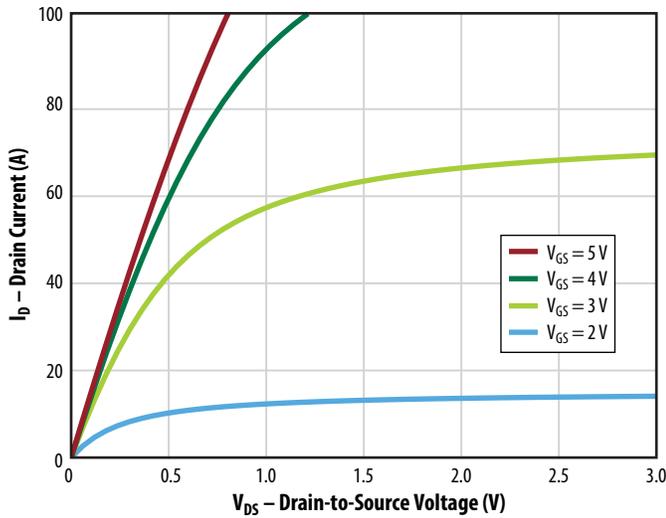


Figure 2: Typical Transfer Characteristics

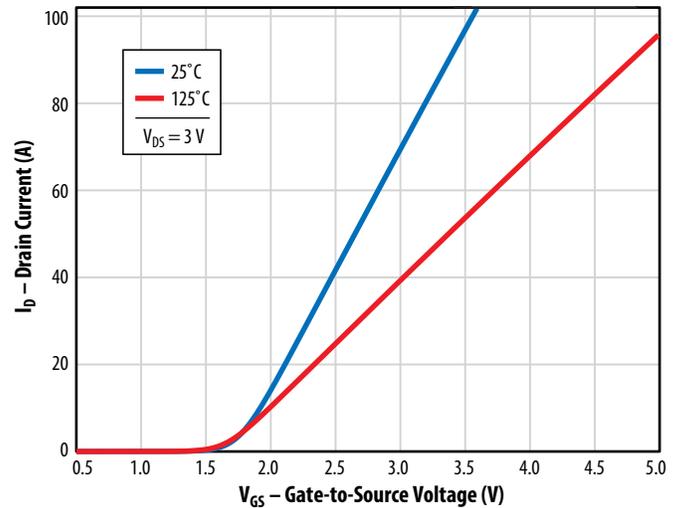


Figure 3: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Drain Currents

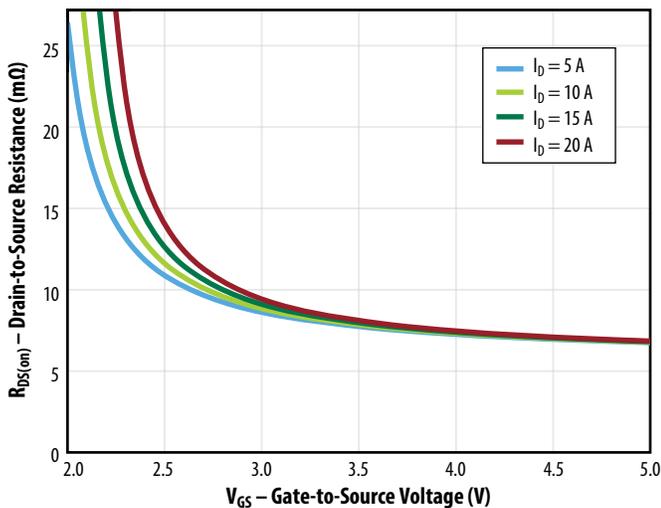


Figure 4: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Temperatures

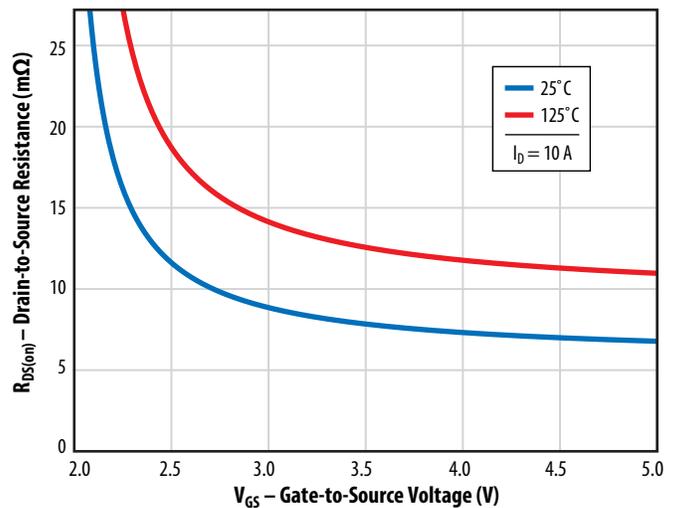


Figure 5a: Typical Capacitance (Linear Scale)

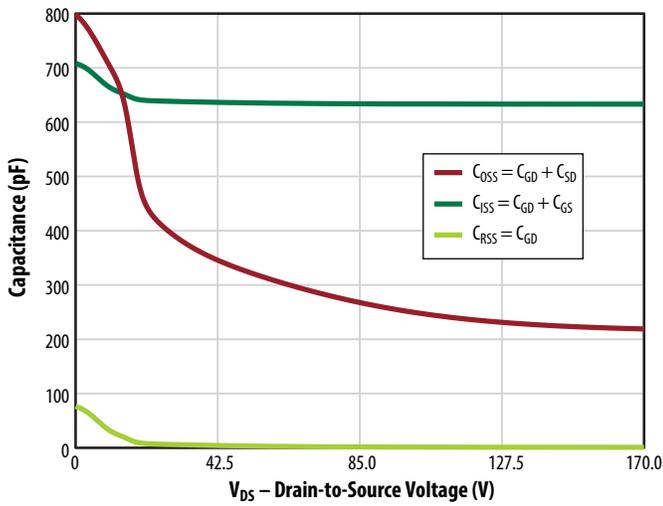


Figure 5b: Typical Capacitance (Log Scale)

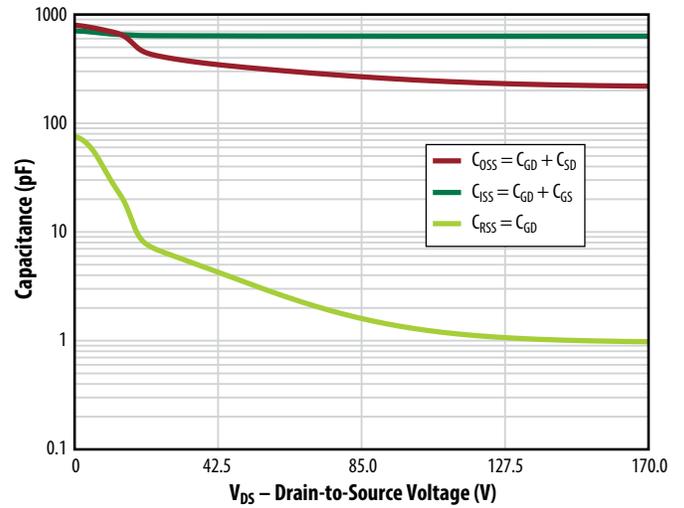


Figure 6: Typical Output Charge and C\_OSS Stored Energy

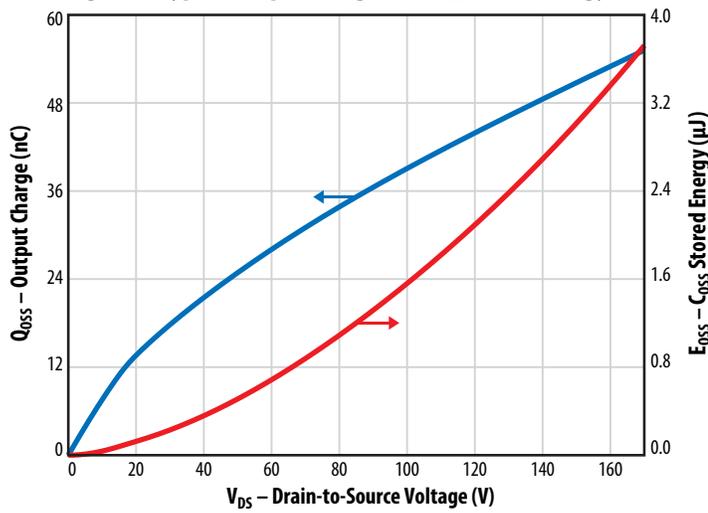


Figure 7: Typical Gate Charge

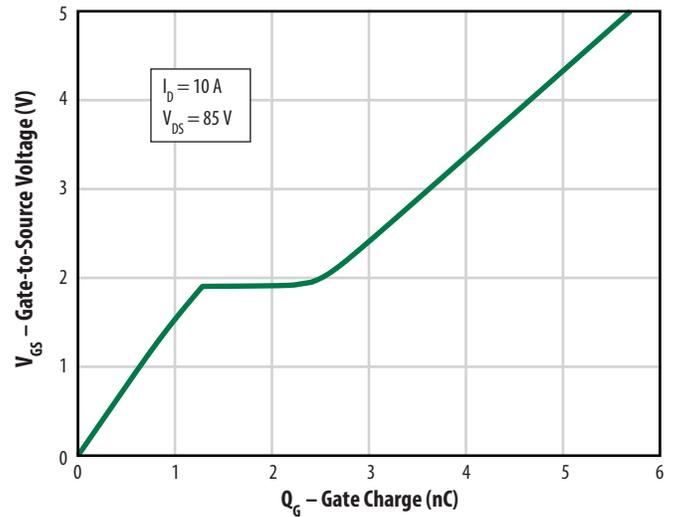


Figure 8: Typical Reverse Drain-Source Characteristics

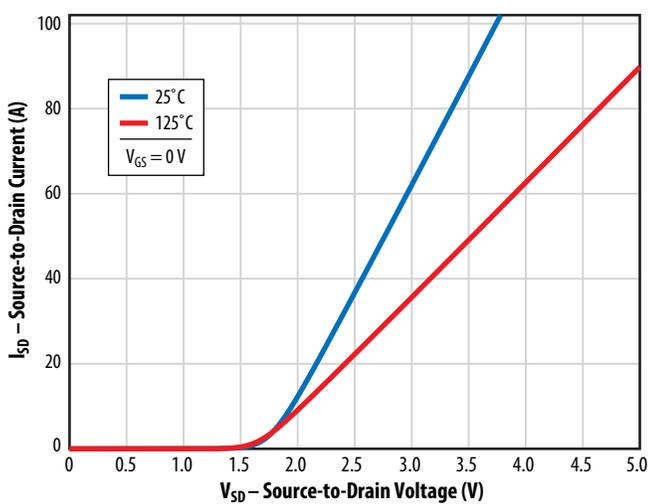
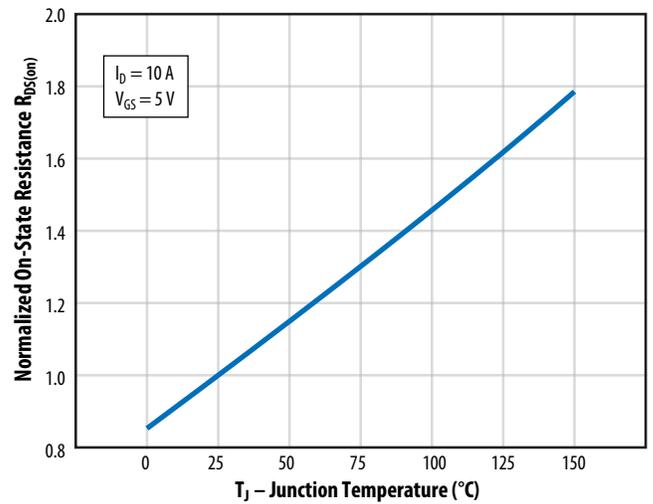


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

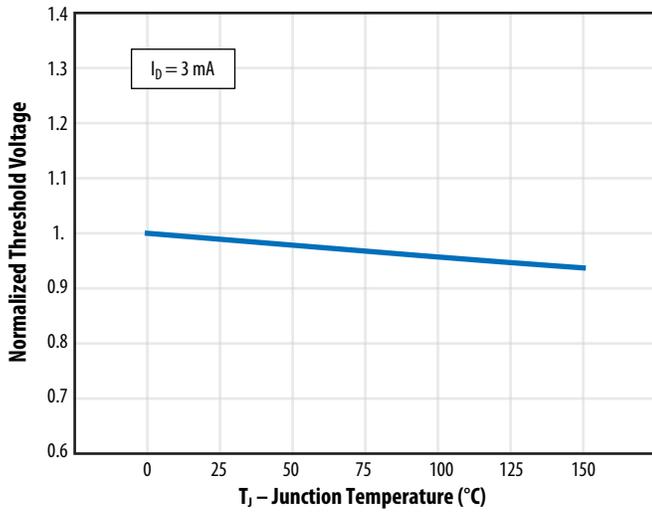


Figure 11: Safe Operating Area

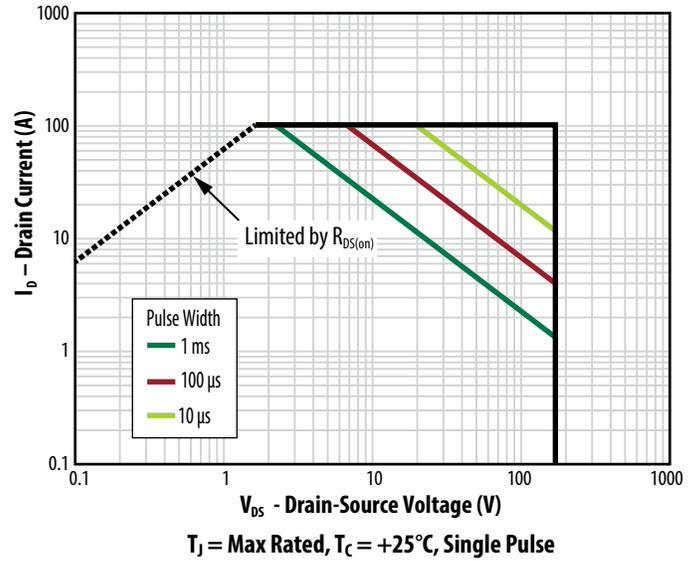
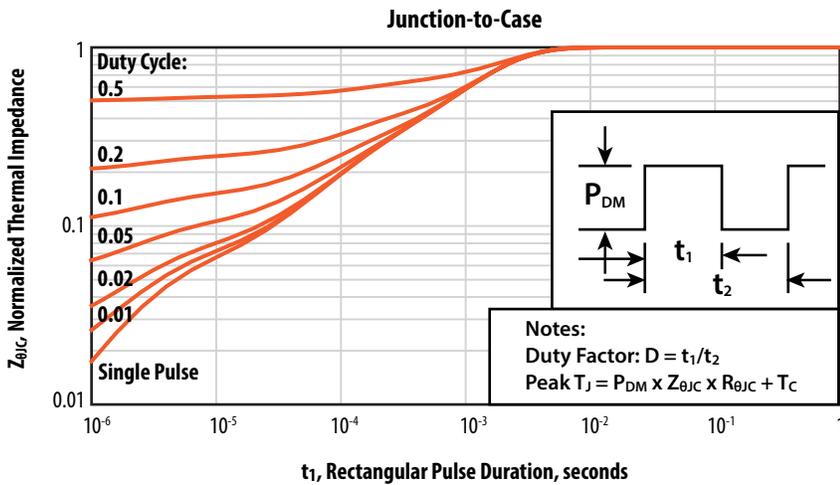
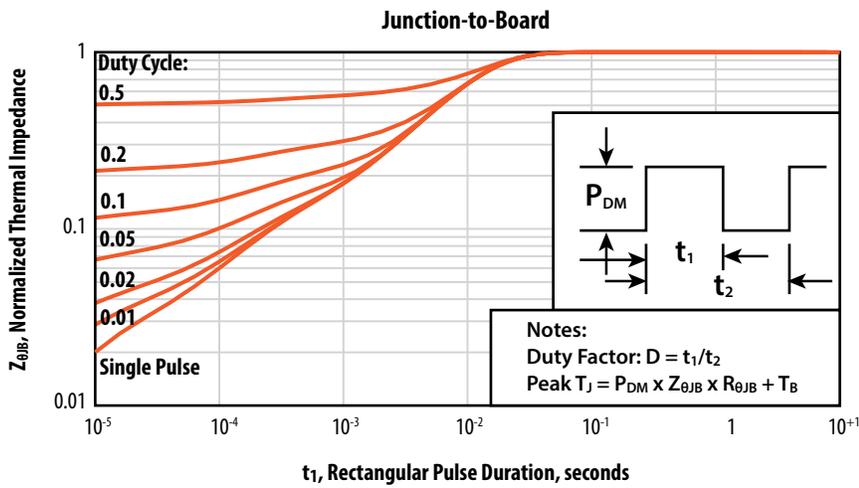
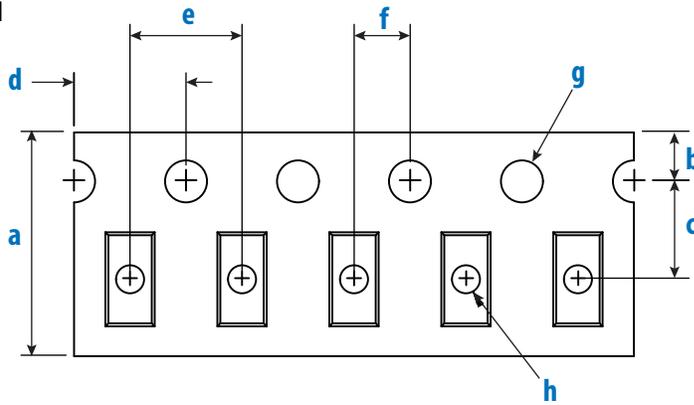
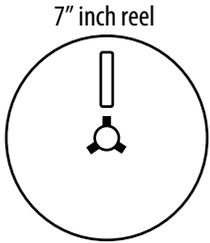


Figure 12: Typical Transient Thermal Response Curves



**TAPE AND REEL CONFIGURATION**

4 mm pitch, 8 mm wide tape on 7" reel



Loaded Tape Feed Direction →



Die orientation dot  
Gate solder bar is under this corner

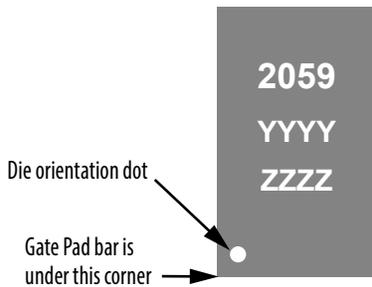
Die is placed into pocket solder bar side down (face side down)

EPC2059 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.00	0.95	1.05

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

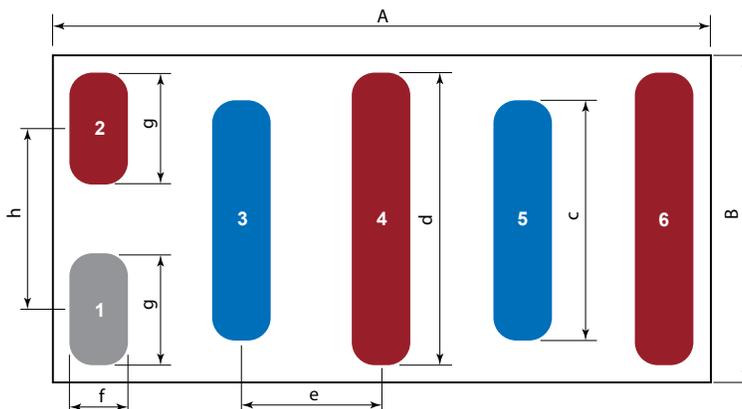
**DIE MARKINGS**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2059	2059	YYYY	ZZZZ

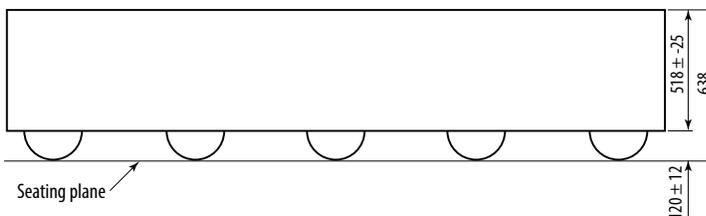
**DIE OUTLINE**

Solder Bump View



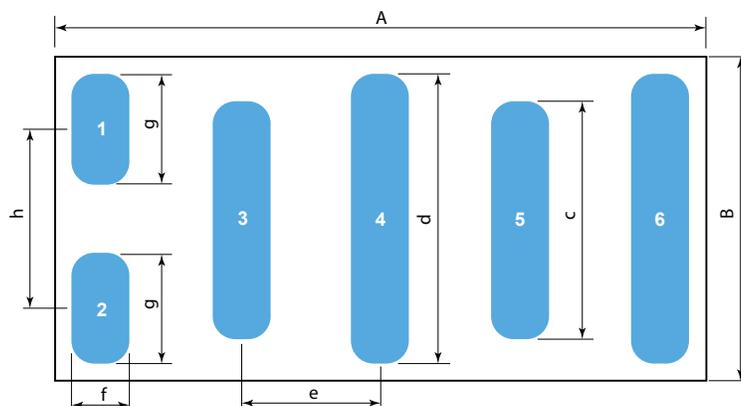
DIM	Micrometers		
	MIN	Nominal	MAX
A	2770	2800	2830
B	1370	1400	1430
c		1010	
d		1250	
e		600	
f		250	
g		475	
h		775	

Side View



Pad 1 is Gate;  
Pads 2, 4, 6 are Source;  
Pads 3, 5 are Drain

**RECOMMENDED LAND PATTERN**  
(units in  $\mu\text{m}$ )

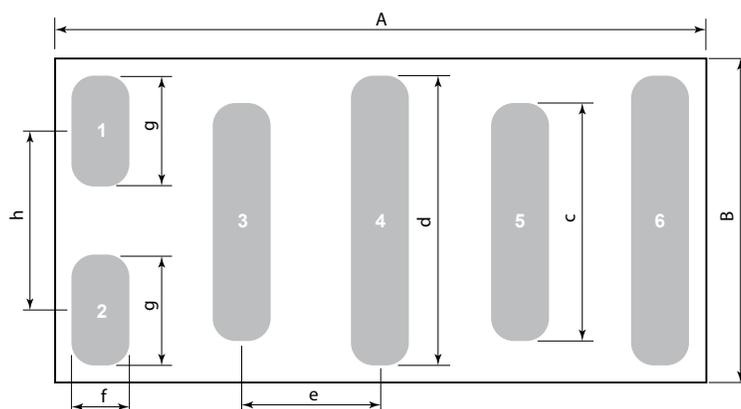


Land pattern is solder mask defined.

Pad 1 is Gate;  
Pads 2, 4, 6  
are Source;  
Pads 3, 5 are Drain

DIM	Nominal
<b>A</b>	2800
<b>B</b>	1400
<b>c</b>	1010
<b>d</b>	1250
<b>e</b>	600
<b>f</b>	250
<b>g</b>	475
<b>h</b>	775

**RECOMMENDED STENCIL DRAWING**  
(units in  $\mu\text{m}$ )



DIM	Nominal
<b>A</b>	2800
<b>B</b>	1400
<b>c</b>	1010
<b>d</b>	1250
<b>e</b>	600
<b>f</b>	250
<b>g</b>	475
<b>h</b>	775

Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at <https://epc-co.com/epc/design-support>

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