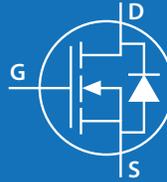# EPC2055 – Enhancement Mode Power Transistor

V_{DS} , 40 V
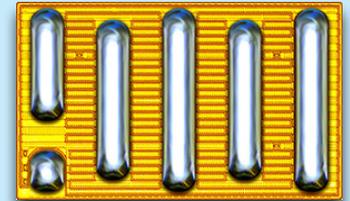
$R_{DS(on)}$, 4.2 mΩ

I_D , 29 A

RoHS   **Halogen-Free**

Revised June 20, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN Expert

Die Size: 2.5 x 1.5 mm

EPC2055 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC converters
- Isolated DC-DC converters
- Sync rectification
- High frequency (2 MHz) ultra-thin point of load converters with input 12 V – 24 V
- Lidar
- USB-C battery chargers
- LED lighting
- 12 V – 24 V input motor drivers

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	48	
I_D	Continuous (T_A = 25℃)	29	A
	Pulsed (25℃, T_{PULSE} = 300 µs)	161	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25℃ unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.5 mA	40			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 32 V		0.01	0.4	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	1.6	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125℃		0.1	5	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.01	0.4	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 7 mA	0.7	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 15 A		3	4.2	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.9		V

Defined by design. Not subject to production test.

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2055

Dynamic Characteristics# ($T_J = 25°C$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 20\,V, V_{GS} = 0\,V$		841	1254	pF
C_{RSS}	Reverse Transfer Capacitance			8.8		
C_{OSS}	Output Capacitance			408	612	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0$ to $20\,V, V_{GS} = 0\,V$		574		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			668		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	$V_{DS} = 20\,V, V_{GS} = 5\,V, I_D = 15\,A$		6.6	8.5	nC
Q_{GS}	Gate-to-Source Charge			2.3		
Q_{GD}	Gate-to-Drain Charge	$V_{DS} = 20\,V, I_D = 15\,A$		0.7		
$Q_{G(TH)}$	Gate Charge at Threshold			1.6		
Q_{OSS}	Output Charge	$V_{DS} = 20\,V, V_{GS} = 0\,V$		13	20	
Q_{RR}	Source-Drain Recovery Charge			0		

\# Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

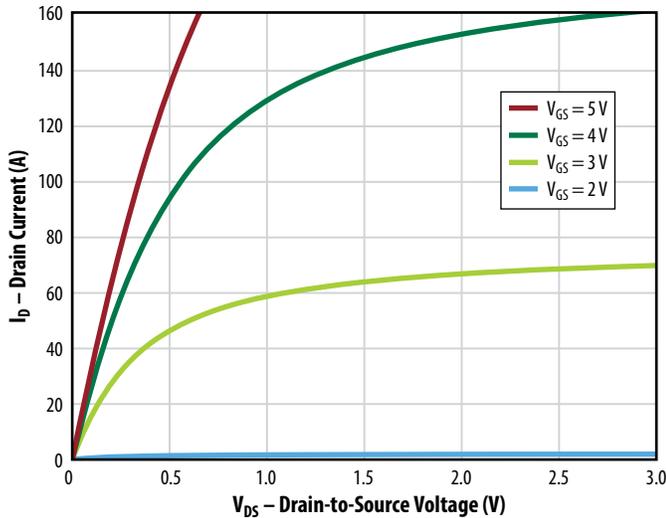### Figure 1: Typical Output Characteristics at 25°C

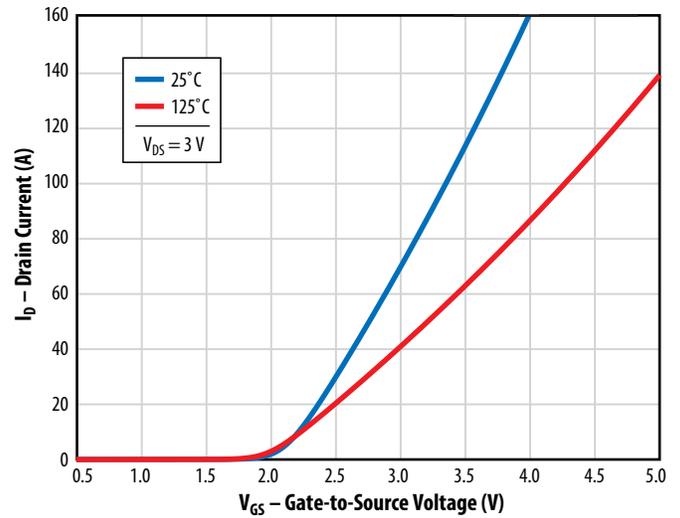### Figure 2: Typical Transfer Characteristics

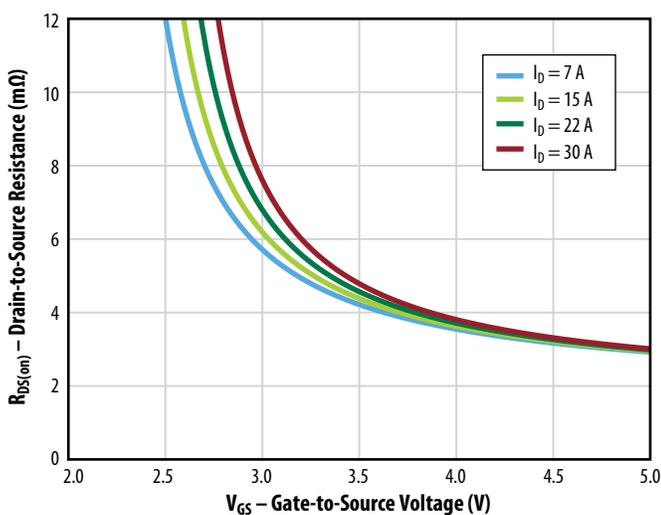### Figure 3: Typical R$_{DS(on)}$ vs. V$_{GS}$ for Various Drain Currents

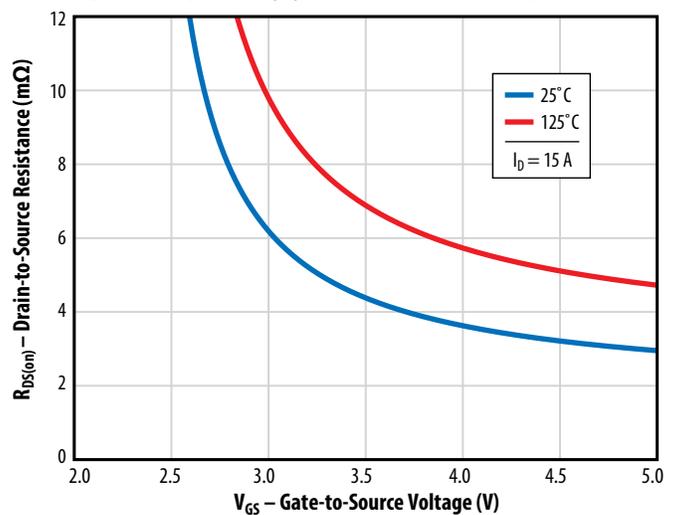### Figure 4: Typical R$_{DS(on)}$ vs. V$_{GS}$ for Various Temperatures
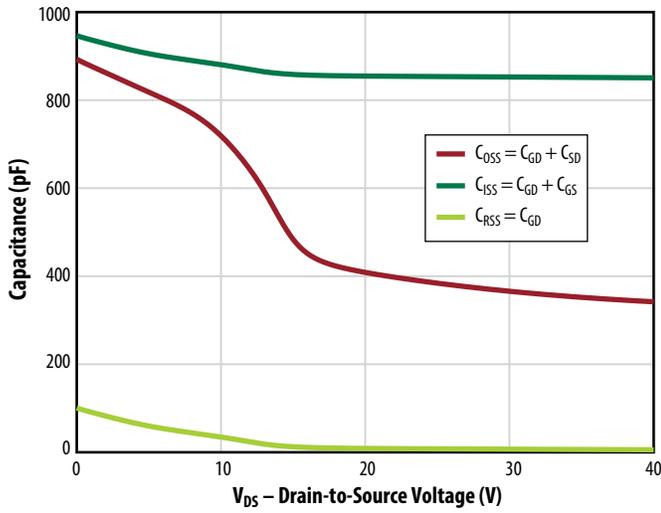
Figure 5a: Typical Capacitance (Linear Scale)

Legend:
$C_{OSS} = C_{GD} + C_{SD}$
$C_{ISS} = C_{GD} + C_{GS}$
$C_{RSS} = C_{GD}$

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Y-axis: Capacitance (pF)

Figure 5b: Typical Capacitance (Log Scale)

Legend:
$C_{OSS} = C_{GD} + C_{SD}$
$C_{ISS} = C_{GD} + C_{GS}$
$C_{RSS} = C_{GD}$

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Y-axis: Capacitance (pF)
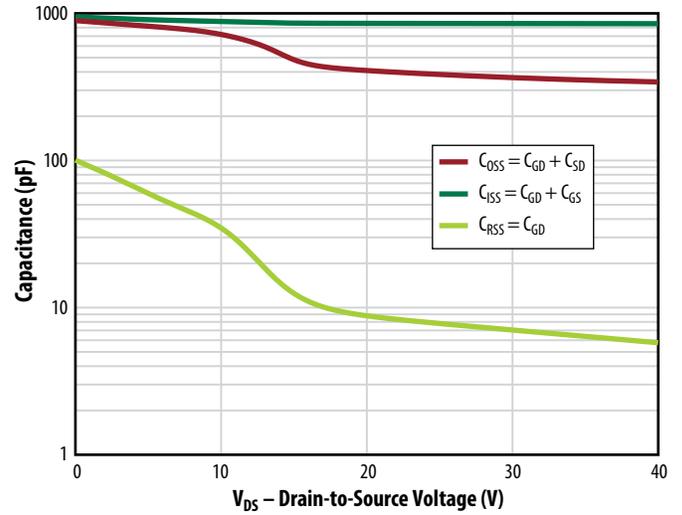
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Left Y-axis: Q_{OSS} – Output Charge (nC)
Right Y-axis: E_{OSS} – C_{OSS} Stored Energy (µJ)
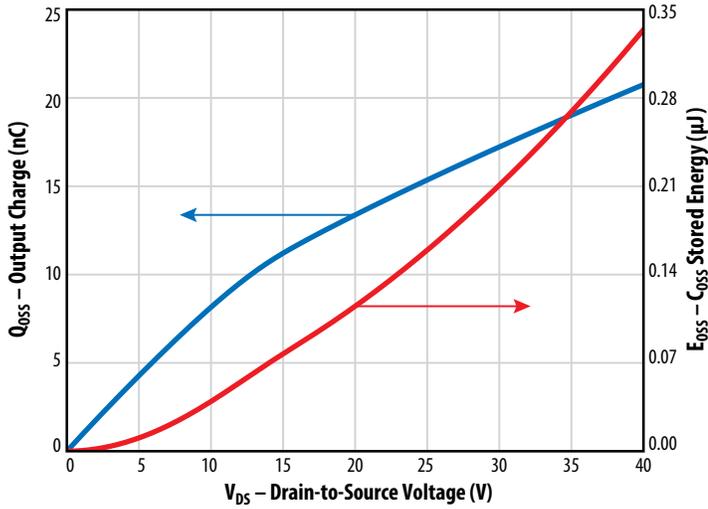
Figure 7: Typical Gate Charge

$I_D = 15\ A$
$V_{DS} = 20\ V$

X-axis: Q_G – Gate Charge (nC)
Y-axis: V_{GS} – Gate-to-Source Voltage (V)
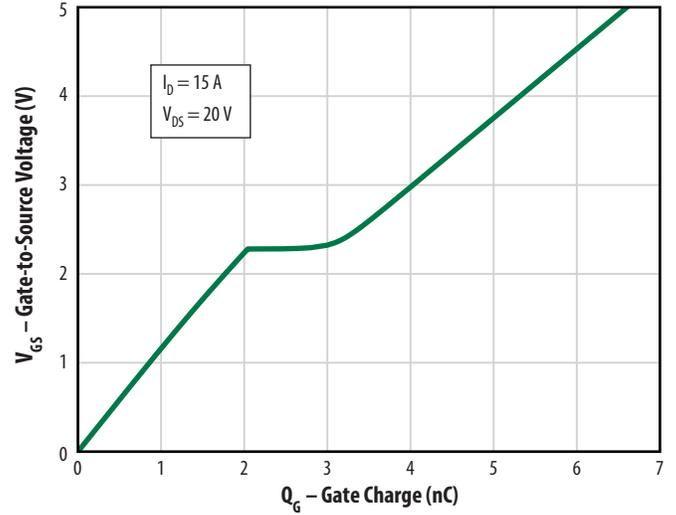
Figure 8: Typical Reverse Drain-Source Characteristics

Legend:
25°C
125°C
$V_{GS} = 0\ V$

X-axis: V_{SD} – Source-to-Drain Voltage (V)
Y-axis: I_{SD} – Source-to-Drain Current (A)

Figure 9: Typical Normalized On-State Resistance vs. Temp.

$I_D = 15\ A$
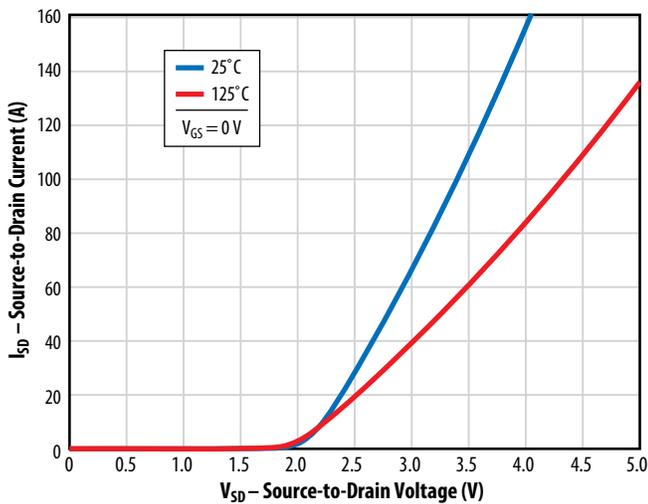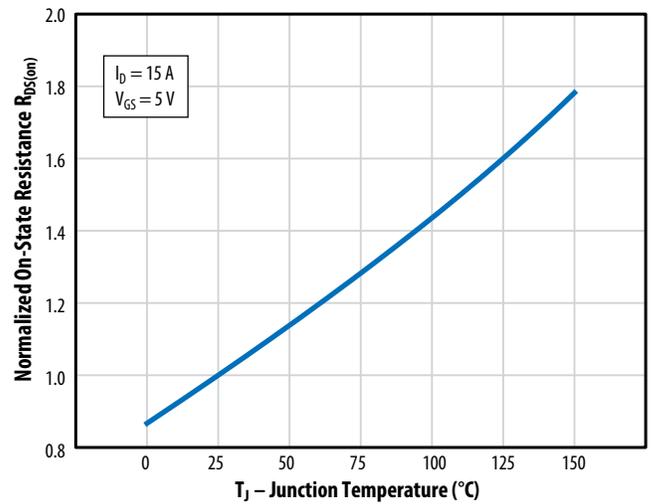$V_{GS} = 5\ V$

X-axis: T_J – Junction Temperature (°C)
Y-axis: Normalized On-State Resistance $R_{DS(on)}$

Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

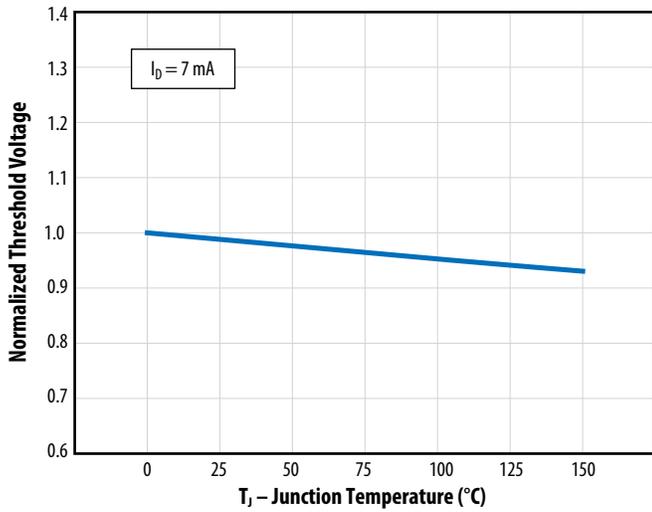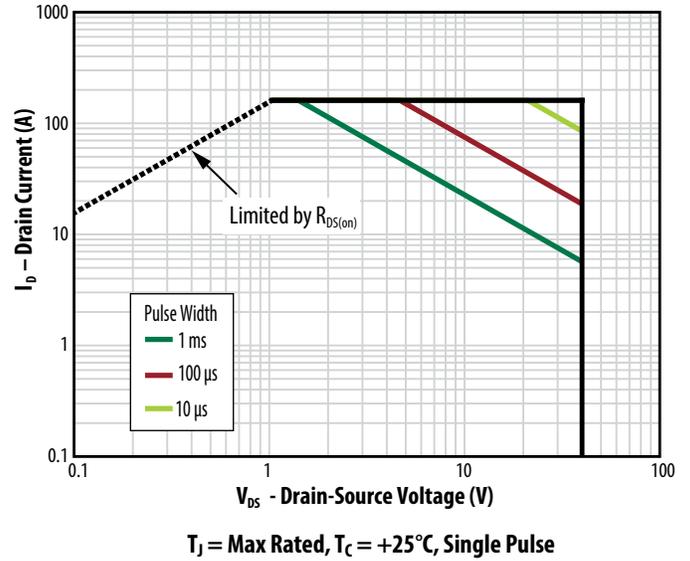### Figure 10: Typical Normalized Threshold Voltage vs. Temp.

$I_D = 7$ mA

Figure 11: Safe Operating Area

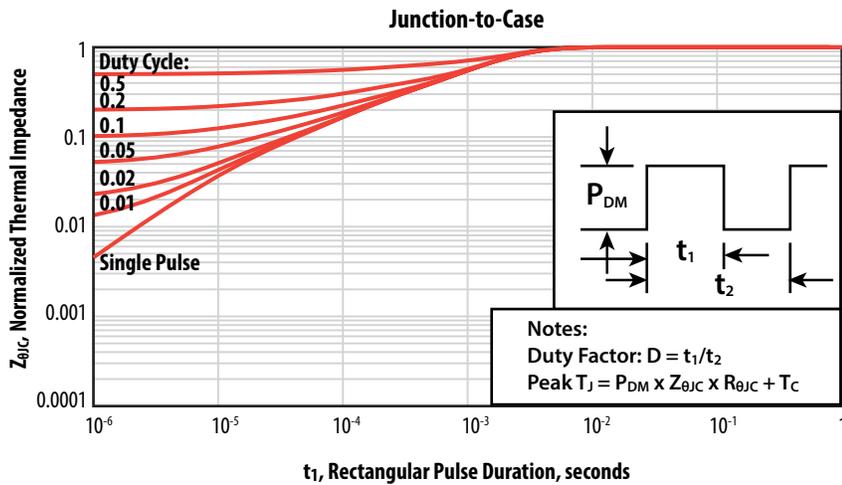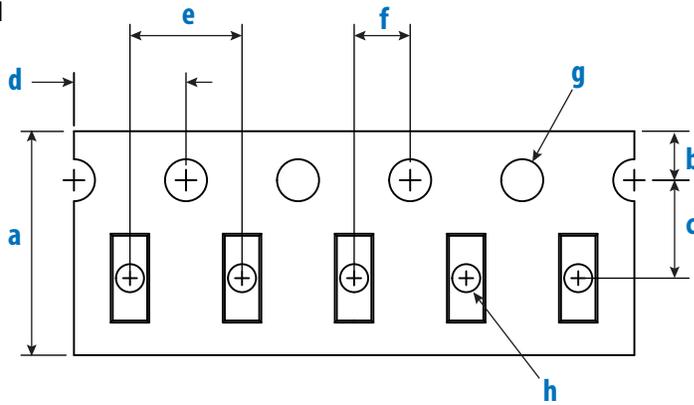Limited by $R_{DS(on)}$

Pulse Width
— 1 ms
— 100 µs
— 10 µs

T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Typical Transient Thermal Response Curves

Junction-to-Board

Duty Cycle:
0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Junction-to-Case

Duty Cycle:
0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$
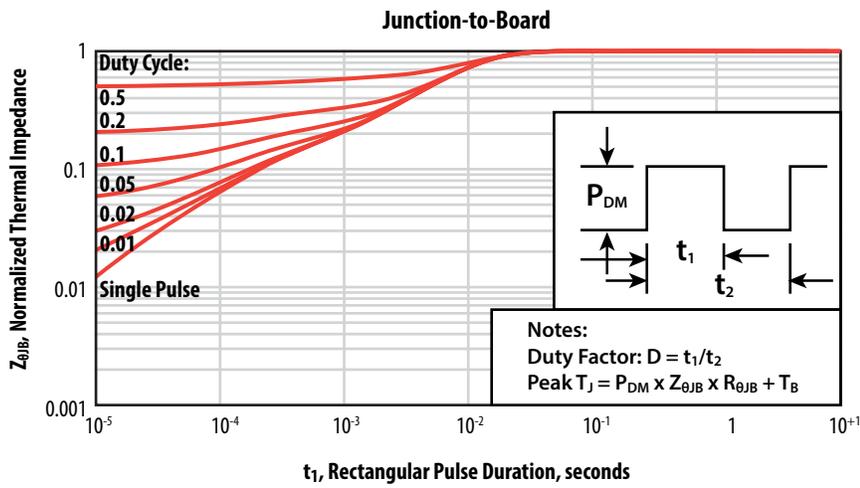
TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

7" inch reel
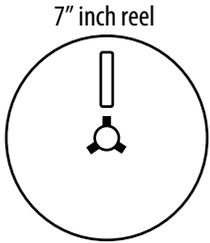
Loaded Tape Feed Direction ⇨

Die orientation dot

Gate solder bar is under this corner

Die is placed into pocket solder bar side down (face side down)

EPC2055 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.
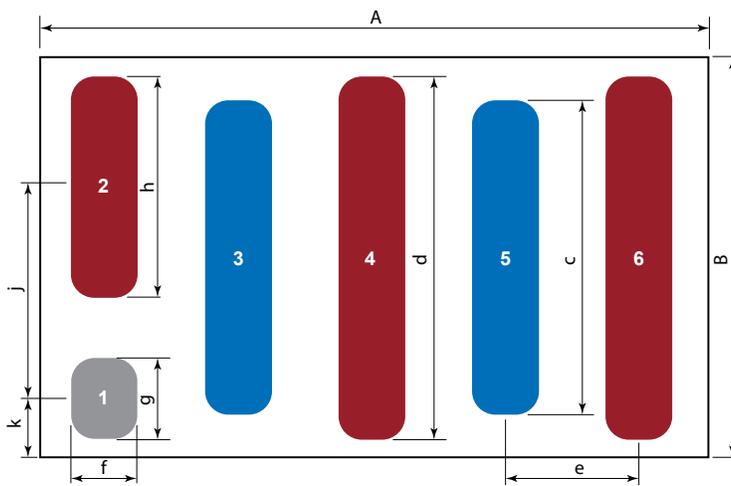
DIE MARKINGS

2055
YYYY
ZZZZ

Die orientation dot

Gate Pad bar is under this corner
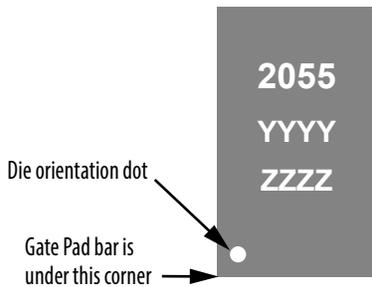
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2055	2055	YYYY	ZZZZ

DIE OUTLINE
Solder Bump View
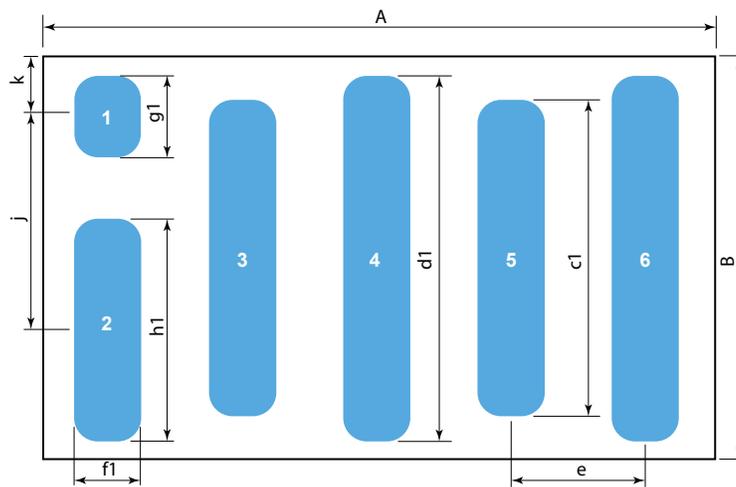
Side View

Seating plane

DIM	Micrometers		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c		1175	
d		1350	
e		500	
f		250	
g		300	
h		825	
j		787.5	
k		225	

Pad 1 is Gate;

Pads 2, 4, 6 are Source;

Pads 3, 5 are Drain

518 ± 25
638

120 ± 12
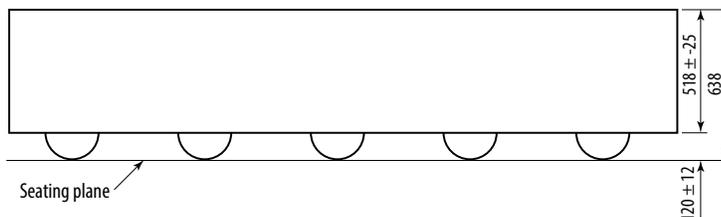
RECOMMENDED LAND PATTERN
(units in μm)

Land pattern is solder mask defined

DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5
k	225

Pad 1 is Gate;
Pads 2 ,4, 6 are Source;
Pads 3, 5 are Drain

RECOMMENDED STENCIL DRAWING
(units in μm)
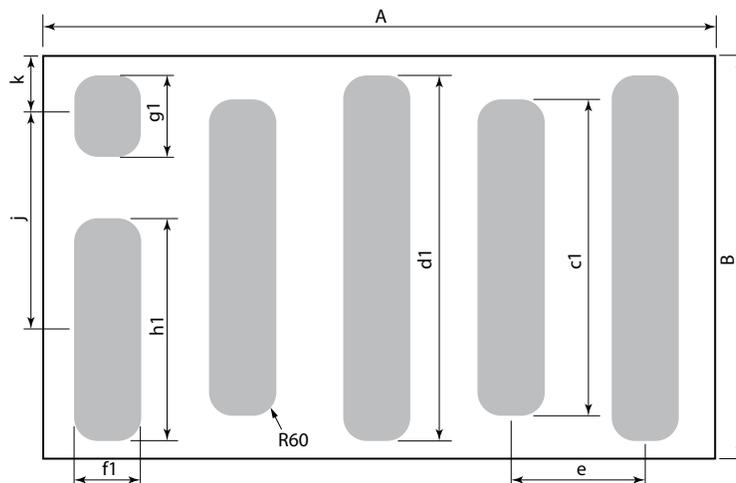
DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5
k	225

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at https://epc-co.com/epc/design-support