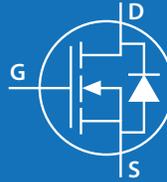


EPC2045 – Enhancement Mode Power Transistor

 $V_{DS}, 100\text{ V}$
 $R_{DS(on)}, 7\text{ m}\Omega$
 $I_D, 16\text{ A}$


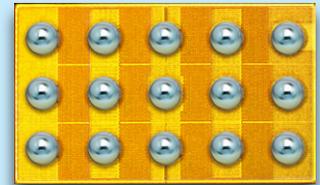
Revised February 4, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:
Ask a GaN
Expert



Die size: 2.5 x 1.5 mm

EPC2045 eGaN® FETs are supplied passivated die form with solder bumps

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	16	A
	Pulsed (25°C , $T_{PULSE} = 300\ \mu\text{s}$)	130	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	8.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 300\ \mu\text{A}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$		40	250	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.01	1.3	mA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}$, $T_J = 125^\circ\text{C}$		0.1	5	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		40	500	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 16\text{ A}$		5.6	7	m Ω
V_{SD}	Source-Drain Forward Voltage [#]	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$		1.7		V

[#] Defined by design. Not subject to production test.

Applications

- Open rack server architectures
- Lidar/pulsed power applications
- USB-C
- Isolated power supplies
- Point of load converters
- Class D audio
- Led lighting
- Low inductance motor drive

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2045>

Dynamic Characteristics[#] (T_j = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		767	1016	pF
C _{RSS}	Reverse Transfer Capacitance			3		
C _{OSS}	Output Capacitance			295	443	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 50 V, V _{GS} = 0 V		383		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			500		
R _G	Gate Resistance			0.6		Ω
Q _G	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 16 A		6	7.8	nC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 50 V, I _D = 16 A		1.9		
Q _{GD}	Gate-to-Drain Charge			0.8		
Q _{G(TH)}	Gate Charge at Threshold			1.3		
Q _{OSS}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		25	38	
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

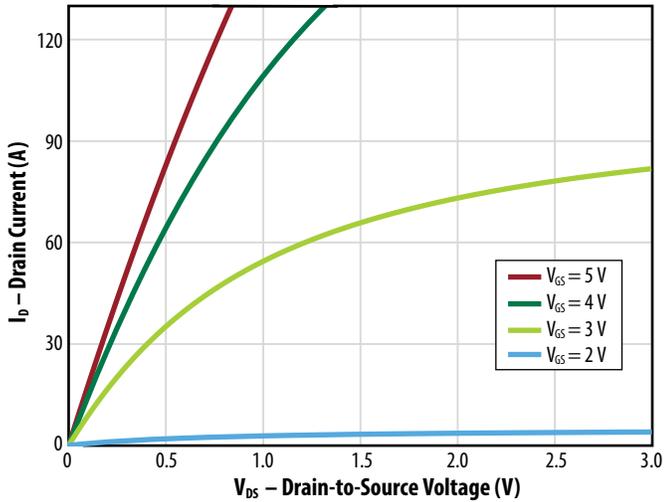


Figure 2: Typical Transfer Characteristics

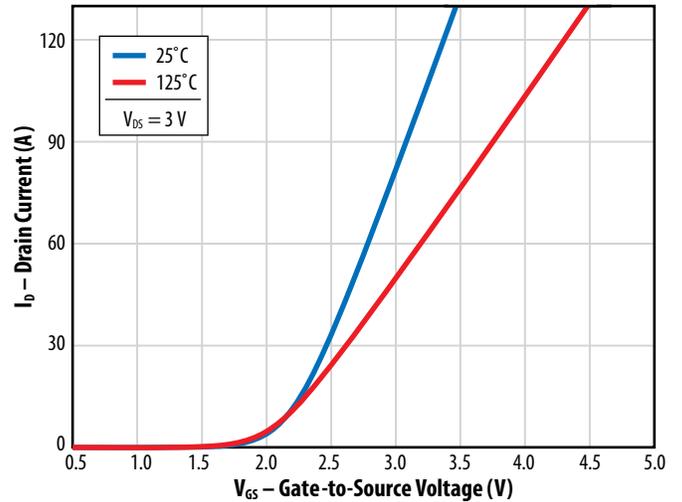


Figure 3: Typical R_{DS(on)} vs. V_{GS} for Various Drain Currents

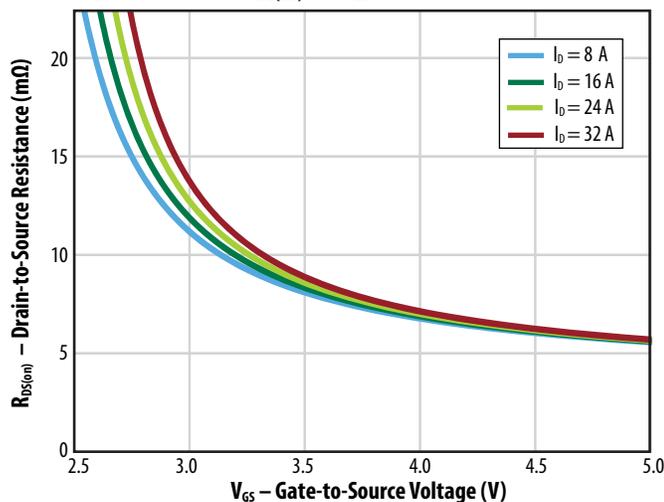


Figure 4: Typical R_{DS(on)} vs. V_{GS} for Various Temperatures

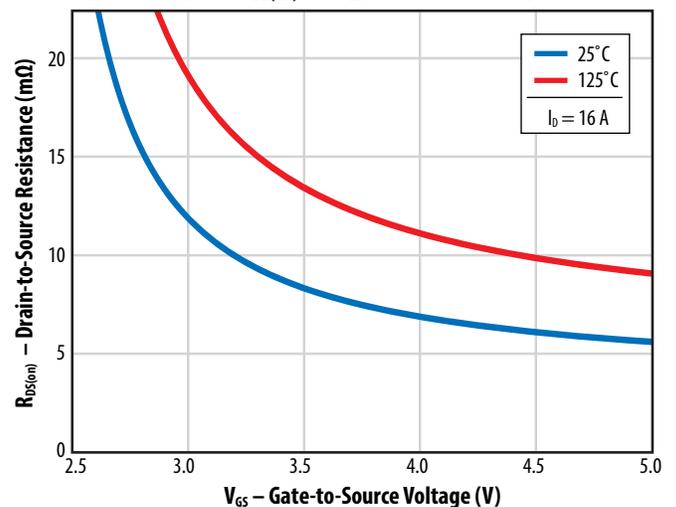


Figure 5a: Typical Capacitance (Linear Scale)

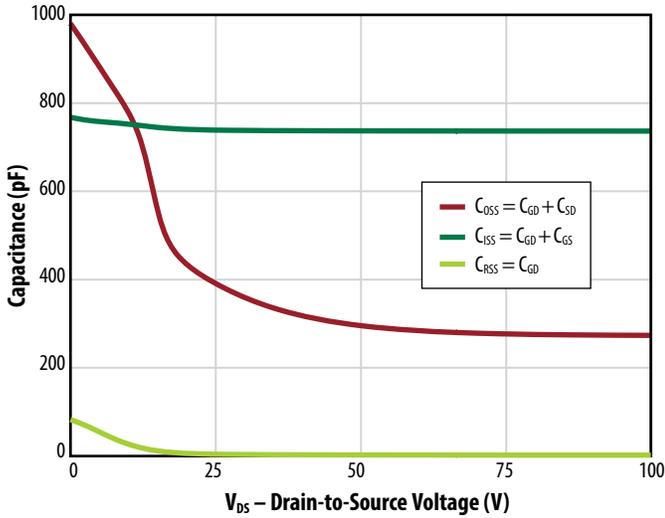


Figure 5b: Typical Capacitance (Log Scale)

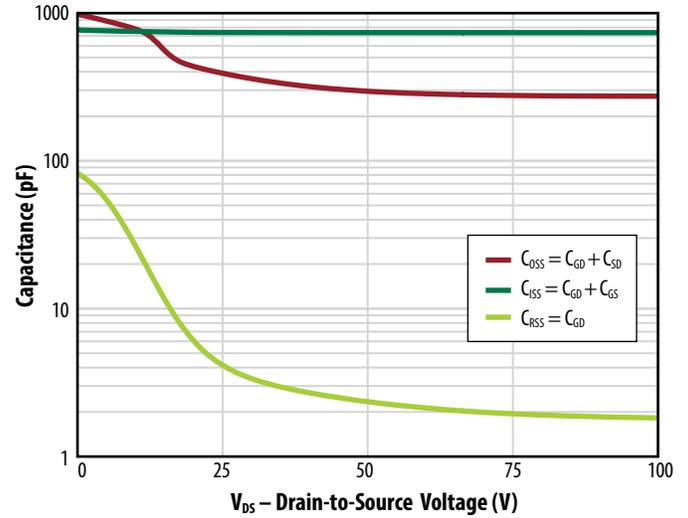


Figure 6: Typical Output Charge and C_OSS Stored Energy

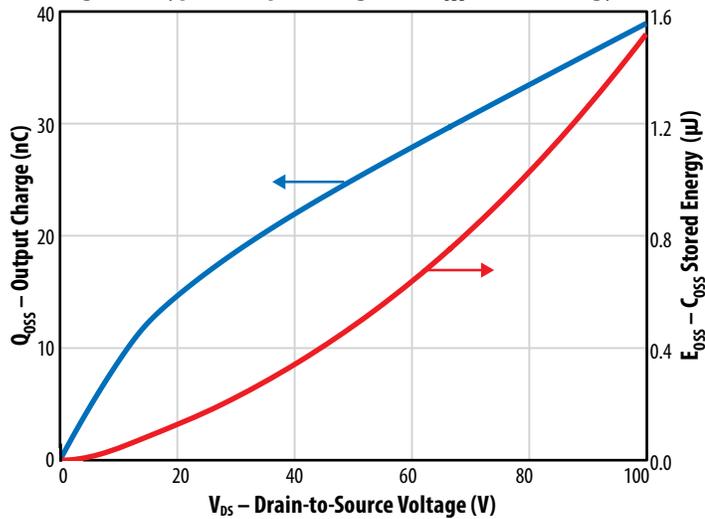


Figure 7: Typical Gate Charge

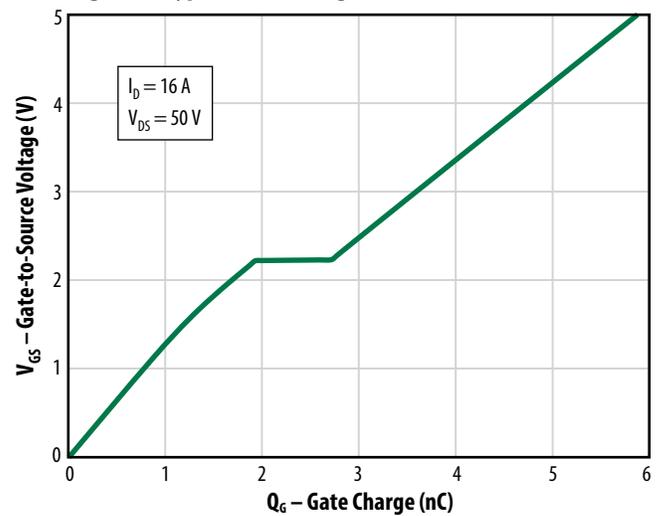


Figure 8: Typical Reverse Drain-Source Characteristics

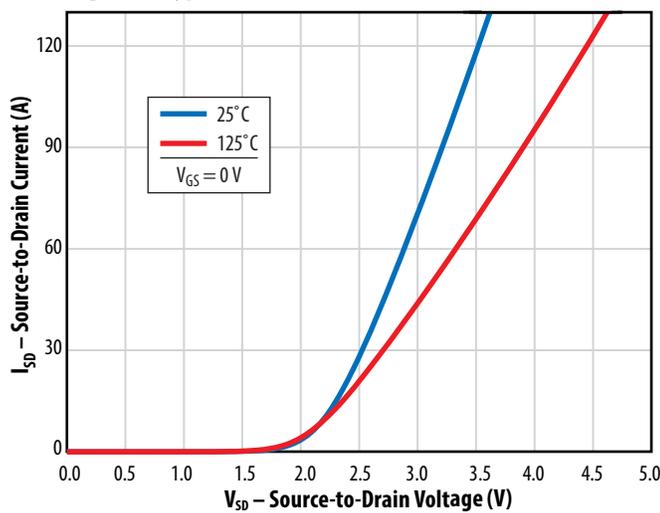
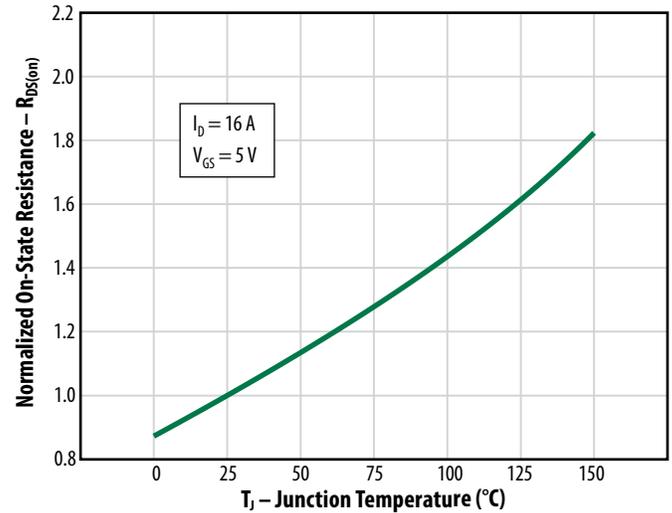


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

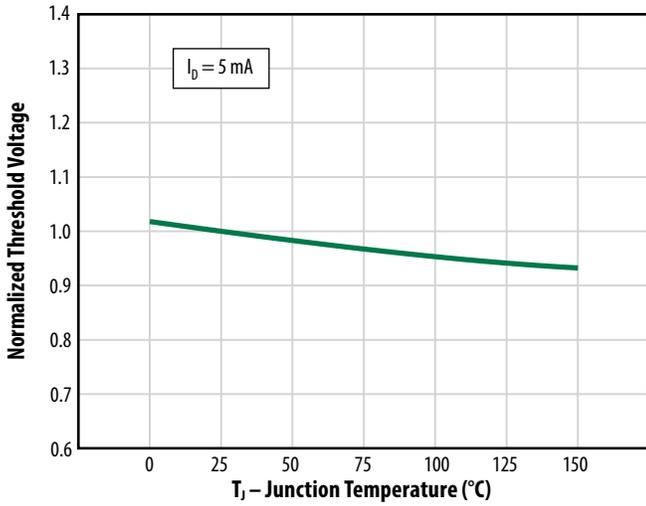


Figure 11: Safe Operating Area

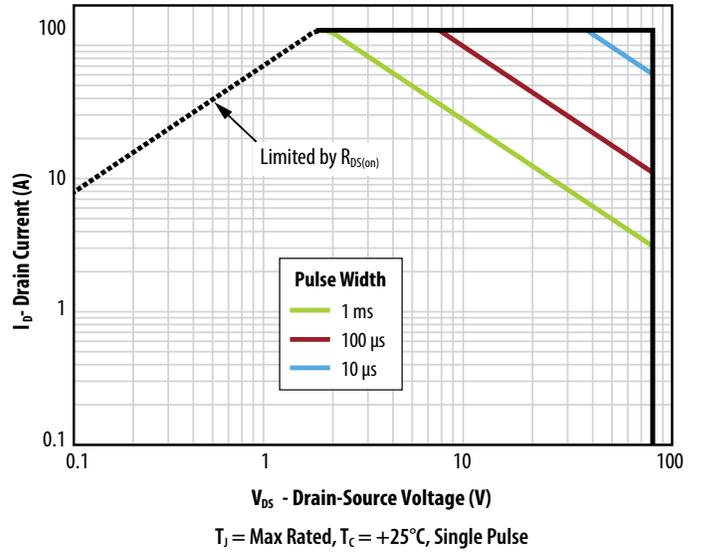
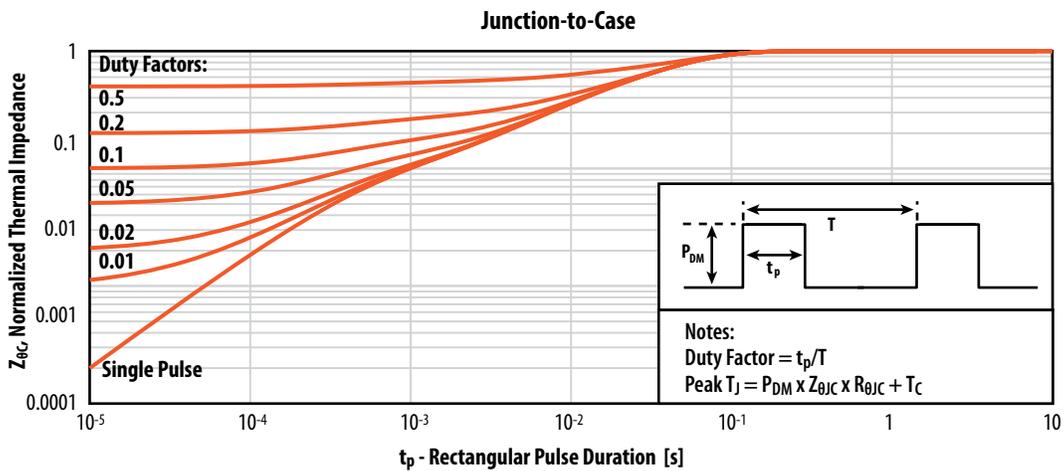
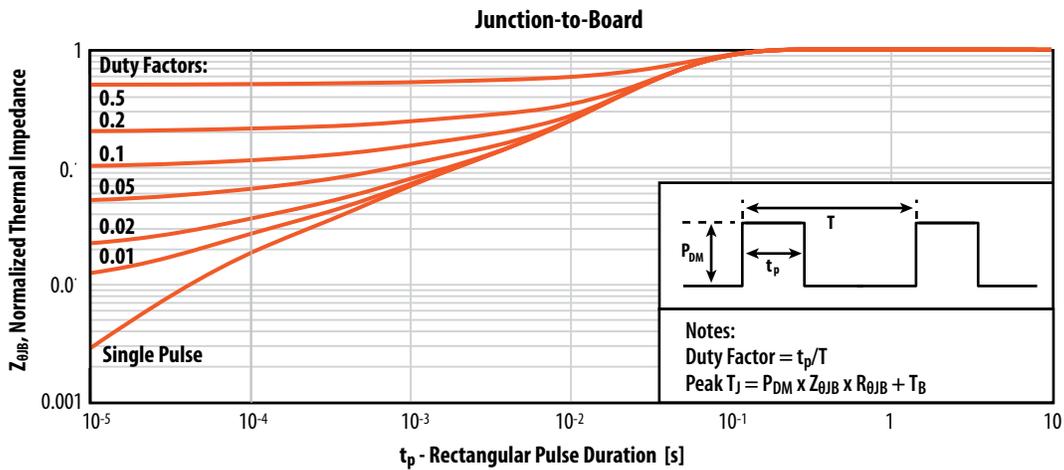
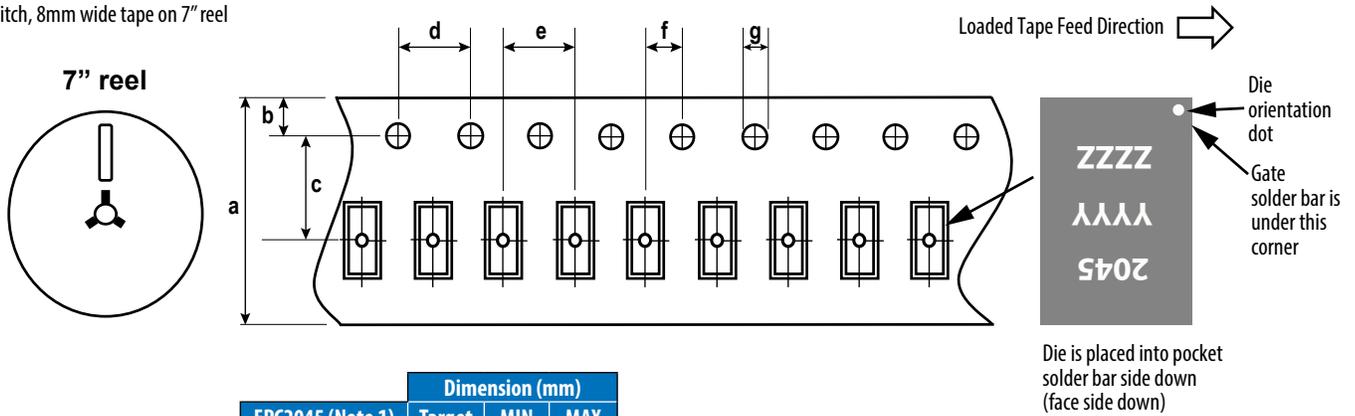


Figure 12: Typical Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

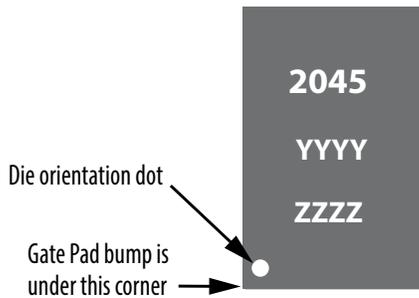
4mm pitch, 8mm wide tape on 7" reel



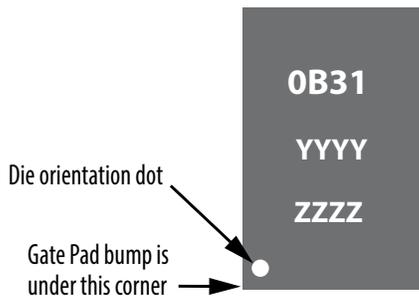
EPC2045 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



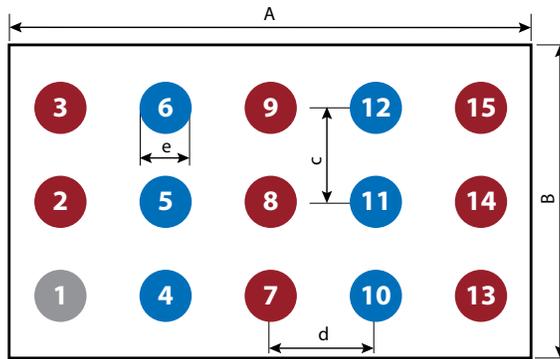
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2045	2045	YYYY	ZZZZ



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2045	0B31	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



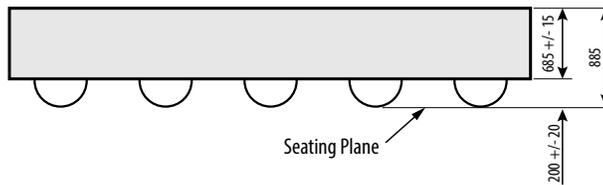
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c		450	
d		500	
e	238	264	290

Pads 1 is Gate;

Pads 2, 3, 7, 8, 9, 13, 14, 15 are Source;

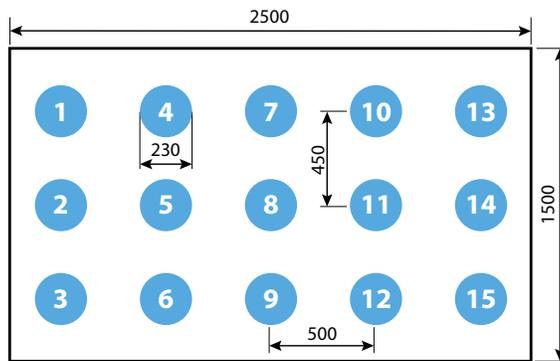
Pads 4, 5, 6, 10, 11, 12 are Drain;

Side View



Solder bump material: Solder Alloy Sn/1.8Ag :
IPC/JEDEC J-STD-609 solder alloy e-code : e2

RECOMMENDED LAND PATTERN
(units in μm)



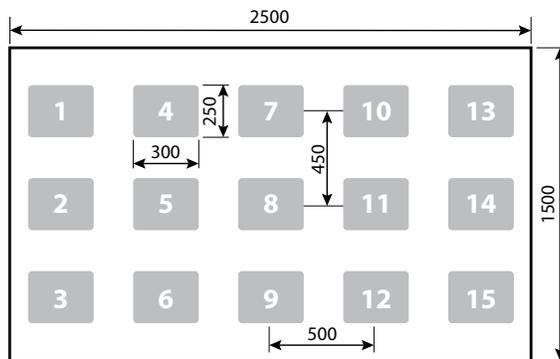
The land pattern is solder mask defined.
Copper is larger than the solder mask opening.

Pads 1 is Gate;

Pads 2, 3, 7, 8, 9, 13, 14, 15 are Source;

Pads 4, 5, 6, 10, 11, 12 are Drain;

RECOMMENDED STENCIL DRAWING
(measurements in μm)



Recommended stencil should be 4 mil (100 μm) thick, laser cut. The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
<https://epc-co.com/epc/design-support>

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EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

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