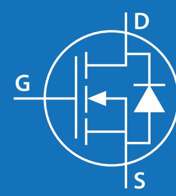
EPC2001C – Enhancement Mode Power Transistor

V_{DS} , 100 V
$R_{DS(on)}$, 7 mΩ
I_D , 36 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised July 17, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

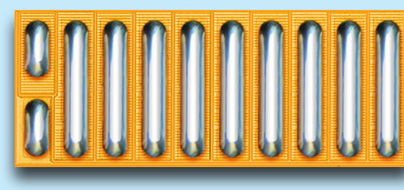
Application Notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_A = 25°C, $R_{θJA}$ = 7.3)	36	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	150	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	2	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	54	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



Die size: 4.1 x 1.6 mm

EPC2001C eGaN® FETs are supplied only in passivated die form with solder bars

Applications
- High-frequency DC-DC conversion
- Industrial automation
- Synchronous rectification
- Class-D audio
- Low inductance motor drives

Benefits
- Ultra high efficiency
- Ultra low switching and conduction losses
- Zero Q_{RR}
- Ultra small footprint

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 300 µA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		100	250	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		1	5	mA
	Gate-to-Source Reverse Leakage#	V_{GS} = -4 V		0.1	0.25	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 5 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 25 A		5.6	7	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

Defined by design. Not subject to production test.

Dynamic Characteristics # (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		770	900	pF
C_{OSS}	Output Capacitance			430	650	
C_{RSS}	Reverse Transfer Capacitance			10	15	
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 25 A		7.5	9	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 25 A		2.4		
Q_{GD}	Gate-to-Drain Charge			1.2	2	
$Q_{G(TH)}$	Gate Charge at Threshold			1.6		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		31	45	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.
\# Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

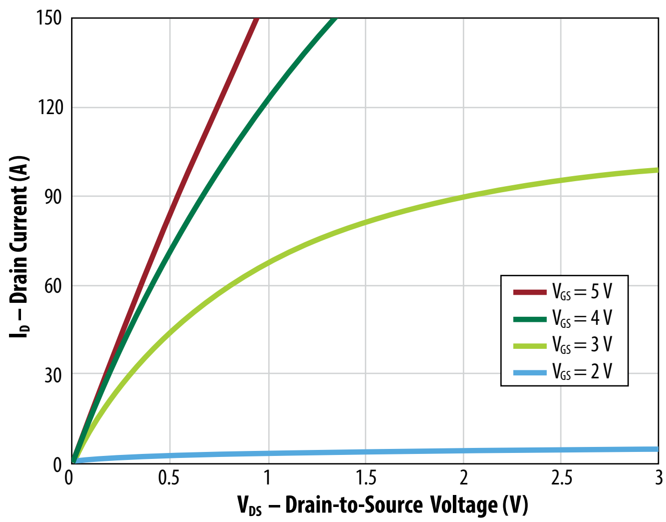


Figure 2: Typical Transfer Characteristics

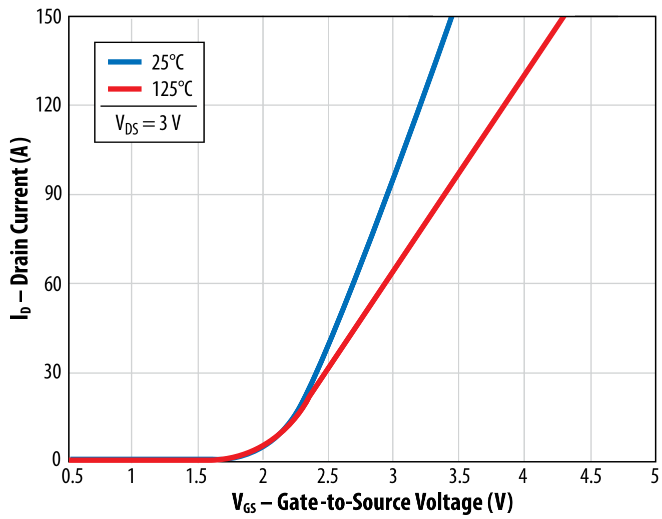


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Currents

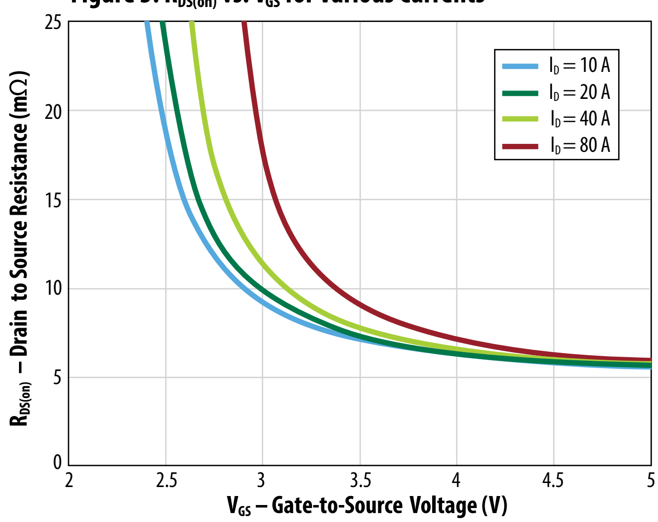


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

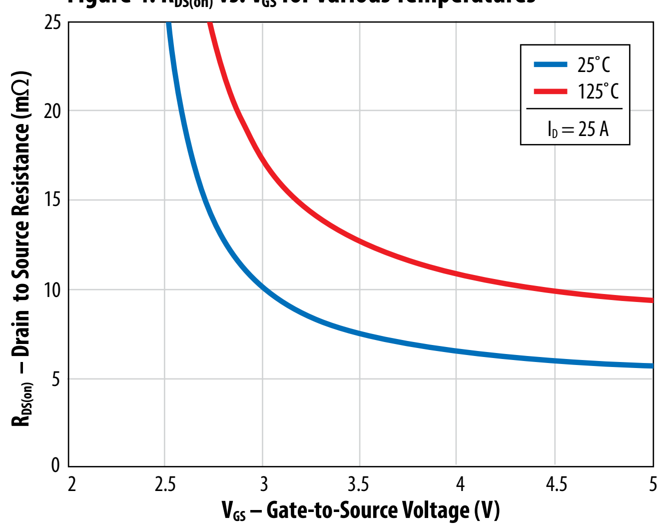


Figure 5a: Typical Capacitance (Linear Scale)

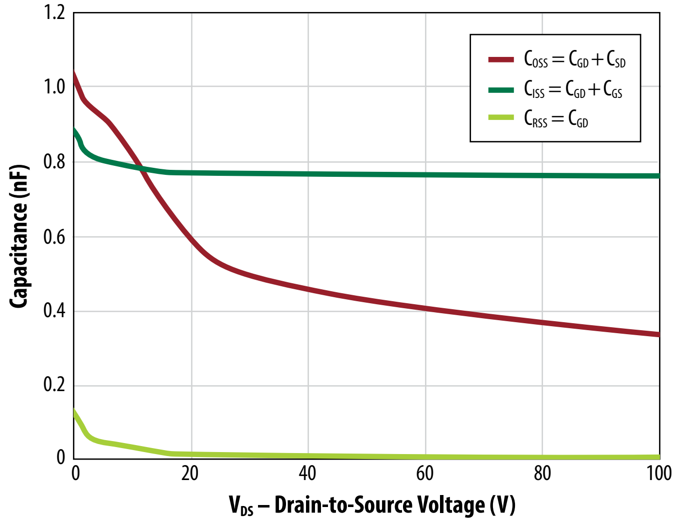


Figure 5b: Typical Capacitance (Log Scale)

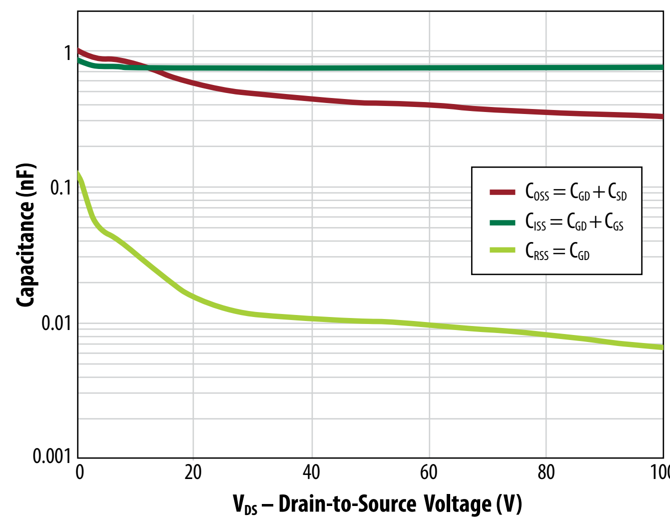


Figure 6: Typical Gate Charge

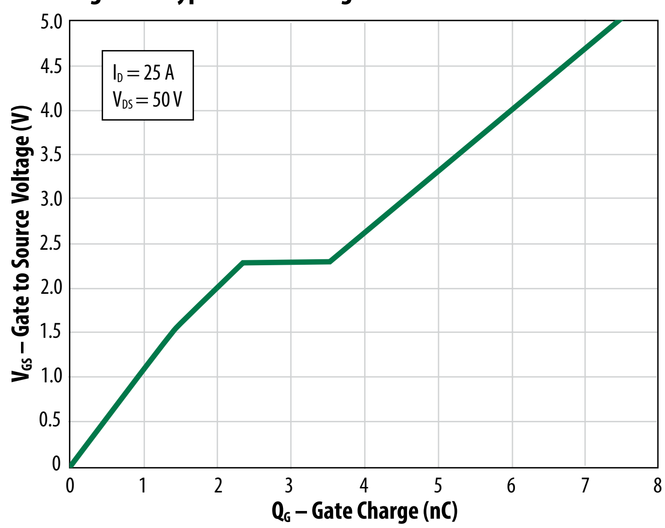


Figure 7: Typical Reverse Drain-Source Characteristics

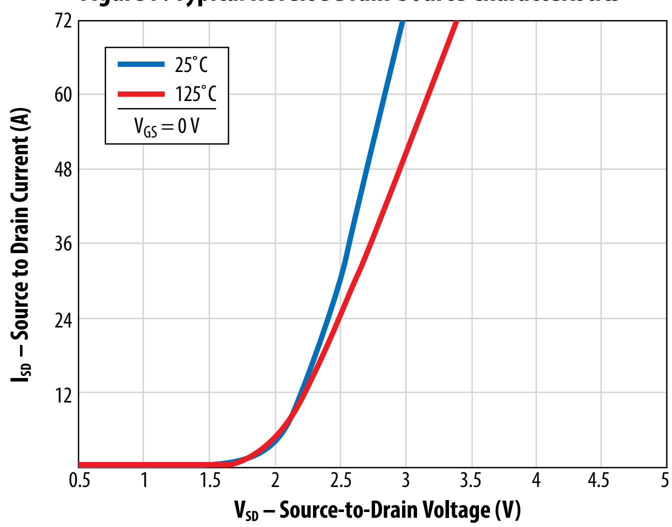


Figure 8: Normalized On Resistance vs. Temperature

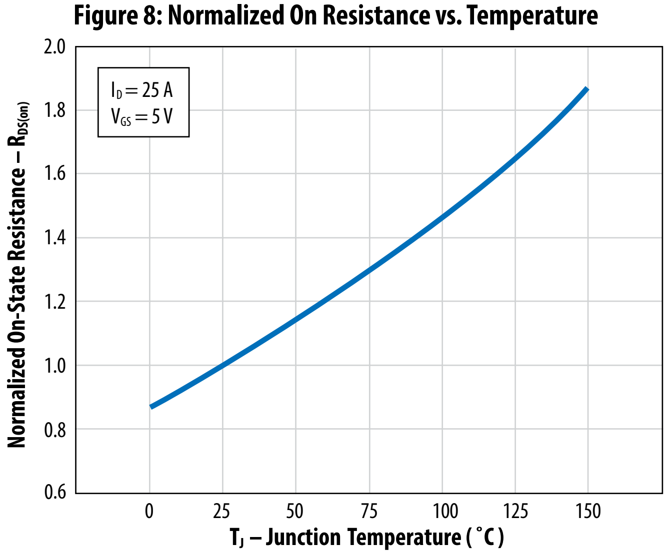
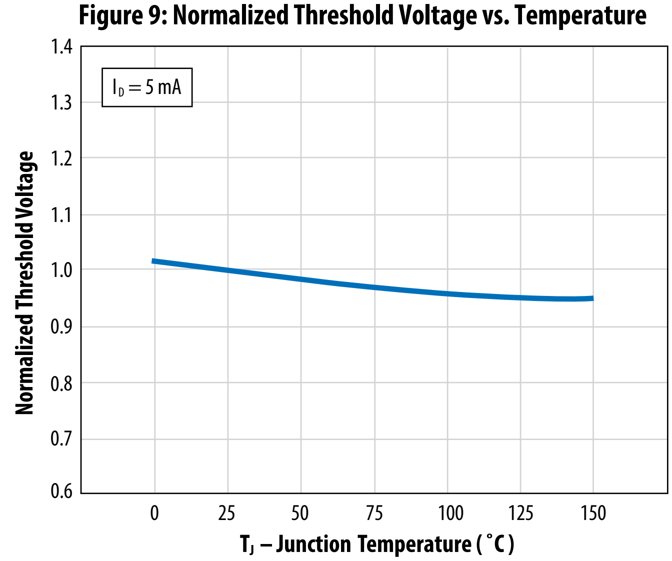


Figure 9: Normalized Threshold Voltage vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Gate Current

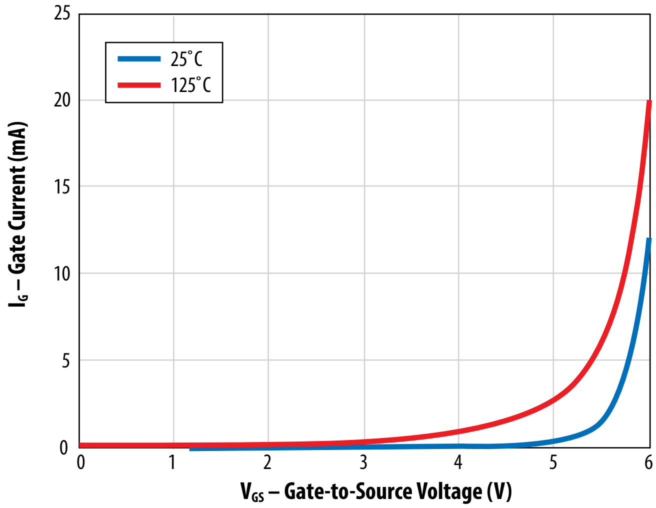
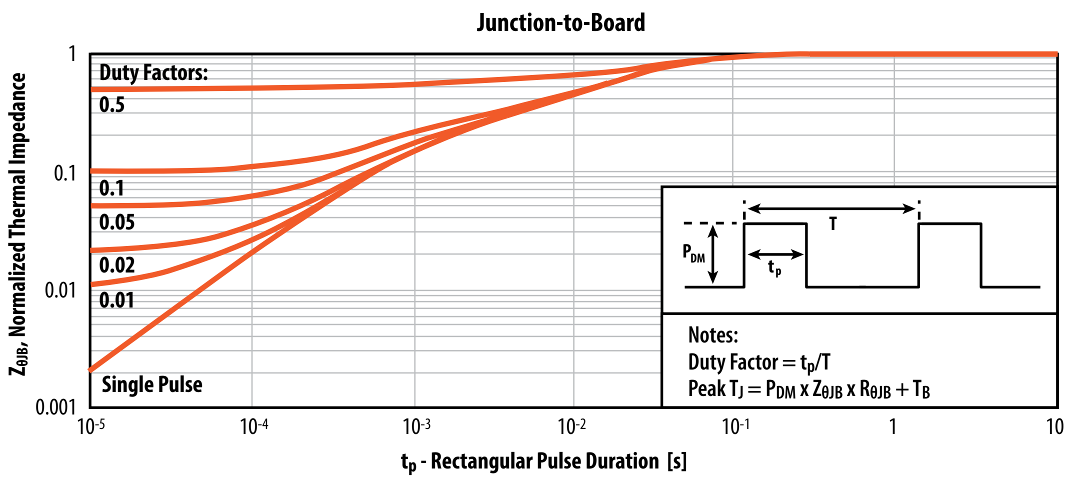


Figure 11: Transient Thermal Response Curves



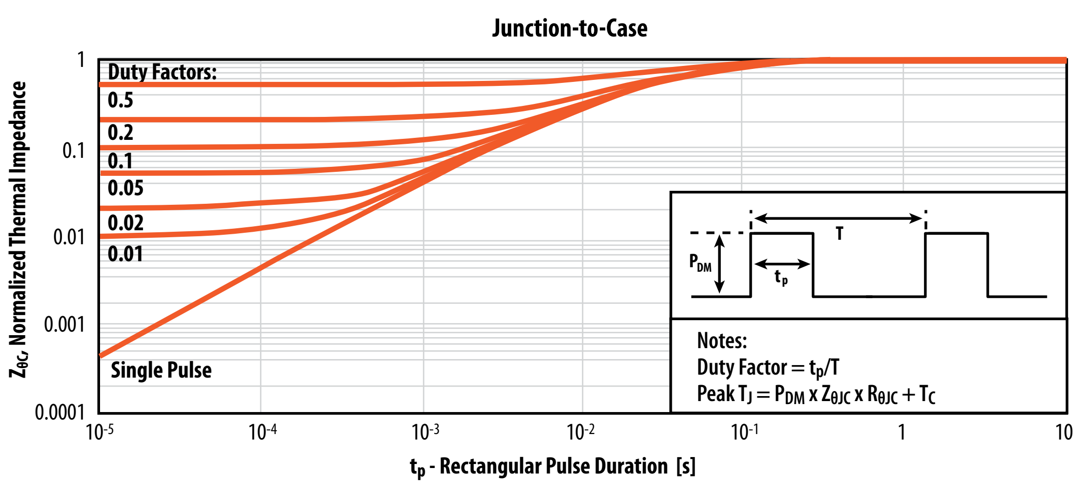
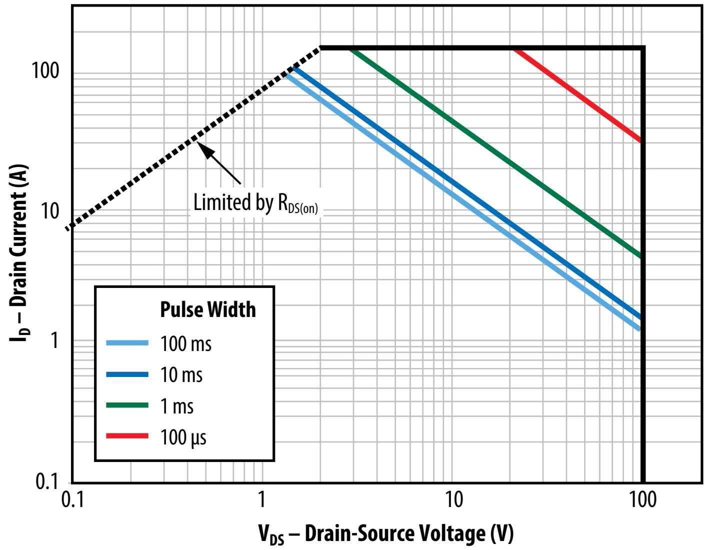


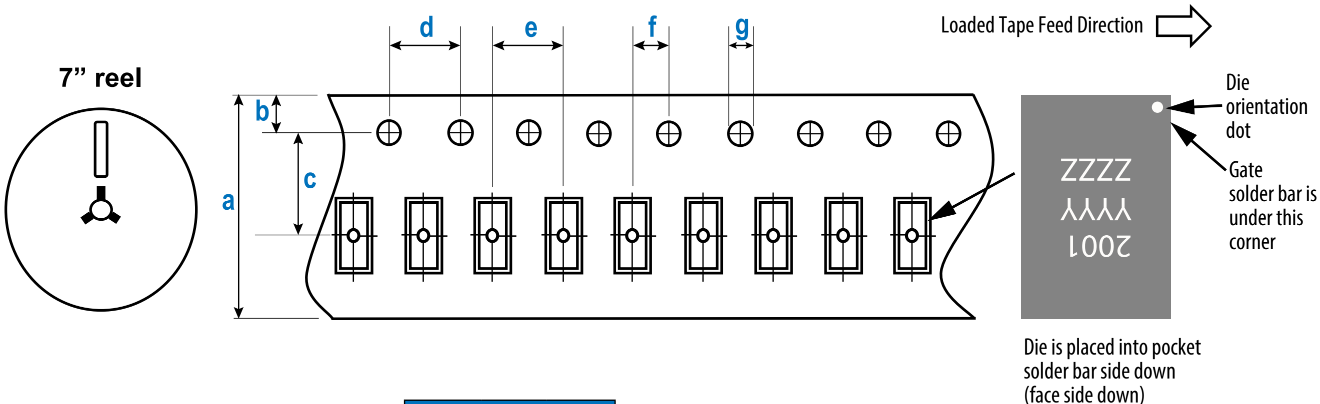
Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

4 mm pitch, 12 mm wide tape on 7" reel

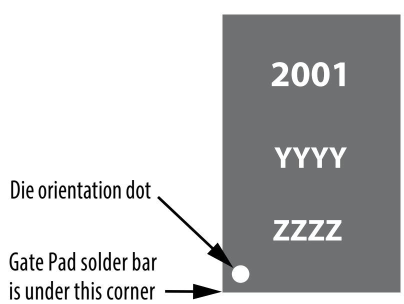


	Dimension (mm)		
EPC2001C (Note 1)	**Target**	**MIN**	**MAX**
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

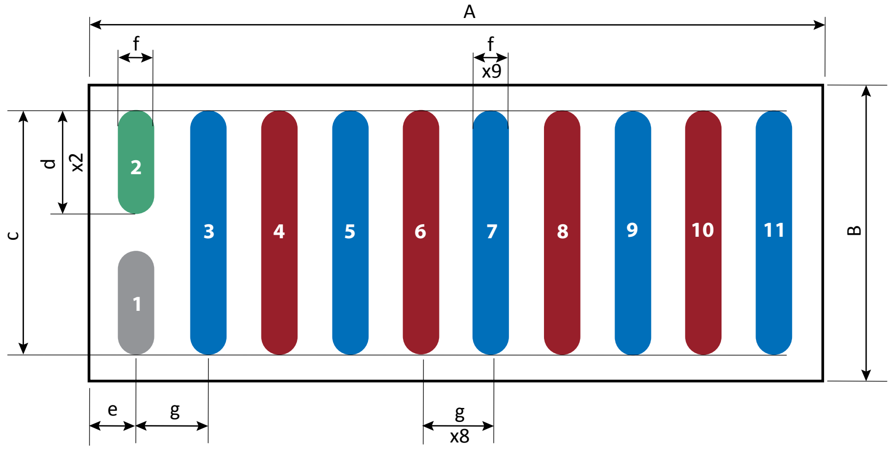
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	**Lot_Date Code Marking Line 2**	**Lot_Date Code Marking Line 3**
EPC2001C	2001	YYYY	ZZZZ

DIE OUTLINE

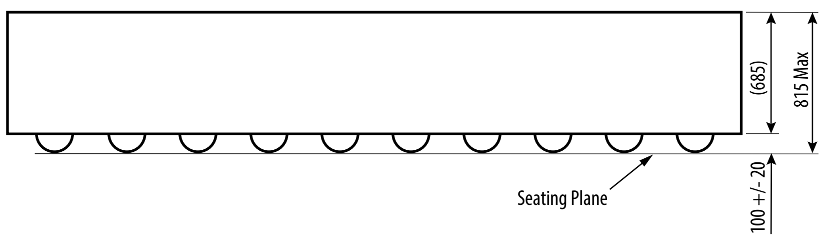
Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1602	1635	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;
Pads no. 3, 5, 7, 9, 11 are Drain;
Pads no. 4, 6, 8, 10 are Source;
Pad no. 2 is Substrate.*

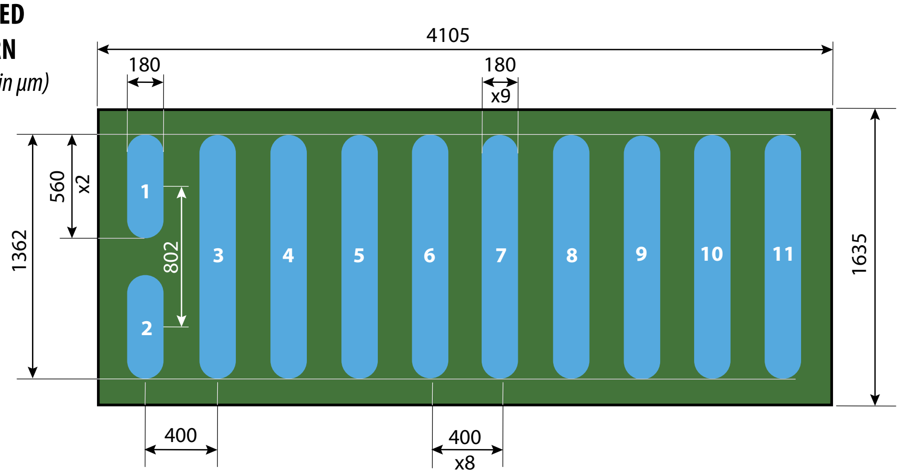
Side View



*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(measurements in µm)



The land pattern is solder mask defined.

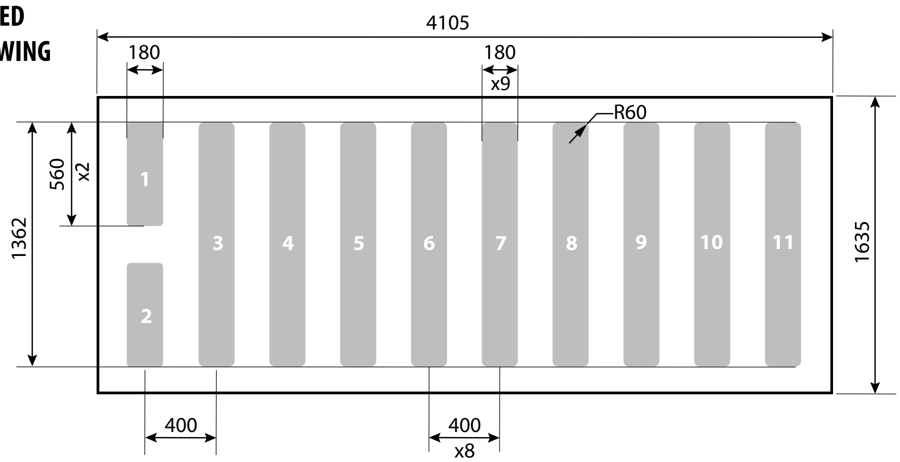
Pad no. 1 is Gate;
Pads no. 3, 5, 7, 9, 11 are Drain;
Pads no. 4, 6, 8, 10 are Source;
Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

Solder mask
(for solder mask defined pads)

RECOMMENDED STENCIL DRAWING

(units in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

TYPICAL THERMAL CONCEPT

The EPC2001C can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs.

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

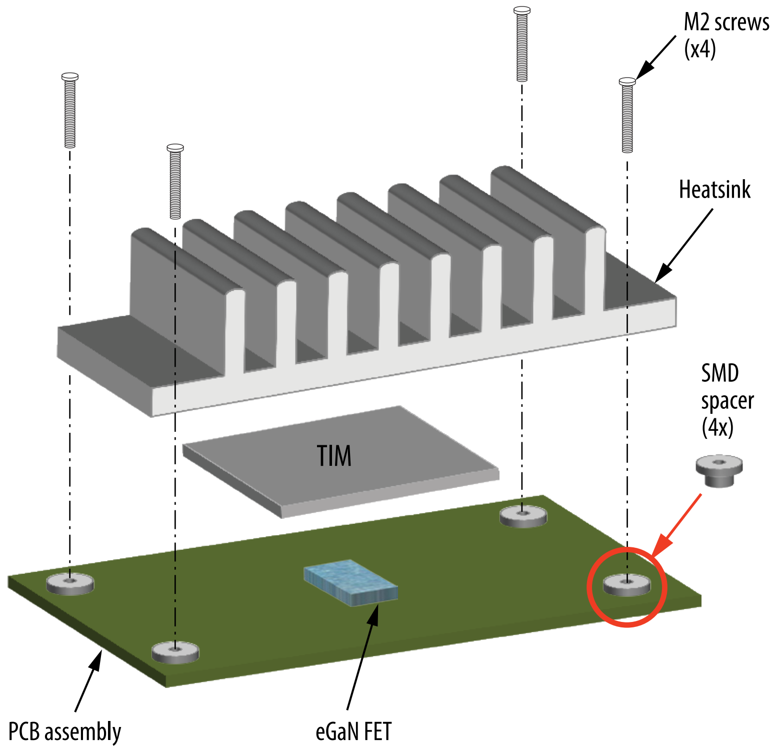


Figure 12: Exploded view of heatsink assembly using screws

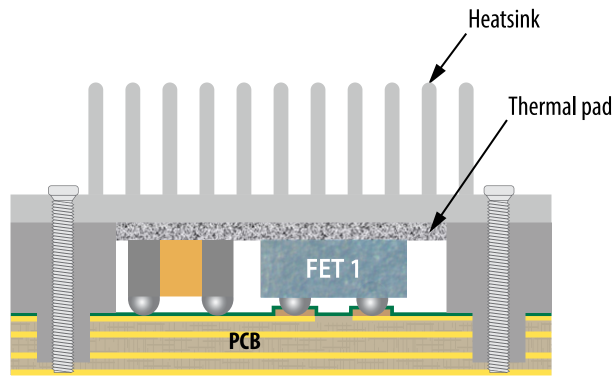


Figure 13: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

Solder mask defined pads are recommended for best reliability.

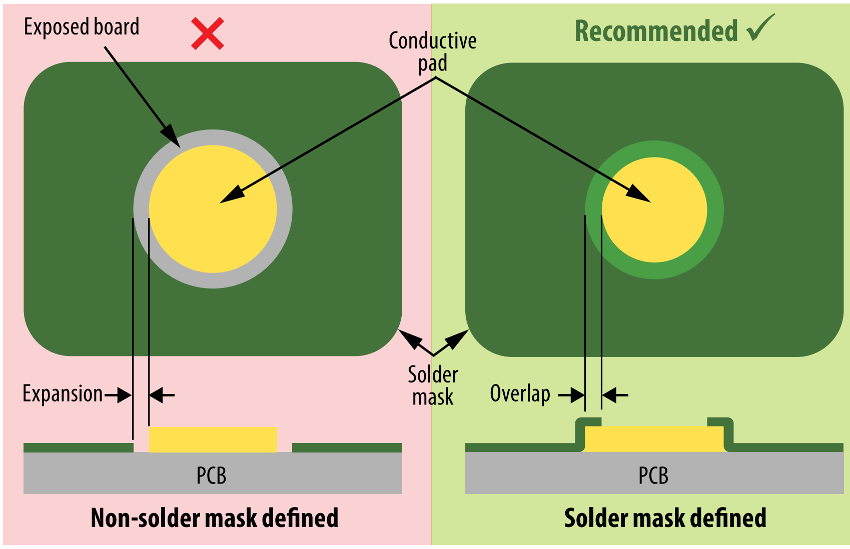


Figure 14: Solder mask defined versus non-solder mask defined pad

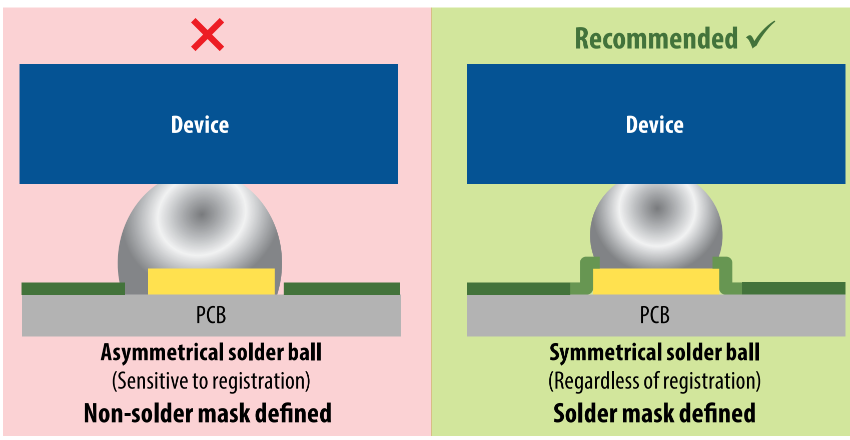


Figure 15: Effect of solder mask design on the solder ball symmetry

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip** (for preliminary device Altium footprints, contact EPC)