

## CSD25480F3 –20-V P-Channel FemtoFET™ MOSFET

### 1 Features

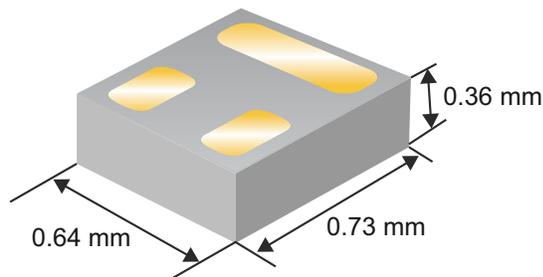
- Low on-resistance
- Ultra-low  $Q_g$  and  $Q_{gd}$
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Low profile
  - 0.36-mm max height
- Integrated ESD protection diode
- Lead and halogen free
- RoHS compliant

### 2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

### 3 Description

This –20-V, 110-m $\Omega$ , P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.



**Typical Part Dimensions**

### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–20	V
$Q_g$	Gate Charge Total (–4.5 V)	0.7	nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.10	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = -1.8\text{ V}$	420
		$V_{GS} = -2.5\text{ V}$	203
		$V_{GS} = -4.5\text{ V}$	132
		$V_{GS} = -8.0\text{ V}$	110
$V_{GS(th)}$	Threshold Voltage	–0.95	V

### Device Information<sup>(1)</sup>

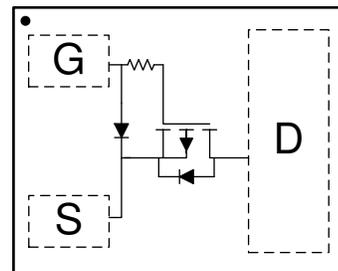
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25480F3	3000	7-Inch Reel	Femto 0.73-mm × 0.64-mm Land Grid Array (LGA)	Tape and Reel
CSD25480F3T	250			

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ (unless otherwise stated)		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–20	V
$V_{GS}$	Gate-to-Source Voltage	–12	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	–1.7	A
$I_{DM}$	Pulsed Drain Current <sup>(1) (2)</sup>	–10.6	A
$P_D$	Power Dissipation <sup>(1)</sup>	500	mW
$V_{(ESD)}$	Human-Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	2000	
$T_{J, T_{stg}}$	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

- (1) Typical  $R_{\theta JA} = 255^\circ\text{C/W}$  mounted on FR4 material with minimum Cu mounting area.  
 (2) Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .



**Top View**



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## 4 Revision History

<b>Changes from Revision A (August 2017) to Revision B (February 2022)</b>	<b>Page</b>
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.....	1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm.....	1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm.....	8
• Added FemtoFET Surface Mount Guide note.....	9

<b>Changes from Revision * (April 2016) to Revision A (August 2017)</b>	<b>Page</b>
• Added the <a href="#">Section 6.1</a> section in <a href="#">Section 6</a> .....	7
• Added <a href="#">Recommended Minimum PCB Layout</a> .....	9
• Updated the <a href="#">Section 7.3</a> .....	9

## 5 Specifications

### 5.1 Electrical Characteristics

T<sub>A</sub> = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>DS</sub> = -250 μA	-20			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			-50	nA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -12 V			-25	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = -250 μA	-0.70	-0.95	-1.20	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = -1.8 V, I <sub>DS</sub> = -0.1 A		420	840	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>DS</sub> = -0.4 A		203	260	
		V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.4 A		132	159	
		V <sub>GS</sub> = -8 V, I <sub>DS</sub> = -0.4 A		110	132	
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -0.4 A		8.0		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -10 V, f = 1 MHz		119	155	pF
C <sub>oss</sub>	Output capacitance			48	62	pF
C <sub>riss</sub>	Reverse transfer capacitance			3.6	4.7	pF
R <sub>G</sub>	Series gate resistance			16		Ω
Q <sub>g</sub>	Gate charge total (-4.5 V)	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -0.4 A		0.70	0.91	nC
Q <sub>gd</sub>	Gate charge gate-to-drain			0.10		nC
Q <sub>gs</sub>	Gate charge gate-to-source			0.26		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			0.15		nC
Q <sub>oss</sub>	Output charge		V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V		1.3	
t <sub>d(on)</sub>	Turnon delay time	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.4 A, R <sub>G</sub> = 10 Ω		9		ns
t <sub>r</sub>	Rise time			5		ns
t <sub>d(off)</sub>	Turnoff delay time			13		ns
t <sub>f</sub>	Fall time			7		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = -0.4 A, V <sub>GS</sub> = 0 V		-0.78	-1.0	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = -10 V, I <sub>F</sub> = -0.4 A, di/dt = 100 A/μs		1.2		nC
t <sub>rr</sub>	Reverse recovery time			6.4		ns

### 5.2 Thermal Information

T<sub>A</sub> = 25°C (unless otherwise stated)

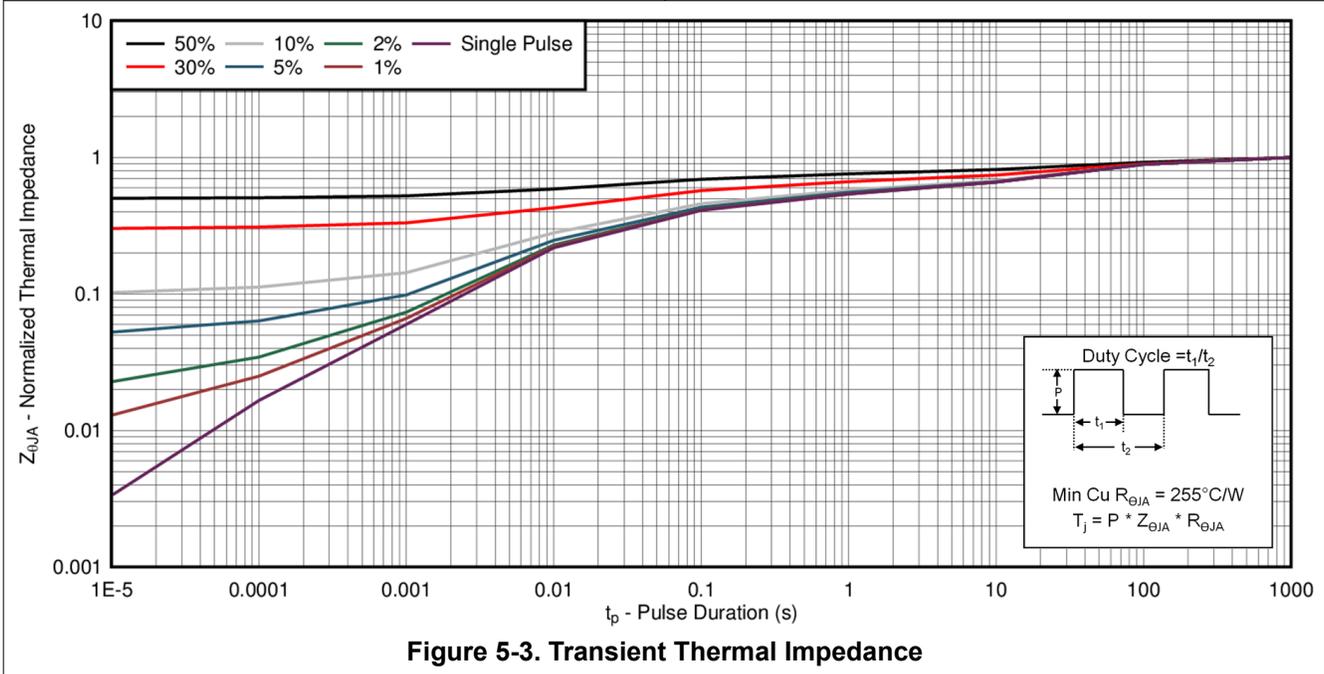
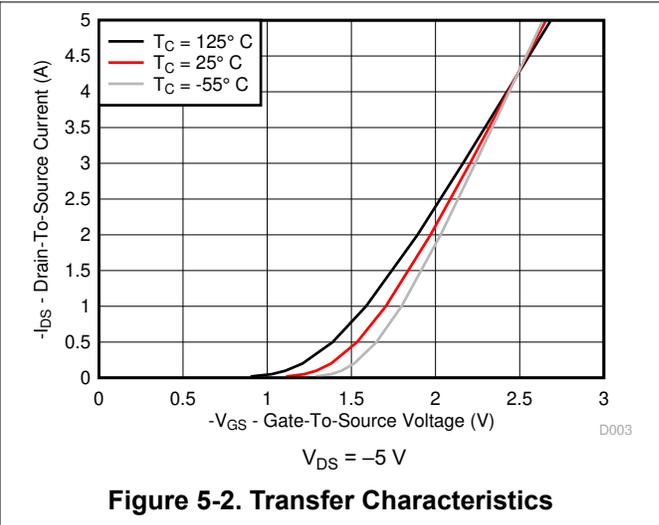
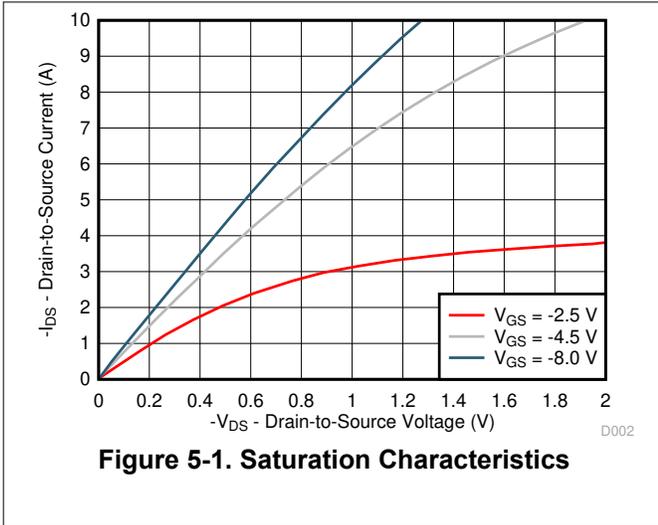
THERMAL METRIC		TYPICAL VALUES	UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	90	°C/W
	Junction-to-ambient thermal resistance <sup>(2)</sup>	255	

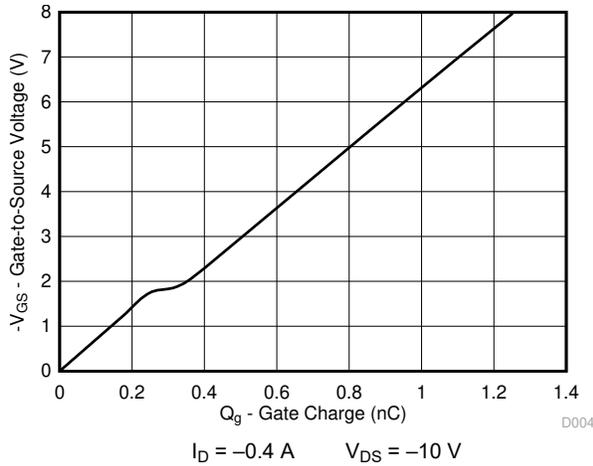
(1) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm) thick Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

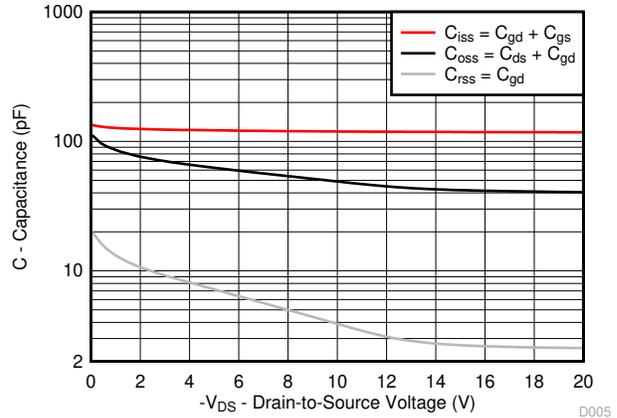
### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise stated)

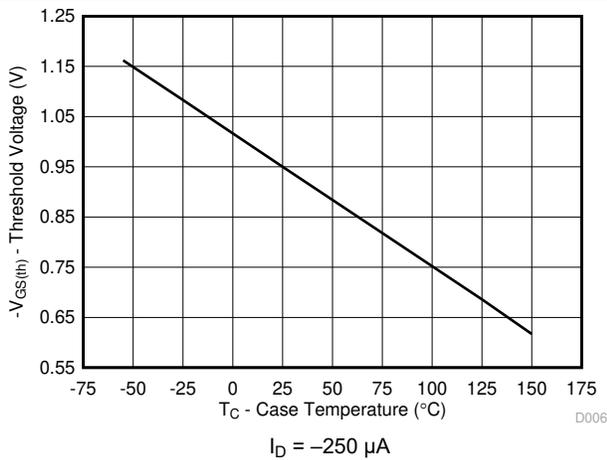




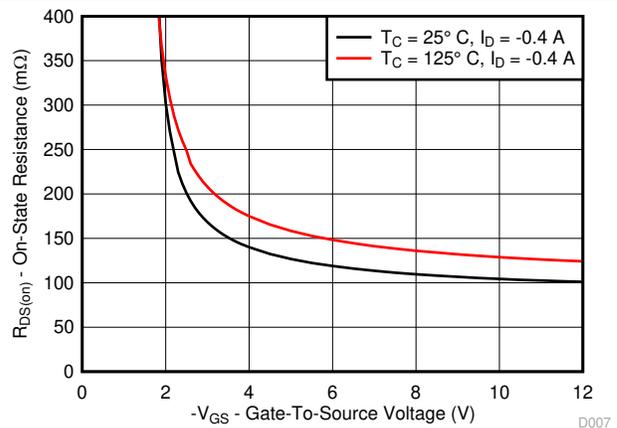
**Figure 5-4. Gate Charge**



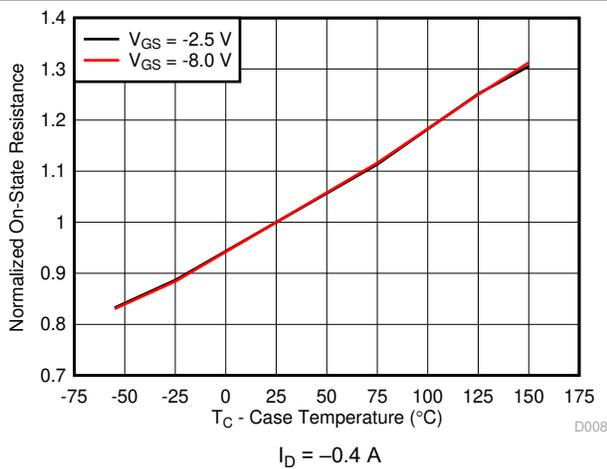
**Figure 5-5. Capacitance**



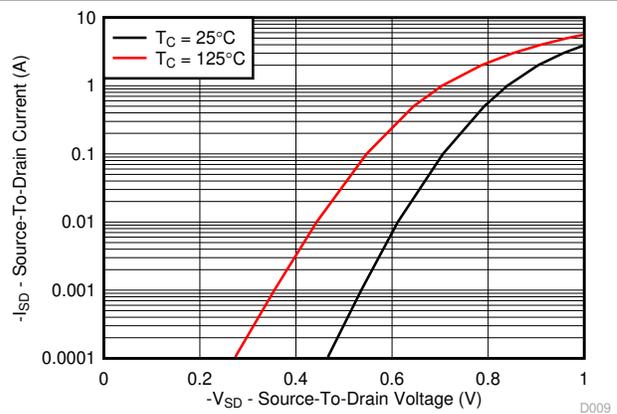
**Figure 5-6. Threshold Voltage vs Temperature**



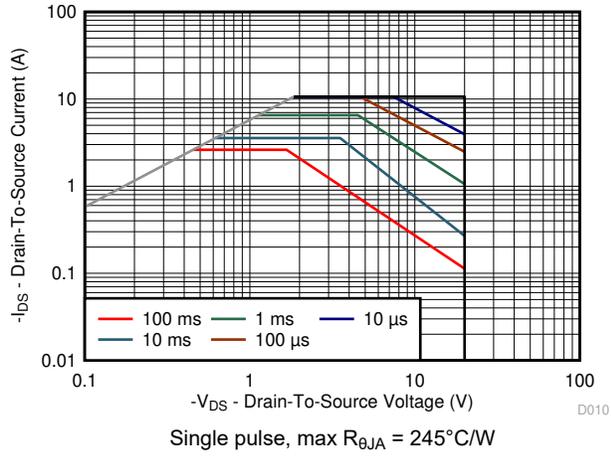
**Figure 5-7. On-State Resistance vs Gate-to-Source Voltage**



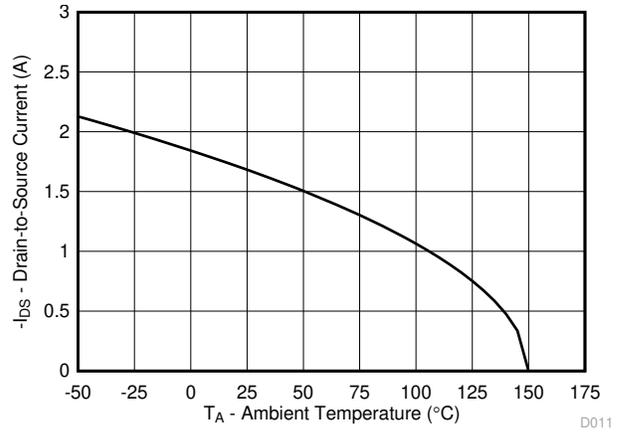
**Figure 5-8. Normalized On-State Resistance vs Temperature**



**Figure 5-9. Typical Diode Forward Voltage**



**Figure 5-10. Maximum Safe Operating Area**



**Figure 5-11. Maximum Drain Current vs Temperature**

## **6 Device and Documentation Support**

### **6.1 Receiving Notification of Documentation Updates**

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

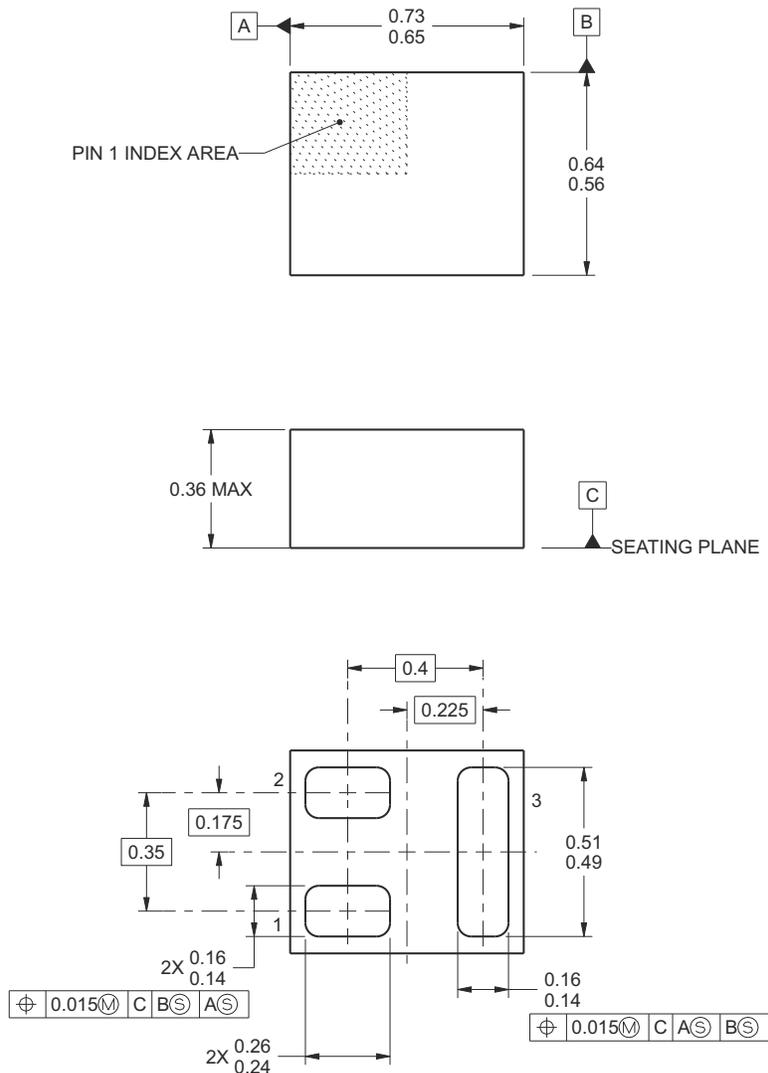
### **6.2 Trademarks**

FemtoFET™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Mechanical Dimensions

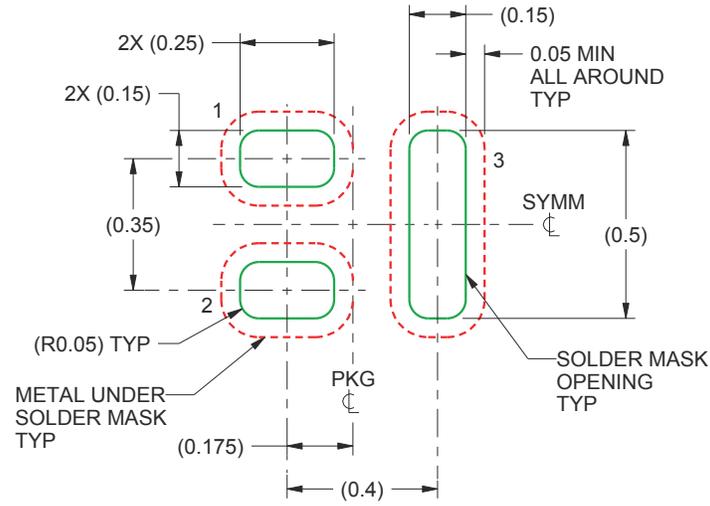


- A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- B. This drawing is subject to change without notice.
- C. This package is a lead-free solder land design.

**Table 7-1. Pin Configuration**

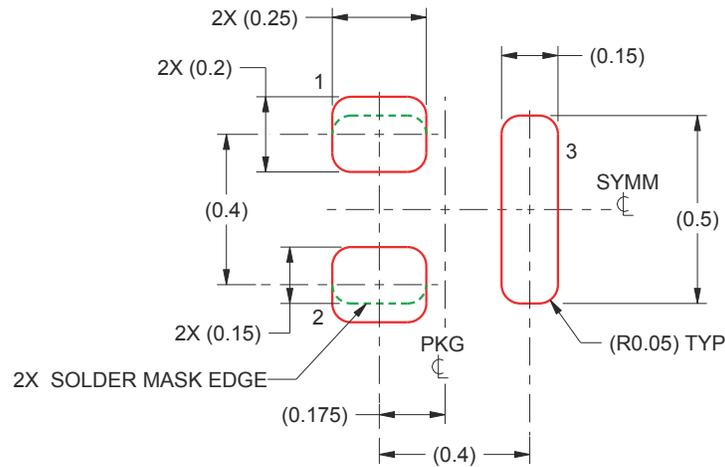
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

## 7.2 Recommended Minimum PCB Layout



- A. All dimensions are in millimeters.
- B. For more information, see [FemtoFET Surface Mount Guide](#) (SLRA003D).

## 7.3 Recommended Stencil Pattern



- A. All dimensions are in millimeters.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CSD25480F3</a>	Active	Production	PICOSTAR (YJM)   3	3000   LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4
CSD25480F3.B	Active	Production	PICOSTAR (YJM)   3	3000   LARGE T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4
<a href="#">CSD25480F3T</a>	Active	Production	PICOSTAR (YJM)   3	250   SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4
CSD25480F3T.B	Active	Production	PICOSTAR (YJM)   3	250   SMALL T&R	Yes	NIAU	Level-1-260C-UNLIM	-55 to 150	4

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

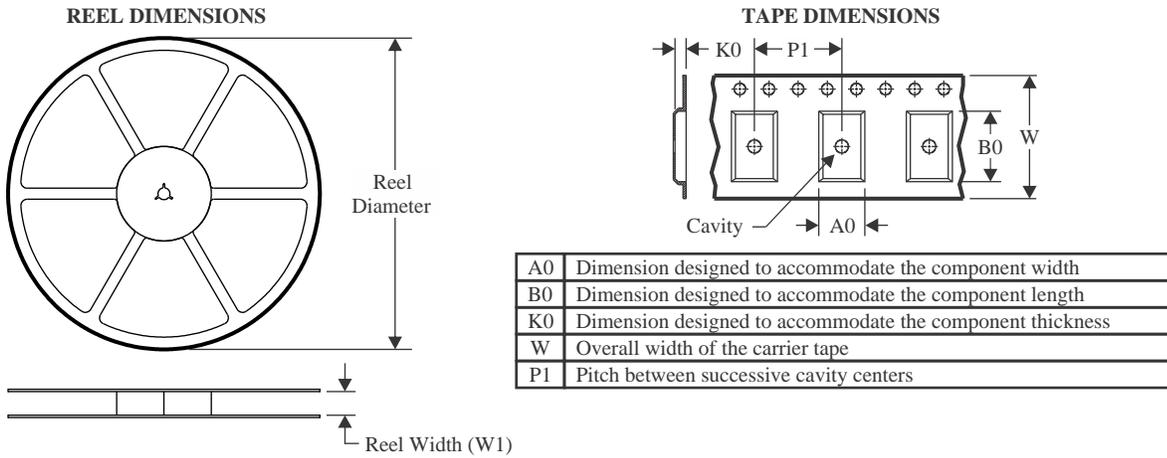
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

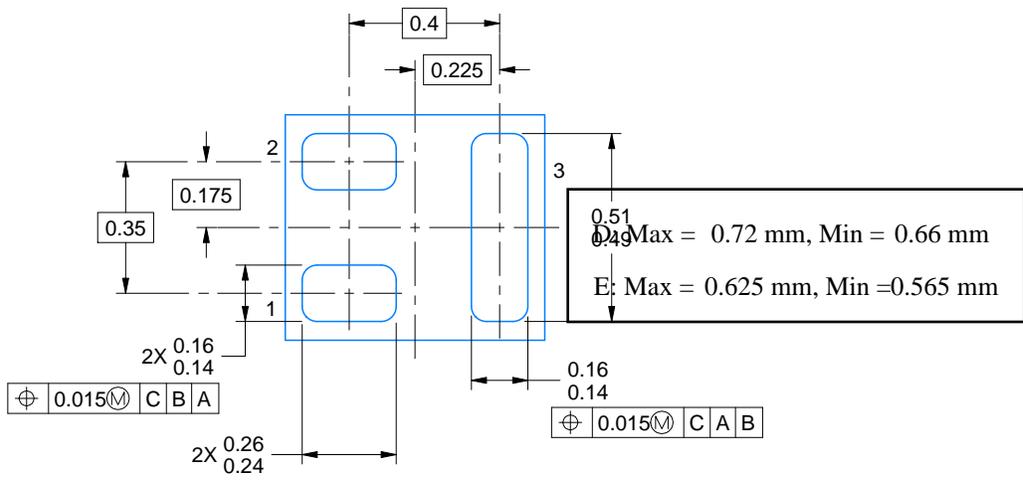
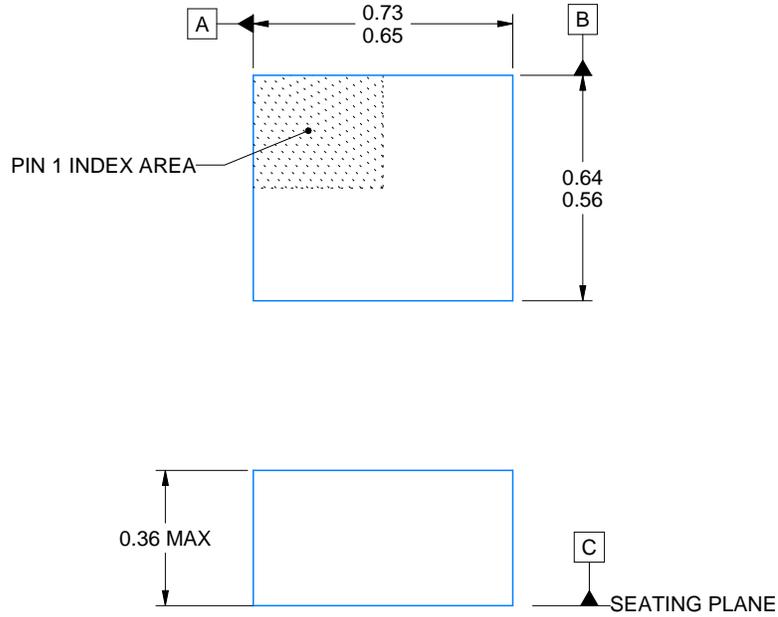

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25480F3	PICOSTAR	YJM	3	3000	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2
CSD25480F3T	PICOSTAR	YJM	3	250	180.0	8.4	1.94	0.79	0.44	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25480F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD25480F3T	PICOSTAR	YJM	3	250	182.0	182.0	20.0

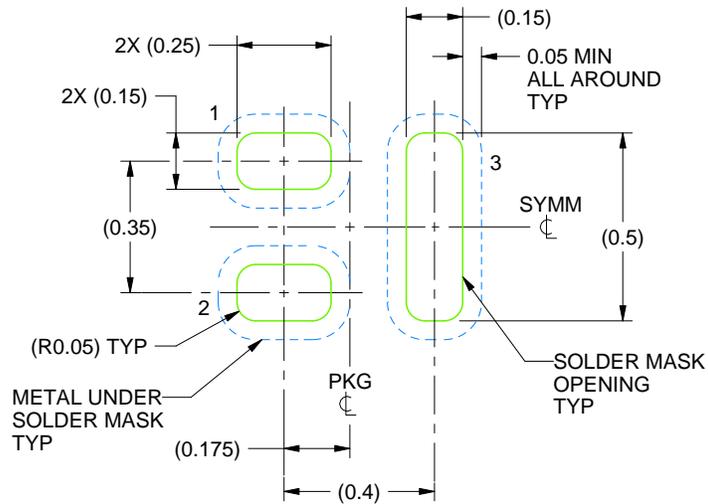


4222304/B 03/2022

NOTES:

PicoStar is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.

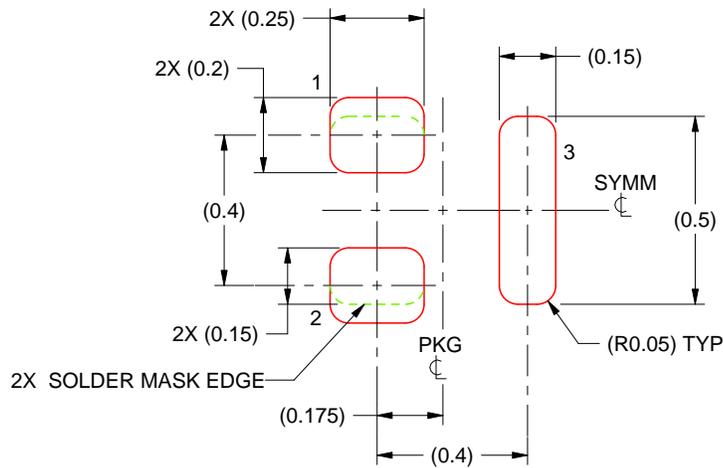


LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:50X

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NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).



**SOLDER PASTE EXAMPLE**  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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