



ALPHA & OMEGA
SEMICONDUCTOR

AONS66920
100V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Logic Level Driving
- Excellent $Q_G \times R_{DS(ON)}$ Product (FOM)
- Skipe Optimized Process
- RoHS and Halogen-Free Compliant

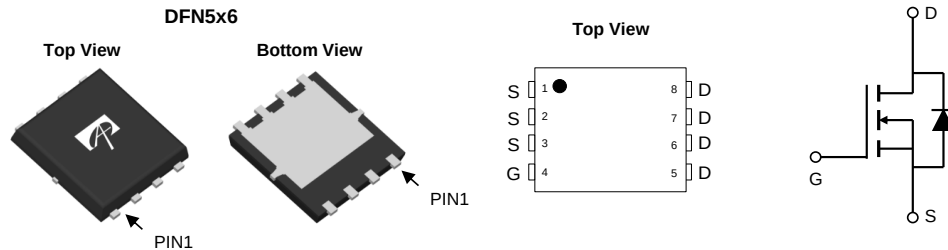
Applications

- High Frequency Switching and Synchronous Rectification

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	48A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 8.2mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 10.7mΩ

100% UIS Tested
100% Rg Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONS66920	DFN 5x6	Tape & Reel	3000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	48	A
$T_C=25^\circ\text{C}$		37	
Pulsed Drain Current ^C	I_{DM}	125	A
Continuous Drain Current	I_{DSM}	17.5	A
$T_A=25^\circ\text{C}$		14	
Avalanche Current ^C	I_{AS}	38	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}	72	mJ
Power Dissipation ^B	P_D	56.5	W
$T_C=25^\circ\text{C}$		22.5	
Power Dissipation ^A	P_{DSM}	5.0	W
$T_A=25^\circ\text{C}$		3.2	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	$^\circ\text{C/W}$
$t \leq 10\text{s}$		45	55	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JC}$	1.8	2.2	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.5	2.0	2.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		6.7 11.6	8.2 14	mΩ
		V _{GS} =4.5V, I _D =20A		8.5	10.7	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		65		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				48	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz		2500		pF
C _{oss}	Output Capacitance			485		pF
C _{rss}	Reverse Transfer Capacitance			13		pF
R _g	Gate resistance	f=1MHz	0.5	1.1	1.8	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =20A		35	50	nC
Q _{g(4.5V)}	Total Gate Charge			16.7	25	nC
Q _{gs}	Gate Source Charge			8		nC
Q _{gd}	Gate Drain Charge			5		nC
Q _{oss}	Output Charge	V _{GS} =0V, V _{DS} =50V		44		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =2.5Ω, R _{GEN} =3Ω		10		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			31		ns
t _f	Turn-Off Fall Time			6		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, di/dt=500A/μs		34		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, di/dt=500A/μs		170		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T_{J(MAX)}=150° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

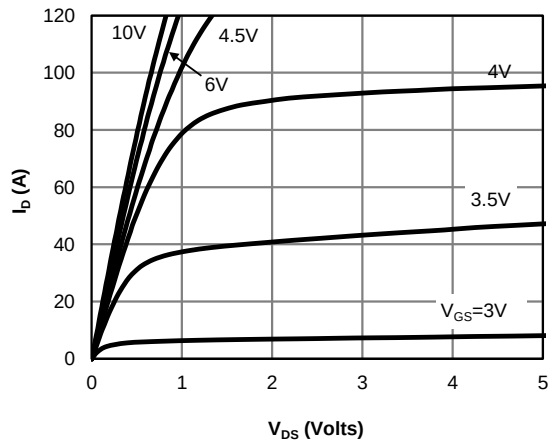


Figure 1: On-Region Characteristics (Note E)

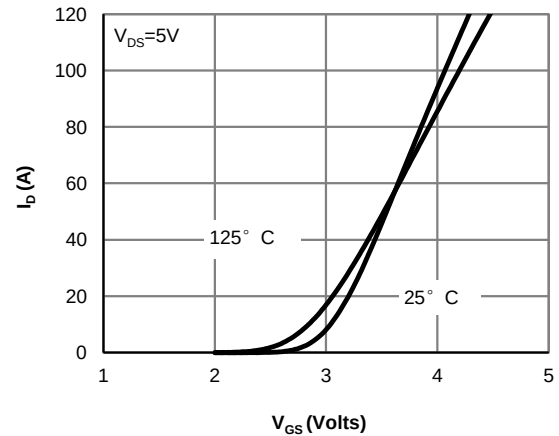


Figure 2: Transfer Characteristics (Note E)

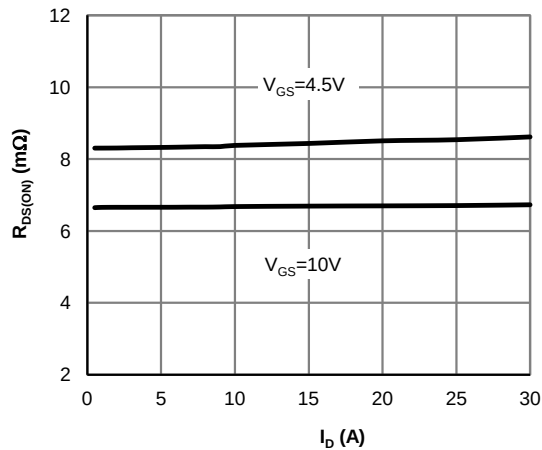


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

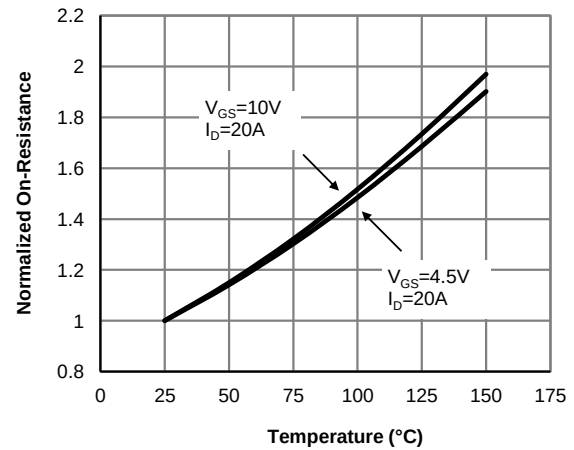


Figure 4: On-Resistance vs. Junction Temperature (Note E)

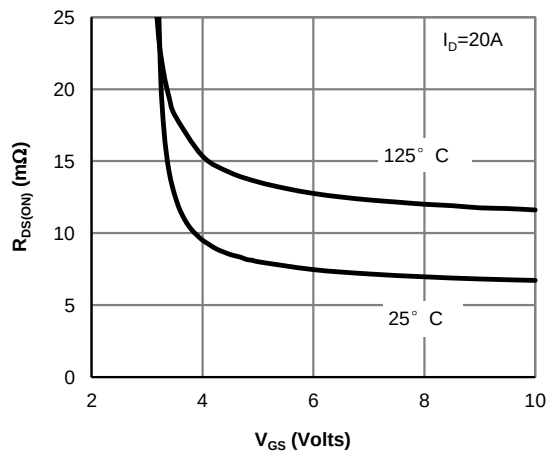


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

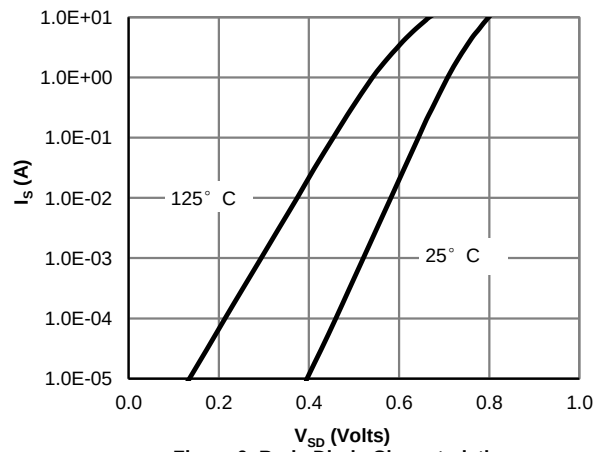


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

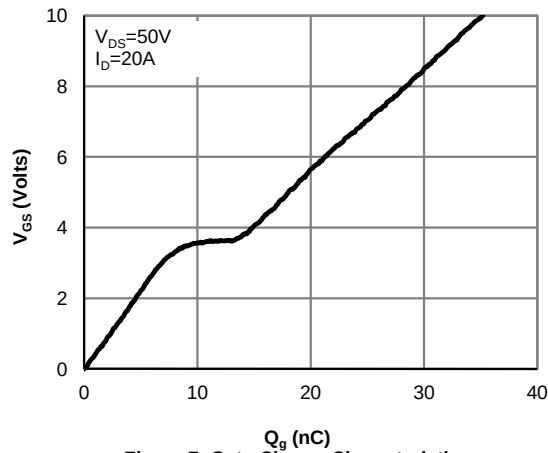


Figure 7: Gate-Charge Characteristics

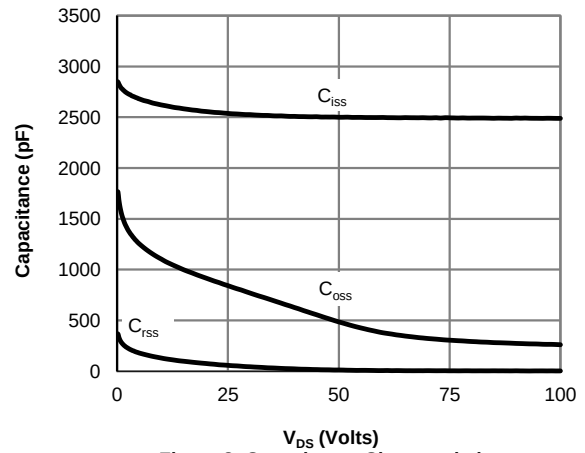


Figure 8: Capacitance Characteristics

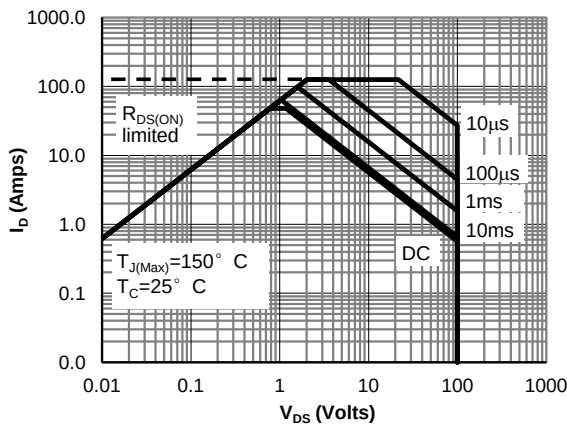


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

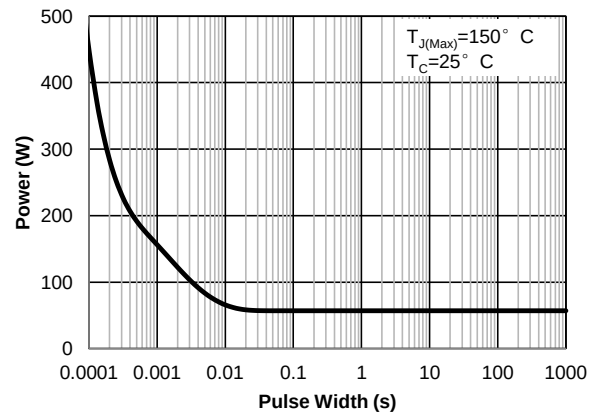


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

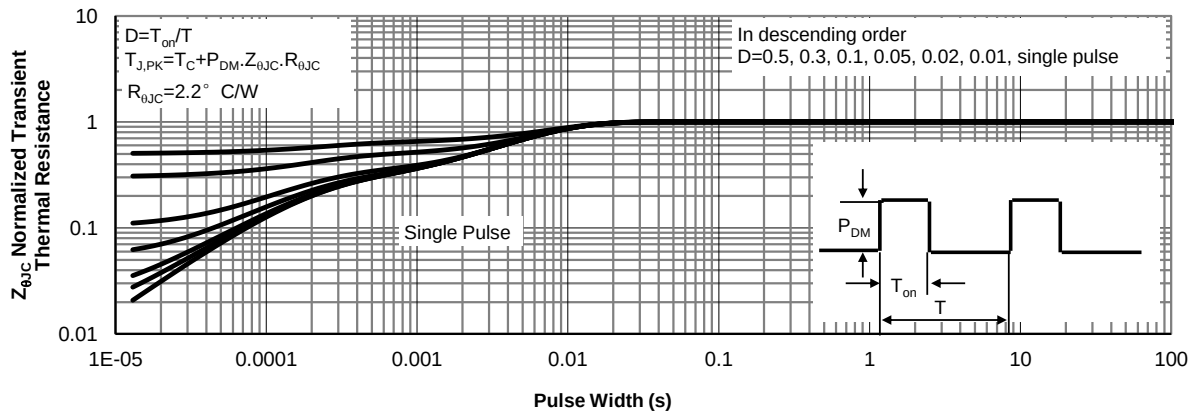


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

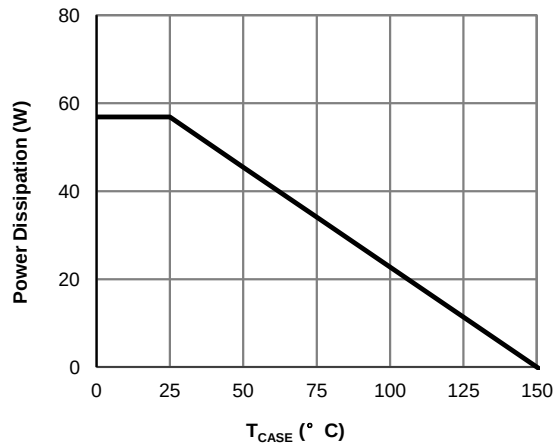


Figure 12: Power De-rating (Note F)

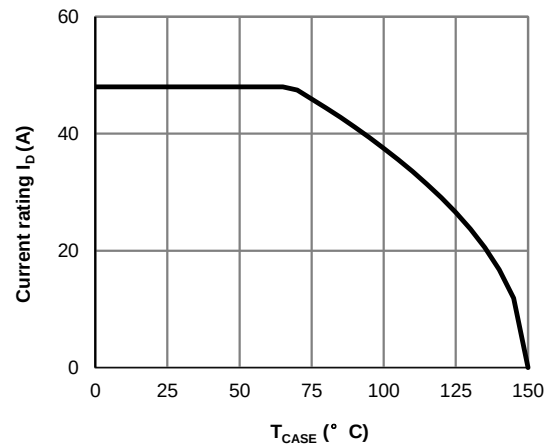


Figure 13: Current De-rating (Note F)

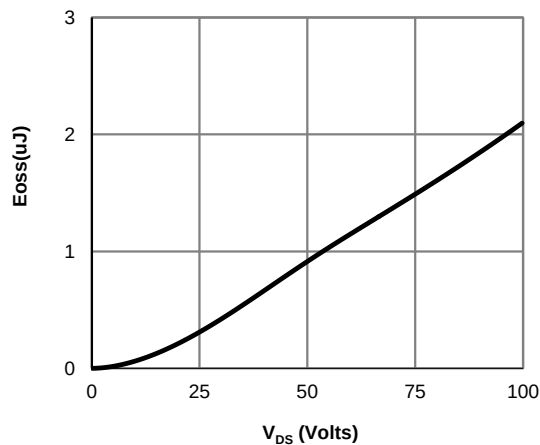


Figure 14: Coss stored Energy

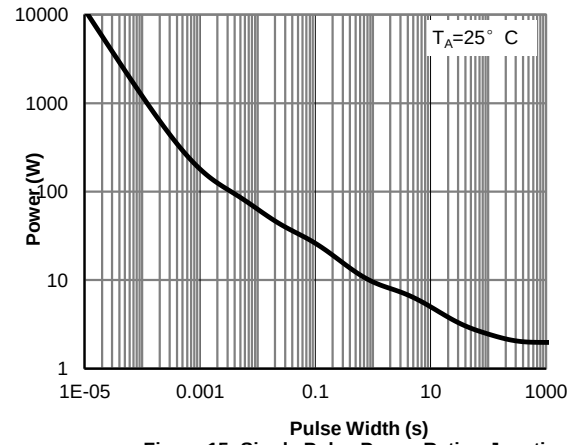


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

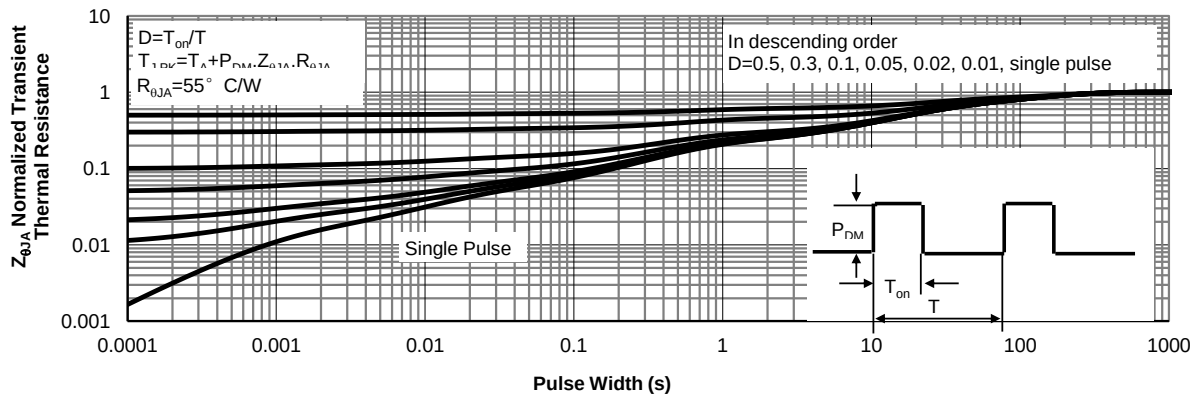


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

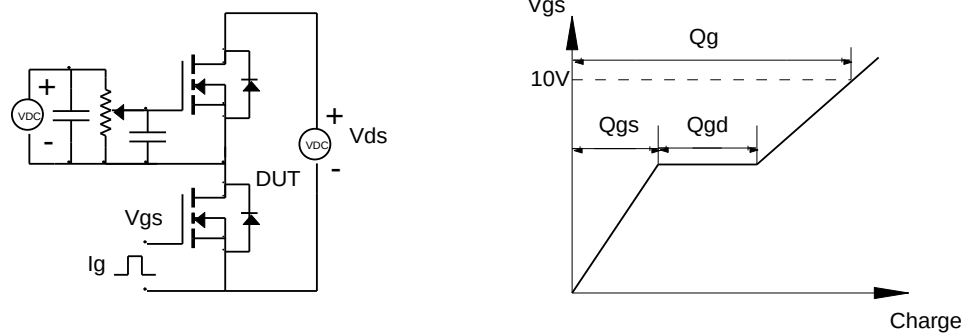


Figure B: Resistive Switching Test Circuit & Waveforms

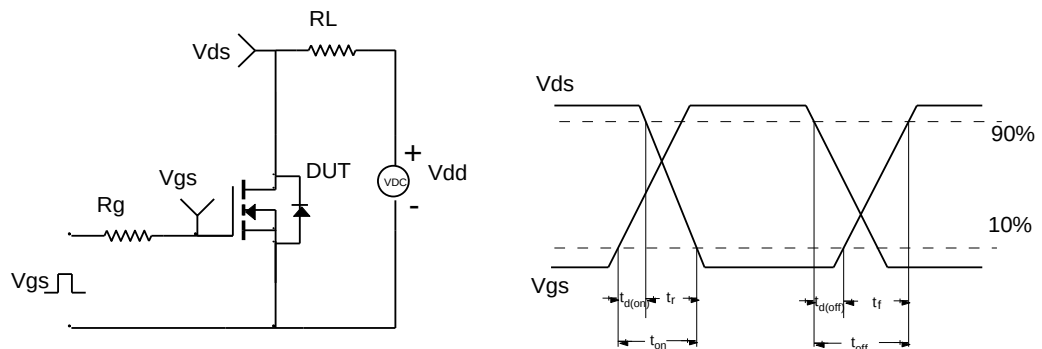


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

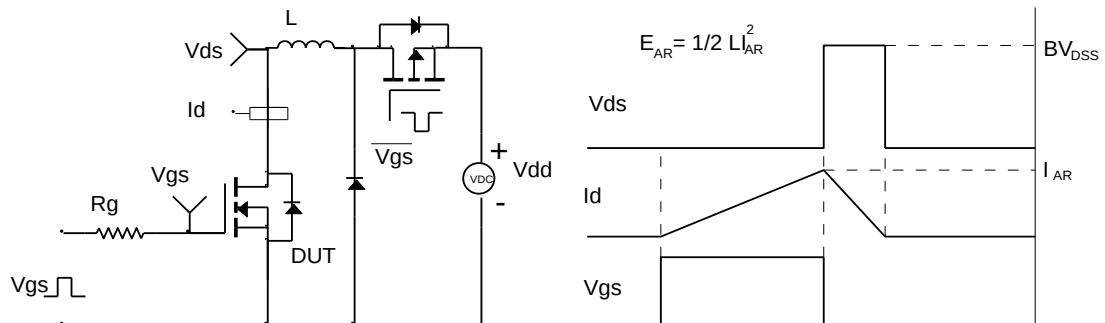
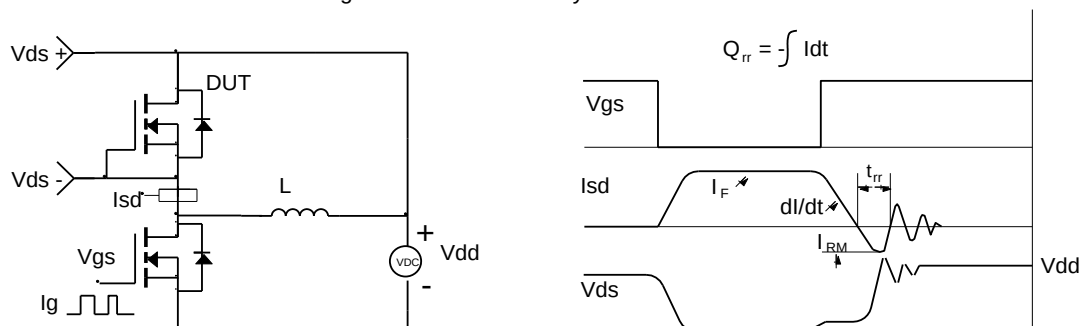


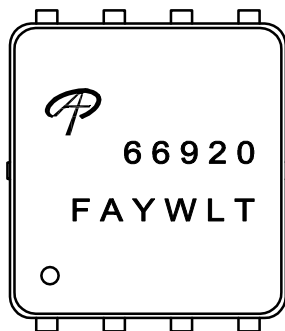
Figure D: Diode Recovery Test Circuit & Waveforms





Document No.	PD-03011
Version	A
Title	AONS66920 Marking Description

DFN5x6 PACKAGE MARKING DESCRIPTION



Green product

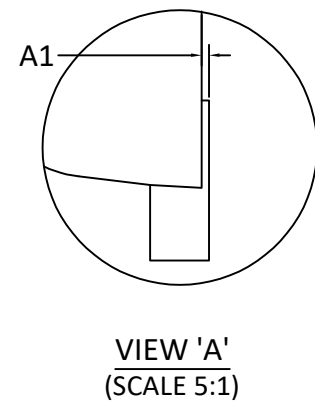
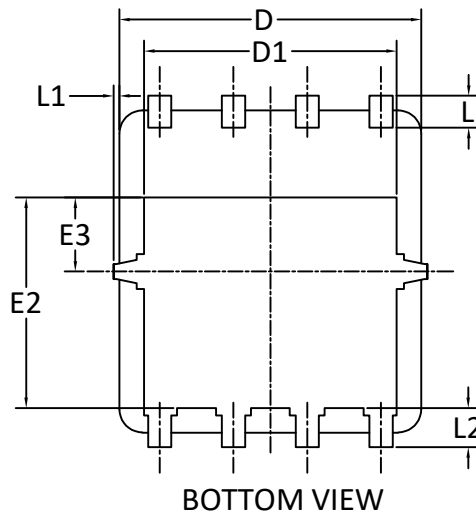
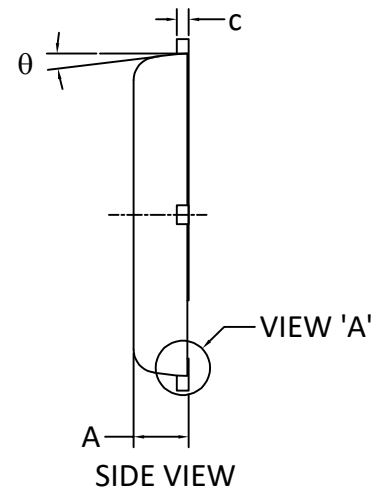
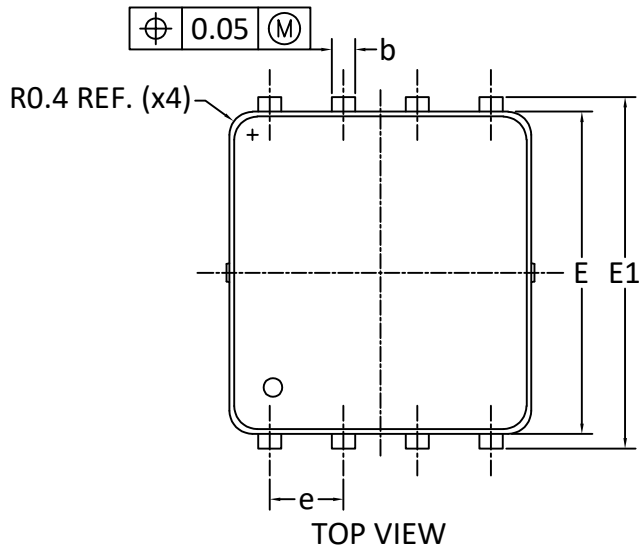
NOTE:

LOGO - AOS Logo
66920 - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

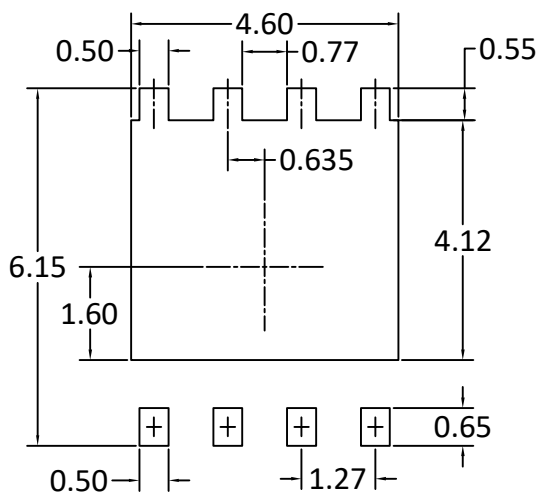
PART NO.	DESCRIPTION	CODE
AONS66920	Green product	66920



DFN5x6_8L_EP1_P PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	-	0.05	0.000	-	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0.00	-	0.15	0.000	-	0.006
L2	0.68 REF			0.027 REF		
θ	0°	-	10°	0°	-	10°

NOTE:

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
3. THIS PACKAGE WAS QUALIFIED USING IR REFLOW PROCESS (JEDEC STANDARD). FOR USAGE
IN OTHER SOLDERING PROCESSES, PLEASE CONTACT LOCAL AOS REPRESENTATIVES.



ALPHA & OMEGA
SEMICONDUCTOR

AOS Semiconductor Product Reliability Report

AONS66920, rev A

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

Dec, 2018

This AOS product reliability report summarizes the qualification result for AONS66920. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AONS66920 passes AOS quality and reliability requirements. The released product will be categorized by the process family and be routine monitored for continuously improving the product quality.

I. Reliability Stress Test Summary and Results

Test Item	Test Condition	Time Point	Total Sample Size	Number of Failures	Reference Standard
HTGB	Temp = 150°C , Vgs=100% of Vgsmax	168 / 500 / 1000 hours	462 pcs	0	JESD22-A108
HTRB	Temp = 150°C , Vds=100% of Vdsmax	168 / 500 / 1000 hours	462 pcs	0	JESD22-A108
Precondition (Note A)	168hr 85°C / 85%RH + 3 cycle reflow@260°C (MSL 1)	-	4620 pcs	0	JESD22-A113
HAST	130°C , 85%RH, 33.3 psia, Vds = 80% of Vdsmax up to 42V	96 hours	693 pcs	0	JESD22-A110
H3TRB	85°C , 85%RH, Vds = 80% of Vdsmax	1000 hours	693 pcs	0	JESD22-A101
Autoclave	121°C , 29.7psia, RH=100%	96 hours	924 pcs	0	JESD22-A102
Temperature Cycle	-65°C to 150°C , air to air,	1000cycles	924 pcs	0	JESD22-A104
HTSL	Temp = 150°C	1000 hours	693 pcs	0	JESD22-A103
IOL	$\Delta T_j = 100^\circ\text{C}$	15000 cycles	693 pcs	0	MIL-STD-750 Method 1037

Note: The reliability data presents total of available generic data up to the published date.

Note A: MSL (Moisture Sensitivity Level) 1 based on J-STD-020

II. Reliability Evaluation

FIT rate (per billion): 3.82

MTTF = 29919 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size. Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $\text{Chi}^2 \times 10^9 / [2 (N) (H) (Af)] = 3.82$

MTTF = $10^9 / \text{FIT} = 29919$ years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval

N = Total Number of units from burn-in tests

H = Duration of burn-in testing

Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)

Acceleration Factor **[Af]** = $\text{Exp} [E_a / k (1/T_j u - 1/T_j s)]$

Acceleration Factor ratio list:

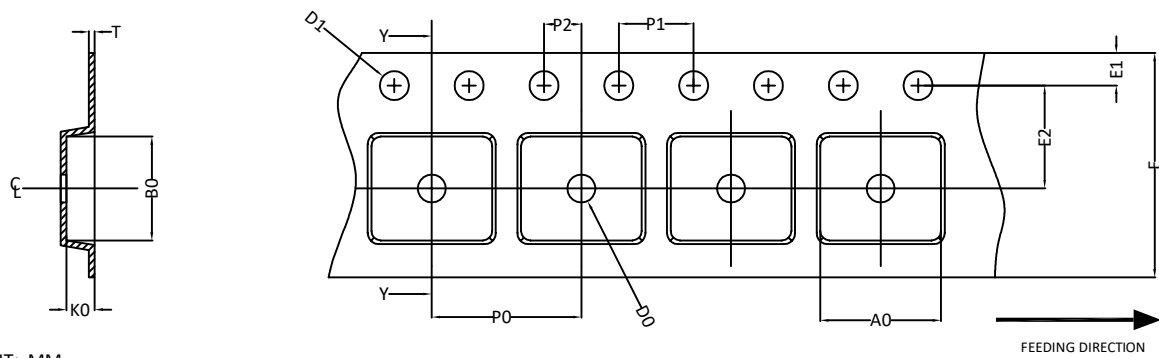
	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	259	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16

Tj u = The use junction temperature in degree (Kelvin), K = C+273.16

k = Boltzmann's constant, $8.617164 \times 10^{-5} \text{ eV} / \text{K}$

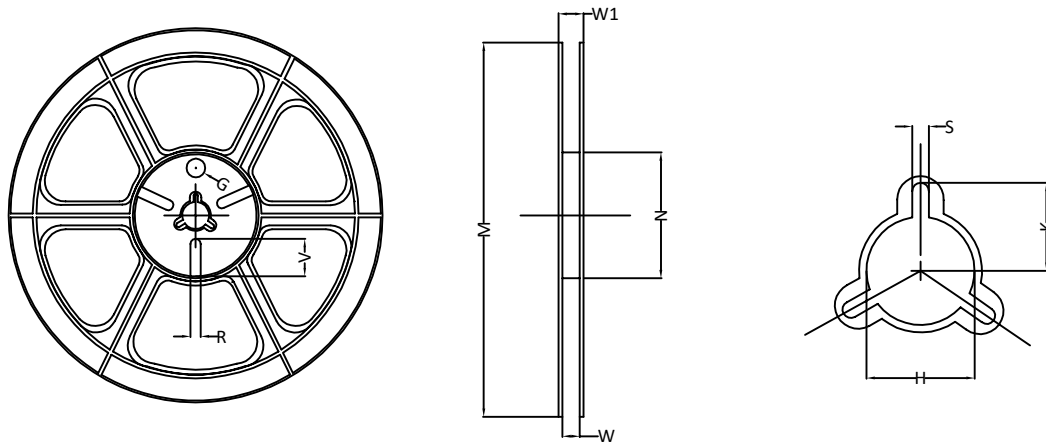
DFN5x6 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN5x6 (12 mm)	6.30 ±0.10	5.45 ±0.10	1.30 ±0.10	1.50 MIN.	1.55 ±0.05	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

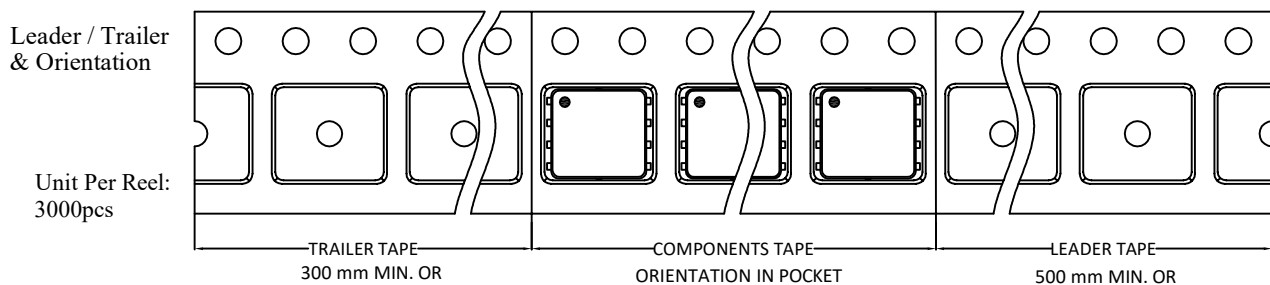
DFN5x6 Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.00 ±0.50	Ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	Ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	---	---	---

DFN5x6 Punch Package Tape



DFN5x6 Sawing Package (Except DFN5x6 7L EP1 TEP1 S/DFN5x6 2L EP3 TEP1 S /DFN5x6 8L EP1 TEP1 S/DFN5x6 8L EP1 TEP2 S/DFN5x6 8L EP2 TEP1 S/DFN5x6A 8L EP2 TEP1 S)Tape

