Si82Ax Single-Channel Isolated Gate Driver with 1 Amp Drive

The Si82Ax family consists of single-channel isolated gate drivers, offering a feature-rich and easy-to-use solution for various power applications. The Si82Ax series comprises devices with either a single output or split outputs, allowing for independent control of the output rise and fall times. These drivers can operate with a 3 to 20 V input supply and a maximum gate driver supply voltage of 30 V. The inputs are CMOS, which provides robust noise margin.

The Si82Ax is ideal for driving power silicon MOSFETs and IGBTs used in various switched power and motor control applications. These drivers utilize Skyworks' proprietary silicon isolation technology, supporting up to 6 kV_{RMS} for 1-minute isolation voltage. This technology enables high CMTI (200 kV/µs), lower propagation delays and skew, little variation with temperature and age, and tight part-to-part matching. The Si82Ax family offers longer service life and higher reliability than optocoupled gate drivers.

The output stage operates as a voltage source with robust current output across operating conditions. The output stage features voltage-mode drive technology using a familiar current-limiting resistor, allowing power designers to optimize for switching speed, emissions control, and overshoot limitation. The driver family also offers features, such as Undervoltage Lockout (UVLO), input overlap protection, and defined output states in all operating conditions.

Automotive Grade is available. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Applications

- Si MOSFET and IGBT gate drive
- UPS inverters
- Onboard chargers
- Solar (PV) inverters
- Energy Storage systems
- Motor drives

Safety Regulator Approvals (Pending)

- UL 1577 recognized
  - Up to 6000 V_{RMS} for one minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

Key Features

- Wide input range of 3 to 20 V
- Wide gate supply voltage of 5 to 30 V
- CMOS input with selectable deglitch filter
- Overlap protection with VI+/VI– inputs
- Safety by default with VI/EN inputs
- Voltage mode drive
- Unipolar or bipolar output voltages
- CMTI > 200 kV/µs
- 1500 V_{RMS} working voltage
- Optimized UVLOs of 4 V, 8 V, 12 V, and 15 V
- 4 kV HBM ESD rating
- No unknown output states
- 40 ns propagation delay with 5 ns part-to-part skew
- 6 kV_{RMS} safety rated isolation
- 10 kV bipolar surge
- Wide temperature range: –40 to 125 °C
- Narrow-body 8-pin SOIC and wide-body 8-pin SOIC packages
- AEC-Q100 qualification
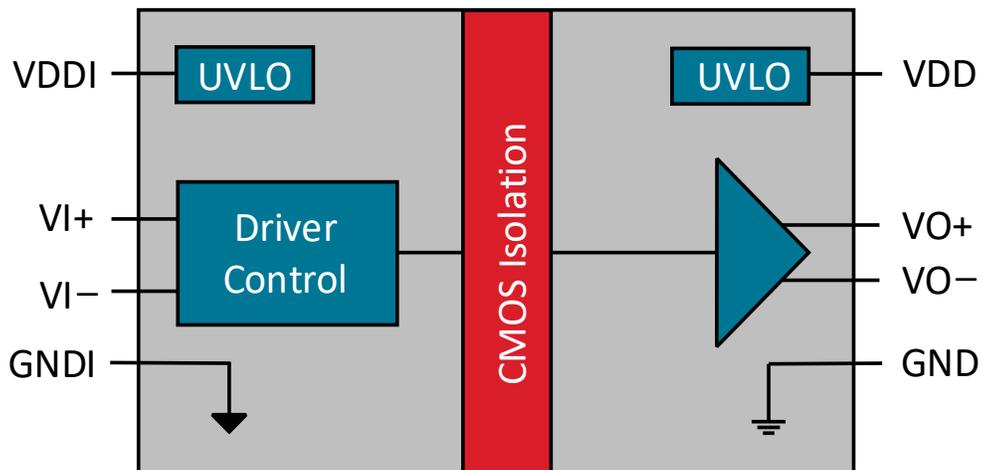- Automotive-grade OPNs available

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.
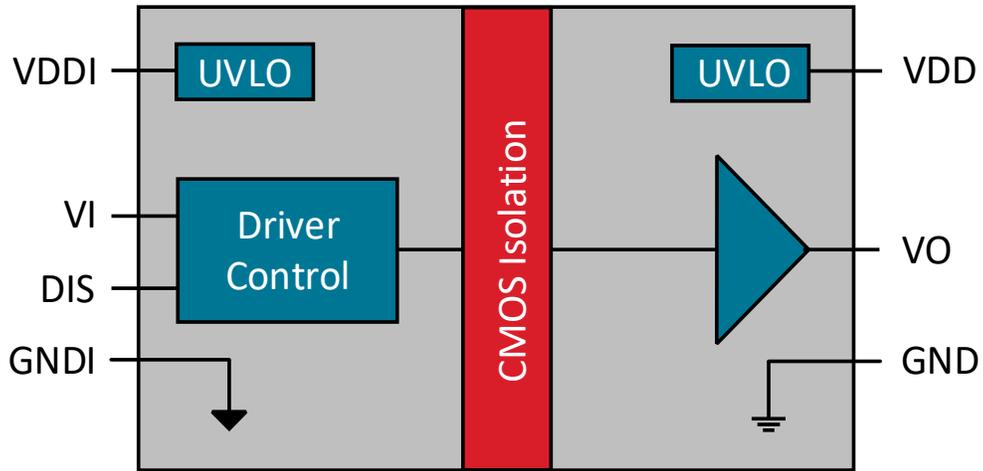
Si82A28x
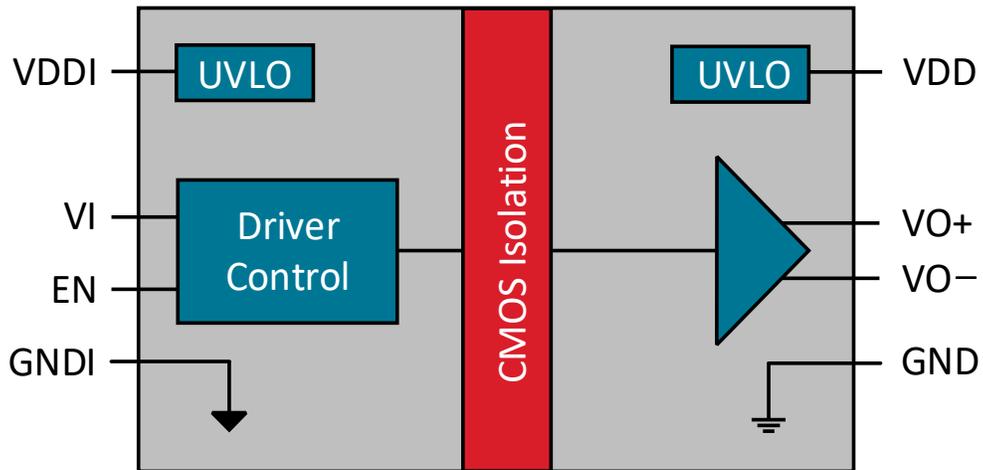
Si82A30x

Si82A40x/43x

1. Pin Descriptions

1.1. Device Pinouts

The Si82Ax consists of multiple dies in packages with different bond-outs for different customer needs. Each bond-out corresponds to a pin-out below. See "10. Ordering Guide" on page 42 for the part numbers and features of these products.

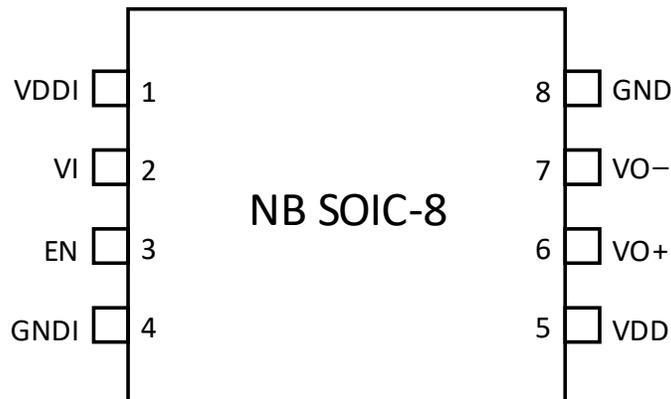### 1.1.1. NB SOIC-8 Pinouts

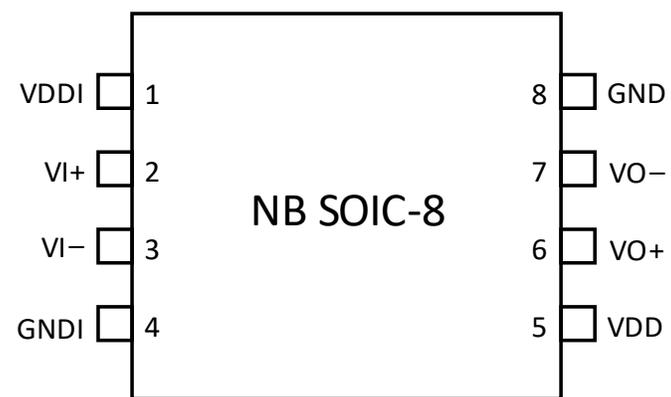**Figure 1. Si82A28x Pinout**

Figure 2. Si82A30x Pinout

Figure 3. Si82A40x Pinout

1.1.2. SSO-8 Pinouts

Figure 4. Si82A30x Pinout

Figure 5. Si82A40x Pinout

Figure 6. Si82A43x Pinout

1.2. Pin Details

Table 1. Si82Ax Pin Details

Pin Name	Pin Description
VDDI	Logic input power supply.
GNDI	Logic input ground terminal.
VI	Non-inverting logic input terminal for the driver.
VI+	Non-inverting complimentary digital logic input terminal for the driver. Connect to VDDI when using the inverting input alone, or it should be connected to the inverting input of the HI/LO side driver in a half-bridge configuration for overlap protection.
VI–	Inverting complimentary digital logic input terminal for the driver. Connect to GNDI when using the non-inverting input alone, or it should be connected to the non-inverting input of the HI/LO side driver in a half-bridge configuration for overlap protection.
EN	Device ENABLE. When asserted, the device is enabled to perform in normal operating mode. When deasserted, this input unconditionally drives the output V_O or V_{O-} low. When high, the device is enabled to perform in normal operating mode.
DIS	Device DISABLE. When asserted, this input unconditionally drives the output V_O or V_{O-} low. When deasserted, the device is enabled to perform in normal operating mode.
VDD	Gate driver power supply.
GND	Gate driver ground.
VO	Combined pull-up and pull-down output for the gate driver.
VO+	Pull-up (sourcing) output for the gate driver.
VO–	Pull-down (sinking) output for the gate driver.

2. Device Overview

The Si82Ax is an isolated single-channel gate driver available in a single- or split-output configuration. Each configuration can be purchased with either an asynchronous enable or disable input. Additional features such as undervoltage lockout (UVLO) level and deglitch filter time can be configured through device selection. Refer to "10. Ordering Guide" on page 42 for more details. Safety-rated isolation is provided from logic input to gate driver output by a pair of high-voltage silicon dioxide (SO_2) capacitors. These capacitors are duplicated to form a differential path for signals modulated with an RF carrier and using an on-off keying (OOK) modulation scheme. This optimizes for fault tolerance and timing performance between input and output.

The digital logic inputs are high-voltage capable, CMOS-compatible, Schmitt triggered, and deglitched for high noise immunity and a wide range of compatibility. See "4.4. Logic Input Signals" on page 11 for more details. The gate driver outputs operate as a voltage source. Output current is adjusted through the selection of gate resistors. See "5.1. Recommended Application Circuits" on page 14 for more information.
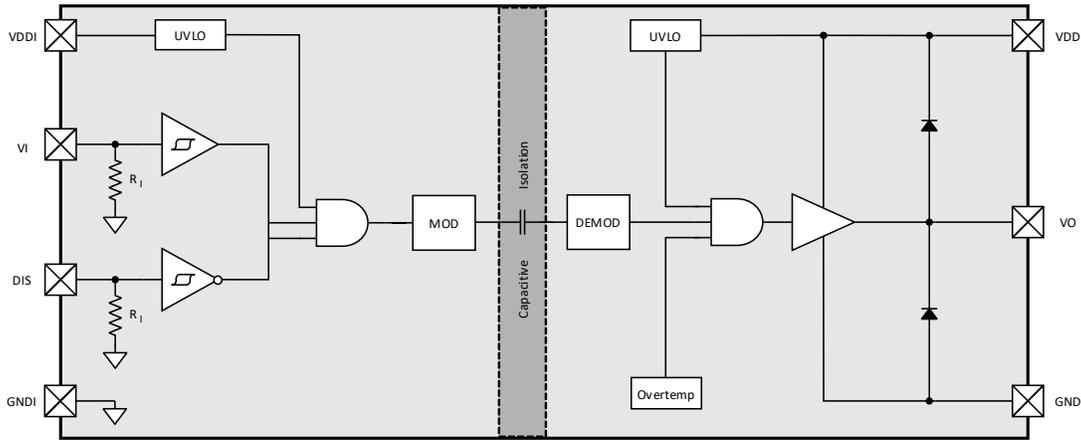
3. Functional Block Diagrams

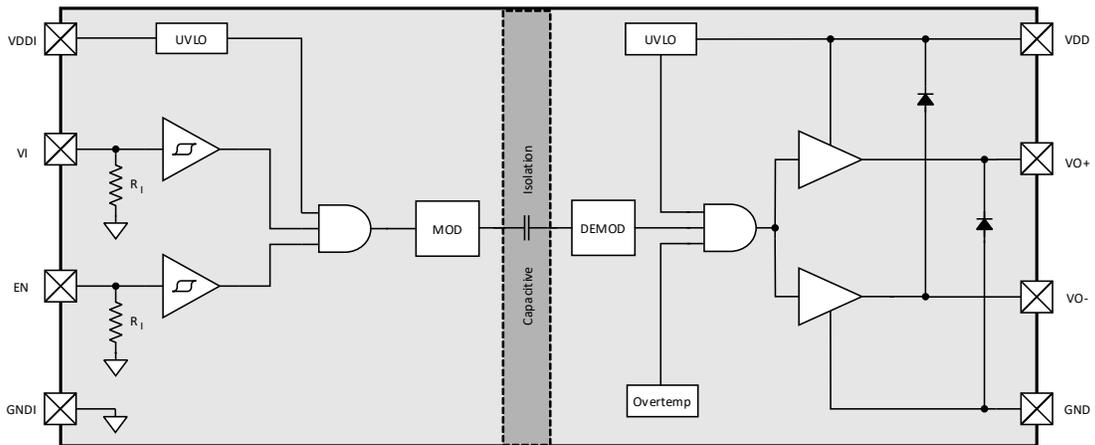**Figure 7. Si82A28x Device with Single Output and Disable Input**

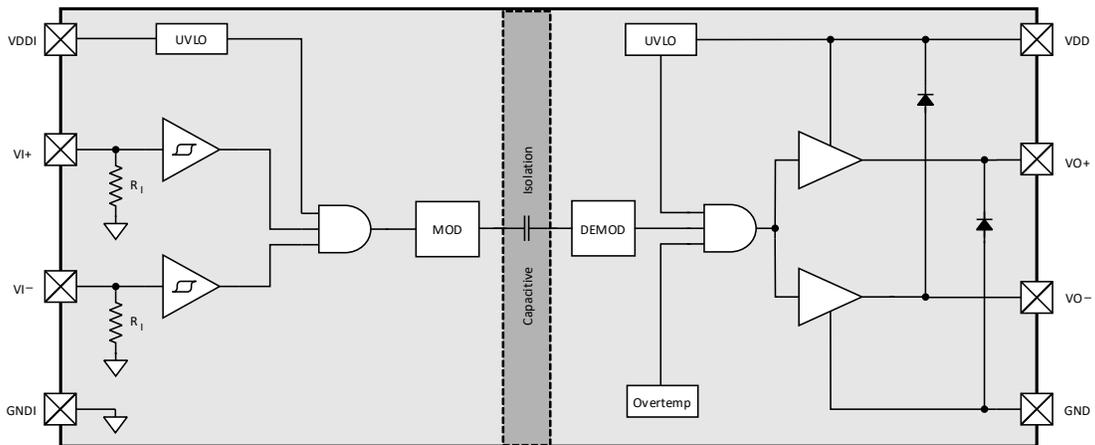**Figure 8. Si82A30x with Split Output and Enable Input**

Figure 9. Si82A40x with Split Output and Complimentary Input

4. Device Operation

This section describes the capabilities of the device and how it should be used to achieve different goals within a design. Refer to "5.1. Recommended Application Circuits" on page 14 and "10. Ordering Guide" on page 42 for information on how to best utilize each device for different applications.

4.1. Truth Tables

The following tables describe the logical behavior of the Si82Ax Isolated Gate Driver devices.

Table 2. Si82A28x Truth Table

Inputs[1]		Power Supply State[2]		Output[3]
VI	DIS	VDDI[4]	VDD[5]	VO
H	E	P	P	H
L	X	—	—	L
X	D	—	—	L
X	X	—	NP	L

1. "X" is any logic value; "H" is a logic high (true) value, and "L" is a logic low (false) value. "E" indicates the driver is enabled (DIS = L or EN = H), "D" indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see "4.7. Shutdown Clamp" on page 12) if the gate driver's power supply (VDD) is not powered (NP).
4. "Not powered" (NP) state is defined as $VDDI < VDDI_{UV}$. "Powered" (P) state is defined as $VDDI > VDDI_{UV}$.
5. "Not powered" (NP) state is defined as $VDD < VDD_{UV}$. "Powered" (P) state is defined as $VDD > VDD_{UV}$.

Table 3. Si82A30x Truth Table

Inputs[1]		Power Supply State[2]		Outputs[3]	
VI	EN	VDDI[4]	VDD[5]	VO+	VO−
H	E	P	P	H	High-Z
L	X	—	—	High-Z	L
X	D	—	—	High-Z	L
X	X	—	NP	High-Z	L

1. "X" is any logic value; "H" is a logic high (true) value, and "L" is a logic low (false) value. "E" indicates the driver is enabled (DIS = L or EN = H), "D" indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see "4.7. Shutdown Clamp" on page 12) if the gate driver's power supply (VDD) is not powered (NP).
4. "Not powered" (NP) state is defined as $VDDI < VDDI_{UV}$. "Powered" (P) state is defined as $VDDI > VDDI_{UV}$.
5. "Not powered" (NP) state is defined as $VDD < VDD_{UV}$. "Powered" (P) state is defined as $VDD > VDD_{UV}$.

Table 4. Si82A40x Truth Table

Inputs[1]		Power Supply State[2]		Outputs[3]	
VI+	VI−	VDDI[4]	VDD[5]	VO+	VO−
H	L	P	P	H	High-Z
L	X	—	—	High-Z	L
X	H	—	—	High-Z	L
X	X	—	NP	High-Z	L

1. "X" is any logic value; "H" is a logic high (true) value, and "L" is a logic low (false) value. "E" indicates the driver is enabled (DIS = L or EN = H), "D" indicates the driver is disabled (DIS = H or EN = L). Input pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the power supply state.
2. "NP" is the "not powered" state; "P" is the "powered" state, and "—" is an irrelevant state.
3. "H" is a logic high (true) value, and "L" is a logic low (false). The logic low (L) value is enforced by the shutdown clamp (see "4.7. Shutdown Clamp" on page 12) if the gate driver's power supply (VDD) is not powered (NP).
4. "Not powered" (NP) state is defined as $VDDI < VDDI_{UV}$. "Powered" (P) state is defined as $VDDI > VDDI_{UV}$.
5. "Not powered" (NP) state is defined as $VDD < VDD_{UV}$. "Powered" (P) state is defined as $VDD > VDD_{UV}$.

4.2. Power Sequence and Timing Behavior

The device exhibits different timing behavior depending on the state of the power supplies as well as the driver inputs. Figure 10, "Gate Driver Timing Behavior," below shows how the analog power supply voltages are plotted against the digital input and output state of the device, with relevant device timings listed.
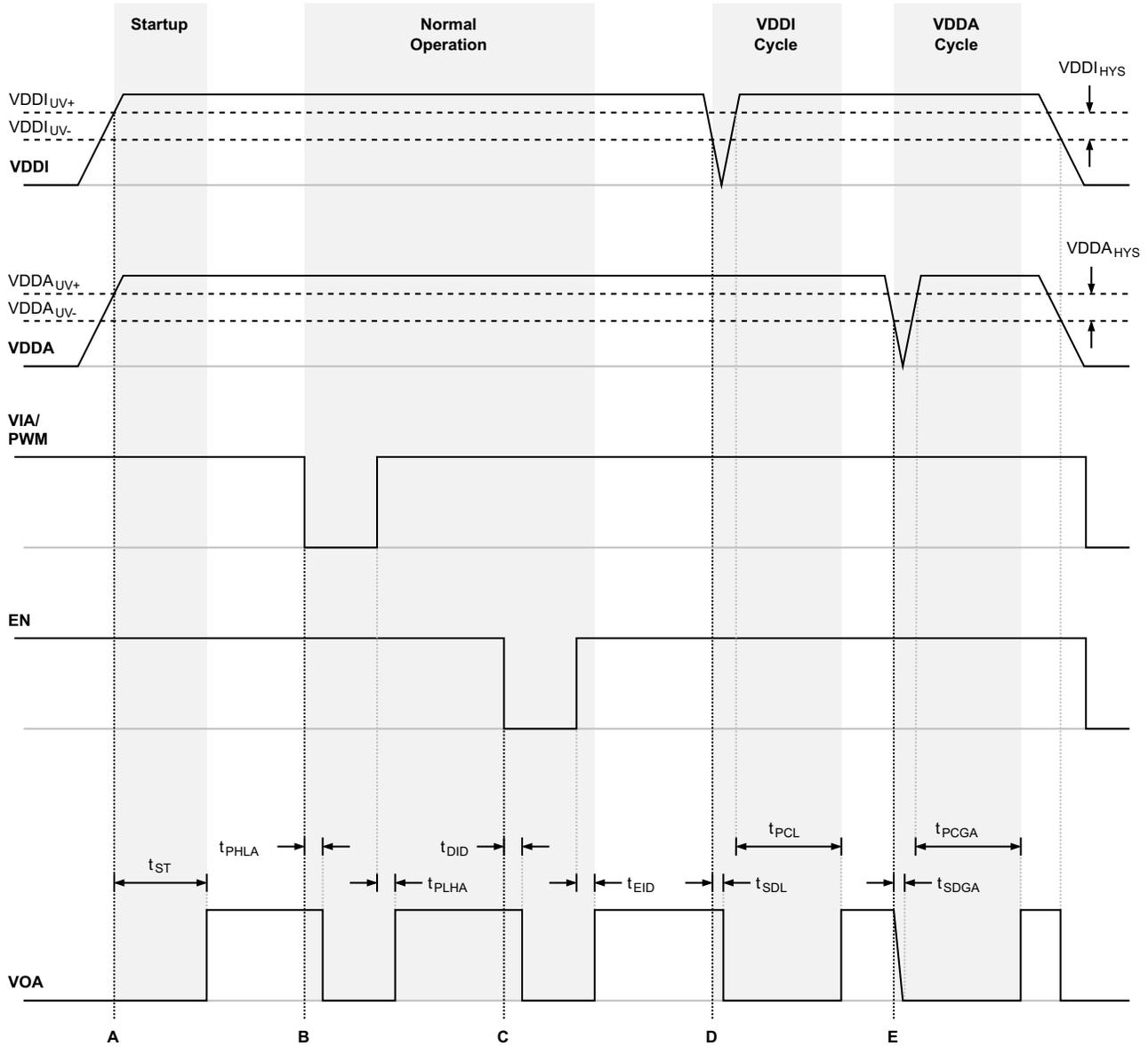

Figure 10. Gate Driver Timing Behavior

Note that this diagram shows the timing relationship between VDDA, VIA/PWM and VOA. However, the same timing relationship applies for VDDB, VIB and VOB.

4.3. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDDI or VDD is below its specified operating circuits range. The power supplies associated with the logic input and the gate driver each have undervoltage lockout monitors. The device's logic input enters UVLO when VDDI ≤ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The gate driver output (VO/VO+/VO−/MC) remains low when the logic input supply of the device is in UVLO and its respective power supply (VDD) is within the specified range. See "4.2. Power Sequence and Timing Behavior" on page 10 and "4.1. Truth Tables" on page 8 for more details.

4.4. Logic Input Signals

4.4.1. Control Inputs

VI, VI+, VI−, EN, and DIS inputs are CMOS level-compatible, active-high inputs. When VDDI is in undervoltage lockout (UVLO), the inputs of these pins are ignored and the gate driver's output is pulled low. For VI input devices, the output follows the corresponding VI input logic. For complimentary input devices with a split output, VO+ is high and VO− is High-Z when VI+ input is high and VI− input is low, and VO+ is High-Z and VO− is low when the VO− input is high. For complimentary input devices with a combined output and Miller clamp, VO is high when VI+ input is high and VI− input is low, and VO and MC are low when VO− input is high. Refer to "4.1. Truth Tables" on page 8 for detailed information on overlap protection behavior.

4.4.2. Enable and Disable Input

For devices with an enable (EN) input, when the EN input is driven low, it unconditionally drives VO− low and VO+ to High-Z regardless of the states of VI. Device operation terminates within t_{DID} after EN falls below VIL and resumes within tEID after EN rises above VIH. For devices with a disable (DIS) input, when the DIS input is brought high, it unconditionally drives VO/VO-/MC low and VO+ High-Z regardless of the states of VI. Device operation terminates within tDID after DIS rises above VIH and resumes within tEID after DIS falls below VIL. See "4.2. Power Sequence and Timing Behavior" on page 10 for more details. The EN and DIS inputs have no effect if VDDI is below its UVLO level (i.e., VO/VO-/MC remain low and VO+ remains High-Z).

4.4.3. Deglitch Filter

A deglitch feature is provided on some devices. The deglitch feature ignores input noise with a duration shorter than the deglitch filter setting, but also introduces additional propagation delay. See "6.2.4. Timing Characteristics" on page 22 for the delays associated with this feature. The deglitch filter can be adjusted by selecting different product options. See "10. Ordering Guide" on page 42 for more details.

4.5. Short-Circuit Clamp

The short circuit clamp is used to clamp voltages at the driver output (VOA/B) to slightly higher than the VDDA/B voltage during short circuit conditions. The short circuit clamp helps protect the driven switch gate from overvoltage breakdown or degradation. The clamp is implemented by adding a diode connection between VOA/B and the VDDA/B pins inside the driver. See "6.2.3. Gate Driver Characteristics" on page 21 for detailed specifications of this clamping feature. External diodes between VOA/B and VDDA/B can increase current conduction capability as needed.

4.6. Thermal Protection

The device includes a temperature sensor in each gate driver. Each sensor is monitored continuously. If the temperature exceeds the Trigger Temperature (T_{SD+}), a thermal shutdown fault will occur, and the driver will pull low. After 1 ms, if the driver temperature fails to fall below the Reset Temperature (T_{SD-}), the driver will pull weakly low. The driver will continuously pull weakly low until the temperature falls below T_{SD-}. Once the fault is removed, normal operation resumes.

4.7. Shutdown Clamp

The device includes a voltage clamp between the gate driver output (VOA/B) and ground (GNDA/B) when the gate driver is unpowered (VDDA/B = high-Z). This clamp is sometimes referred to as an "active pull-down clamp". It provides a path to ground for transient currents which could otherwise cause parasitic turn-on of a driven switch when the gate driver is unpowered. See "6.2.3. Gate Driver Characteristics" on page 21 and "4.1. Truth Tables" on page 8 for details.

4.8. Short Circuit Clamp

The short circuit clamp is used to clamp voltages at the driver output (VO/VO+) to slightly higher than the VDD voltage during short circuit conditions. The short circuit clamp helps protect the driven switch gate from overvoltage breakdown or degradation. The clamp is implemented by adding a diode connection between VO/VO+ and the VDD pin inside the driver. See "6.2.3. Gate Driver Characteristics" on page 21 for detailed specifications of this clamping feature. External diodes between VO/VO+ and VDD can increase current conduction capability as needed.

4.9. Thermal Protection

The device includes a temperature sensor in the gate driver. The sensor is monitored continuously. If the temperature exceeds the Trigger Temperature (T_{SD+}), a thermal shutdown fault will occur, and the driver will pull low. After 1 ms, if the driver temperature fails to fall below the Reset Temperature (T_{SD-}), the driver will pull weakly low. The driver will continuously pull weakly low until the temperature falls below T_{SD-}. Once the fault is removed, normal operation resumes.

4.10. Shutdown Clamp

The device includes a voltage clamp between the gate driver output or Miller clamp pin (VO/VO– or MC) and ground (GND) when the gate driver is unpowered (VDD = High-Z). This clamp is sometimes referred to as an "active pull-down clamp". It provides a path to ground for transient currents, which could otherwise cause parasitic turn-on of a driven switch when the gate driver is unpowered. See "6.2.3. Gate Driver Characteristics" on page 21 and "4.1. Truth Tables" on page 8 for details.

4.11. ESD Structure

The Si82Ax device's I/O pin electrostatic discharge (ESD) diodes and associated supply pin ESD clamp diodes are illustrated in Figure 11 and Figure 12 below. On the logic input side, a pair of ESD protection diodes are used on each input pin, and all upper diodes are connected to one shared clamp diode. This structure prevents the VDDI pin from being powered up through the input pin when the VDDI power supply is lost. The other clamp diode is present between the VDDI pin and the GNDI pin. The ESD structure of the gate driver output is similar to the logic input, except that the gate driver output's upper ESD diode is connected to a clamp diode at the VDD pin.
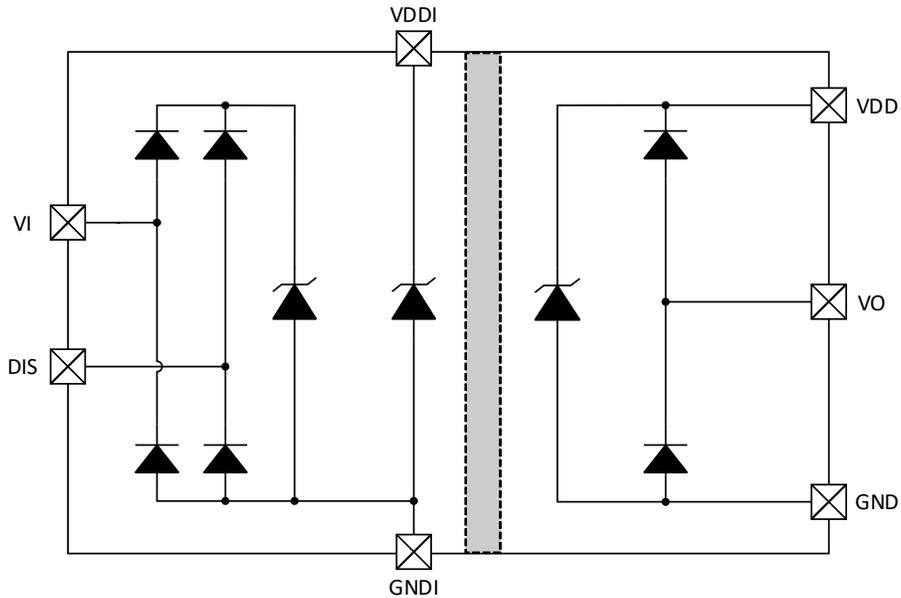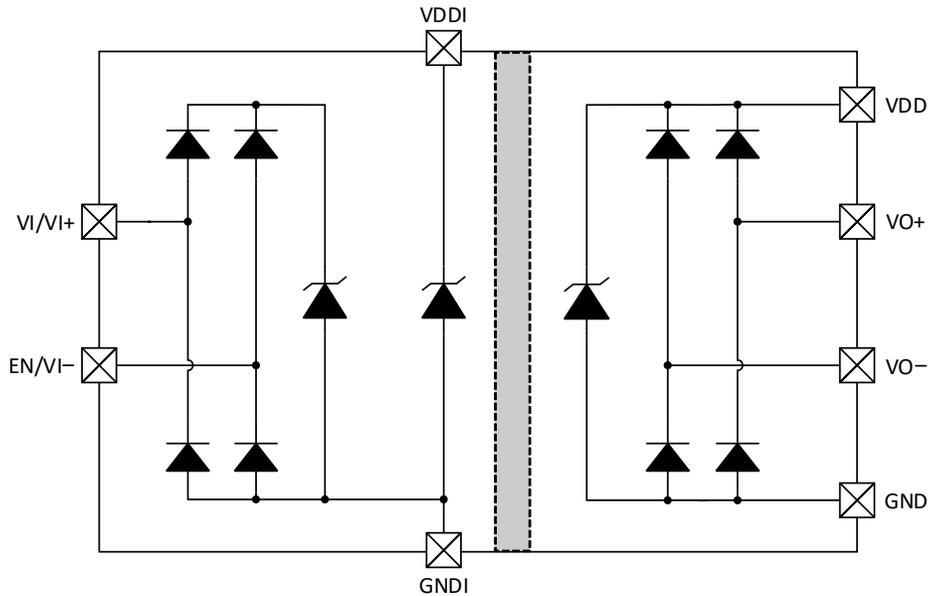
Figure 11. Si82A28x Device ESD Structure

Figure 12. Si82B30x/40x Device ESD Structure

5. Application Information

The Si82Ax is designed to be both flexible and robust to meet a wide range of application requirements, safely survive overloads, and rapidly recover normal operation. To achieve these objectives, the appropriate Si82Ax device must be selected and its circuit carefully designed.

5.1. Recommended Application Circuits

Figure 13 below and Figure 14 on page 15 illustrate Si82Ax typical application circuits. The controller provides the Si82Ax input signal and can also use the EN/DIS signal to turn off the driver immediately once a system fault is detected.

On the gate driver side, the Si82Ax device's output current is controlled by the external gate resistors R15 and R21. The peak sourcing current for gate drivers is shown in Equation 1, and the peak sinking current for the gate driver is shown in Equation 2.

$$\frac{VDD}{R15 \parallel R21 + R_{ON-}}$$

Equation 1. Peak Sourcing Current for Gate Drivers

$$\frac{VDDA}{R15 + R_{ON+}}$$

Equation 2. Peak Sinking Current for Gate Driver

The gate resistor values should be selected to meet the gate voltage rise-time/fall-time requirement based on the actual capacitive loading of FET Q1. When the package supports the split output, the D1 diode can be eliminated. On the part numbers which has the dedicated MC (Miller clamp) pin, the MC pin should be connected to FET Q1's gate.

The high-voltage Y2-class capacitor (not shown in the diagrams) between the logic input reference (GNDI) and the gate driver reference (GND) is recommended if additional radiated emissions or electrostatic discharge (ESD) mitigation is desired. The typical value for Y2 capacitor is between 47 pF and 100 pF. See "AN1131: Design Guide for Reducing Radiated and Conducted Emissions in Isolated Systems Using Skyworks' Isolators" for additional techniques to mitigate radiated and conducted emissions. Note that the Si82Ax device provides excellent common-mode transient immunity (CMTI) without employing any additional components or techniques. However, if your application requires extremely high common mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI). This will help improve the CMTI performance.
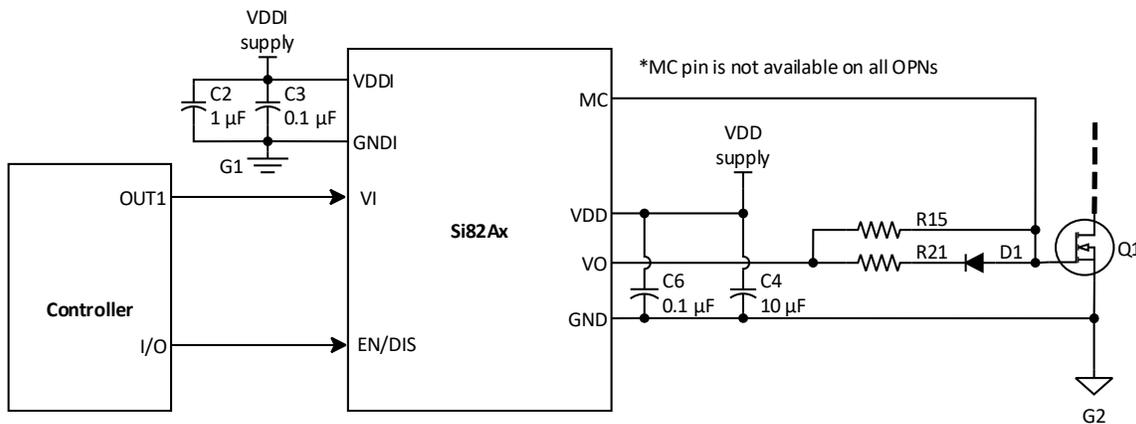

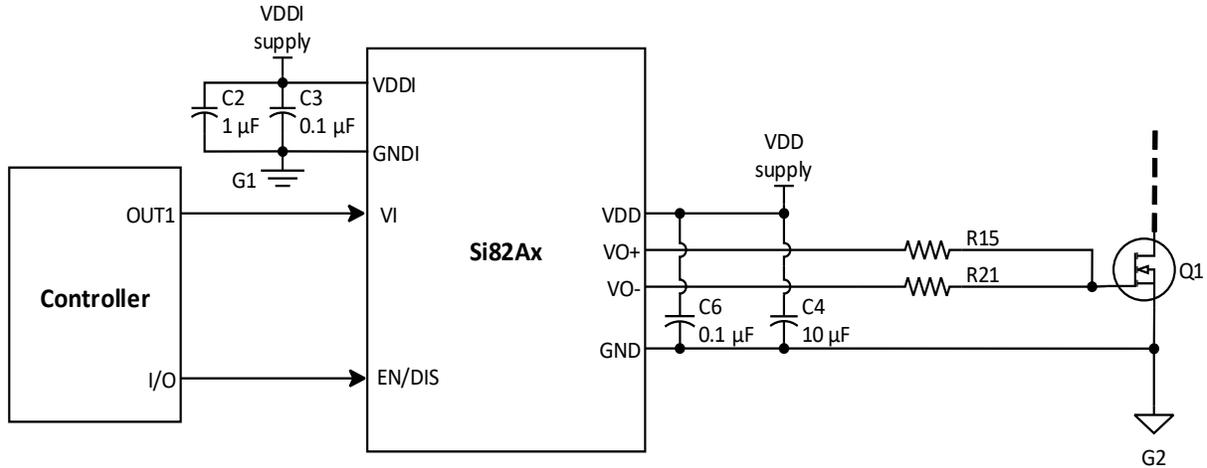**Figure 13. Si82Ax Single Supply Application**

Figure 14. Si82Ax Split Output Application

The diagram shown in Figure 15, "Bipolar Output Connection," on page 15 is similar to the above circuits except that the drivers produce the bipolar V_{GS} output voltage. The bipolar V_{GS} output requires the system to provide positive and negative voltage sources. Please note that the bootstrap circuit cannot be used to share the low-side voltage sources with the high-side gate driver for a bipolar V_{GS} output application. In this example, +15 V and −5 V sources are used. The voltage sources' reference G2 is electrically connected to FET Q1's source.

For the bipolar V_{GS} output application, the additional bypass capacitors form a capacitor divider in order to shorten the current flow loop. These capacitors should be placed close to the Si82Ax device's output power pins (VDD/GND). The ac component of the gate drive current flows from the VDDA net to the Si82Ax device's VDD pin, VO pin, external gate resistor, Q1's gate, Q1's source, the midpoint of capacitors C16 and C17, and back to VDDA. Since the original bypass capacitors, C6 and C4, do not connect to reference G2 (which is connected to FET Q1's source), without capacitor C16, the return current needs to travel further to the system's +15 V source to complete the loop. This prolonged loop increases the chance of radiated emissions.
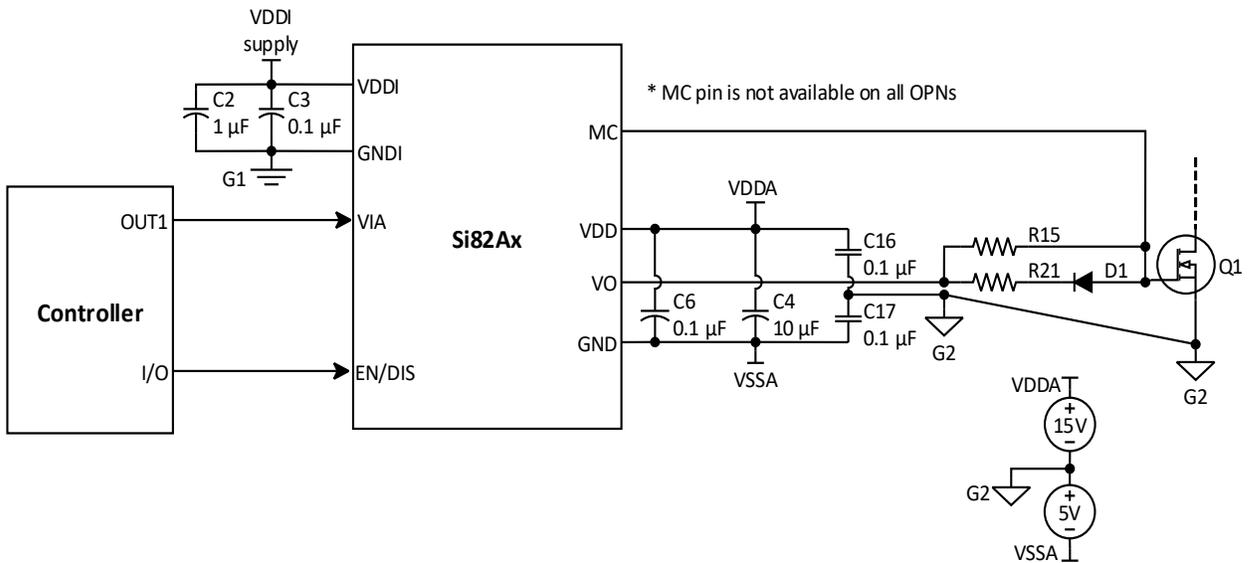
Figure 15. Bipolar Output Connection

5.2. Layout Considerations

The layout considerations are divided into general considerations for the entire device, the logic input side of the device, and the gate driver side. Refer to "5.1. Recommended Application Circuits" on page 14 for specific parts referenced.

5.2.1. General Considerations

- The bypass capacitors (usually 0.1 µF || 10 µF) should be placed close to the device's power supply pins and connected to the device with thick and short traces.
- The isolation barrier should have the required distance for the traces, power planes, ground planes, and copper areas on the device's logic input and gate drive sides.
- Safety isolation between two Si82Ax drivers is usually not required. If the system needs the safety isolation between two drivers, the trace, power plane, ground plane, and the copper area between the two gate drivers should have the required distance. Even though safety isolation between two drivers is usually not required, to avoid arcing through the air, the traces operating at high voltage should have some distance (approximately 1 mm per 1 kV) from the low voltage signals
- The Si82Ax device is often used in high-power systems with significant switching current and transient voltage. Attention should be paid to the proximity and orientation of the Si82Bx device and any high-current switching circuits. This should also apply to the traces and components surrounding the Si82Bx device to avoid unwanted noise coupling.

5.2.2. Logic Input Considerations

- If the application requires extremely high common mode transient immunity (CMTI) performance, it is recommended to add a 10 nF capacitor between each of the logic input pins and the logic input ground (GNDI), including the no connect (NC) pins. This will help improve the CMTI performance.
- Using ≥6 mil trace width on all logic input pins is recommended. The interconnection between the controller and the Si82Ax device should be kept from any noisy signals in the system.

5.2.3. Gate Driver Considerations

- If the system is designed to provide a bipolar V_{GS} output, additional bypass capacitors (C16 and C17 in Figure 15, "Bipolar Output Connection," on page 15) are required to minimize the return path length of the gate drive signals.
- It is recommended to use ≥20 mil trace width for the VO gate driver trace and its return path.
- For a unipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/emitter to the Si82Ax device's gate driver ground pin (GND). Explicitly use ≥20 mil trace width for this return current path and route this trace close to the VO gate driver trace to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a bipolar V_{GS} output, the return path of the V_{GS} gate drive signal is from the power device's source/emitter to the midpoint of capacitors C16 and C17. Therefore, these capacitors must be placed close to the Si82Ax device to minimize this current loop. Explicitly use ≥20 mil trace width for the return current path and route this return trace close to the VO gate driver trace to reduce the loop area of the whole V_{GS} gate drive signal. Moreover, it is a good practice to set the copper keep-out region along the return path trace so the system ground copper will not flood over this return trace.
- For a multiple-layer PCB design, ground and power planes are recommended to create a power supply current path with the least inductance. If there is no dedicated power or ground plane on the gate driver side, please use ≥20 mil trace width for the power supply connections.
- If the design utilizes Y2 capacitor between the logic input and the gate driver, the Y2 capacitor across the isolation barrier should be placed as close as possible to the sides of the Si82Ax device without pins.

5.3. Power Dissipation Considerations

The device's average power dissipation is often required in order to estimate the silicon junction temperature and can be estimated using the equation provided in "AN1339: Driver Power Dissipation Considerations". To solve the equation, the intended supply voltages, the load characteristics, the gate resistor values, and the switching frequency need to be collected. Skyworks provides a Microsoft Excel® based calculator as part of AN1339 to easily estimate the device's power dissipation and silicon junction temperature.

6. Specifications

6.1. Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min	Max	Unit
Storage temperature	T_{STG}		−65	150	°C
Operating temperature	T_A		−40	125	°C
Junction temperature	T_J		—	150	°C
Logic input supply voltage	VDDI		−0.30	24.0	V
Gate driver supply voltage	VDD		−0.30	36.0	V
Input signal voltage	VI, VI+, VI−, EN, DIS		−0.30	VDDI + 0.30	V
	VI, VI+, VI−, EN, DIS	Transient for 100 ns[2]	−5.00	VDDI + 0.30	V
Output signal voltage	VO		−0.30	$V_{DD} + V_{SCC}$	V
		Transient for 200 ns[2]	−2.00	$V_{DD} + V_{SCC}$	V
Lead solder temperature		Duration = 10 s	—	260	°C
ESD per AEC-Q100					
Human body model	HBM		−4	4	kV
Charged device model	CDM		−2	2	kV

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This parameter is not subject to production test. It is guaranteed by characterization.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

6.2. Electrical Characteristics

The following tables provide electrical parametric data for this device.

6.2.1. Power Supply Characteristics

Table 6. Power Supply Characteristics[1]

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq$ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage						
Logic Input Supply	VDDI		3.00	—	20.0	V
Gate Driver Supply	VDD		5.00	—	30.0	V
Supply Current						
Logic Input Supply						
Quiescent Current	$IDDI_Q$	EN = logic low or DIS = logic high	—	0.81	1.27	mA
Active Current	IDDI	VIA = 1 MHz; 50% duty cycle	—	1.30	1.77	mA
Gate Driver Supply						
4 V Undervoltage Lockout (Si82AxxxGx) Devices						
Quiescent Current	IDD_Q	EN = logic low or DIS = logic high	—	1.50	2.46	mA
Active Current	IDD	VO = 1 MHz; 50% duty cycle; no load	—	2.90	10.4	mA
8 V Undervoltage Lockout (Si82AxxxBx) Devices						
Quiescent Current	IDD_Q	EN = logic low or DIS = logic high	—	1.52	2.46	mA
Active Current	IDD	VOA/B = 1 MHz; 50% duty cycle; no load	—	3.65	10.4	mA
12 V Undervoltage Lockout (Si82AxxxCx) Devices						
Quiescent Current	IDD_Q	EN = logic low or DIS = logic high	—	1.53	2.46	mA
Active Current	IDD	VO = 1 MHz; 50% duty cycle; no load	—	4.59	10.4	mA
15 V Undervoltage Lockout (Si82AxxxEx) Devices						
Quiescent Current	IDD_Q	EN = logic low or DIS = logic high	—	1.54	2.46	mA
Active Current	IDD	VO = 1 MHz; 50% duty cycle; no load	—	5.13	10.4	mA

Table 6. Power Supply Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Undervoltage Lockout						
Logic Input Supply						
Positive-Going Threshold	VDDI$_{UV+}$	VDDI rising	2.76	2.88	2.99	V
Negative-Going Threshold	VDDI$_{UV-}$	VDDI falling	2.64	2.78	2.94	
Threshold Hysteresis	VDDI$_{HYS}$		—	100	—	mV
Gate Driver Supply						
4 V Undervoltage Lockout (Si82AxxxGx) Devices						
Positive-Going Threshold	VDD$_{UV+}$	VDD rising	4.17	4.32	4.47	V
Negative-Going Threshold	VDD$_{UV-}$	VDD falling	3.97	4.12	4.26	
Threshold Hysteresis	VDD$_{HYS}$		—	200	—	mV
8 V Undervoltage Lockout (Si82AxxxBx) Devices						
Positive-Going threshold	VDD$_{UV+}$	VDD rising	7.81	8.07	8.41	V
Negative-Going Threshold	VDD$_{UV-}$	VDD falling	7.28	7.57	7.89	
Threshold Hysteresis	VDD$_{HYS}$		—	500	—	mV
12 V Undervoltage Lockout (Si82AxxxCx) Devices						
Positive-Going Threshold	VDD$_{UV+}$	VDD rising	11.5	11.9	12.4	V
Negative-Going Threshold	VDD$_{UV-}$	VDD falling	10.5	10.9	11.4	
Threshold Hysteresis	VDD$_{HYS}$		—	1.00	—	V
15 V Undervoltage Lockout (Si82AxxxEx) Devices						
Positive-Going Threshold	VDD$_{UV+}$	VDD rising	14.6	15.2	15.8	V
Negative-Going Threshold	VDD$_{UV-}$	VDD falling	14.1	14.7	15.3	
Threshold Hysteresis	VDD$_{HYS}$		—	450	—	mV

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either Gate Driver A or Gate Driver B.

6.2.2. Logic Input Characteristics

Table 7. Logic Input Characteristics

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Threshold						
High Input	V_{IH}	V_I, V_{I+}, $V_{I–}$, EN, DIS rising	V_{DDI} x 0.85	—	—	V
Low Input	V_{IL}	V_I, V_{I+}, $V_{I–}$, EN, DIS falling	—	—	VDDI x 0.22	V
Hysteresis	V_{HYS}	V_I, V_{I+}, $V_{I–}$, EN, DIS	V_{DDI} x 0.06	V_{DDI} x 0.15	—	V
Input Pull-Down Resistance	R_I	V_I, V_{I+}, $V_{I–}$, EN, DIS	152	223	279	kΩ
Input Leakage Current	$|I_{LKG}|$	V_I, V_{I+}, $V_{I–}$, EN, DIS	—	—	131	µA

6.2.3. Gate Driver Characteristics

Table 8. Gate Driver Characteristics[1]

Operating range for the following specifications: V_{DDI} = 3.0–20 V; V_{DD} = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz

Typical specifications: V_{DDI} = 5 V; V_{DD} = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage						
Logic high (sourcing)	V_{OH}	I_O = –20 mA	V_{DD} x 0.96	—	—	V
Logic low (sinking)	V_{OL}	I_O = 20 mA	—	—	0.132	V
Output Resistance						
Logic high (sourcing)	R_{ON+}		2.79	4.50	8.58	Ω
Logic low (sinking)	$R_{ON–}$		1.13	3.20	6.50	Ω
Peak Output Current						
Logic high (sourcing)	I_{O+}	V_{DD} = 6 V, V_O = 1.5 V	—	0.63	—	A
		V_{DD} = 10 V, V_O = 3 V	—	0.87	—	A
		V_{DD} = 15 V, V_O = 5 V	—	1.05	—	A
		V_{DD} = 18 V, V_O = 6 V	0.77	1.10	—	A
Logic low (sinking)	$I_{O–}$	V_{DD} = 6 V, V_O = 4.5 V	—	0.66	—	A
		V_{DD} = 10 V, V_O = 7 V	—	0.84	—	A
		V_{DD} = 15 V, V_O = 10 V	—	0.93	—	A
		V_{DD} = 18 V, V_O = 12 V	0.76	0.94	—	A
Switch Short Circuit Clamp						
Clamping voltage	V_{SCC}	$V_{OA/B} – V_{DDA/B}$ or $GND_{A/B} – V_{OA/B}$, $I_{OA/B}$ = 70 mA	—	70.0	—	mV
		$V_O – V_{DD}$ or $GND – V_O$, I_O = 500 mA, t_{SCC} = 10 µs	—	530	—	mV

Table 8. Gate Driver Characteristics[1]

Operating range for the following specifications: V_{DDI} = 3.0–20 V; V_{DD} = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz

Typical specifications: V_{DDI} = 5 V; V_{DD} = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices. T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal shutdown						
Threshold temperature	T_{SD+}	T_J rising	—	163	—	°C
Release temperature	T_{SD-}	T_J falling	—	131	—	°C
Shutdown clamp output voltage	V_{SDC}	V_{DD} = high-Z, I_O = 20 mA	—	1.78	2.07	V

1. Adding the suffix +/- to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to the pull-up (sourcing) output V_{O+} or the pull-down (sourcing) output V_{O-}.

6.2.4. Timing Characteristics

Table 9. Timing Characteristics[1]

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; F_{IN} ≤ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width						
Si82AxxAx Devices	PW_{MIN}	No load	—	6.56	—	ns
Si82AxxBx Devices			—	25.8	—	ns
Propagation Delay						
Positive-Going Control Input Delay[2]						
0 ns Deglitch (Si82AxxAx) Devices	t_{PLH}	V_I, V_{I+}, V_{I-}; no load	13.5	21.0	31.4	ns
30 ns Deglitch (Si82AxxBx) Devices			39.4	46.0	55.8	ns
Negative-Going Control Input Delay[2]						
0 ns Deglitch (Si82AxxAx) Devices	t_{PLH}	V_I, V_{I+}, V_{I-}; no load	13.5	21.0	31.4	ns
30 ns Deglitch (Si82AxxBx) Devices			39.4	46.0	55.8	ns
Enable Input Delay[3]	t_{EID}	EN rising or DIS falling, no load	14.5	21.0	28.8	ns
Disable Input Delay[3]	t_{DID}	EN falling or DIS rising, no load	14.5	21.0	28.8	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	0.10	10.0	ns

Table 9. Timing Characteristics[1] (Continued)

Operating range for the following specifications: VDDI = 3.0–20 V; VDD = 5.0–30 V; T_A = –40 to +125 °C; $F_{IN} \leq$ 1 MHz.

Typical specifications: VDDI = 5 V; VDD = 6 V for 4 V UVLO devices, 10 V for 8 V UVLO devices, 15 V for 12 V UVLO devices, and 18 V for 15 V UVLO devices; T_A = 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Part-to-Part Propagation Delay Skew						
0 ns Deglitch (Si82AxxAx) Devices	$t_{PSK(CC)}$	MAX{ |t_{PLHA}–t_{PLHB}|, |t_{PHLA}–t_{PHLB}| }	—	—	5.00	ns
30 ns Deglitch (Si82AxxBx) Devices			—	—	8.00	ns
Part-to-Part[4]						
0 ns Deglitch (Si82DxxAx) Devices	$t_{PSK(PP)}$	MAX{ |t_{PLHx}–t_{PLHy}|, |t_{PHLx}–t_{PHLy}| }	—	—	7.00	ns
30 ns Deglitch (Si82DxxBx) Devices			—	—	12.0	ns
Output Rise Time[2]	t_R	VDD = 6 V, C_L = 1 nF, R_G = 0 Ω	—	7.50	—	ns
		VDD = 10 V, C_L = 1 nF, R_G = 0 Ω	—	7.20	—	ns
		VDD = 15 V, C_L = 1 nF, R_G = 0 Ω	—	7.90	—	ns
		VDD = 18 V, C_L = 1 nF, R_G = 0 Ω	—	8.30	—	ns
Output Fall Time[2]	t_F	VDDA = 6 V, C_L = 1 nF, R_G = 0 Ω	—	6.60	—	ns
		VDD = 10 V, C_L = 1 nF, R_G = 0 Ω	—	7.00	—	ns
		VDD = 15 V, C_L = 1 nF, R_G = 0 Ω	—	7.95	—	ns
		VDD = 18 V, C_L = 1 nF, R_G = 0 Ω	—	8.60	—	ns
Startup Time[5]	t_{ST}		—	125	—	µs
VDDI Logic Input Power Cycle Time[7]	t_{PCL}		—	60.0	—	µs
VDDI Logic Input Shutdown Time[7]	t_{SDL}		—	90.0	—	µs
VDD Gate Driver Power Cycle Time[7]	t_{PCG}		—	125	—	µs
VDD Gate Driver Shutdown Time[7]	t_{SDG}		—	7.00	—	µs
Common Mode Transient Immunity	CMTI		200	—	—	kV/µs

1. Adding the suffix A/B to any symbol, parameter, or test condition variable denotes that the term applies interchangeably to either gate driver A or gate driver B.
2. See Figure 16, "Control Input Timing Measurements," on page 24 for details.
3. See Figure 17, "Enable or Disable Input Timing Measurements," on page 24 for details.
4. $t_{PSK(PP)}$ is the largest absolute value difference in propagation delays measured between different channels on different units operating at the same supply voltages, load, and ambient temperature.
5. Startup, power cycle, and shutdown timing are detailed in "4.2. Power Sequence and Timing Behavior" on page 10.
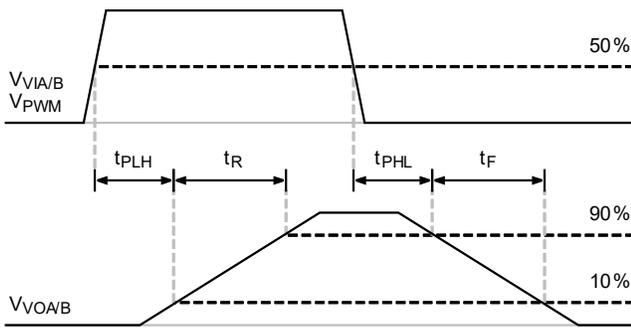
EN = Logic High
DIS = Logic Low

Figure 16. Control Input Timing Measurements
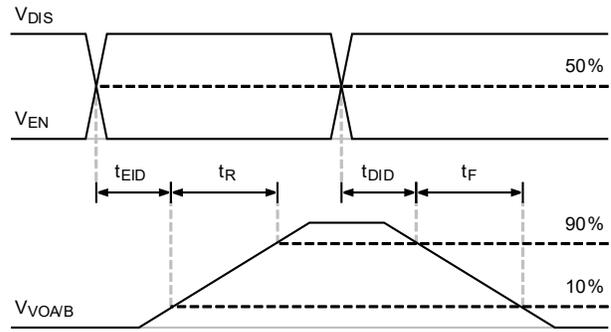
VI/VI+ = Logic High
VI = Logic Low

Figure 17. Enable or Disable Input Timing Measurements
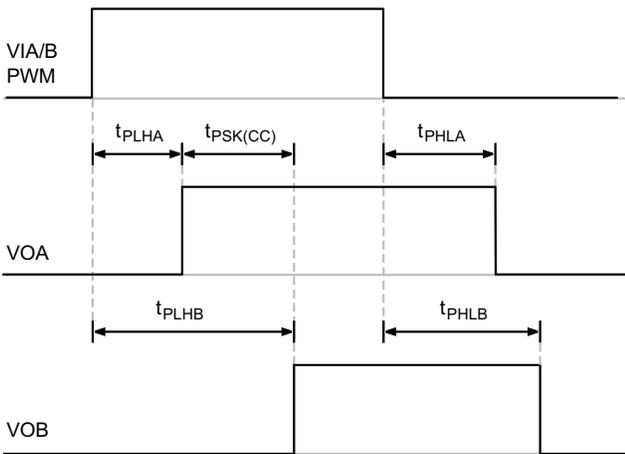
EN = Logic high
DIS = Logic low

Figure 18. Propagation Delay Parameters
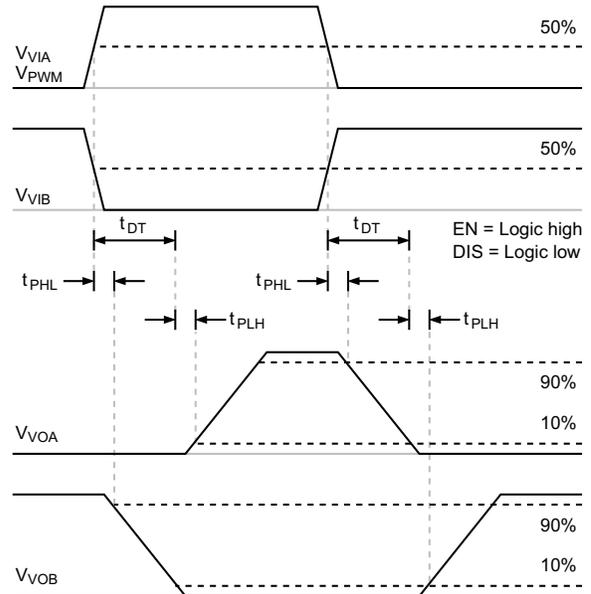
Figure 19. Dead Time Timing Measurement

6.3. Typical Performance Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in "6.2. Electrical Characteristics" on page 19 for actual specification limits.
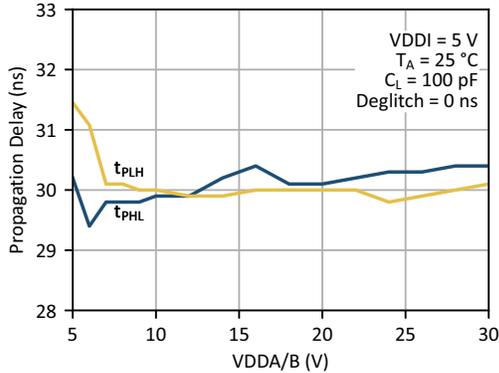
Figure 20. Propagation Delay vs. Gate Driver Supply Voltage
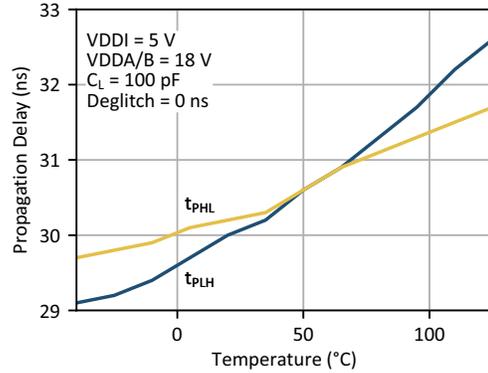
Figure 21. Propagation Delay vs. Ambient Temperature
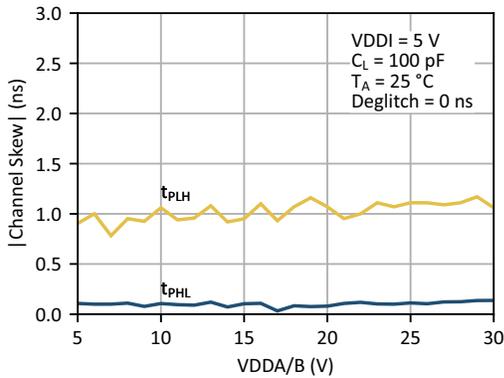
Figure 22. Channel-to-Channel Skew vs. Gate Driver Supply Voltage
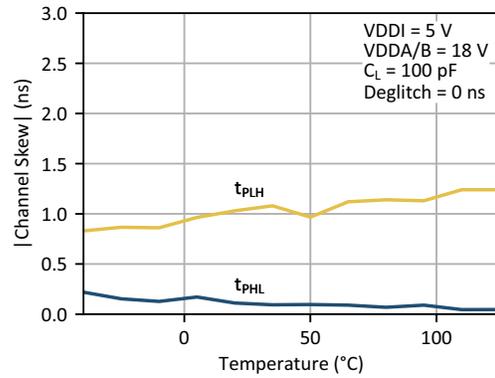
Figure 23. Channel-to-Channel Skew vs. Ambient Temperature
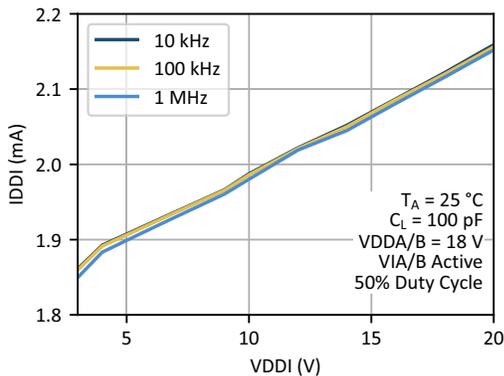
Figure 24. Logic Input Active Supply Current vs. Logic Input Supply Voltage
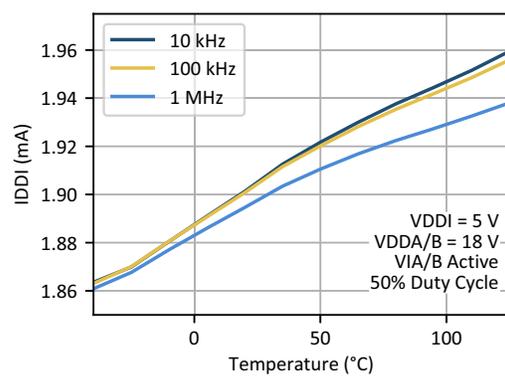
Figure 25. Logic Input Active Supply Current vs. Ambient Temperature
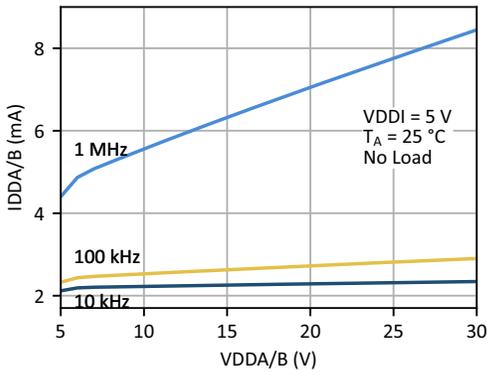
Figure 26. Gate Driver Active Supply Current vs. Gate Driver Supply Voltage
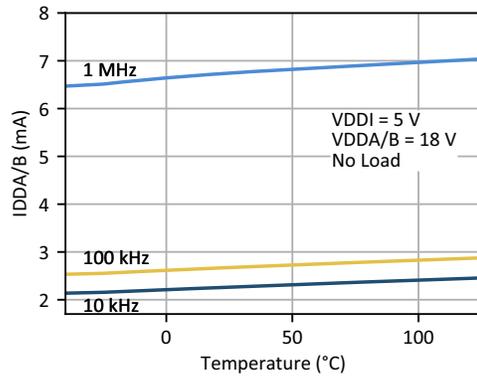
Figure 27. Gate Driver Active Supply Current vs. Ambient Temperature
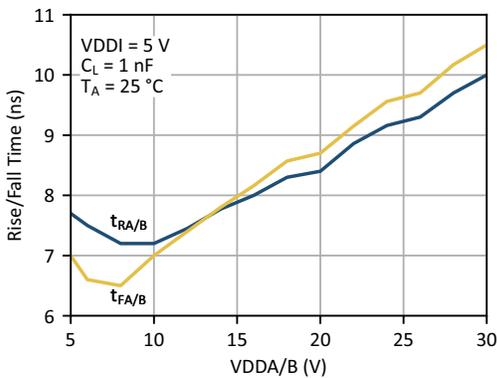
Figure 28. Output Rise/Fall Time vs. Gate Driver Supply Voltage
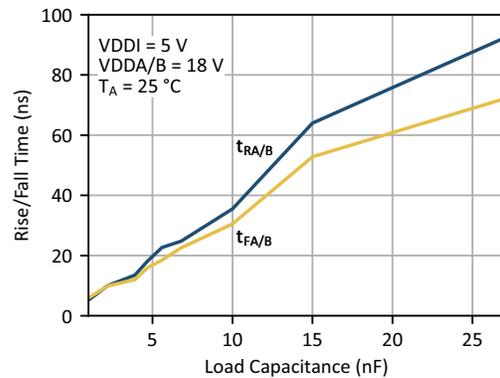
Figure 29. Output Rise/Fall Time vs. Output Load
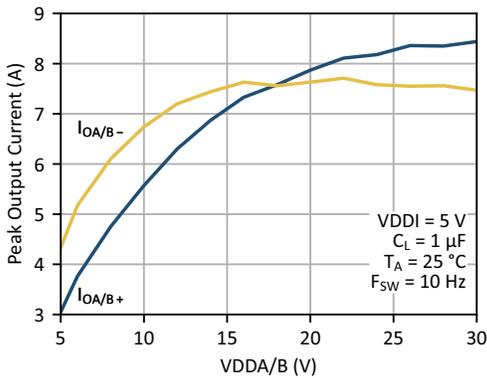
Figure 30. Peak Output Current vs. Gate Driver Supply Voltage
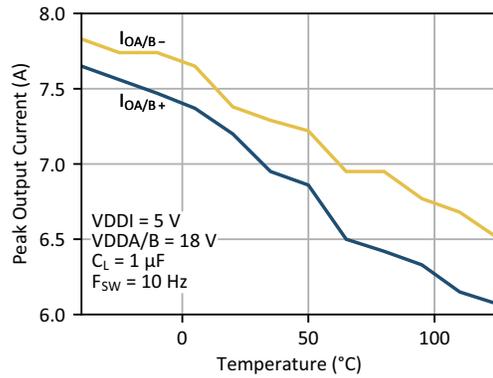
Figure 31. Peak Output Current vs. Ambient Temperature
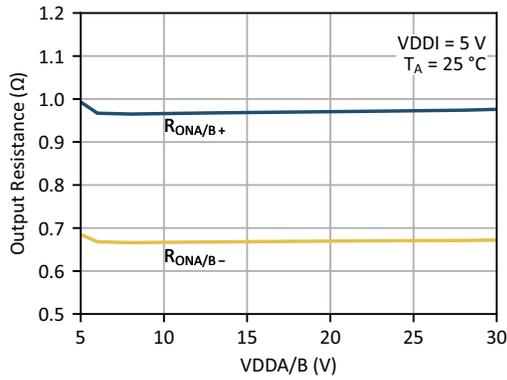
**Figure 32. Output Resistance vs.
Gate Driver Supply Voltage**
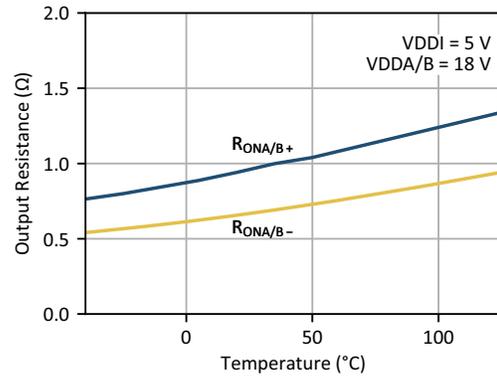
**Figure 33. Output Resistance vs.
Ambient Temperature**
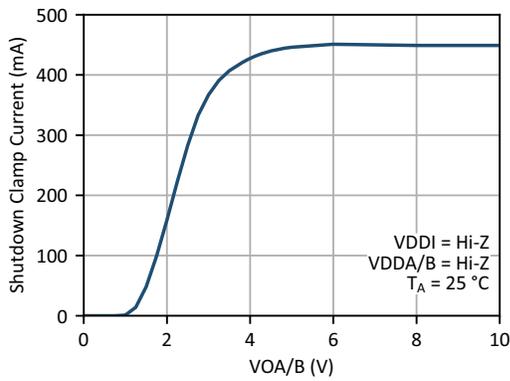
**Figure 34. Shutdown Clamp Current vs.
Shutdown Clamp Voltage**
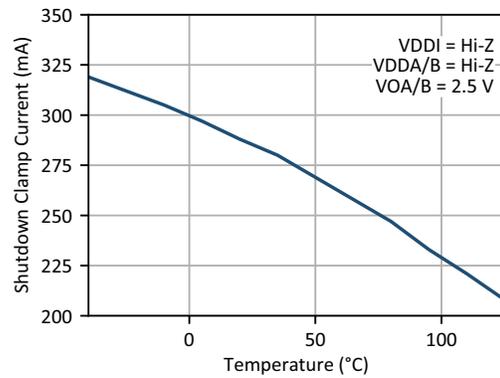
**Figure 35. Shutdown Clamp Current vs.
Ambient Temperature**

6.4. Thermal Characteristics

Table 10. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-16	WB SOIC-14	Unit
Thermal Resistance					
Junction-to-Ambient	θ_{JA}	4-layer, 2s2p JEDEC test board	63	59	°C/W
Characterization Parameter					
Junction-to-Top	Ψ_{JT}	4-layer, 2s2p JEDEC test board	7.5	14	°C/W
Junction-to-Board	Ψ_{JB}	4-layer, 2s2p JEDEC test board	31	34	°C/W

6.5. Safety Certifications and Specifications

Table 11. Regulatory Information[1]

CSA
The Si82Ax is certified under CSA. For more details, see Master Contract Number 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si82Ax is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 V_{PEAK} for reinforced insulation working voltage.
UL
The Si82Ax is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 6.0 kV_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si82Ax is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see .

Table 12. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-16	WB SOIC-14	
Nominal External Air Gap (Clearance)	CLR		3.90	8.00	mm
Nominal External Tracking (Creepage)	CRP		3.90	8.00	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.036	0.036	mm
Tracking Resistance	CTI or PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.031	0.040	mm
Resistance (Input-Output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	0.5	0.5	pF
Input Capacitance[2]	C_I	f = 100 kHz	2.00	2.00	pF

1. To determine resistance and capacitance, the device is converted into a 2-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 13. IEC-60664-1 Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-16	WB SOIC-14
Material group		I	I
Overvoltage category	Rated mains voltage $\leq$ 150 V_{RMS}	I-IV	I-IV
	Rated mains voltage $\leq$ 300 V_{RMS}	I-III	I-IV
	Rated mains voltage $\leq$ 600 V_{RMS}	I-II	I-IV
	Rated mains voltage $\leq$ 1000 V_{RMS}	I	I-III

Table 14. IEC60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-16	WB SOIC-14	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	445	1500	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	630	2121	V_{PEAK}
Apparent charge	Q_{PD}	Method b: At routine test (100% production) and preconditioning (type test); V_{INI} = 1.2 x V_{IOTM}, t_{INI} = 1 s; $V_{PD(M)}$ = 1.875 x V_{IORM}, t_M = 1 s (method b1) or $V_{PD(M)}$ = V_{INI}, t_M = t_{INI} (method b2)	$\leq$ 5	$\leq$ 5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	5302	8484	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile (qualification)	10400	10400	V_{PEAK}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile (qualification)	5000	8000	V_{PEAK}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	>10^9	>10^9	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 15. UL1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			NB SOIC-16	WB SOIC-14	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	3750	6000	V_{RMS}

Table 16. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Max[1]		Unit
			NB SOIC-16	**WB SOIC-14**	
Safety temperature	T_S		150	150	°C
Safety input, output, or supply current	I_S	Refer to $\varnothing_{JA}$ in "6.4. Thermal Characteristics" on page 28; VDDI = 5 V, VDDA/B = 30 V, T_J = 150 °C, T_A = 25 °C	66	70	mA
Safety input, output, or total power	P_S		1.98	2.11	W

1. Maximum value allowed in the event of a failure; also see the temperature derating curves below.
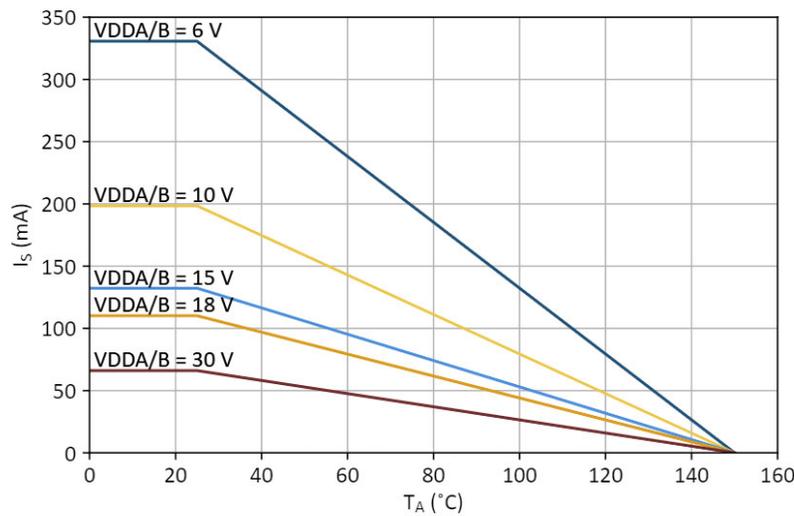
Figure 36. NB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve
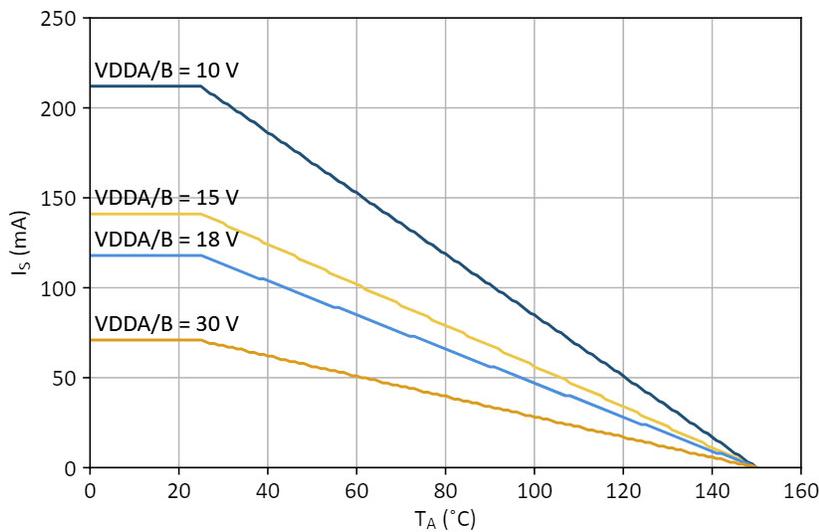
Figure 37. WB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve

7. Package Drawings

7.1. NB SOIC-8 Package Drawing
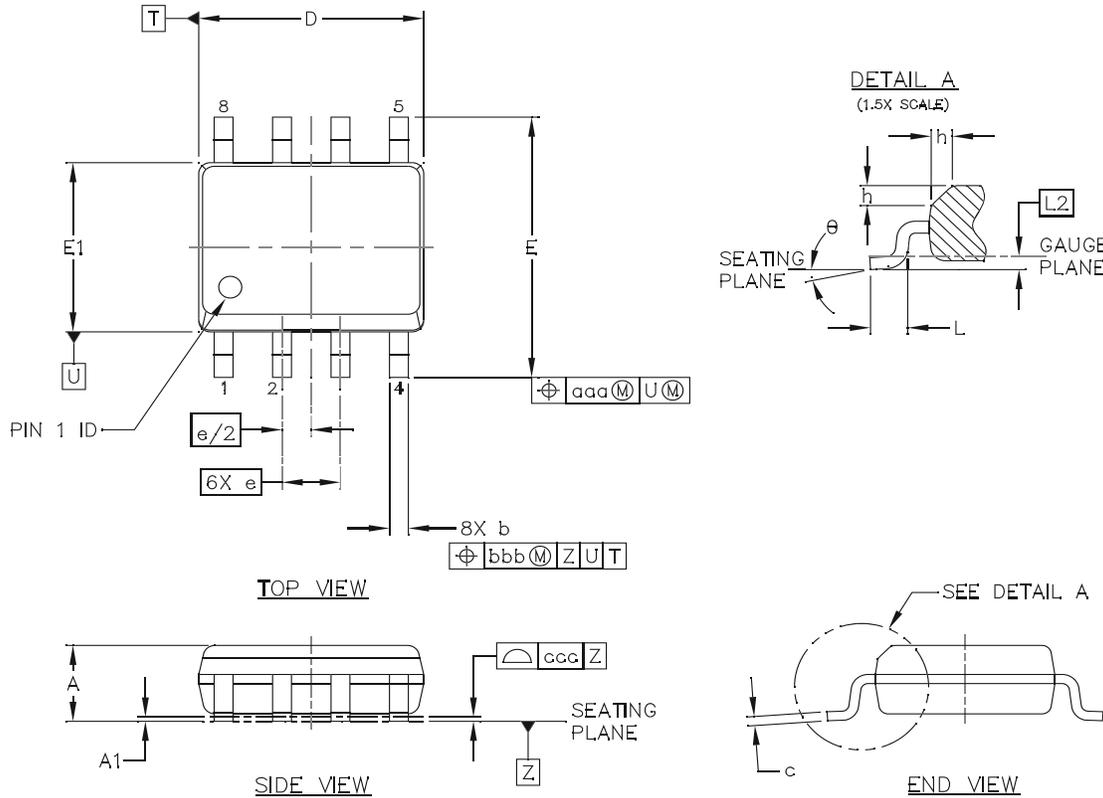
Figure 38. NB SOIC-8 Package Drawing

Table 17. NB SOIC-8 Package Drawing Dimensions[1,2,3,4,5]

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.19	0.25
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50

Table 17. NB SOIC-8 Package Drawing Dimensions[1,2,3,4,5] (Continued)

Dimension	Min	Max
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   a.BSC: Basic Dimension. Theoretically exact shown without tolerance
   b.REF: Reference Dimension. Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-137, Variation AB.
5. Recommended reflow profile per the JEDEC J-STD-020C specification for small body, lead-free components.

7.2. WB SOIC-8 Package Drawing
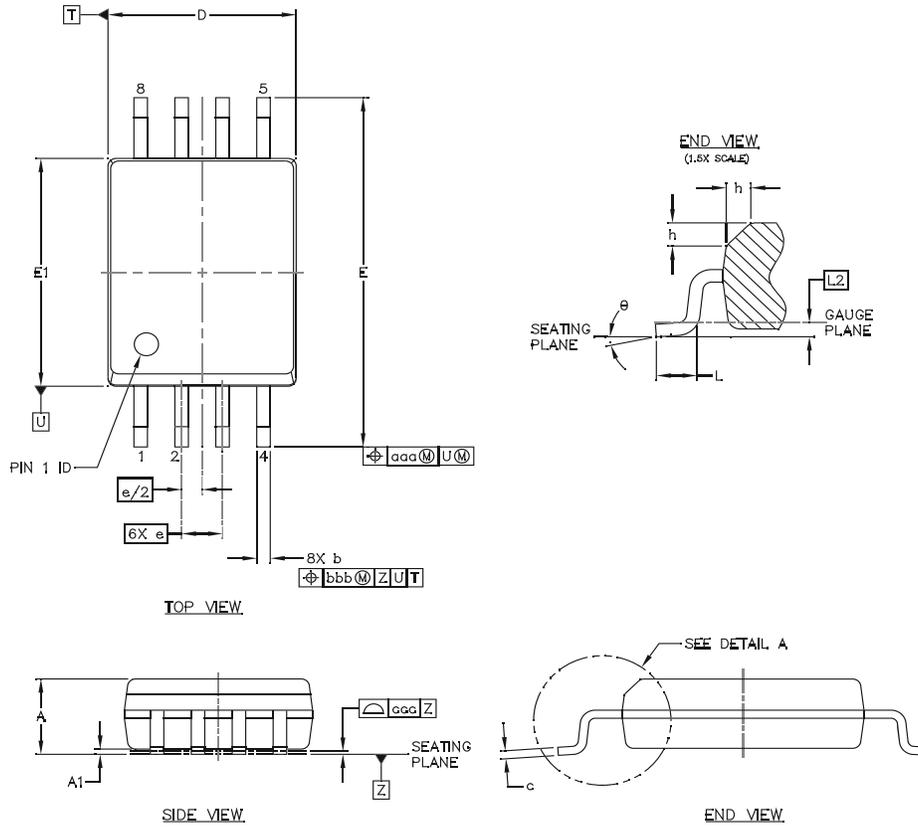
Figure 39. WB SOIC-8 Package Drawing

Table 18. WB SOIC-8 Package Drawing Dimensions[1,2,3,4]

Dimension	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.13	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
L2	0.25 BSC	
h	0.25	0.76
θ	0°	8°

Table 18. WB SOIC-8 Package Drawing Dimensions[1,2,3,4] (Continued)

Dimension	Min	Max
aaa	0.25	
bbb	0.25	
ccc	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M.
   a.BSC: Basic Dimension. Theoretically exact shown without tolerance
   b.REF: Reference Dimension. Usually without tolerance, for information purposes only.
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25mm per side.
4. 4- Recommended reflow profile per the JEDEC J-STD-020C specification for small body, lead-free components.

8. Land Patterns

8.1. NB SOIC-8 Land Pattern
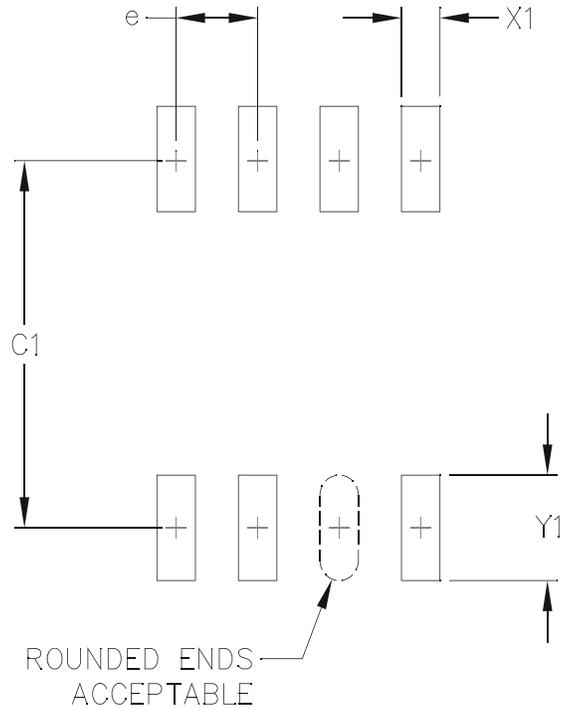
Figure 40. NB SOIC-8 Land Pattern

Table 19. NB SOIC-8 PCB Land Pattern Dimensions[1,2,3]

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8AN for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.

8.2. SSO-8 Land Pattern
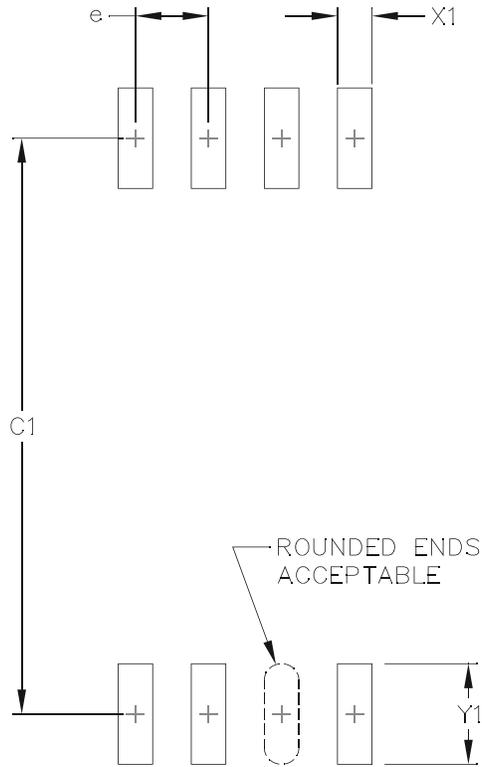
Figure 41. SSO-8 PCB Land Pattern

Table 20. SSO-8 PCB Land Pattern Dimensions[1,2,3]

Dimension	Feature	mm
C1	Pad Column Spacing	9.80
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 Guidelines.
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Top Markings

9.1. NB SOIC-8 Top Marking
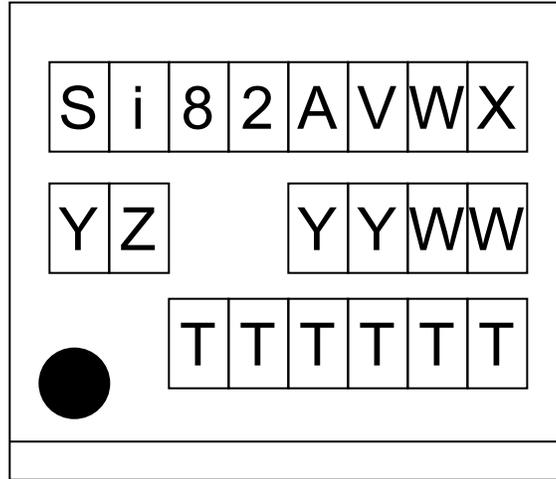
Figure 42. 8-Pin Narrow-Body SOIC Top Marking

Table 21. 16-Pin Narrow-Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options
	
	(See "10. Ordering Guide" on page 42 for more information)
		Si82A = One-channel Value IsoDriver product series
		
		V = Input Pinout
		
		    2 = VIA and DIS inputs
		
		    3 = VI and EN inputs
		
		    4 = VI+ and VI– inputs
		
		W = Output Pinout
		
		    0 = Split (VO+ and VO-) outputs
		
		    8 = Single (VO) output
		
		X = Input Configuration
		
		    A = No deglitch filter
		
		    B = 30 ns deglitch filter
		
		Y = Output Configuration
		
		    G = 4 V UVLO
		
		    B = 8 V UVLO
		
		    C = 12 V UVLO
		
		    E = 15 V UVLO
		
		Z = Isolation Rating
		
		    C = 3.75 kV$_{RMS}$

Table 21. 16-Pin Narrow-Body SOIC Top Marking Explanation

Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.

9.2. WB SOIC-8 Top Marking
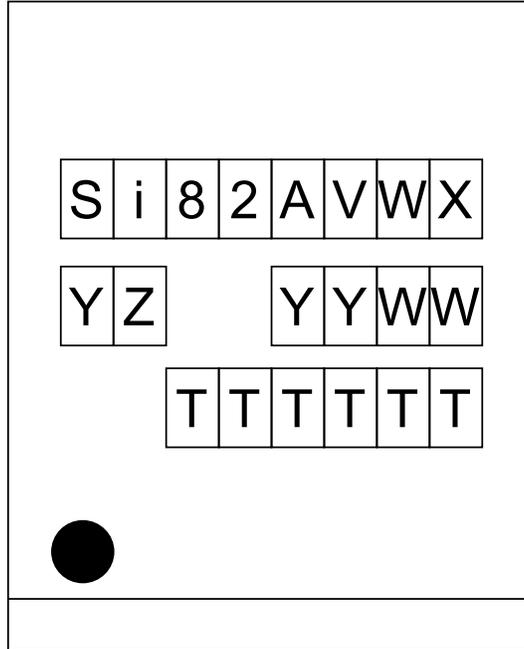
Figure 43. 8-Pin Wide Body SOIC Top Marking

Table 22. 8-Pin Wide Body SOIC Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options
	
	(See "10. Ordering Guide" on page 42 for more information)
		Si82A = One-channel Value IsoDriver product series
		
		V = Input Pinout
		
		    3 = VI and EN inputs
		
		    4 = VI+ and VI– inputs
		
		W = Output Pinout
		
		    0 = Split (VO+ and VO-) outputs
		
		    3 = Split (VO+ and VO-) outputs
		
		X = Input Configuration
		
		    A = No deglitch filter
		
		    B = 30 ns deglitch filter
		
		Y = Output Configuration
		
		    B = 8 V UVLO
		
		    C = 12 V UVLO
		
		    E = 15 V UVLO
		
		Z = Isolation Rating
		
		    E = 6.0 kV$_{RMS}$

Table 22. 8-Pin Wide Body SOIC Top Marking Explanation

Line 2 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg. Trace Code	Manufacturing Traceability Code The Manufacturing Traceability Code represented by "TTTTTT" contains, as its first character, a letter in the range A through M to indicate Industrial-Grade, or a letter in the range N through Z to indicate Automotive-Grade.
Line 3 Marking:	e4 circle is 1.7 mm diameter	The "e4" symbol indicates Pb-free lead finish.

10. Ordering Guide

Table 23. Si82Axx Ordering Guide[1,2,3,4,5,6,7]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Outputs	Enable/ Disable	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
NB SOIC-8 Package Options								
Si82A28AGC-IS	Si82A28AGC-AS	VI	VO	Disable	NA	4 V	3.75 kVRMS	NB SOIC-8
Si82A28ABC-IS	Si82A28ABC-AS	VI	VO	Disable	NA	8 V	3.75 kVRMS	NB SOIC-8
Si82A28ACC-IS	Si82A28ACC-AS	VI	VO	Disable	NA	12 V	3.75 kVRMS	NB SOIC-8
Si82A30AGC-IS	Si82A30AGC-AS	VI	VO+, VO−	Enable	NA	4 V	3.75 kVRMS	NB SOIC-8
Si82A30ABC-IS	Si82A30ABC-AS	VI	VO+, VO−	Enable	NA	8 V	3.75 kVRMS	NB SOIC-8
Si82A30ACC-IS	Si82A30ACC-AS	VI	VO+, VO−	Enable	NA	12 V	3.75 kVRMS	NB SOIC-8
Si82A30AEC-IS	Si82A30AEC-AS	VI	VO+, VO−	Enable	NA	15 V	3.75 kVRMS	NB SOIC-8
Si82A30BGC-IS	Si82A30BGC-AS	VI	VO+, VO−	Enable	30 ns	4 V	3.75 kVRMS	NB SOIC-8
Si82A30BBC-IS	Si82A30BBC-AS	VI	VO+, VO−	Enable	30 ns	8 V	3.75 kVRMS	NB SOIC-8
Si82A30BCC-IS	Si82A30BCC-AS	VI	VO+, VO−	Enable	30 ns	12 V	3.75 kVRMS	NB SOIC-8
Si82A30BEC-IS	Si82A30BEC-AS	VI	VO+, VO−	Enable	30 ns	15 V	3.75 kVRMS	NB SOIC-8
Si82A40AGC-IS	Si82A40AGC-AS	VI+, VI−	VO+, VO−	NA	NA	4 V	3.75 kVRMS	NB SOIC-8
Si82A40ABC-IS	Si82A40ABC-AS	VI+, VI−	VO+, VO−	NA	NA	8 V	3.75 kVRMS	NB SOIC-8
Si82A40ACC-IS	Si82A40ACC-AS	VI+, VI−	VO+, VO−	NA	NA	12 V	3.75 kVRMS	NB SOIC-8
Si82A40AEC-IS	Si82A40AEC-AS	VI+, VI−	VO+, VO−	NA	NA	15 V	3.75 kVRMS	NB SOIC-8
Si82A40BGC-IS	Si82A40BGC-AS	VI+, VI−	VO+, VO−	NA	30 ns	4 V	3.75 kVRMS	NB SOIC-8
Si82A40BBC-IS	Si82A40BBC-AS	VI+, VI−	VO+, VO−	NA	30 ns	8 V	3.75 kVRMS	NB SOIC-8
Si82A40BCC-IS	Si82A40BCC-AS	VI+, VI−	VO+, VO−	NA	30 ns	12 V	3.75 kVRMS	NB SOIC-8
Si82A40BEC-IS	Si82A40BEC-AS	VI+, VI−	VO+, VO−	NA	30 ns	15 V	3.75 kVRMS	NB SOIC-8

Table 23. Si82Axx Ordering Guide[1,2,3,4,5,6,7]

Ordering Part Number (OPN)	Automotive OPN	Inputs	Outputs	Enable/ Disable	Deglitch Filter	Undervoltage Lockout (UVLO)	Isolation Rating	Package Type
SSO-8 Package Options								
Si82A30ABE-IS4	Si82A30ABE-AS4	VI	VO+, VO−	Enable	NA	8 V	6 kVRMS	SSO-8
Si82A30ACE-IS4	Si82A30ACE-AS4	VI	VO+, VO−	Enable	NA	12 V	6 kVRMS	SSO-8
Si82A30AEE-IS4	Si82A30AEE-AS4	VI	VO+, VO−	Enable	NA	15 V	6 kVRMS	SSO-8
Si82A30BBE-IS4	Si82A30BBE-AS4	VI	VO+, VO−	Enable	30 ns	8 V	6 kVRMS	SSO-8
Si82A30BCE-IS4	Si82A30BCE-AS4	VI	VO+, VO−	Enable	30 ns	12 V	6 kVRMS	SSO-8
Si82A30BEE-IS4	Si82A30BEE-AS4	VI	VO+, VO−	Enable	30 ns	15 V	6 kVRMS	SSO-8
Si82A40ABE-IS4	Si82A40ABE-AS4	VI+, VI−	VO+, VO−	NA	NA	8 V	6 kVRMS	SSO-8
Si82A40ACE-IS4	Si82A40ACE-AS4	VI+, VI−	VO+, VO−	NA	NA	12 V	6 kVRMS	SSO-8
Si82A40AEE-IS4	Si82A40AEE-AS4	VI+, VI−	VO+, VO−	NA	NA	15 V	6 kVRMS	SSO-8
Si82A40BBE-IS4	Si82A40BBE-AS4	VI+, VI−	VO+, VO−	NA	30 ns	8 V	6 kVRMS	SSO-8
Si82A40BCE-IS4	Si82A40BCE-AS4	VI+, VI−	VO+, VO−	NA	30 ns	12 V	6 kVRMS	SSO-8
Si82A40BEE-IS4	Si82A40BEE-AS4	VI+, VI−	VO+, VO−	NA	30 ns	15 V	6 kVRMS	SSO-8
Si82A43ACE-IS4	Si82A43ACE-AS4	VI+, VI−	VO+, VO−	NA	NA	12 V	6 kVRMS	SSO-8

1. "Si" and "SI" are used interchangeably.
2. An "R" at the end of the Ordering Part Number indicates tape and reel packaging option.
3. ll packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
4. All devices with VI+ and VI- inputs operate as complementary digital inputs.
5. All devices with VO+ and VO- outputs source current out of the VO+ pin and sink current into the VO- pin.
6. Automotive-Grade devices (with an "-A" suffix) are identical in construction materials and electrical parameters to their Industrial Grade (with an "-I" suffix) version counterpart. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
7. In Top Markings, the Manufacturing Code represented by either "RTTTTT" or "TTTTTT" contains as its first character a letter in the range N through Z to indicate Automotive-Grade

11. Revision History

Revision	Date	Description	Notes
A	December, 2024	Initial release.	CNxxxxxxx