Data Sheet

ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E

3.0 kV RMS/3.75 kV RMS Quad Digital Isolators

FEATURES

- High common-mode transient immunity: 100 kV/µs
- High robustness to radiated and conducted noise
- Low propagation delay
  - 13 ns maximum for 5 V operation
  - 15 ns maximum for 1.8 V operation
- 150 Mbps maximum guaranteed data rate
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 3000 V rms for 1 minute
  - IEC/EN/CSA 60950-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB 4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 565 V peak
- Backward compatibility
  - ADuM140E1/ADuM141E1/ADuM142E1 pin-compatible with ADuM1400/ADuM1401/ADuM1402
- Low dynamic power consumption
- 1.8 V to 5 V level translation
- High temperature operation: 125°C
- Fail-safe high or low options
- 16-lead, RoHS compliant, SOIC package
- AEC-Q100 qualified for automotive applications

APPLICATIONS

- General-purpose multichannel isolation
- Serial peripheral interface (SPI)/data converter isolation
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E[1] are quad-channel digital isolators based on Analog Devices, Inc., *i*Coupler® technology. Combining high speed, complementary metal-oxide semiconductor (CMOS) and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated couplers. The maximum propagation delay is 13 ns with a pulse width distortion of less than 3 ns at 5 V operation. Channel matching is tight at 3.0 ns maximum.

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E data channels are independent and are available in a variety of configurations with a withstand voltage rating of 3.0 kV rms or 3.75 kV rms (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 1.8 V to 5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

Unlike other optocoupler alternatives, dc correctness is ensured in the absence of input logic transitions. Two different fail-safe options are available, by which the outputs transition to a pre-determined state when the input power supply is not applied or the inputs are disabled. The ADuM140E1/ADuM141E1/ADuM142E1 are pin-compatible with the ADuM1400/ADuM1401/ADuM1402.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

Rev. K

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FUNCTIONAL BLOCK DIAGRAMS

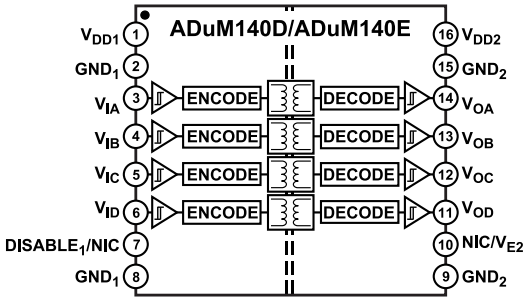

Figure 1. ADuM140D/ADuM140E Functional Block Diagram

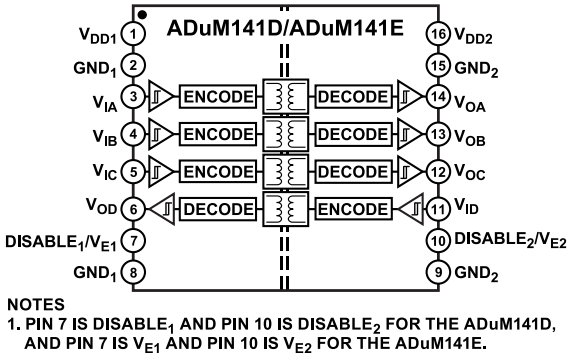

Figure 2. ADuM141D/ADuM141EFunctional Block Diagram

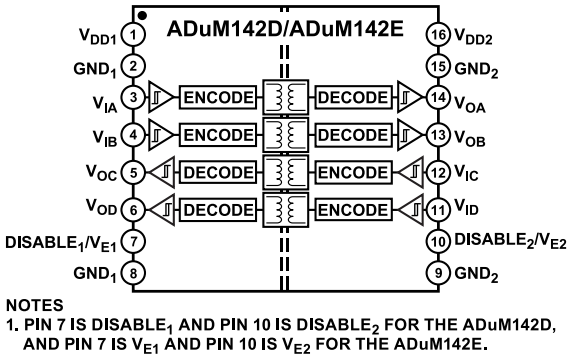

Figure 3. ADuM142D/ADuM142E Functional Block Diagram

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within pulse width distortion (PWD) limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	7.2	13	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.5	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.1	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.5	3.0	ns	
Opposing Direction	t_{PSKOD}		0.5	3.0	ns	
Jitter			490		ps p-p	See the Jitter Measurement section
			70		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −4 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 4 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	μA	$DISABLE_1$ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}
Quiescent Supply Current						
ADuM140D/ADuM140E						
	$I_{DD1 (Q)}$		1.2	2.2	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.72	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		12.0	20.0	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.92	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM141D/ADuM141E						
	$I_{DD1 (Q)}$		1.6	2.46	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.9	2.62	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		10.0	17.0	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		6.0	10.0	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM142D/ADuM142E						
	$I_{DD1 (Q)}$		1.6	2.46	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.6	2.46	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.2	11.5	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]

SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		8.4	11.5	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

1 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

2 I_{Ox} is the Channel x output current, where x = A, B, C, or D.

3 V_{IxH} is the input side logic high.

4 V_{IxL} is the input side logic low.

5 V_I is the voltage input.

6 E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

7 $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM140D/ADuM140E											
Supply Current Side 1	I_{DD1}		6.8	10		7.8	12		11.8	17.4	mA
Supply Current Side 2	I_{DD2}		2.1	3.7		3.9	5.7		9.2	13	mA
ADuM141D/ADuM141E											
Supply Current Side 1	I_{DD1}		5.8	10.3		7.0	10.9		11.4	15.9	mA
Supply Current Side 2	I_{DD2}		4.0	6.85		5.5	8.5		10.3	14.0	mA
ADuM142D/ADuM142E											
Supply Current Side 1	I_{DD1}		4.3	7.7		6.0	9.3		10.3	14.2	mA
Supply Current Side 2	I_{DD2}		5.3	8.7		6.7	10.1		11.0	14.9	mA

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	4.8	6.8	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			580		ps p-p	See the Jitter Measurement section
			120		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	μA	$DISABLE_1$ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}
Quiescent Supply Current						
ADuM140D/ADuM140E						
	$I_{DD1 (Q)}$		1.2	2.12	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.68	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		12.0	19.6	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.8	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM141D/ADuM141E						
	$I_{DD1 (Q)}$		1.5	2.36	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.8	2.52	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		9.8	16.7	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		5.7	9.7	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM142D/ADuM142E						
	$I_{DD1 (Q)}$		1.6	2.4	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.6	2.4	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.2	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		8.4	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

[2] I_{Ox} is the Channel x output current, where x = A, B, C, or D.

[3] V_{IxH} is the input side logic high.

[4] V_{IxL} is the input side logic low.

[5] V_I is the voltage input.

[6] E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

[7] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM140D/ADuM140E											
Supply Current Side 1	I_{DD1}		6.6	9.8		7.4	11.2		10.7	15.9	mA
Supply Current Side 2	I_{DD2}		2.0	3.7		3.5	5.5		8.2	11.6	mA
ADuM141D/ADuM141E											
Supply Current Side 1	I_{DD1}		5.65	10.1		6.65	10.5		10.4	14.9	mA
Supply Current Side 2	I_{DD2}		3.9	6.65		5.2	8.0		9.4	12.8	mA
ADuM142D/ADuM142E											
Supply Current Side 1	I_{DD1}		4.3	7.7		5.6	9.0		9.1	13	mA
Supply Current Side 2	I_{DD2}		5.0	8.4		6.2	9.6		9.8	13.7	mA

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.0	7.0	14	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			6.8	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			800		ps p-p	See the Jitter Measurement section
			190		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	μA	$DISABLE_1$ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}
Quiescent Supply Current						
ADuM140D/ADuM140E						
	$I_{DD1 (Q)}$		1.2	2.0	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.64	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		1.2	19.6	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.76	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM141D/ADuM141E						
	$I_{DD1 (Q)}$		1.46	2.32	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.75	2.47	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		9.7	16.6	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		5.67	9.67	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM142D/ADuM142E						
	$I_{DD1 (Q)}$		1.6	2.32	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.6	2.32	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.2	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]

SPECIFICATIONS

Table 5. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		8.4	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\lvert CM_H \rvert$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\lvert CM_L \rvert$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

[1] 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

[2] I_{Ox} is the Channel x output current, where x = A, B, C, or D.

[3] V_{IxH} is the input side logic high.

[4] V_{IxL} is the input side logic low.

[5] V_I is the voltage input.

[6] E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

[7] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 6. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM140D/ADuM140E											
Supply Current Side 1	I_{DD1}		6.5	9.8		7.3	11.1		10.4	15.5	mA
Supply Current Side 2	I_{DD2}		2.0	3.6		3.3	5.2		7.3	10.2	mA
ADuM141D/ADuM141E											
Supply Current Side 1	I_{DD1}		5.6	10.0		6.4	10.4		9.7	14.5	mA
Supply Current Side 2	I_{DD2}		3.8	6.55		4.8	7.7		8.3	11.5	mA
ADuM142D/ADuM142E											
Supply Current Side 1	I_{DD1}		4.3	7.7		5.4	8.8		8.8	12.7	mA
Supply Current Side 2	I_{DD2}		5.0	8.4		6.1	9.5		9.5	13.4	mA

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ELECTRICAL CHARACTERISTICS—1.8 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 1.8 V. Minimum/maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1} ≤ 1.9 V, 1.7 V ≤ V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	6.6			ns	Within PWD limit
Data Rate[1]		150			Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	5.8	8.7	15	ns	50% input to 50% output
Pulse Width Distortion	PWD		0.7	3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			7.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0.7	3.0	ns	
Opposing Direction	t_{PSKOD}		0.7	3.0	ns	
Jitter			470		ps p-p	See the Jitter Measurement section
			70		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.2	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
V_{E2} Enable Input Pull-Up Current	I_{PU}	−10	−3		μA	V_{E2} = 0 V
$DISABLE_1$ Input Pull-Down Current	I_{PD}		9	15	μA	$DISABLE_1$ = V_{DDx}
Tristate Output Current per Channel	I_{OZ}	−10	+0.01	+10	μA	0 V ≤ V_{Ox} ≤ V_{DDx}
Quiescent Supply Current						
ADuM140D/ADuM140E						
	$I_{DD1 (Q)}$		1.2	1.92	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.64	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		12.0	19.6	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		2.0	2.76	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM141D/ADuM141E						
	$I_{DD1 (Q)}$		1.4	2.28	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.73	2.45	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		9.6	16.5	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
	$I_{DD2 (Q)}$		5.6	9.6	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
ADuM142D/ADuM142E						
	$I_{DD1 (Q)}$		1.6	2.28	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD2 (Q)}$		1.6	2.28	mA	V_I[5] = 0 (E0, D0), 1 (E1, D1)[6]
	$I_{DD1 (Q)}$		7.2	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]

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Table 7. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
	$I_{DD2\ (Q)}$		8.4	11.2	mA	V_I[5] = 1 (E0, D0), 0 (E1, D1)[6]
Dynamic Supply Current						
Dynamic Input	$I_{DDI\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO\ (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}		1.6		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		1.5		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[7]	$\|CM_H\|$	75	100		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

1 150 Mbps is the highest data rate that can be guaranteed, although higher data rates are possible.

2 I_{Ox} is the Channel x output current, where x = A, B, C, or D.

3 V_{IxH} is the input side logic high.

4 V_{IxL} is the input side logic low.

5 V_I is the voltage input.

6 E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

7 $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output (V_O) > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 8. Total Supply Current vs. Data Throughput

		1 Mbps			25 Mbps			100 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
ADuM140D/ADuM140E											
Supply Current Side 1	I_{DD1}		6.4	9.8		7.2	11		10.2	15.2	mA
Supply Current Side 2	I_{DD2}		1.9	3.5		3.1	5.0		6.8	10	mA
ADuM141D/ADuM141E											
Supply Current Side 1	I_{DD1}		5.5	9.1		6.3	10.0		9.6	14.0	mA
Supply Current Side 2	I_{DD2}		3.72	6.45		4.8	7.5		8.4	11.2	mA
ADuM142D/ADuM142E											
Supply Current Side 1	I_{DD1}		4.3	7.7		5.3	8.7		8.6	12.6	mA
Supply Current Side 2	I_{DD2}		4.9	8.3		6.0	9.4		9.3	13.3	mA

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INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 9. R-16 Narrow Body [SOIC_N] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L (I01)	4.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)[2]	L (I02)	4.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	µm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)[3]	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

1 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

2 In accordance with IEC 60950-1/IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

3 CTI rating for the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E is >400 V and a Material Group II isolation group.

Table 10. RW-16 Wide Body [SOIC_W] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3750	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L (I01)	7.8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)[2]	L (I02)	7.8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	µm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)[3]	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

1 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

2 In accordance with IEC 60950-1/IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

3 CTI rating for the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E is >400 V and a Material Group II isolation group.

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Table 11. RQ-16 [QSOP] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L (I01)	3.5	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)[2]	L (I02)	3.5	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	3.8	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		29	µm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)[3]	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

1 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

2 In accordance with IEC 60950-1/IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

3 CTI rating for the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E is >400 V and a Material Group II isolation group.

PACKAGE CHARACTERISTICS

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance						
R-16 Narrow Body [SOIC_N] Package	θ_{JA}		76		°C/W	Thermocouple located at center of package underside
RW-16 Wide Body [SOIC_W] Package	θ_{JA}		45		°C/W	Thermocouple located at center of package underside
RQ-16 [QSOP] Package	θ_{JA}		76		°C/W	Thermocouple located at center of package underside

1 The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

2 Input capacitance is from any input data pin to ground.

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REGULATORY INFORMATION

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E certification approvals are listed in Table 13, Table 14, and Table 15.

Table 13. R-16 Narrow Body [SOIC_N] Package

UL	CSA	VDE	CQC
UL 1577[1] Single Protection, 3000 V rms	IEC/EN/CSA 60950-1 Basic insulation, 400 V rms Reinforced insulation, 200 V rms IEC/CSA 60601-1 Basic insulation (1 MOPP). 250 V rms IEC/CSA 61010-1 Basic insulation, 300 V rms, Overvoltage Category III Basic insulation, 150 V rms, Overvoltage Category IV	DIN EN IEC 60747-17 (VDE 0884-17)[2] Reinforced insulation, 565 V peak	CQC GB4943.1 Basic insulation, 400 V rms
File E214100	File No. 205078	Certificate No. 40051926	File CQC16001160842

[1] In accordance with UL 1577, each ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E in the R-16 narrow body [SOIC_N] package is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E in the R-16 narrow body [SOIC_N] package is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 14. RW-16 Wide Body [SOIC_W] Package

UL	CSA	VDE	CQC
UL 1577[1] Single Protection, 3750 V rms	IEC/EN/CSA 62368-1 Basic insulation, 780 V rms Reinforced insulation, 390 V rms IEC/CSA 60601-1 Reinforced insulation (2 MOPP) 237.5 V rms IEC/CSA 61010-1 Basic insulation, 600 V rms, Overvoltage Category III Reinforced insulation, 300 V rms	DIN EN IEC 60747-17 (VDE 0884-17)[2] Reinforced insulation, 565 V peak	CQC GB4943.1 Basic insulation, 760 V rms Reinforced insulation, 380 V rms
File E214100	File No. 205078	Certificate No. 40051926	File CQC16001147385

[1] In accordance with UL 1577, each ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec.

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17, each ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

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Table 15. RQ-16 [QSOP] Package

UL	CSA	VDE	CQC
UL 1577[1] Single Protection, 3000 V rms	IEC/EN/CSA 62368-1 Basic insulation, 350 V rms Reinforced insulation, 175 V rms IEC/CSA 60601-1 Basic insulation (1 MOPP) 187.5 V rms IEC/CSA 61010-1 Basic insulation, 300 V rms, Overvoltage Category III Basic insulation, 150 V rms	DIN EN IEC 60747-17 (VDE 0884-17)[2] Reinforced insulation, 565 V peak	CQC GB4943.1 Basic insulation, 320 V rms
File (Pending)	File No. 205078	Certificate No. 40051926	File CQC18001192421

[1] In accordance with UL 1577, each ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E in the RQ-16 [QSOP] package is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17, each ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E in the RW-16 wide body [SOIC_W] package is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN EN IEC 60747-17 (VDE 0884-17) approval.

SPECIFICATIONS

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 16. DIN EN IEC 60747-17 Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
≤ 150 V rms			I to IV	
≤ 300 V rms			I to IV	
≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	565	V peak
Maximum Working Insulation Voltage		V_{IOWM}	400	V rms
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd\ (m)}$, 100% production test, t_{ini} = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	1059	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	904	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd\ (m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\ (m)}$	678	V peak
Maximum Transient Isolation Voltage	V_{TEST} = 1.2 × V_{IOTM}, t =1s (100% production)	V_{IOTM}	4200	V peak
RW-16 Package		V_{IOTM}	5300	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	4200	V peak
RW-16 Package		V_{IMP}	5300	V peak
Maximum Surge Isolation Voltage	V_{TEST} ≥ 1.3 × V_{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	10000	V peak
RW-16 Package		V_{IOSM}	12800	V peak
Safety Limiting Values per VDE certification	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.64	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

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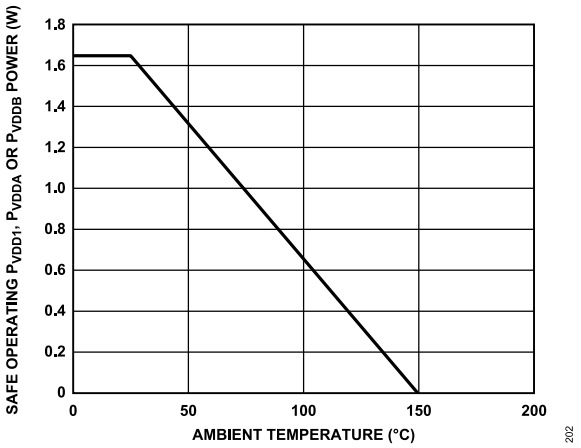

Figure 4. Thermal Derating Curve for R-16 Narrow Body [SOIC_N] Package, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

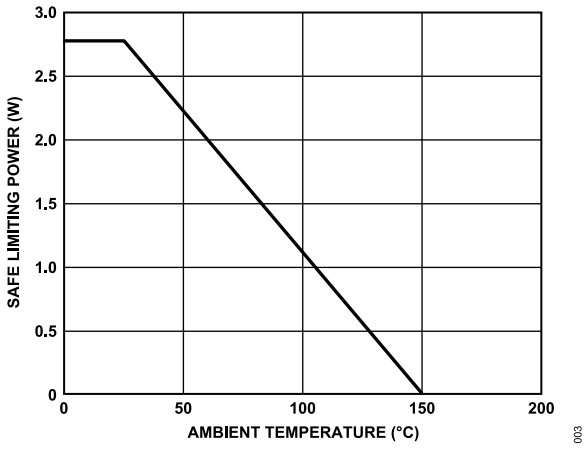

Figure 5. Thermal Derating Curve for RW-16 Wide Body [SOIC_W] Package, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

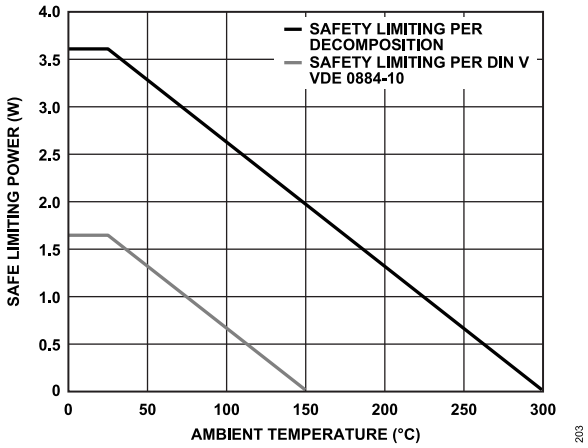

Figure 6. Thermal Derating Curve for RQ-16 [QSOP] Package, Dependence of Safety Limiting Values with Ambient Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages	V_{DD1}, V_{DD2}	1.7 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 18.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature(T_A) Range	−40°C to +125°C
Maximum Fault Junction Temperature (TJ) per DIN V VDE V 0884-11	150°C
Maximum Fault Junction Temperature (TJ) per Mold Compound	300°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}, $DISABLE_1$, $DISABLE_2$)	−0.5 V to V_{DDI}[1] + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD})	−0.5 V to V_{DDO}[2] + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−150 kV/µs to +150 kV/µs

1 V_{DDI} is the input side supply voltage.

2 V_{DDO} is the output side supply voltage.

3 See Figure 4 for the R-16 narrow body [SOIC_N] package, Figure 5 for the RW-16 wide body [SOIC_W] package, or Figure 6 for the RQ-16 [QSOP] package for the maximum rated current values at various temperatures.

4 Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 19. Maximum Continuous Working Voltage

Parameter	Max	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	565	V peak	Reinforced insulation as per DIN EN IEC 60747-17 (VDE 0884-17)[1].

1 Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS

TRUTH TABLES

Table 20. ADuM140D/ADuM141D/ADuM142D Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	$V_{DISABLEx}$ Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (D0), V_{Ox} Output[1, 2, 3]	Default High (D1), V_{Ox} Output[1, 2, 3]	Test Conditions/Comments
L	L or NC	Powered	Powered	L	L	Normal operation
H	L or NC	Powered	Powered	H	H	Normal operation
X	H	Powered	Powered	L	H	Inputs disabled, fail-safe output
X[4]	X[4]	Unpowered	Powered	L	H	Fail-safe output
X[4]	X[4]	Powered	Unpowered	Indeterminate	Indeterminate	

1 L means low, H means high, X means don't care, and NC means not connected.

2 V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). $V_{DISABLEx}$ refers to the input disable signal on the same side as the V_{Ix} inputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

3 D0 is the ADuM140D0/ADuM141D0/ADuM142D0 models, and D1 is the ADuM140D1/ADuM141D1/ADuM142D1 models. See the Ordering Guide section.

4 Input pins (V_{Ix}, $DISABLE_1$, and $DISABLE_2$) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

Table 21. ADuM140E/ADuM141E/ADuM142E Truth Table (Positive Logic)

V_{Ix} Input[1, 2]	V_{Ex} Input[1, 2]	V_{DDI} State[2]	V_{DDO} State[2]	Default Low (E0), V_{Ox} Output[1, 2, 3]	Default High (E1), V_{Ox} Output[1, 2, 3]	Test Conditions/Comments
L	H or NC	Powered	Powered	L	L	Normal operation
H	H or NC	Powered	Powered	H	H	Normal operation
X	L	Powered	Powered	Z	Z	Outputs disabled
L	H or NC	Unpowered	Powered	L	H	Fail-safe output
X[4]	L[4]	Unpowered	Powered	Z	Z	Outputs disabled
X[4]	X[4]	Powered	Unpowered	Indeterminate	Indeterminate	

1 L means low, H means high, X means don't care, NC means not connected, and Z means high impedance.

2 V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D). V_{Ex} refers to the output enable signal on the same side as the V_{Ox} outputs. V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

3 E0 is the ADuM140E0/ADuM141E0/ADuM142E0 models, and E1 is the ADuM140E1/ADuM141E1/ADuM142E1 models. See the Ordering Guide section.

4 Input pins (V_{Ix}, V_{E1}, and V_{E2}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

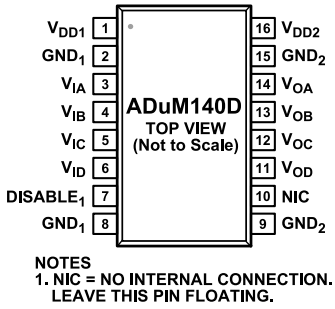

Figure 7. ADuM140D Pin Configuration

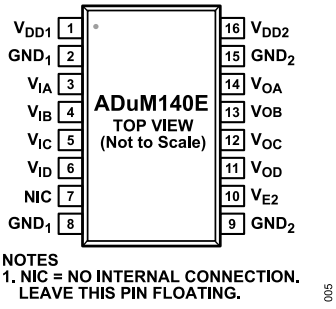

Figure 8. ADuM140E Pin Configuration

Table 22. Pin Function Descriptions

Pin No.[1]			
ADuM140D	**ADuM140E**	**Mnemonic**	**Description**
1	1	V_{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND_1	Ground Reference for Isolator Side 1.
3	3	V_{IA}	Logic Input A.
4	4	V_{IB}	Logic Input B.
5	5	V_{IC}	Logic Input C.
6	6	V_{ID}	Logic Input D.
7	Not applicable	$DISABLE_1$	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
9, 15	9, 15	GND_2	Ground Reference for Isolator Side 2.
10	7	NIC	No Internal Connection. Leave this pin floating.
Not applicable	10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, V_{OC}, and V_{OD} outputs are disabled to the high-Z state.
11	11	V_{OD}	Logic Output D.
12	12	V_{OC}	Logic Output C.
13	13	V_{OB}	Logic Output B.
14	14	V_{OA}	Logic Output A.
16	16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

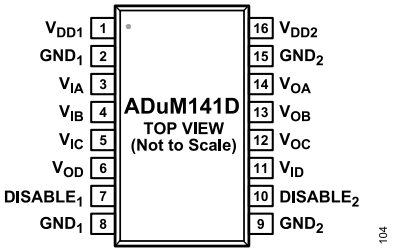

Figure 9. ADuM141D Pin Configuration

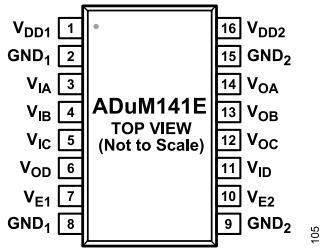

Figure 10. ADuM141E Pin Configuration

Table 23. Pin Function Descriptions

Pin No.[1]			
ADuM141D	**ADuM141E**	**Mnemonic**	**Description**
1	1	V_{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND_1	Ground Reference for Isolator Side 1.
3	3	V_{IA}	Logic Input A.
4	4	V_{IB}	Logic Input B.
5	5	V_{IC}	Logic Input C.
6	6	V_{OD}	Logic Output D.
7	Not applicable	$DISABLE_1$	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
Not applicable	7	V_{E1}	Output Enable 1. Active high logic input. When V_{E1} is high or disconnected, the V_{OD} output is enabled. When V_{E1} is low, the V_{OD} output is disabled to the high-Z state.
9, 15	9, 15	GND_2	Ground Reference for Isolator Side 2.
10	Not applicable	$DISABLE_2$	Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
Not applicable	10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA}, V_{OB}, and V_{OC} outputs are enabled. When V_{E2} is low, the V_{OA}, V_{OB}, and V_{OC} outputs are disabled to the high-Z state.
11	11	V_{ID}	Logic Input D.
12	12	V_{OC}	Logic Output C.
13	13	V_{OB}	Logic Output B.
14	14	V_{OA}	Logic Output A.
16	16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

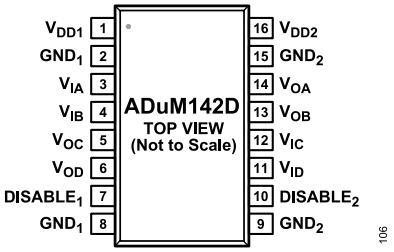

Figure 11. ADuM142D Pin Configuration

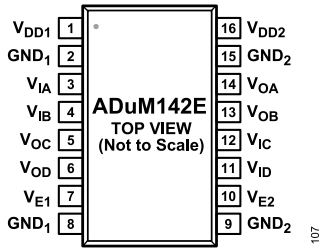

Figure 12. ADuM142E Pin Configuration

Table 24. Pin Function Descriptions

Pin No.[1]			
ADuM142D	**ADuM142E**	**Mnemonic**	**Description**
1	1	V_{DD1}	Supply Voltage for Isolator Side 1.
2, 8	2, 8	GND_1	Ground Reference for Isolator Side 1.
3	3	V_{IA}	Logic Input A.
4	4	V_{IB}	Logic Input B.
5	5	V_{OC}	Logic Output C.
6	6	V_{OD}	Logic Output D.
7	Not applicable	$DISABLE_1$	Input Disable 1. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
Not applicable	7	V_{E1}	Output Enable 1. Active high logic input. When V_{E1} is high or disconnected, the V_{OC} and V_{OD} outputs are enabled. When V_{E1} is low, the V_{OC} and V_{OD} outputs are disabled to thehigh-Z state.
9, 15	9, 15	GND_2	Ground Reference for Isolator Side 2.
10	Not applicable	$DISABLE_2$	Input Disable 2. This pin disables the isolator inputs. Outputs take on the logic state determined by the fail-safe option shown in the Ordering Guide.
Not applicable	10	V_{E2}	Output Enable 2. Active high logic input. When V_{E2} is high or disconnected, the V_{OA} and V_{OB} outputs are enabled. When V_{E2} is low, the V_{OA} and V_{OB} outputs are disabled to the high-Z state.
11	11	V_{ID}	Logic Input D.
12	12	V_{IC}	Logic Input C.
13	13	V_{OB}	Logic Output B.
14	14	V_{OA}	Logic Output A.
16	16	V_{DD2}	Supply Voltage for Isolator Side 2.

[1] Reference the AN-1109 Application Note for specific layout guidelines.

TYPICAL PERFORMANCE CHARACTERISTICS

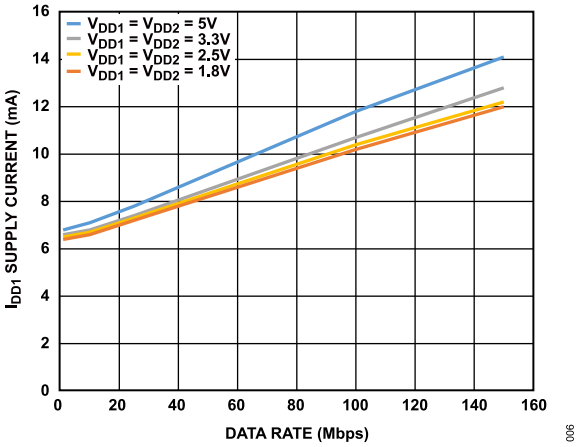

Figure 13. ADuM140D/ADuM140E I_{DD1} Supply Current vs. Data Rate at Various Voltages

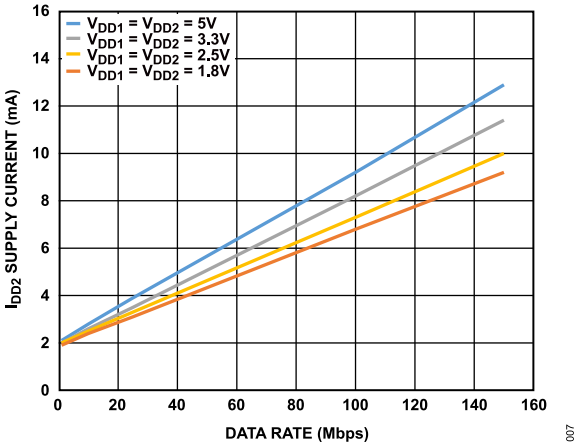

Figure 14. ADuM140D/ADuM140E I_{DD2} Supply Current vs. Data Rate at Various Voltages

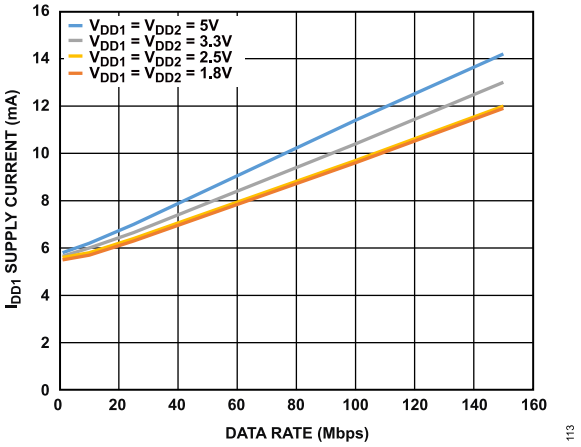

Figure 15. ADuM141D/ADuM141E I_{DD1} Supply Current vs. Data Rate at Various Voltages

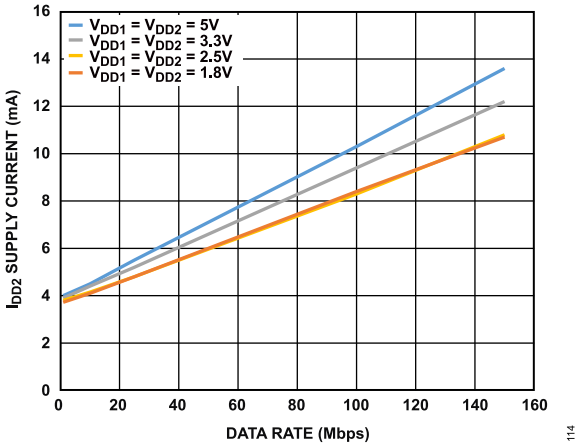

Figure 16. ADuM141D/ADuM141E I_{DD2} Supply Current vs. Data Rate at Various Voltages

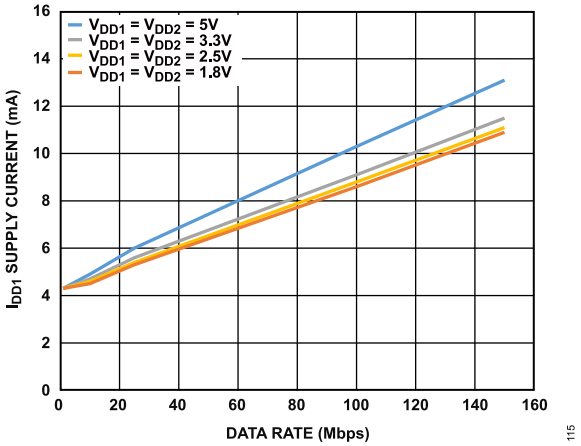

Figure 17. ADuM142D/ADuM142E I_{DD1} Supply Current vs. Data Rate at Various Voltages

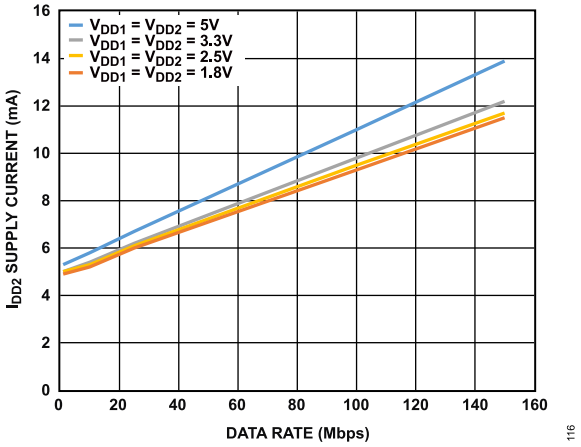

Figure 18. ADuM142D/ADuM142E I_{DD2} Supply Current vs. Data Rate at Various Voltages

TYPICAL PERFORMANCE CHARACTERISTICS

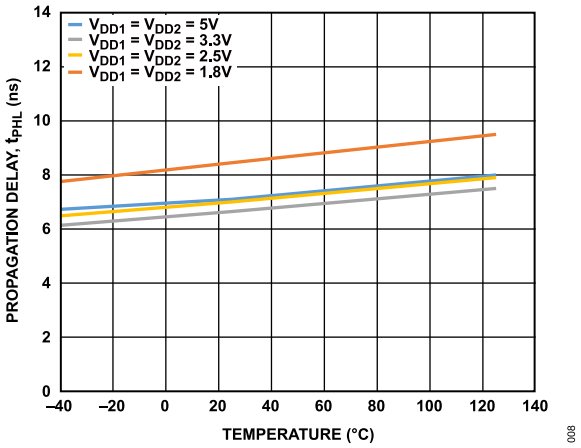

Figure 19. Propagation Delay, t_{PLH} vs. Temperature at Various Voltages

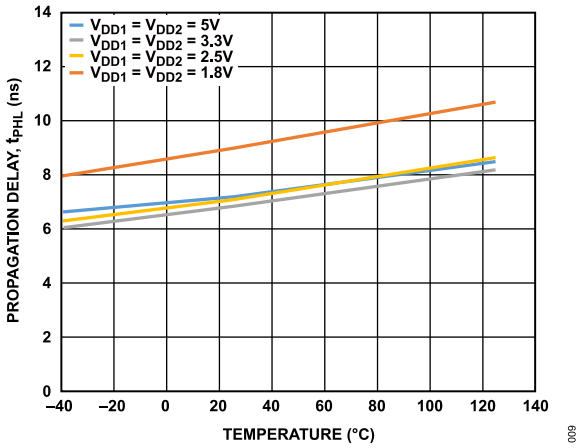

Figure 20. Propagation Delay, t_{PHL} vs. Temperature at Various Voltages

APPLICATIONS INFORMATION

OVERVIEW

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying (OOK) technique and the differential architecture shown in Figure 22 and Figure 23, theADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E have very low propagation delay and high speed. Internal regulators and input/output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, offering voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques.

Figure 22 illustrates the waveforms for models of the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state (ADuM140D0/ADuM140E0/ADuM141D0/ADuM141E0/ADuM142D0/ADuM142E0) sets the output to low. For the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E that have a high fail-safe output state, Figure 23 illustrates the conditions where the carrier waveform is off when the input state is high. When the input side is off or not operating, the fail-safe output state of high (ADuM140D1/ADuM140E1/ADuM141D1/ADuM141E1/ADuM142D1/ADuM142E1) sets the output to high. See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 21). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 must also be considered, unless the ground pair on each package side is connected close to the package.

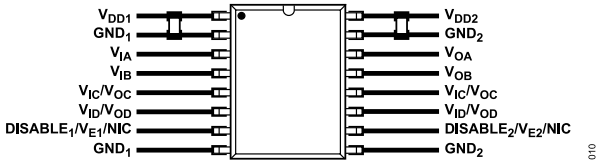

Figure 21. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

See the AN-1109 Application Note for board layout guidelines.

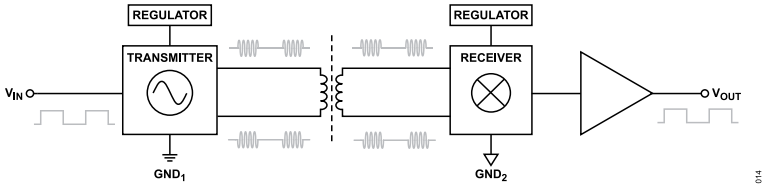

Figure 22. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State

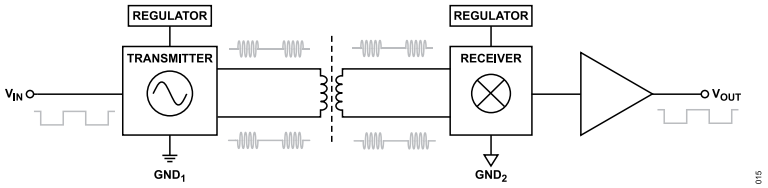

Figure 23. Operational Block Diagram of a Single Channel with a High Fail-Safe Output State

APPLICATIONS INFORMATION

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time required for a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

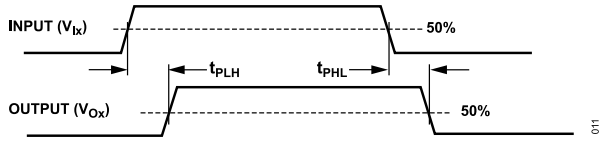

Figure 24. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E component.

Propagation delay skew is the maximum amount the propagation delay that differs between multiple ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E components operating under the same conditions.

JITTER MEASUREMENT

Figure 25 shows the eye diagram for the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E. The measurement was taken using an Agilent 81110A pulse pattern generator at 150 Mbps with pseudorandom bit sequences (PRBS) 2(n − 1), n = 14, for 5 V supplies. Jitter was measured with the Tektronix Model 5104B oscilloscope, 1 GHz, 10 GSPS with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E with 490 ps p-p jitter.

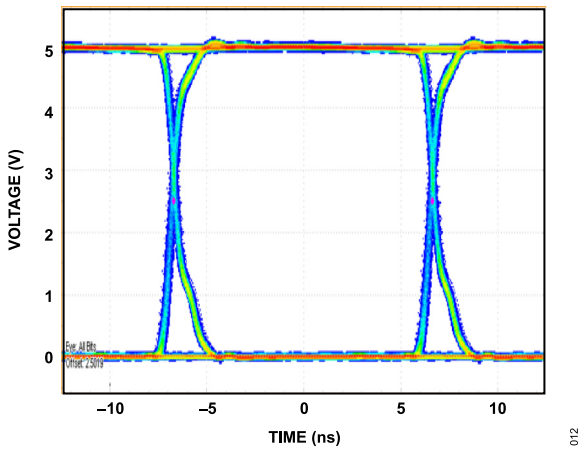

Figure 25. ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM140D/ADuM140E/ADuM141D/ADuM141E/ADuM142D/ADuM142E.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 19 summarize the maximum continuous working voltages as per DIN EN IEC 60747-17 (VDE 0884-17). Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
R-16	SOIC_N	16-Lead Standard Small Outline Package, Narrow Body
RW-16	SOIC_W	16-Lead Standard Small Outline Package, Wide Body
RQ-16	QSOP	16-Lead Shrink Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM140D1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM140D1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM140D0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM140D0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM140E1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM140E1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM140E0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM140E0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM140D1BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM140D1BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM140D0BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM140D0BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM140D1BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM140D1BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM140D0BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM140D0BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM140E1BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM140E1BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM140E1WBRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM140E1WBRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM140E0BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM140E0BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM140E1BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM140E1BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM140E0BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM140E0BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM141D1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM141D1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM141D0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM141D0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM141E1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM141E1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM141E0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM141E0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM141D1BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM141D1BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM141D0BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM141D0BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM141D1BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16

OUTLINE DIMENSIONS

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM141D1BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM141D0BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM141D0BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM141E1BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM141E1BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM141E1WBRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM141E1WBRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM141E0BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM141E0BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM141E1BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM141E1BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM141E0BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM141E0BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM141E0WBRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM141E1WBRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM141E1WBRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM142D1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 98	R-16
ADuM142D1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM142D0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM142D0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM142E1BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM142E1BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM142E0BRZ	−40°C to +125°C	16-Lead SOIC_N	Tube, 48	R-16
ADuM142E0BRZ-RL7	−40°C to +125°C	16-Lead SOIC_N	Reel, 1000	R-16
ADuM142D1BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM142D1BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM142D0BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM142D0BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM142D1BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM142D1BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM142D0BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM142D0BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM142E1BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM142E1BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM142E1WBRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM142E1WBRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM142E0BRWZ	−40°C to +125°C	16-Lead SOIC_W	Tube, 47	RW-16
ADuM142E0BRWZ-RL	−40°C to +125°C	16-Lead SOIC_W	Reel, 1000	RW-16
ADuM142E1BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM142E1BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM142E0BRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM142E0BRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16
ADuM142E1WBRQZ	−40°C to +125°C	16-Lead QSOP	Tube, 98	RQ-16
ADuM142E1WBRQZ-RL7	−40°C to +125°C	16-Lead QSOP	Reel, 1000	RQ-16

[1] Z = RoHS Compliant Part.

[2] The ADuM140E1WBRWZ, ADuM140E1WBRWZ-RL, ADuM141E1WBRWZ, ADuM141E1WBRWZ-RL, ADuM141E0WBRQZ-RL7, ADuM141E1WBRQZ, ADuM141E1WBRQZ-RL7, ADuM142E1WBRWZ, ADuM142E1WBRWZ-RL, ADuM142E1WBRQZ, and ADuM142E1WBRQZ-RL7 are qualified for automotive applications.

OUTLINE DIMENSIONS

NUMBER OF INPUTS, WITHSTAND VOLTAGE RATING, FAIL-SAFE OUTPUT STATE, INPUT DISABLE, AND OUTPUT ENABLE

Model[1, 2]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Input Disable	Output Enable
ADuM140D1BRZ	4	0	3.0	High	Yes	No
ADuM140D1BRZ-RL7	4	0	3.0	High	Yes	No
ADuM140D0BRZ	4	0	3.0	Low	Yes	No
ADuM140D0BRZ-RL7	4	0	3.0	Low	Yes	No
ADuM140E1BRZ	4	0	3.0	High	No	Yes
ADuM140E1BRZ-RL7	4	0	3.0	High	No	Yes
ADuM140E0BRZ	4	0	3.0	Low	No	Yes
ADuM140E0BRZ-RL7	4	0	3.0	Low	No	Yes
ADuM140D1BRWZ	4	0	3.75	High	Yes	No
ADuM140D1BRWZ-RL	4	0	3.75	High	Yes	No
ADuM140D0BRWZ	4	0	3.75	Low	Yes	No
ADuM140D0BRWZ-RL	4	0	3.75	Low	Yes	No
ADuM140D1BRQZ	4	0	3.0	High	Yes	No
ADuM140D1BRQZ-RL7	4	0	3.0	High	Yes	No
ADuM140D0BRQZ	4	0	3.0	Low	Yes	No
ADuM140D0BRQZ-RL7	4	0	3.0	Low	Yes	No
ADuM140E1BRWZ	4	0	3.75	High	No	Yes
ADuM140E1BRWZ-RL	4	0	3.75	High	No	Yes
ADuM140E1WBRWZ	4	0	3.75	High	No	Yes
ADuM140E1WBRWZ-RL	4	0	3.75	High	No	Yes
ADuM140E0BRWZ	4	0	3.75	Low	No	Yes
ADuM140E0BRWZ-RL	4	0	3.75	Low	No	Yes
ADuM140E1BRQZ	4	0	3.0	High	No	Yes
ADuM140E1BRQZ-RL7	4	0	3.0	High	No	Yes
ADuM140E0BRQZ	4	0	3.0	Low	No	Yes
ADuM140E0BRQZ-RL7	4	0	3.0	Low	No	Yes
ADuM141D1BRZ	3	1	3.0	High	Yes	No
ADuM141D1BRZ-RL7	3	1	3.0	High	Yes	No
ADuM141D0BRZ	3	1	3.0	Low	Yes	No
ADuM141D0BRZ-RL7	3	1	3.0	Low	Yes	No
ADuM141E1BRZ	3	1	3.0	High	No	Yes
ADuM141E1BRZ-RL7	3	1	3.0	High	No	Yes
ADuM141E0BRZ	3	1	3.0	Low	No	Yes
ADuM141E0BRZ-RL7	3	1	3.0	Low	No	Yes
ADuM141D1BRWZ	3	1	3.75	High	Yes	No
ADuM141D1BRWZ-RL	3	1	3.75	High	Yes	No
ADuM141D0BRWZ	3	1	3.75	Low	Yes	No
ADuM141D0BRWZ-RL	3	1	3.75	Low	Yes	No
ADuM141D1BRQZ	3	1	3.0	High	Yes	No
ADuM141D1BRQZ-RL7	3	1	3.0	High	Yes	No
ADuM141D0BRQZ	3	1	3.0	Low	Yes	No
ADuM141D0BRQZ-RL7	3	1	3.0	Low	Yes	No
ADuM141E1BRWZ	3	1	3.75	High	No	Yes
ADuM141E1BRWZ-RL	3	1	3.75	High	No	Yes

OUTLINE DIMENSIONS

Model[1, 2]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Input Disable	Output Enable
ADuM141E1WBRWZ	3	1	3.75	High	No	Yes
ADuM141E1WBRWZ-RL	3	1	3.75	High	No	Yes
ADuM141E0BRWZ	3	1	3.75	Low	No	Yes
ADuM141E0BRWZ-RL	3	1	3.75	Low	No	Yes
ADuM141E1BRQZ	3	1	3.0	High	No	Yes
ADuM141E1BRQZ-RL7	3	1	3.0	High	No	Yes
ADuM141E0BRQZ	3	1	3.0	Low	No	Yes
ADuM141E0BRQZ-RL7	3	1	3.0	Low	No	Yes
ADuM141E0WBRQZ-RL7	3	1	3.0	Low	No	Yes
ADuM141E1WBRQZ	3	1	3.0	High	No	Yes
ADuM141E1WBRQZ-RL7	3	1	3.0	High	No	Yes
ADuM142D1BRZ	2	2	3.0	High	Yes	No
ADuM142D1BRZ-RL7	2	2	3.0	High	Yes	No
ADuM142D0BRZ	2	2	3.0	Low	Yes	No
ADuM142D0BRZ-RL7	2	2	3.0	Low	Yes	No
ADuM142E1BRZ	2	2	3.0	High	No	Yes
ADuM142E1BRZ-RL7	2	2	3.0	High	No	Yes
ADuM142E0BRZ	2	2	3.0	Low	No	Yes
ADuM142E0BRZ-RL7	2	2	3.0	Low	No	Yes
ADuM142D1BRWZ	2	2	3.75	High	Yes	No
ADuM142D1BRWZ-RL	2	2	3.75	High	Yes	No
ADuM142D0BRWZ	2	2	3.75	Low	Yes	No
ADuM142D0BRWZ-RL	2	2	3.75	Low	Yes	No
ADuM142D1BRQZ	2	2	3.0	High	Yes	No
ADuM142D1BRQZ-RL7	2	2	3.0	High	Yes	No
ADuM142D0BRQZ	2	2	3.0	Low	Yes	No
ADuM142D0BRQZ-RL7	2	2	3.0	Low	Yes	No
ADuM142E1BRWZ	2	2	3.75	High	No	Yes
ADuM142E1BRWZ-RL	2	2	3.75	High	No	Yes
ADuM142E1WBRWZ	2	2	3.75	High	No	Yes
ADuM142E1WBRWZ-RL	2	2	3.75	High	No	Yes
ADuM142E0BRWZ	2	2	3.75	Low	No	Yes
ADuM142E0BRWZ-RL	2	2	3.75	Low	No	Yes
ADuM142E1BRQZ	2	2	3.0	High	No	Yes
ADuM142E1BRQZ-RL7	2	2	3.0	High	No	Yes
ADuM142E0BRQZ	2	2	3.0	Low	No	Yes
ADuM142E0BRQZ-RL7	2	2	3.0	Low	No	Yes
ADuM142E1WBRQZ	2	2	3.0	High	No	Yes
ADuM142E1WBRQZ-RL7	2	2	3.0	High	No	Yes

[1] Z = RoHS Compliant Part.

[2] The ADuM140E1WBRWZ, ADuM140E1WBRWZ-RL, ADuM141E1WBRWZ, ADuM141E1WBRWZ-RL, ADuM141E0WBRQZ-RL7, ADuM141E1WBRQZ, ADuM141E1WBRQZ-RL7, ADuM142E1WBRWZ, ADuM142E1WBRWZ-RL, ADuM142E1WBRQZ, and ADuM142E1WBRQZ-RL7 are qualified for automotive applications.

OUTLINE DIMENSIONS

AUTOMOTIVE PRODUCTS

The ADuM140E1W, ADuM141E0W, ADuM141E1W and ADuM142E1W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.