S-19990 Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, LOW EMI, STEP-UP / FLYBACK SWITCHING REGULATOR CONTROLLER

www.ablic.com

Rev.1.4_00

This IC is a step-up / flyback switching regulator controller developed using high withstand voltage CMOS process technologies.
Its wide input operating range of 3.0 V to 36 V makes it suitable for powering automotive start-stop systems and emergency battery backup systems. When this IC is used to configure a converter and the output voltage (V_{OUT}) of the converter is applied to the VIN pin in a bootstrap configuration, the input voltage can be extended below the operating input voltage range after startup.
This IC contributes to system space saving as it adopted suitable packages for high-density mounting like small-sized HSNT-8(2030), can operate at very high switching frequencies, and the peripheral parts can be made compact. A built-in spread spectrum clock generation circuit enhances the EMI performance of the system.
An overcurrent protection circuit protects the IC and the coil from excessive load current, and a thermal shutdown circuit prevents damage from heat generation.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.

■ Features

- Input voltage: 3.0 V to 36.0 V
- Low voltage operation after startup (V_{IN} = 1.5 V, V_{OUT} = 6.8 V, I_{OUT} = 2 A, f_{OSC} = 400 kHz in a bootstrap configuration)
- Control system: Current mode
- FB pin voltage accuracy: ±1.5%
- Oscillation frequency: 2.2 MHz typ., 400 kHz typ.
- Spread spectrum clock generation function: F_{SSS} = +6% typ. (Diffusion rate)
- Overcurrent protection function: Pulse-by-pulse method
- Thermal shutdown function: 170°C typ. (detection temperature)
- Short-circuit protection function: Hiccup control, Latch control
- Soft-start function: 5.8 ms typ.
- Under voltage lockout function (UVLO): 2.75 V typ. (detection voltage)
- Input and output capacitors: Ceramic capacitor compatible
- Operation temperature range: Ta = −40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified*1

*1. Contact our sales representatives for details.

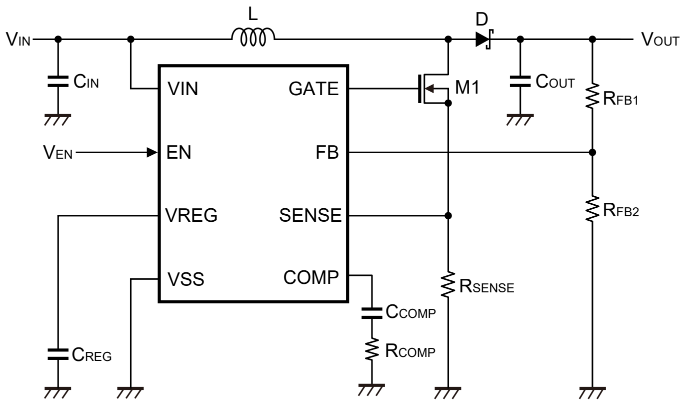
■ Applications

- Automotive and industrial step-up flyback converters
- Automotive start-stop systems
- Emergency battery backup systems
- Automotive LED lamps
- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

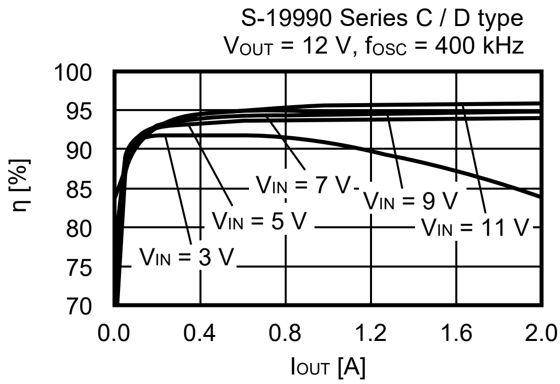
■ Packages

- HTMSOP-8 (4.0 mm × 2.9 mm × t0.8 mm max.)
- HSNT-8(2030) (3.0 mm × 2.0 mm × t0.5 mm max.)

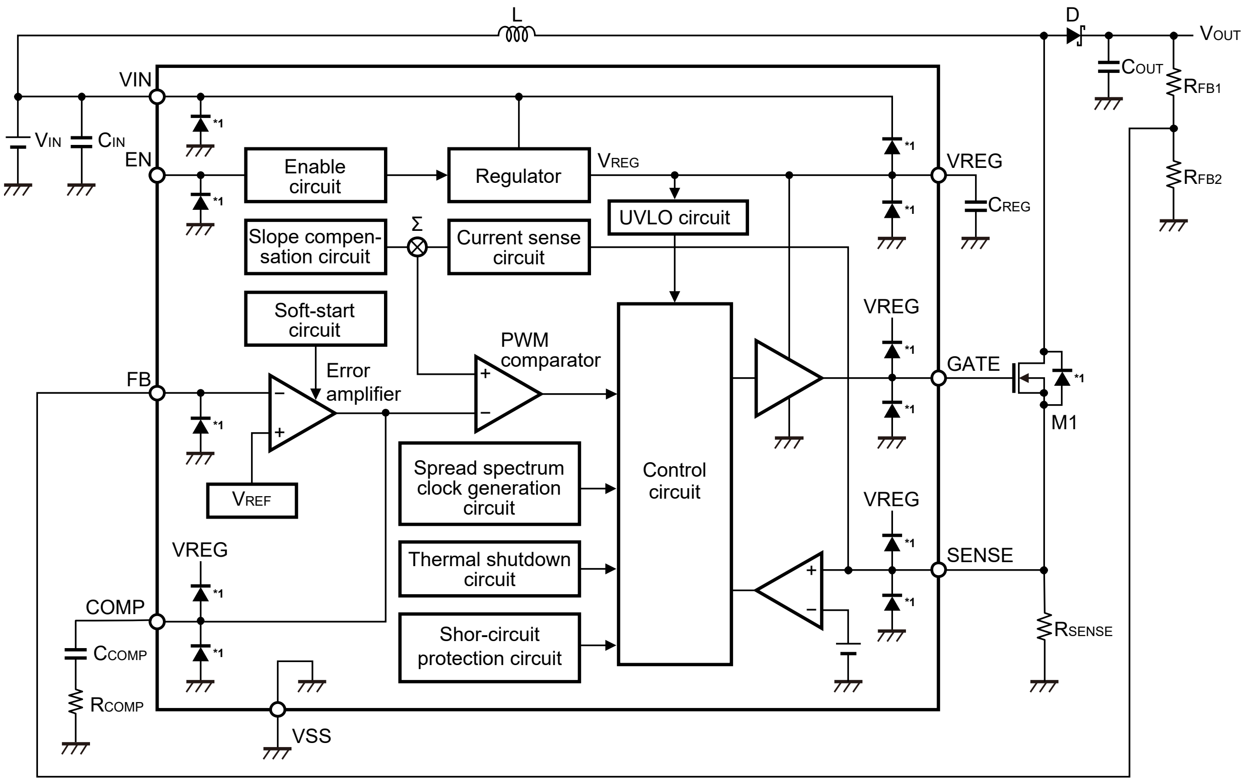
■ Typical Application Circuit



■ Efficiency



■ Block Diagram



***1.** Parasitic diode

Figure 1

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name

S-19990 x A - xxxx U 7

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- xxxx: Package name abbreviation and packing specification*1
  - S8T1: HTMSOP-8, Tape
  - A8T1: HSNT-8(2030), Tape
- A: Operation temperature
  - A: Ta = −40°C to +125°C
- x: Product type*2
  - A to D

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Function list of product types**".

2. Function list of product types

Table 1

Product Type	Oscillation Frequency	Short-circuit Protection Function
A	2.2 MHz	Hiccup control
B	2.2 MHz	Latch control
C	400 kHz	Hiccup control
D	400 kHz	Latch control

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land	Stencil Opening
HTMSOP-8	FP008-A-P-SD	FP008-A-C-SD	FP008-A-R-SD	FP008-A-L-SD	−
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD	PP008-A-L-S1

■ Pin Configurations

1. HTMSOP-8

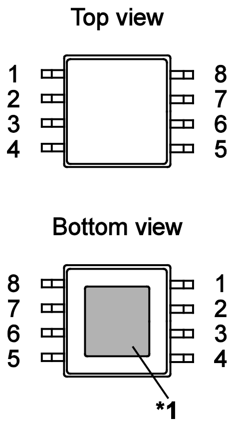


Figure 2

Table 3

Pin No.	Symbol	Description
1	EN	Enable pin
2	COMP	Error amplifier circuit output pin
3	FB	Feedback pin
4	VIN	Power supply pin
5	VREG*2	Internal power supply pin
6	GATE	Gate drive output pin
7	VSS	GND pin
8	SENSE	Current detection input pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
***2.** The VREG pin cannot supply load current outside.

2. HSNT-8(2030)

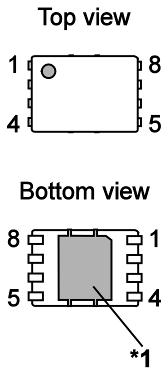


Figure 3

Table 4

Pin No.	Symbol	Description
1	EN	Enable pin
2	COMP	Error amplifier circuit output pin
3	FB	Feedback pin
4	VIN	Power supply pin
5	VREG*2	Internal power supply pin
6	GATE	Gate drive output pin
7	VSS	GND pin
8	SENSE	Current detection input pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.
***2.** The VREG pin cannot supply load current outside.

■ Absolute Maximum Ratings

Table 5

(Unless otherwise specified: Ta = +25°C, V_{SS} = 0 V)

Item	Symbol	Absolute Maximum Ratings	Unit
VIN pin voltage	V_{IN}	$V_{SS} - 0.3$ to $V_{SS} + 45$	V
EN pin voltage	V_{EN}	$V_{SS} - 0.3$ to $V_{SS} + 45$	V
FB pin voltage	V_{FB}	$V_{SS} - 0.3$ to $V_{REG} + 0.3 \leq V_{SS} + 6.0$	V
VREG pin voltage	V_{REG}	$V_{SS} - 0.3$ to $V_{IN} + 0.3 \leq V_{SS} + 6.0$	V
GATE pin voltage	V_{GATE}	$V_{SS} - 0.3$ to $V_{REG} + 0.3 \leq V_{SS} + 6.0$	V
COMP pin voltage	V_{COMP}	$V_{SS} - 0.3$ to $V_{REG} + 0.3 \leq V_{SS} + 6.0$	V
SENSE pin voltage	V_{SENSE}	$V_{SS} - 0.3$ to $V_{REG} + 0.3 \leq V_{SS} + 6.0$	V
Junction temperature	T_j	−40 to +150	°C
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HTMSOP-8	Board A	−	159	−	°C/W
			Board B	−	113	−	°C/W
			Board C	−	39	−	°C/W
			Board D	−	40	−	°C/W
			Board E	−	30	−	°C/W
		HSNT-8(2030)	Board A	−	181	−	°C/W
			Board B	−	135	−	°C/W
			Board C	−	40	−	°C/W
			Board D	−	42	−	°C/W
			Board E	−	32	−	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 7

(V_{IN} = 12 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating input voltage	V_{IN}	−	3.0	−	36.0	V
Current consumption during shutdown	I_{SSS}	V_{EN} = 0 V	−	0.1	5.0	μA
Current consumption during switching off	I_{SS}	V_{FB} = 0.82 V	−	60	120	μA
UVLO detection voltage	V_{UVLO-}	VREG pin voltage	2.55	2.75	2.95	V
UVLO release voltage	V_{UVLO+}	VREG pin voltage	2.65	2.85	3.05	V
FB pin voltage	V_{FB}	−	0.788	0.800	0.812	V
FB pin current	I_{FB}	V_{FB} = 1.0 V	−0.06	−	0.06	μA
Error amplifier transconductance	gm	−	−	220	−	μS
Oscillation frequency	f_{OSC}	A / B type	1.98	2.2	2.42	MHz
		C / D type	360	400	440	kHz
Oscillation frequency modulation rate	F_{SSS}	−	−	+6	−	%
Minimum ON time	t_{ON_MIN}	−	−	45	−	ns
Maximum duty ratio	MaxDuty	A / B type	82	88	94	%
		C / D type	91	95	99	%
Soft-start wait time	t_{SSW}	Time until V_{OUT} starts rising, C_{REG} = 1 μF	0.15	0.37	0.70	ms
Soft-start time	t_{SS}	Time until V_{FB} reaches 90% after it starts rising	3.0	5.8	8.5	ms
GATE pin ON-resistance	R_{ONH}	Output is "H", I_{GATE} = 50 mA	−	1.5	3.0	Ω
	R_{ONL}	Output is "L", I_{GATE} = −50 mA	−	1.0	2.0	Ω
Overcurrent protection detection voltage	V_{LIM}	−	0.128	0.14	0.152	V
VREG pin output voltage	V_{REG}	−	−	5.0	−	V
Thermal shutdown detection temperature	T_{SD}	Junction temperature	−	170	−	°C
Thermal shutdown release temperature	T_{SR}	Junction temperature	−	150	−	°C
High level input voltage	V_{SH}	EN pin	2.0	−	−	V
Low level input voltage	V_{SL}	EN pin	−	−	0.8	V
High level input current	I_{SH}	EN pin, V_{EN} = 2.0 V	−	−	1	μA
Low level input current	I_{SL}	EN pin, V_{EN} = 0 V	−0.5	−	0.5	μA

■ Operation

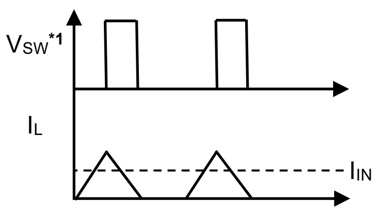
1. Overview of operation

This IC adopts the current mode control. By comparing the current feedback signal which has slope compensation added to the current flows through SENSE resistor with the output signal of error amplifier, the duty ratio of the GATE pin is determined. Using the negative feedback loop configured, the error amplifier output signal is maintained at the value that V_{REF} and FB pin voltage (V_{FB}) will be equalized.

2. Inductor current operating mode

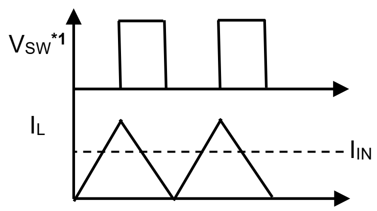
In converters that use diodes as rectifier elements, the inductor current (I_L) shifts between Discontinuous Current Mode (DCM) and Continuous Current Mode (CCM), depending on the load current (I_{OUT}).
The I_{OUT} when the inductor current is exactly zero during the switching cycle is the boundary mode between the discontinuous and continuous current modes. The I_{OUT} at this time is shown below. For details, refer to **Figure 4** to **Figure 6**.

$$I_{OUT} = \frac{V_{IN}^2}{2 \times L \times V_{OUT}}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)T$$



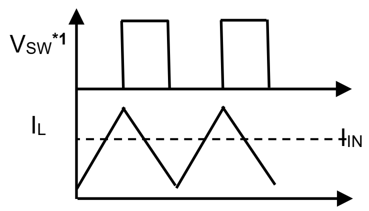
Discontinuous current mode

Figure 4



Boundary mode

Figure 5



Continuous Current Mode

Figure 6

***1.** V_{SW} is the voltage at the point (switching node) where the step-up switching regulator circuit, FET, and diode are connected, which is a square wave.

The duty cycle (D_{dcm}) in discontinuous current mode operation is shown in the equation below. D_{dcm} varies significantly with load changes.

$$D_{dcm} = \frac{\sqrt{2 \times L \times I_{OUT} \times (V_{OUT} + V_F - V_{IN}) \times f_{OSC}}}{V_{IN}}$$

And the duty cycle (D_{ccm}) in continuous current mode operation is shown in the equation below. The input and output voltages determine D_{ccm}.

$$D_{ccm} = 1 - \frac{V_{IN}}{V_{OUT} + V_F}$$

Remark L: Inductor [H]
I_{OUT}: Load current [A]
V_{IN}: Input voltage [V]
V_{OUT}: Output voltage [V]
V_F: Diode forward voltage [V]
f_{OSC}: Oscillation frequency [Hz]
T: Period [s]

3. Minimum ON time

When the external FET M1 in **Figure 1** on "**■ Block Diagram",** is turned on, this IC starts switching at high-speed generating high-frequency spike noise in the inductor current detection resistor (R_{SENSE}). Normally, a slope voltage proportional to the inductor current value is input to the SENSE pin, and the IC's internal latch circuit is reset to the desired voltage value. If there is any spike noise, the occurrence of the noise will reset the latch incorrectly. To prevent such malfunctions, a blank time is set so that a reset is not triggered even if M1 is turned on. This blank time is defined as the minimum ON time (t_{ON_MIN}).

4. PWM / PFM switching control

This IC automatically switches between pulse width modulation method (PWM) and pulse frequency modulation method (PFM) according to the load current. PFM control is selected when under light load, and the pulse will skip according to the load current. Pulse skips will occur when the following conditions are met.

$$D_{dcm} < t_{ON\_MIN} \times f_{OSC}$$

Pulse skipping reduces self-current consumption and improves efficiency at light loads.

5. Under voltage lockout function (UVLO)

This IC has a built-in UVLO circuit to prevent the IC from malfunctioning due to a transient status at power-on or a momentary drop in the supply voltage. When UVLO status is detected, the GATE pin is pulled down. For this reason, switching operation will stop. The soft-start function is reset if UVLO status is detected once and is restarted by releasing the UVLO status.
Note that the other internal circuits operate normally, and the status is different from the disabled status.
Also, there is a hysteresis width for avoiding malfunctions due to generation of noise etc. in the input voltage.

6. Output voltage settings

Set the output voltage (V_{OUT}) by connecting voltage setting resistors R_{FB1} and R_{FB2} to the FB pin as shown in the equation below.

$$V_{OUT} = V_{FB} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}}$$

7. EN pin

This pin starts and stops switching operation. When the EN pin is set to "L", the operation of all internal circuits is stopped, reducing current consumption. When not using the EN pin, connect it to the VIN pin. Since the EN pin is neither pulled down nor pulled up internally, do not use it in the floating status. The structure of the EN pin is shown in **Figure 7**, and the clamp circuit is internally connected.

Table 8

EN Pin	Internal Circuit	GATE
"H"	Enable (normal operation)	Switching operation
"L"	Disable (standby)	Pulled down to V_{SS}

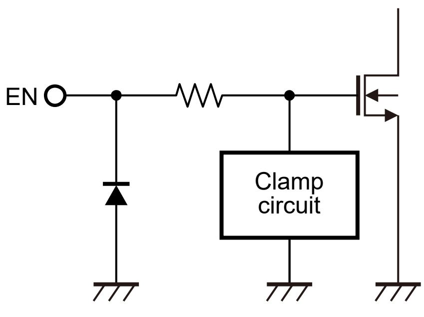


Figure 7

8. Thermal shutdown function

This IC has a built-in thermal shutdown circuit to limit overheating. When the junction temperature increases to 170°C typ., the thermal shutdown circuit becomes the detection status, and the switching operation is stopped. When the junction temperature decreases to 150°C typ., the thermal shutdown circuit becomes the release status, and the switching operation is restarted.
If the thermal shutdown circuit becomes the detection status due to self-heating, the switching operation is stopped and output voltage (V_{OUT}) decreases. For this reason, the self-heating is limited and the temperature of the IC decreases. The thermal shutdown circuit becomes release status when the temperature of the IC decreases, and the switching operation is restarted, thus the self-heating is generated again. Repeating this procedure makes the waveform of V_{OUT} into a pulse-like form. Note that the product may suffer physical damage such as deterioration if the above phenomenon occurs continuously. Switching operation stopping and starting can be stopped by either setting the EN pin to "L", lowering the output current (I_{OUT}) to reduce internal power consumption, or decreasing the ambient temperature.

Table 9

Thermal Shutdown Circuit	GATE
Release: 150°C typ.*1	Switching operation
Detection: 170°C typ.*1	Pulled down to V_{SS}

***1.** Junction temperature

9. Overcurrent protection function

The overcurrent protection circuit monitors the current that flows through the external FET and limits current to prevent thermal destruction of the IC due to an overload, magnetic saturation in the inductor, etc.
When overcurrent flows through the external FET and the potential difference between the SENSE pin and GND exceeds the overcurrent protection detection voltage (V_{LIM}) (0.14 V typ.), the external FET is turned off. It is turned back on when the next switching cycle starts. If the potential difference between the SENSE pin and GND remains above V_{LIM}, the external FET is turned off again, and this sequence of operations is repeated.
However, when the current flowing through the external FET decreases and the potential difference between the SENSE pin and GND drops below V_{LIM}, the IC returns to normal operation.
If the slope of the inductor current is large, the delay time of the overcurrent protection circuit may cause an apparent increase in the potential difference between the SENSE pin and GND. This tends to occur when an inductor with low inductance is used or when V_{IN} is large.

10. Frequency foldback function

The frequency foldback function has FB pin voltage (V_{FB}) and oscillation frequency (f_{OSC}) to have a proportional relation when V_{FB} is 0.7 V typ. or lower.
The frequency foldback function in this IC is set to invalid at start-up.

11. Short-circuit protection function

11. 1 Hiccup control

A / C type of this IC has a built-in short-circuit protection function for Hiccup control.
The hiccup control is a method for periodically carrying out automatic recovery when the IC detects overcurrent and stops the switching operation.

11. 1. 1 When overload status is released

<1> Overcurrent detection
<2> After detection of the FB pin voltage (V_{FB}) < 0.7 V typ., frequency foldback function becomes valid.
<3> Detection of V_{FB} < 0.5 V typ.
<4> 0.3 ms elapse
<5> Switching operation stop (for 21 ms typ.) (short-circuit protection detection status)
<6> Overload status release
<7> The IC restarts, soft-start function starts.
In this case, it is unnecessary to input an external reset signal for restart.
<8> V_{FB} reaches 0.72 V typ. after 5.8 ms typ. elapses.

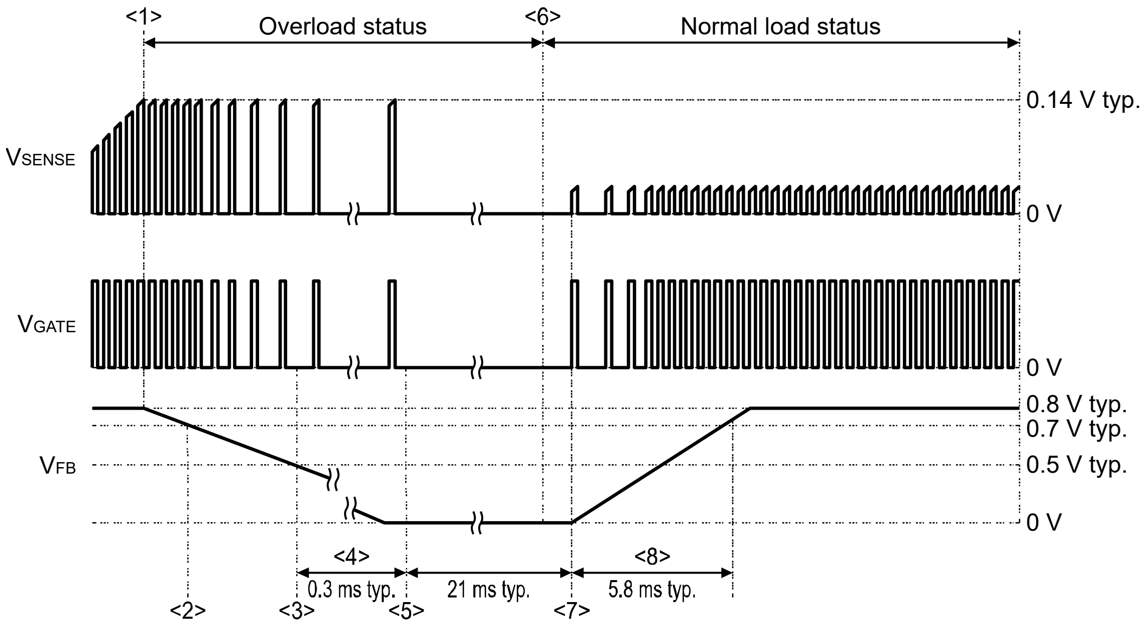


Figure 8

11. 1. 2 When overload status continues

<1> Overcurrent detection
<2> After detection of $V_{FB} < 0.7$ V typ., frequency foldback function becomes valid.
<3> Detection of $V_{FB} < 0.5$ V typ.
<4> 0.3 ms elapse
<5> Switching operation stop (for 21 ms typ.) (short-circuit protection detection status)
<6> The IC restarts, soft-start function starts.
<7> The status returns to <3> when overload status continues after 8.6 ms typ. elapses.

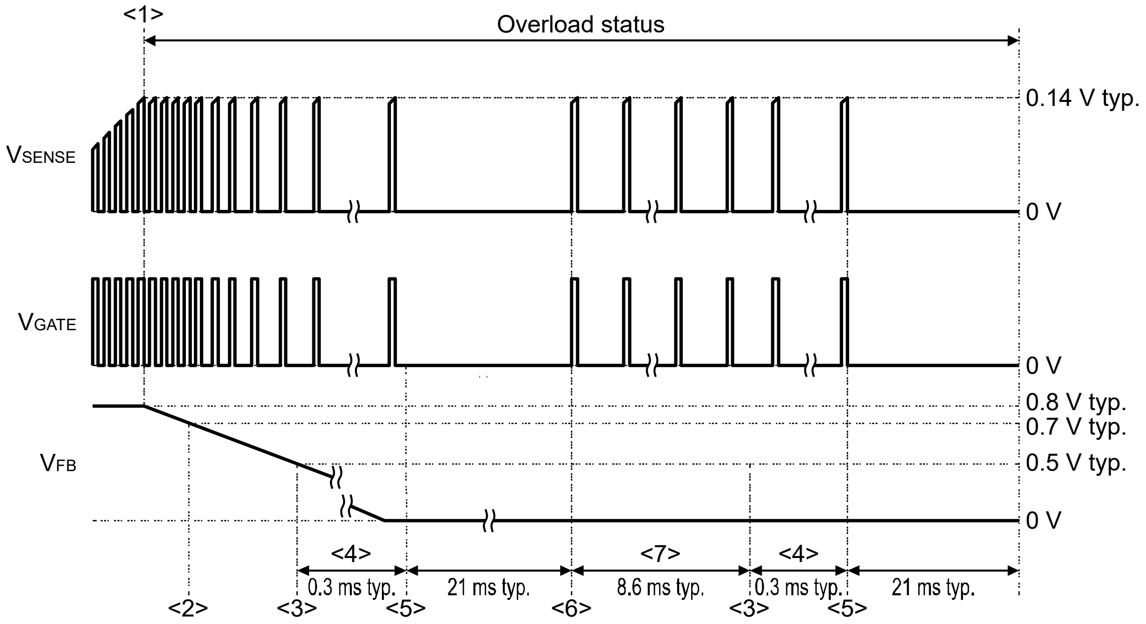


Figure 9

11. 2 Latch control

B / D type of this IC has a built-in short-circuit protection function for Latch control.
The latch control is a method for maintaining the Latch status when the IC detects overcurrent and stops the switching operation.

<1> Overcurrent detection
<2> After detection of V_{FB} < 0.7 V typ., frequency foldback function becomes valid.
<3> Detection of V_{FB} < 0.5 V typ.
<4> 0.3 ms elapse
<5> Switching operation stop (short-circuit protection detection status)

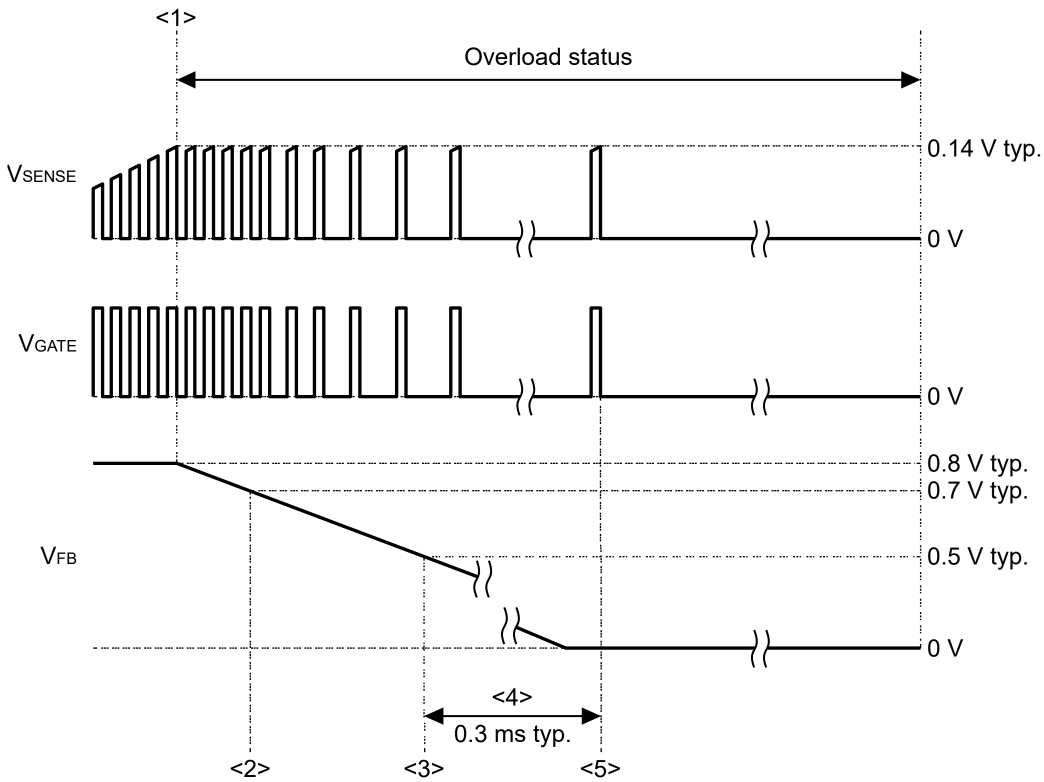


Figure 10

In addition, Latch status is reset under the following conditions.

- At UVLO detection
- When the EN pin changes from "H" to "L".

12. Pre-bias compatible soft-start function

This IC has a built-in pre-bias compatible soft-start circuit.
If the pre-bias compatible soft-start circuit starts when electrical charge remains in the output voltage (V_{OUT}) as a result of power supply restart, etc., or when V_{OUT} is biased beforehand (pre-bias status), switching operation is stopped until the soft-start voltage exceeds the FB pin voltage (V_{FB}), and then V_{OUT} is maintained. If the soft-start voltage exceeds V_{FB}, switching operation will restart and V_{OUT} will rise to the output voltage setting value. This allows the output voltage setting value to be reached without lowering the pre-biased V_{OUT}.

In this IC, V_{OUT} reaches the output voltage setting value gradually due to the soft-start circuit.
In the following cases, rush current and V_{OUT} overshoot are reduced.

- When the EN pin changes from "L" to "H".
- When UVLO operation is released.*1
- When thermal shutdown is released.*1
- When recovering from short-circuit protection detection status*1

***1.** In this case, the soft-start wait time is eliminated.

The soft-start circuit starts operating after "H" is input to the EN pin and the soft-start wait time (t_{SSW}) = 0.37 ms typ. elapses. The soft-start time (t_{SS}) is set to 5.8 ms typ.

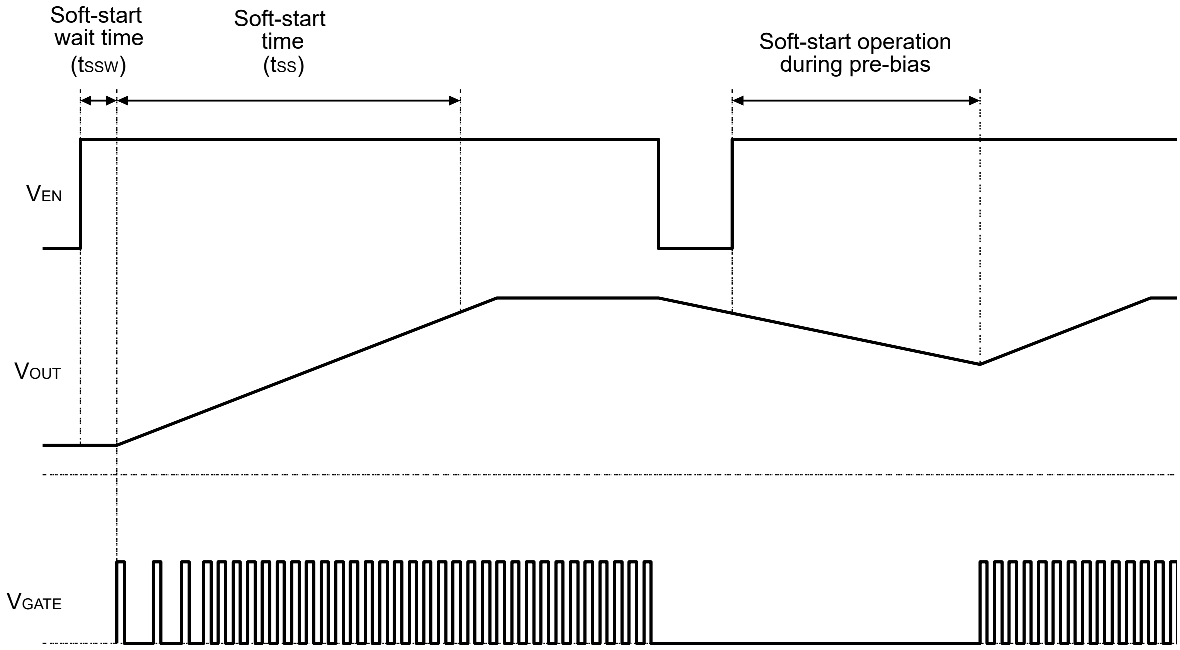


Figure 11

13. Internal power supply (V_{REG})

Some of the circuits in the IC operate using the VREG pin voltage (V_{REG}) as the power supply. To stabilize this internal power supply, a ceramic capacitor with 1 μF needs to be connected between the VREG pin and the VSS pin. To achieve low impedance, this capacitor should be placed as close to the IC as possible. Additionally, note that any external parts other than C_{REG} or any load must not connect to the VREG pin.

14. Spread spectrum clock generation function

This IC has a built-in spread spectrum clock generation circuit to reduce conductive noise and emission noise. The spread spectrum clock generation circuit spreads the operating frequency range across a wide bandwidth during PWM operation to suppress noise peaks for specific frequency ranges. This IC uses the oscillation frequency (f_{OSC}) as a lower limit and turns the frequency to a triangular wave shape using an oscillation frequency modulation rate (F_{SSS}) = +6% typ. range. The modulation period is 320 / f_{OSC} sec typ.

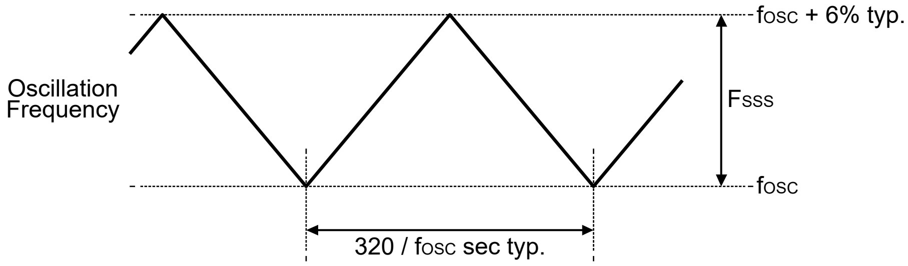
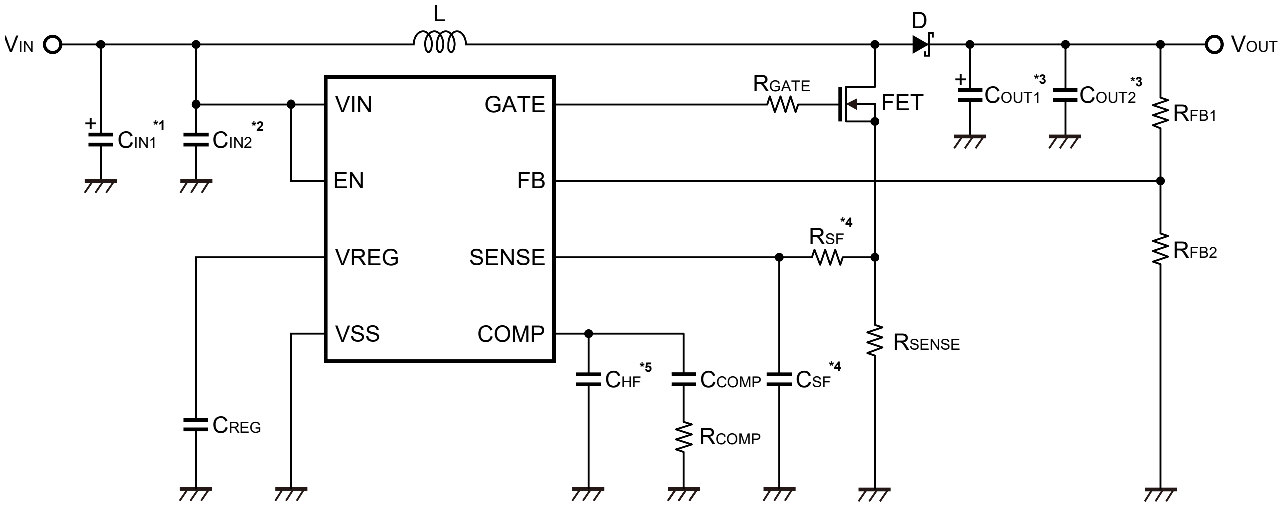


Figure 12

■ Typical Circuits

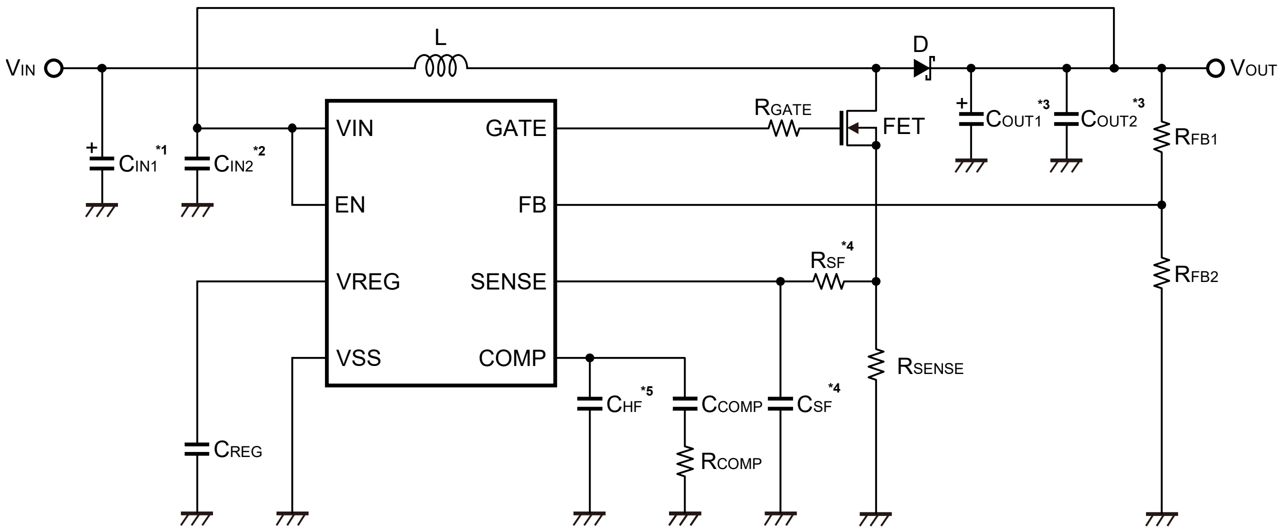
1. Step-up controller configuration



***1.** C_{IN1} is a capacitor for stabilizing the input. If operation is unstable, add a capacitor in parallel.
***2.** C_{IN2} is a bypass capacitor for stabilizing the IC operation. Connect it to the area nearest the VIN pin.
***3.** C_{OUT1} and C_{OUT2} are capacitors for stabilizing the output. If operation is unstable, add a capacitor in parallel.
***4.** R_{SF} and C_{SF} are RC filters to prevent FET switching noise from propagating to the SENSE pin.
***5.** C_{HF} is a high-frequency noise blocking capacitor to prevent malfunctions caused by switching noise.

Figure 13

2. Bootstrap configuration



***1.** C_{IN1} is a capacitor for stabilizing the input. If operation is unstable, add a capacitor in parallel.
***2.** C_{IN2} is a bypass capacitor for stabilizing the IC operation. Connect it to the area nearest the VIN pin.
***3.** C_{OUT1} and C_{OUT2} are capacitors for stabilizing the output. If operation is unstable, add a capacitor in parallel.
***4.** R_{SF} and C_{SF} are RC filters to prevent FET switching noise from propagating to the SENSE pin.
***5.** C_{HF} is a high-frequency noise blocking capacitor to prevent malfunctions caused by switching noise.

Figure 14

■ External Parts Selection

Figure 13 shows a typical circuit based on our evaluation. **Table 10** shows its operating conditions and **Table 11** shows its external component constants.
If the input voltage (V_{IN}) is lower than the VREG pin output voltage (V_{REG}), a bootstrap configuration (**Figure 14**) is recommended. Such a configuration will maintain V_{REG} at 5 V and reduce FET ON-resistance. Also, at a frequency of 2.2 MHz, the FET losses will increase, and the FET may be damaged. Measure FET surface temperature during standard circuit operation to ensure that there is a margin for the maximum junction temperature rating.

Table 10 Design Example

Design Parameter	Value
Input voltage (V_{IN})	6 V
Output voltage (V_{OUT})	12 V
Load current (I_{LOAD})	2 A
Oscillation frequency (f_{OSC})	2.2 MHz

Table 11 Constants for External Components

Symbol	Value	Quantity	Part Number	Manufacturer
L	0.47 μH	1	SPM5030VT-R47M-D	TDK Corporation
FET	−	1	IPC50N04S5L-5R5	Infineon Technologies
D	−	1	PMEG045V100EPD	Nexperia B.V.
C_{IN1}	33 μF	2	GYC1H330MCQ1GS	NICHICON CORPORATION
C_{IN2}	0.1 μF	1	CGA4J2X8R1H104K	TDK Corporation
C_{OUT1}	100 μF	3	GYC1H101MCQ1GS	NICHICON CORPORATION
C_{OUT2}	10 μF	1	CGA5L1X7R1H106K	TDK Corporation
R_{GATE}	10 Ω	1	MCR3 series (1608)	ROHM CO., LTD.
R_{SENSE}	4 mΩ	1	TLR2BPDTD4L00F75	KOA CORPORATION
R_{SF}	22 Ω	1	MCR3 series (1608)	ROHM CO., LTD.
C_{SF}	10 nF	1	CGA3E2X8R1H103K	TDK Corporation
C_{REG}	1 μF	1	CGA5L3X8R1H105K	TDK Corporation
R_{COMP}	12 kΩ	1	MCR3 series (1608)	ROHM CO., LTD.
C_{COMP}	4.7 nF	1	CGA3E2X8R1H472K	TDK Corporation
C_{HF}	220 pF	1	CGA3E2NP01H221J	TDK Corporation
R_{FB1}	200 kΩ + 24 kΩ	1	MCR3 series (1608)	ROHM CO., LTD.
R_{FB2}	16 kΩ	1	MCR3 series (1608)	ROHM CO., LTD.

Caution The connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Board Layout Guidelines

Note the following cautions when determining the board layout for this IC.

- Place C_{IN} (C10) as close to the VIN pin and the VSS pin as possible. Prioritize the layout of C_{IN}.
- Place C_{REG} (C11) as close to the VREG pin and the VSS pin as possible.
- Make the wiring of the FB pin as short as possible. Do not place it near a noise source.
- Make the switching loop composed of C_{OUT} (C13 to C19) → D → FET → R_{SENSE} → C_{OUT} (C13 to C19) as small as possible. This measure effectively reduces inductive high-frequency noise.
- The switching node (SW1) wiring area (Dashed line area in "**Figure 15 Reference Board Pattern**") should be as small as possible to reduce high-frequency radiation noise.
- Place R_{SENSE} close to the FET source.

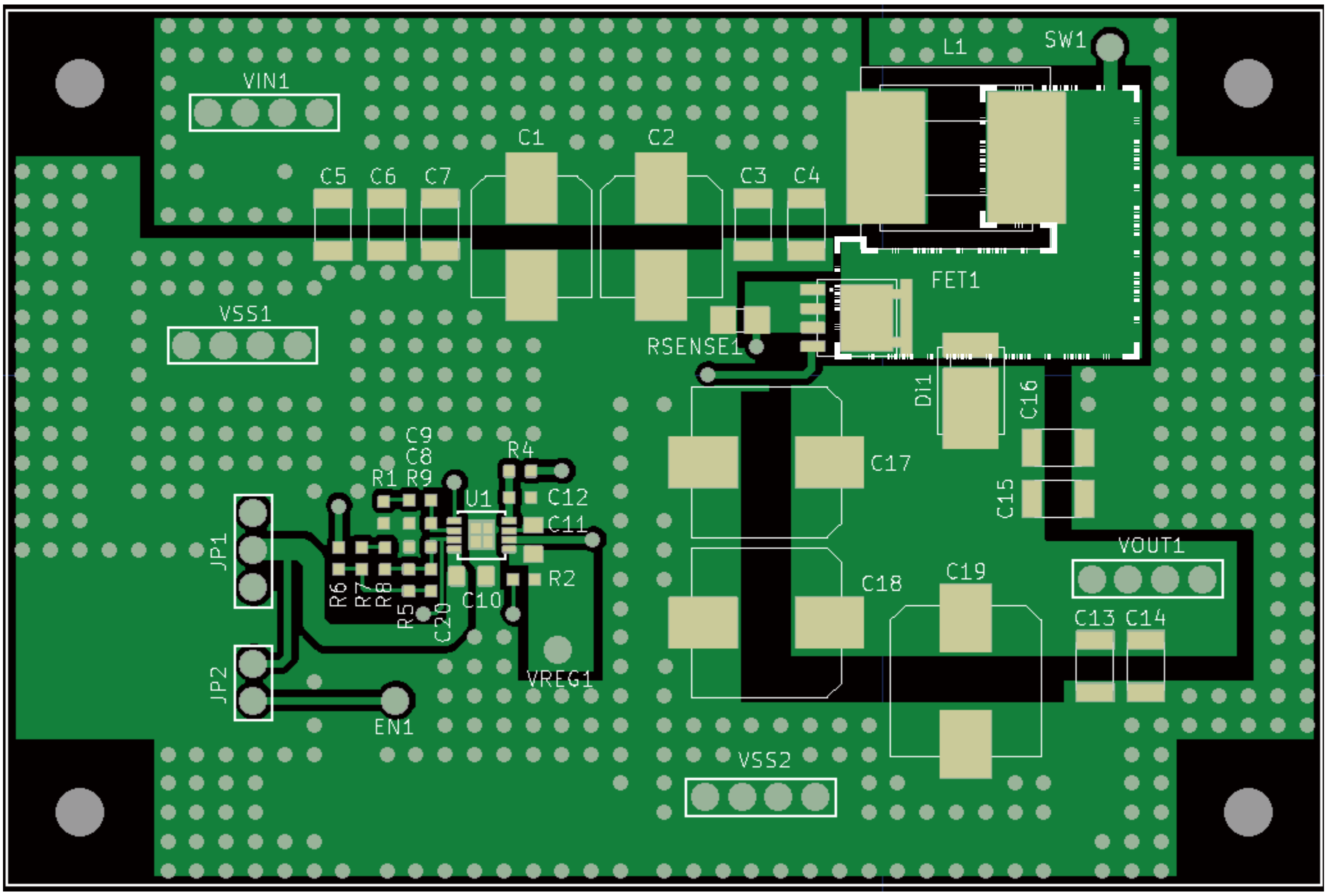


Figure 15 Reference Board Pattern

Caution The above pattern diagram does not guarantee successful operation. Perform thorough evaluation using the actual application to determine the pattern.

■ Related Source

Refer to the following application note for external parts selection and board layout for this IC.

S-19980/19990 Series EXTERNAL PARTS SELECTION Application Note

Refer to the following application note for flyback converter circuit using this IC.

S-19980/19990 Series FLYBACK CONVERTER CIRCUIT Application Note

■ Precautions

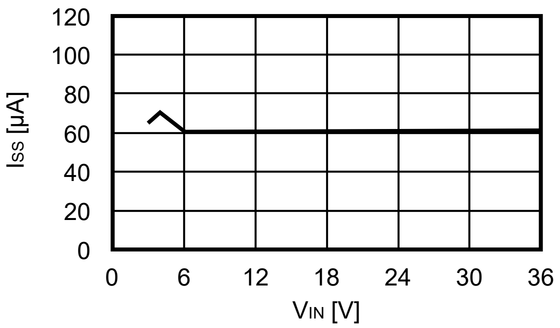
- Mount external capacitors and inductors as close as possible to the IC, and make single GND.
- Characteristic ripple voltage and spike noise occur in the IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply to be used, fully check them using an actually mounted model.
- The 0.1 μF capacitor (C_{IN2} in **Figure 13, Figure 14**) connected between the VIN pin and the VSS pin is a bypass capacitor. It stabilizes the power supply in the IC, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- ABLIC Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does ABLIC Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

■ Characteristics (Typical Data)

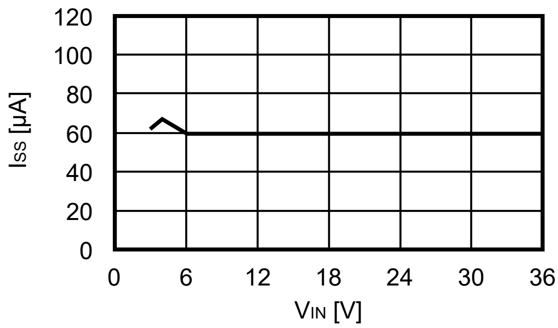
1. Example of major power supply dependence characteristics (Ta = +25°C)

1. 1 Current consumption during switching off (I_{SS}) vs. Input voltage (V_{IN})

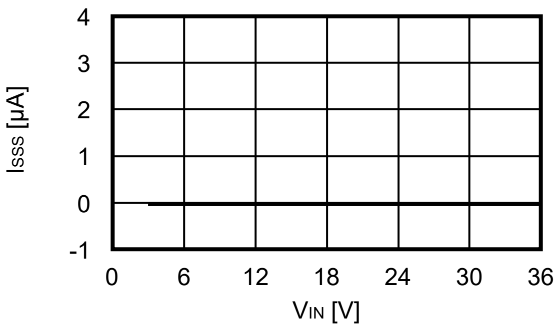
1. 1. 1 S-19990 Series A / B type



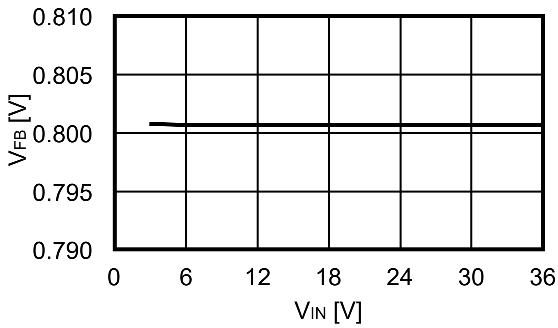
1. 1. 2 S-19990 Series C / D type



1. 2 Current consumption during shutdown (I_{SSS}) vs. Input voltage (V_{IN})

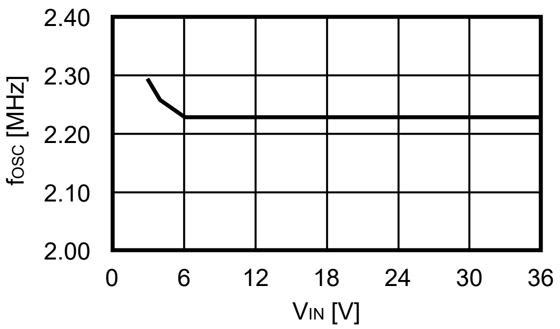


1. 3 FB pin voltage (V_{FB}) vs. Input voltage (V_{IN})

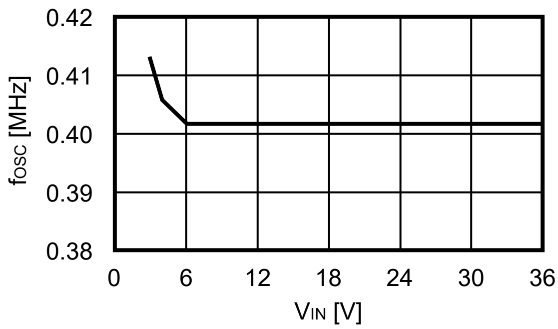


1. 4 Oscillation frequency (f_{OSC}) vs. Input voltage (V_{IN})

1. 4. 1 S-19990 Series A / B type

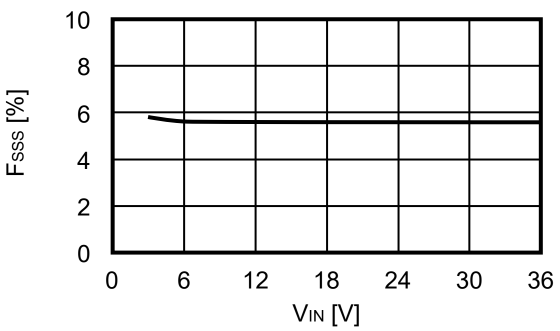


1. 4. 2 S-19990 Series C / D type

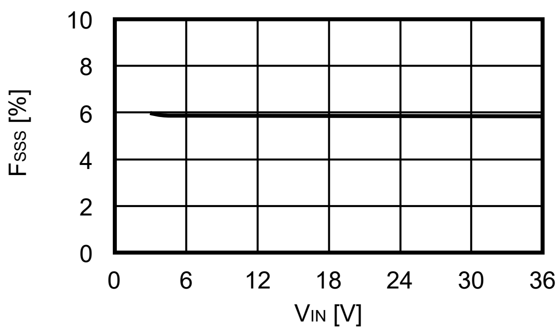


1. 5 Oscillation frequency modulation rate (F_{SSS}) vs. Input voltage (V_{IN})

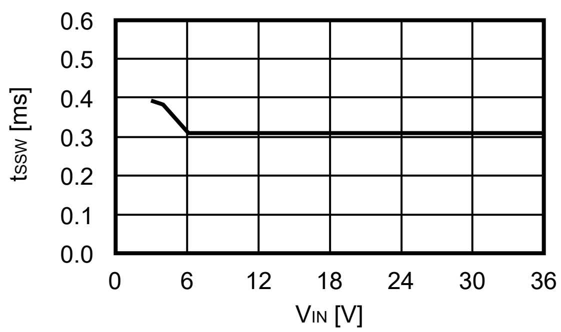
1. 5. 1 S-19990 Series A / B type



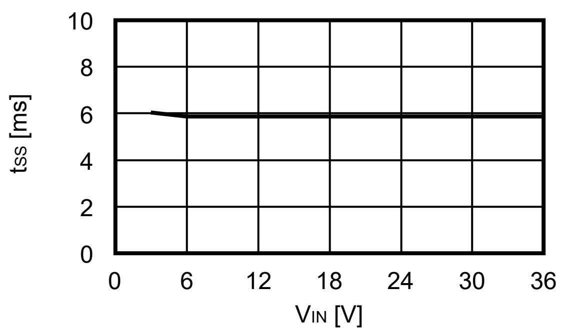
1. 5. 2 S-19990 Series C / D type



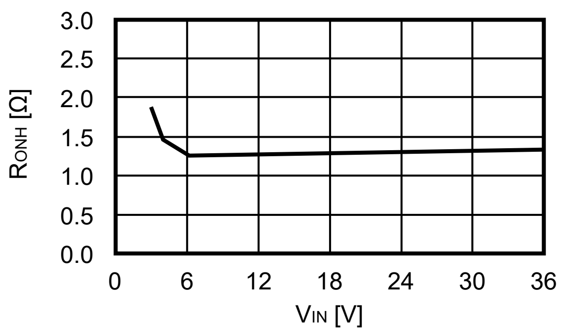
1. 6 Soft-start wait time (t_{SSW}) vs. Input voltage (V_{IN})



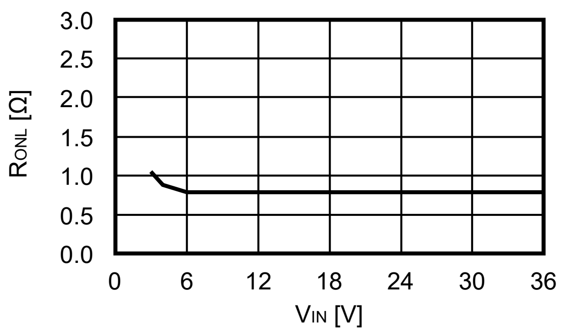
1. 7 Soft-start time (t_{SS}) vs. Input voltage (V_{IN})



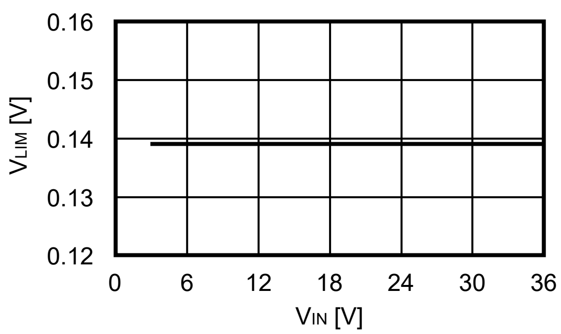
1. 8 GATE pin ON-resistance (R_{ONH}) vs. Input voltage (V_{IN})



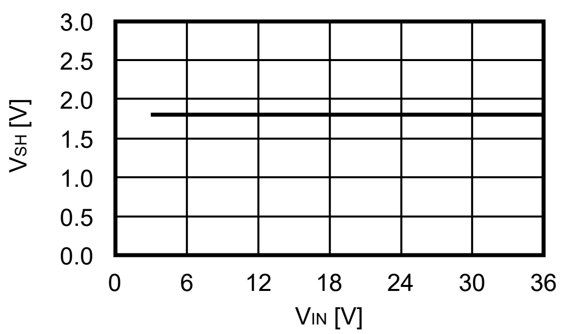
1. 9 GATE pin ON-resistance (R_{ONL}) vs. Input voltage (V_{IN})



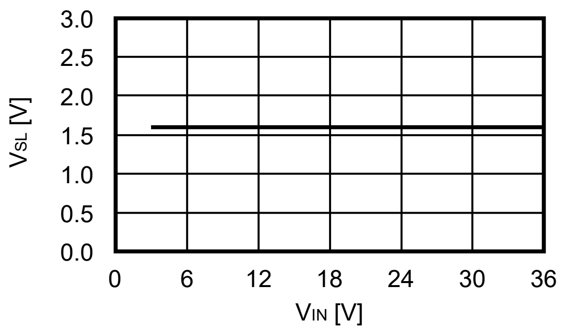
1. 10 Overcurrent protection detection voltage (V_{LIM}) vs. Input voltage (V_{IN})



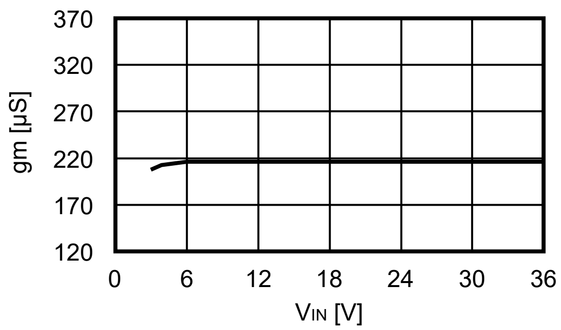
1. 11 High level input voltage (V_{SH}) vs. Input voltage (V_{IN})



1. 12 Low level input voltage (V_{SL}) vs. Input voltage (V_{IN})



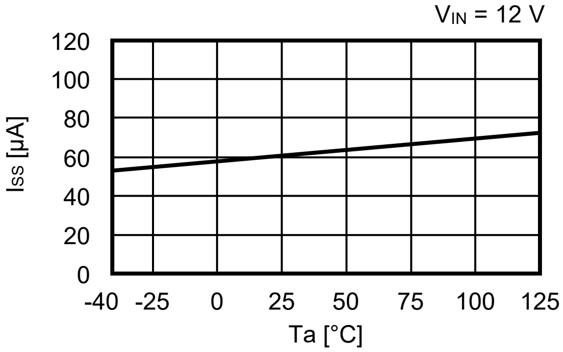
1. 13 Error amplifier transconductance (gm) vs. Input voltage (V_{IN})



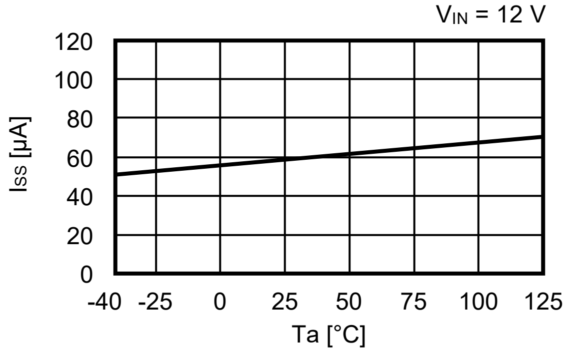
2. Example of major temperature characteristics (Ta = −40°C to +125°C)

2. 1 Current consumption during switching off (I_{SS}) vs. Temperature (Ta)

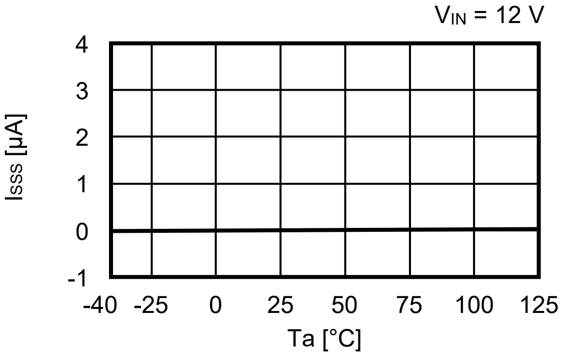
2. 1. 1 S-19990 Series A / B type



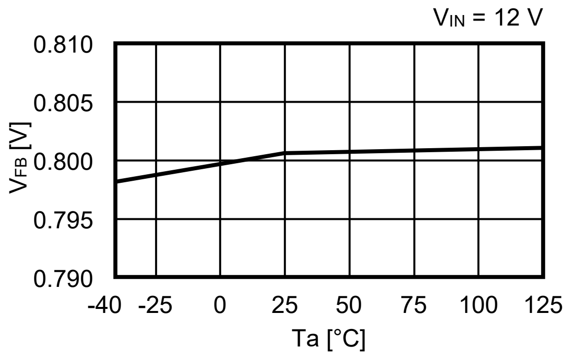
2. 1. 2 S-19990 Series C / D type



2. 2 Current consumption during shutdown (I_{SSS}) vs. Temperature (Ta)

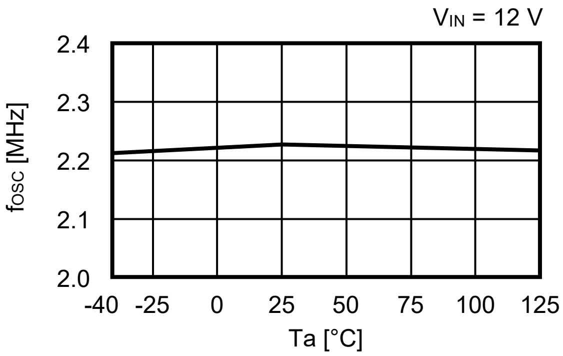


2. 3 FB pin voltage (V_{FB}) vs. Temperature (Ta)

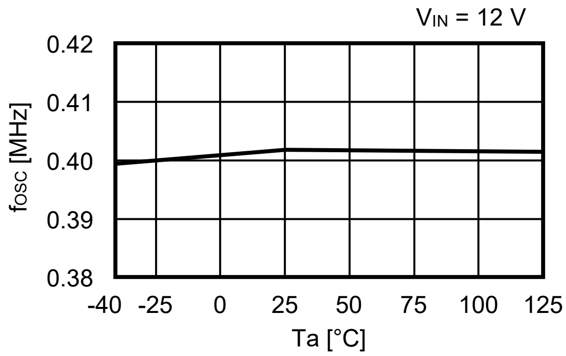


2. 4 Oscillation frequency (f_{OSC}) vs. Temperature (Ta)

2. 4. 1 S-19990 Series A / B type

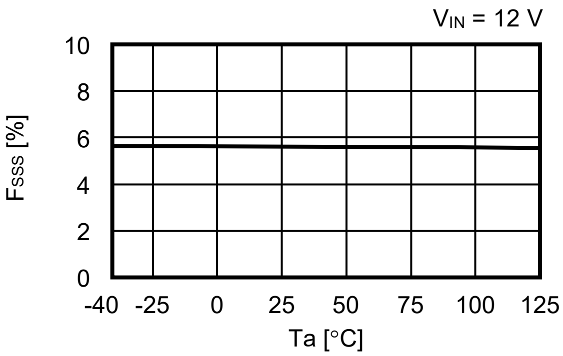


2. 4. 2 S-19990 Series C / D type

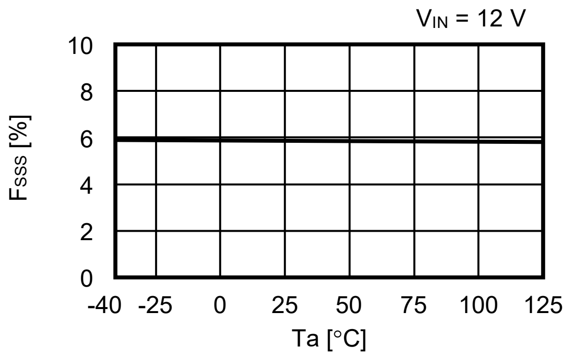


2. 5 Oscillation frequency modulation rate (F_{SSS}) vs. Temperature (Ta)

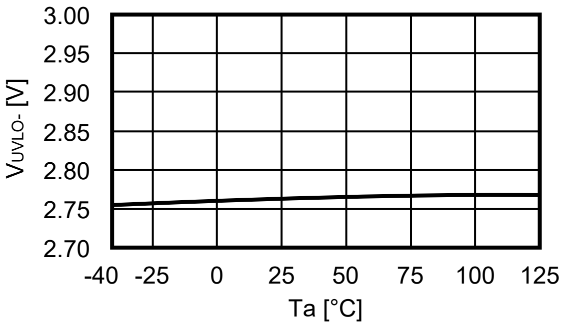
2. 5. 1 S-19990 Series A / B type



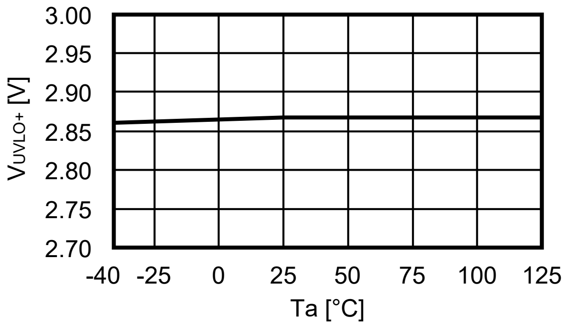
2. 5. 2 S-19990 Series C / D type



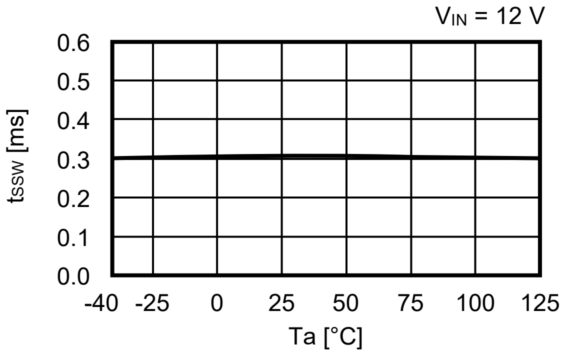
2. 6 UVLO detection voltage (V_{UVLO-}) vs. Temperature (Ta)



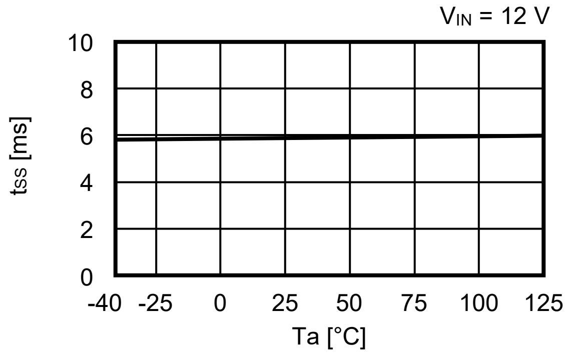
2. 7 UVLO release voltage (V_{UVLO+}) vs. Temperature (Ta)



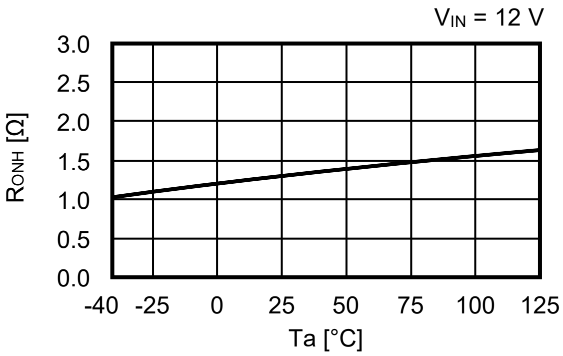
2. 8 Soft-start wait time (t_{SSW}) vs. Temperature (Ta)



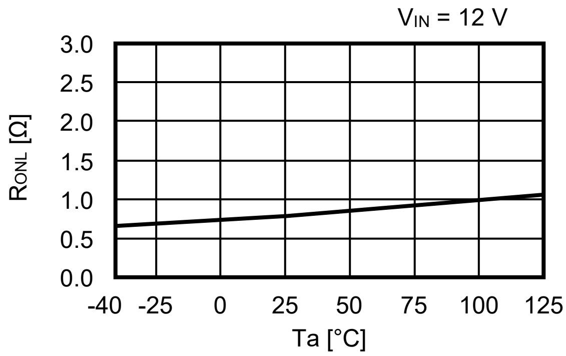
2. 9 Soft-start time (t_{SS}) vs. Temperature (Ta)



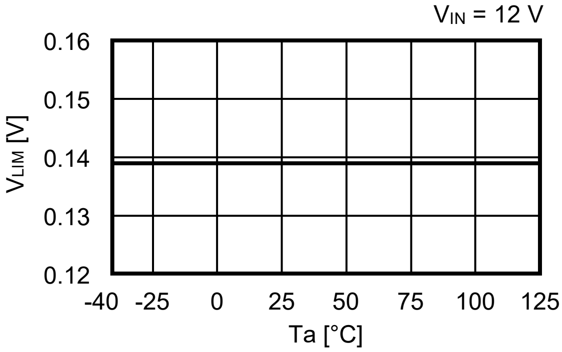
2. 10 GATE pin ON-resistance (R_{ONH}) vs. Temperature (Ta)



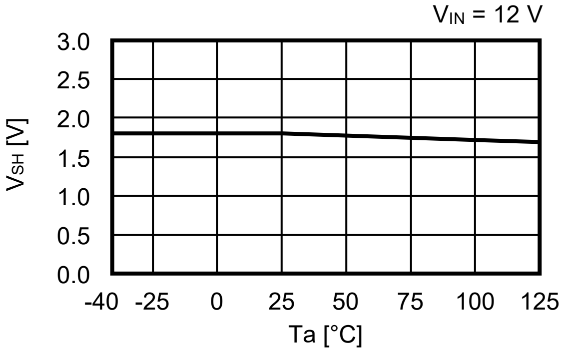
2. 11 GATE pin ON-resistance (R_{ONL}) vs. Temperature (Ta)



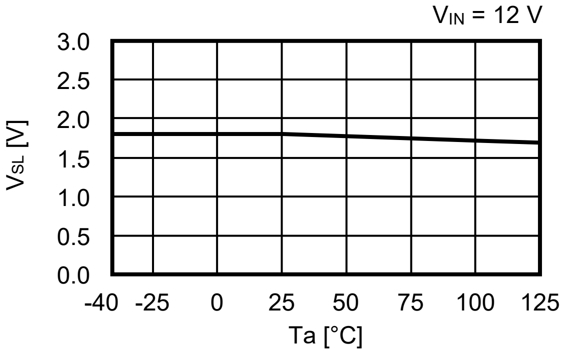
2. 12 Overcurrent protection detection voltage (V_{LIM}) vs. Temperature (Ta)



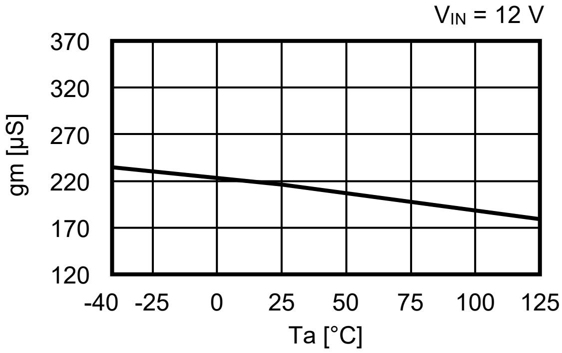
2. 13 High level input voltage (V_{SH}) vs. Temperature (Ta)



2. 14 Low level input voltage (V_{SL}) vs. Temperature (Ta)

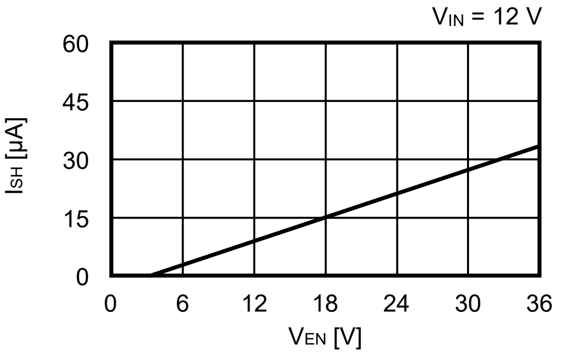


2. 15 Error amplifier transconductance (gm) vs. Temperature (Ta)



3. EN pin characteristics (Ta = +25°C)

3. 1 High level input current (I_{SH}) vs. EN pin voltage (V_{EN})



4. Transient response characteristics

The external parts shown in **Table 12** are used in "**4. Transient response characteristics**".

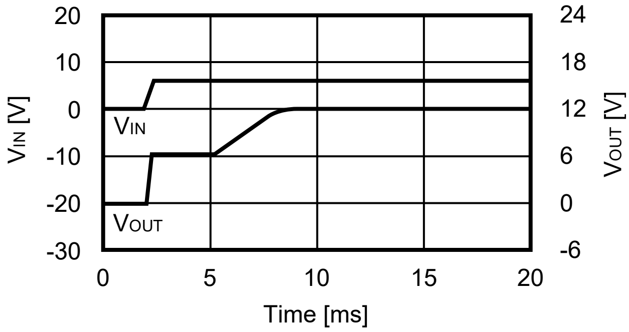
Table 12

Symbol	Value	Part Number	Manufacturer
L	A / B type: 0.47 μH	SPM5030VT-R47M-D	TDK Corporation
	C / D type: 1.5 μH	SPM12565VT-1R5M-D	TDK Corporation
FET	–	IPC50N04S5L-5R5	Infineon Technologies
D	–	PMEG045V100EPD	Nexperia B.V.
C_{IN1}	33 μF	GYC1H330MCQ1GS	NICHICON CORPORATION
C_{IN2}	0.1 μF	CGA4J2X8R1H104K	TDK Corporation
C_{OUT1}	100 μF	GYC1H101MCQ1GS	NICHICON CORPORATION
C_{OUT2}	10 μF	CGA5L1X7R1C106K	TDK Corporation

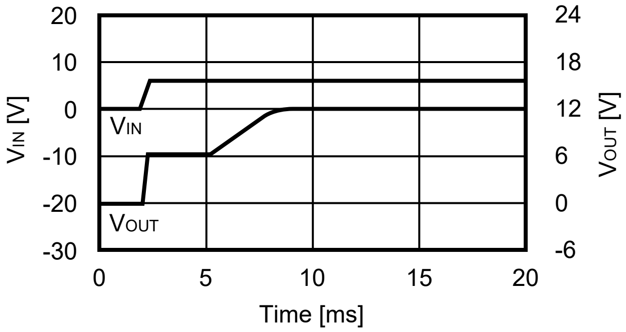
4. 1 Power-on (V_{OUT} = 12 V, V_{IN} = V_{EN} = 0 V → 6 V, Ta = +25°C)

4. 1. 1 S-19990 Series A / B type

(1) I_{OUT} = 1 mA

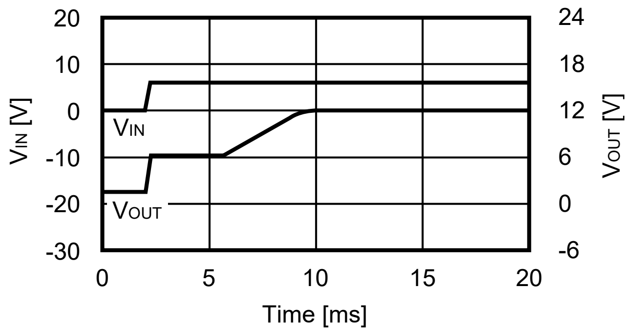


(2) I_{OUT} = 1 A

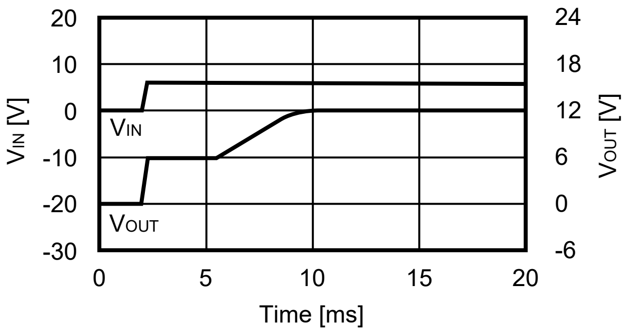


4. 1. 2 S-19990 Series C / D type

(1) I_{OUT} = 1 mA



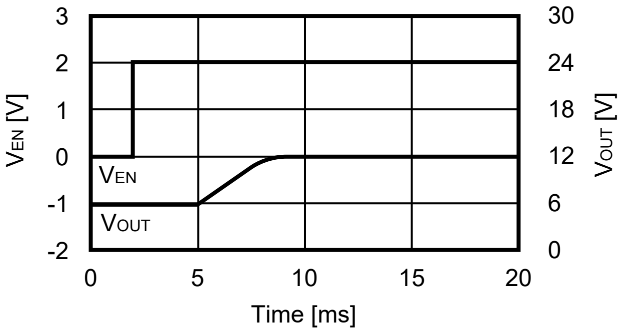
(2) I_{OUT} = 1 A



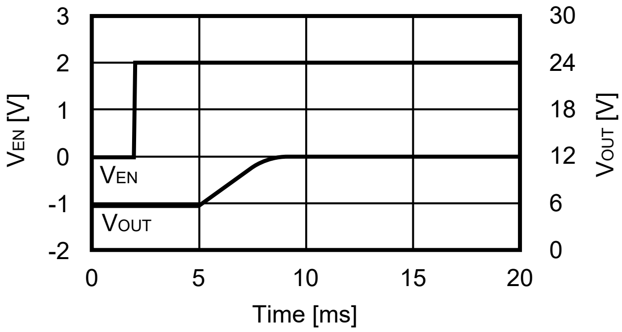
4. 2 Transient response characteristics of EN pin (V_{OUT} = 12 V, V_{IN} = 6 V, V_{EN} = 0 V → 2.0 V, Ta = +25°C)

4. 2. 1 S-19990 Series A / B type

(1) I_{OUT} = 1 mA

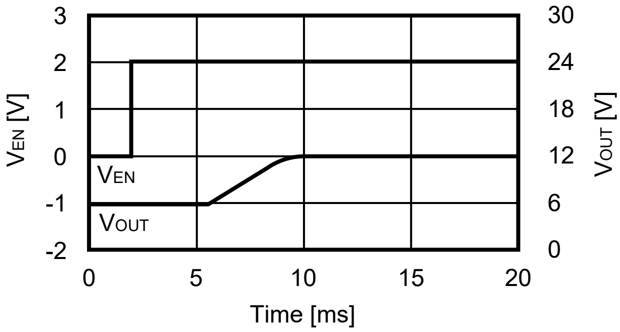


(2) I_{OUT} = 1 A

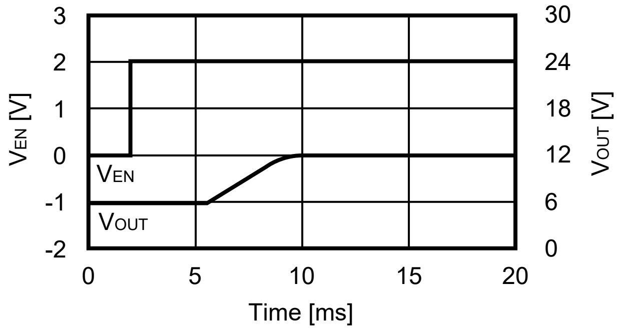


4. 2. 2 S-19990 Series C / D type

(1) I_{OUT} = 1 mA



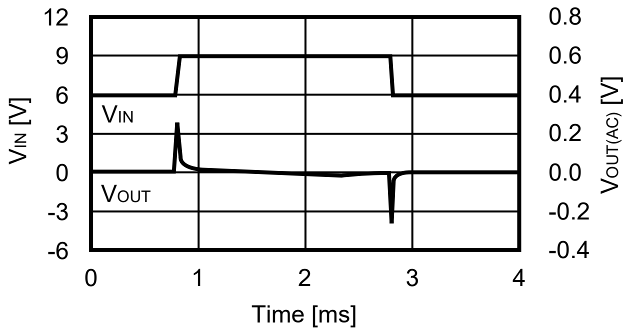
(2) I_{OUT} = 1 A



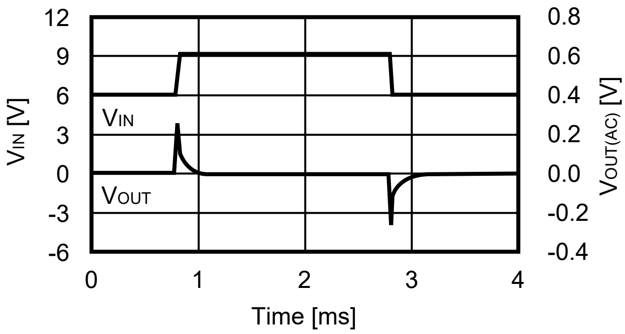
4. 3 Line transient response (V_{OUT} = 12 V, V_{IN} = 6 V → 9 V → 6 V, Ta = +25°C)

4. 3. 1 S-19990 Series A / B type

(1) I_{OUT} = 1 mA

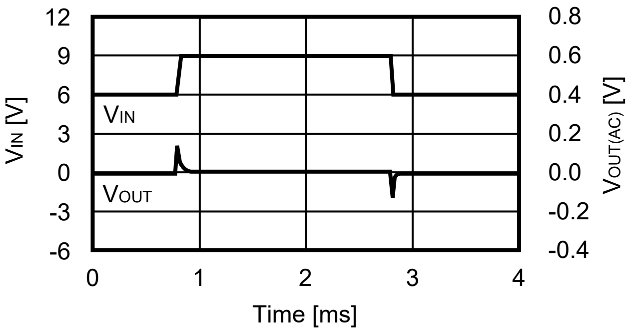


(2) I_{OUT} = 500 mA

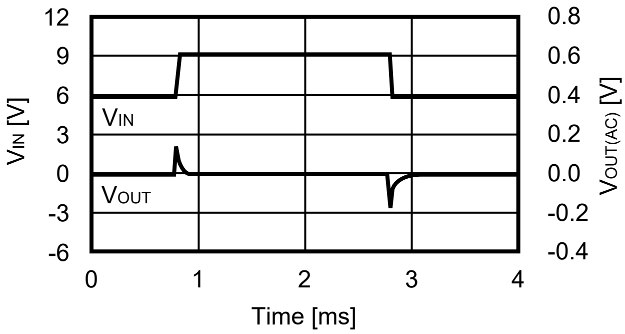


4. 3. 2 S-19990 Series C / D type

(1) I_{OUT} = 1 mA



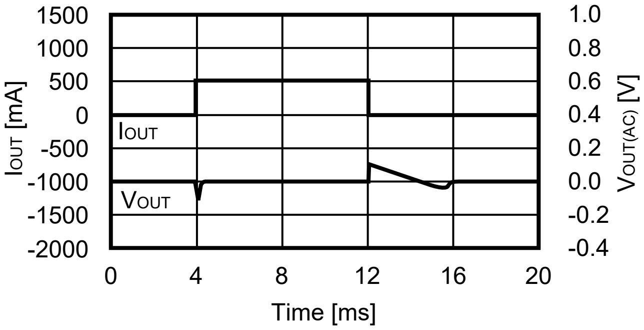
(2) I_{OUT} = 500 mA



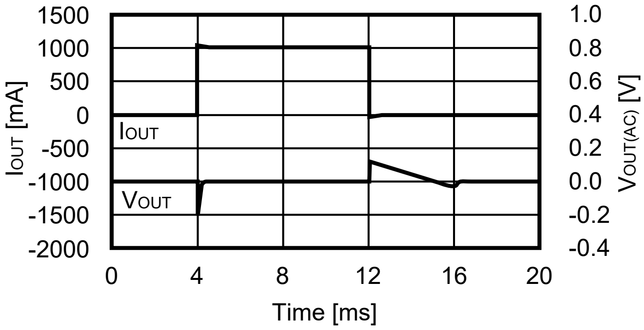
4. 4 Load transient response (V_{OUT} = 12 V, V_{IN} = 6 V, Ta = +25°C)

4. 4. 1 S-19990 Series A / B type

(1) I_{OUT} = 10 mA → 500 mA → 10 mA

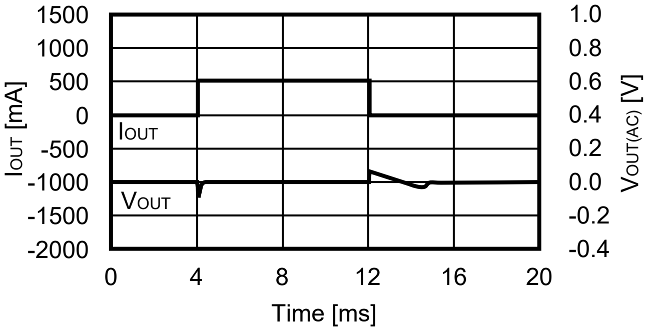


(2) I_{OUT} = 10 mA → 1000 mA → 10 mA

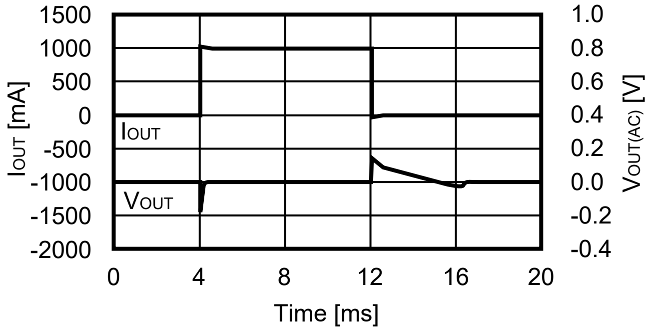


4. 4. 2 S-19990 Series C / D type

(1) I_{OUT} = 10 mA → 500 mA → 10 mA



(2) I_{OUT} = 10 mA → 1000 mA → 10 mA



■ Reference Data

The external parts shown in **Table 13** are used in "**■ Reference Data**".

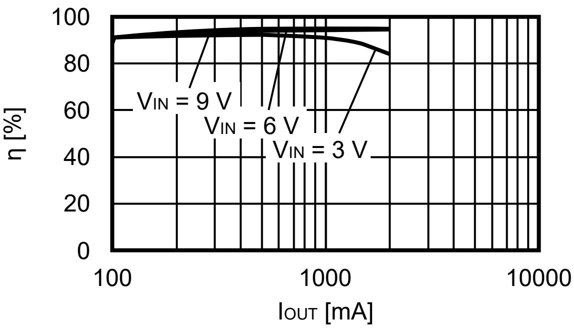
Table 13

Condition	Symbol	Value	Quantity	Part Number	Manufacturer
<1>	L	1.5 μH	1	SPM12565VT-1R5M-D	TDK Corporation
	FET	−	1	IPC50N04S5L-5R5	Infineon Technologies
	D	−	1	PMEG045V100EPD	Nexperia B.V.
	C_{IN}	0.1 μF	1	CGA4J2X8R1H104K	TDK Corporation
		33 μF	2	GYC1H330MCQ1GS	NICHICON CORPORATION
	C_{OUT}	10 μF	2	CGA5L1X7R1C106K	TDK Corporation
		100 μF	3	GYC1H101MCQ1GS	NICHICON CORPORATION
<2>	L	0.47 μH	1	SPM5030VT-R47M-D	TDK Corporation
	FET	−	1	IPC50N04S5L-5R5	Infineon Technologies
	D	−	1	PMEG045V100EPD	Nexperia B.V.
	C_{IN}	0.1 μF	1	CGA4J2X8R1H104K	TDK Corporation
		33 μF	2	GYC1H330MCQ1GS	NICHICON CORPORATION
	C_{OUT}	10 μF	2	CGA5L1X7R1C106K	TDK Corporation
		100 μF	3	GYC1H101MCQ1GS	NICHICON CORPORATION

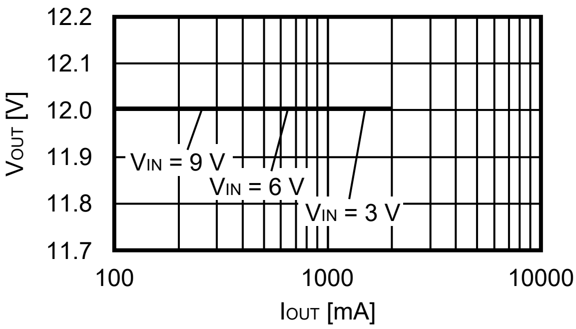
1. V_{OUT} = 12 V (External parts: Condition <1>)

1. 1 S-19990 Series C / D type

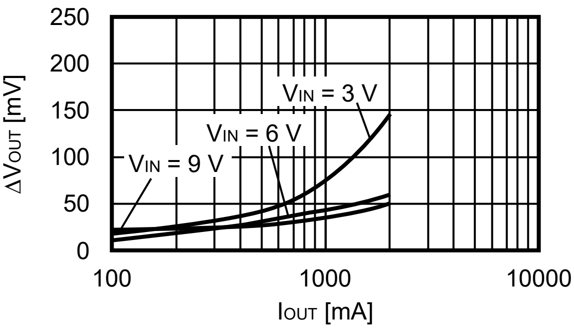
1. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



1. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



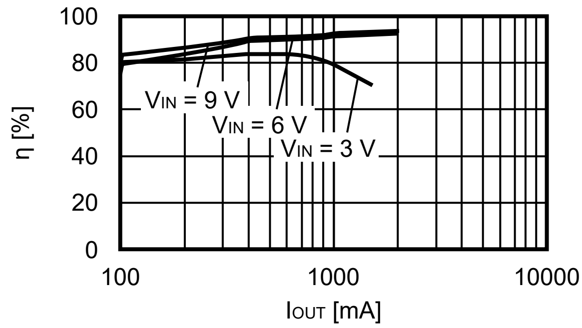
1. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



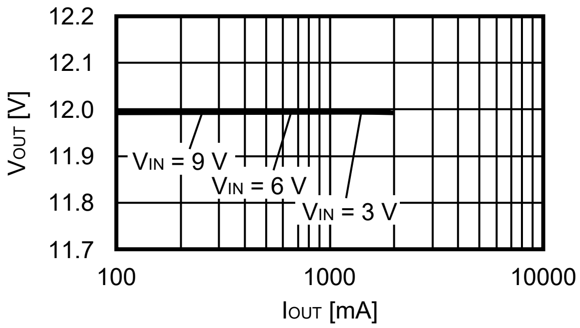
2. V_{OUT} = 12 V (External parts: Condition <2>)

2. 1 S-19990 Series A / B type

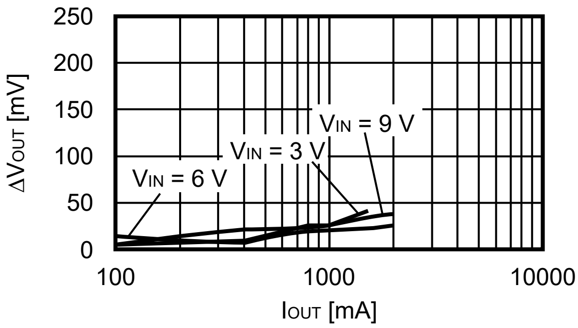
2. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



2. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



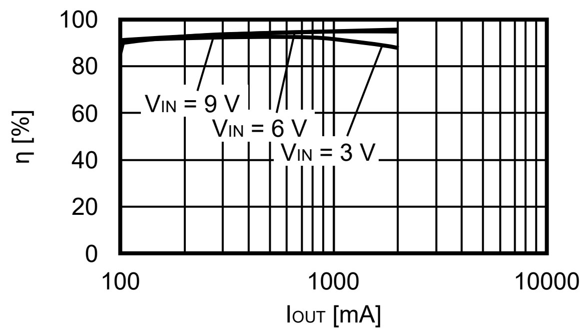
2. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



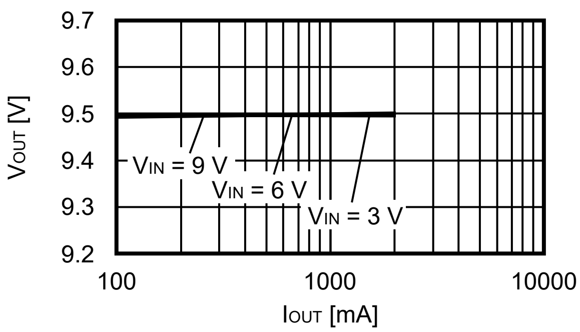
3. V_{OUT} = 9.5 V (External parts: Condition <1>)

3. 1 S-19990 Series C / D type

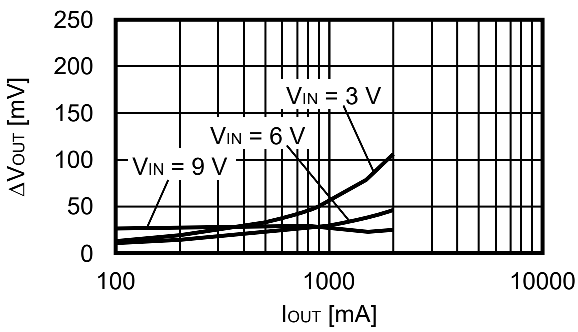
3. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



3. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})



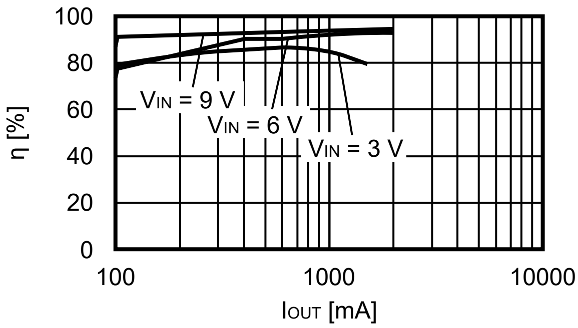
3. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



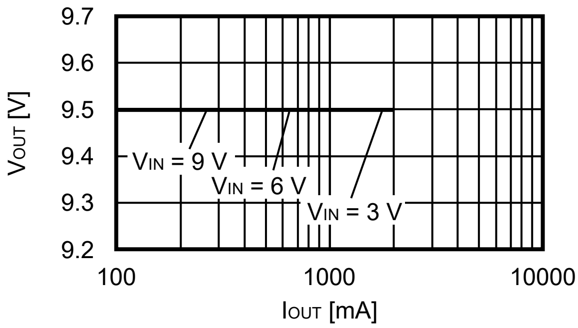
4. V_{OUT} = 9.5 V (External parts: Condition <2>)

4. 1 S-19990 Series A / B type

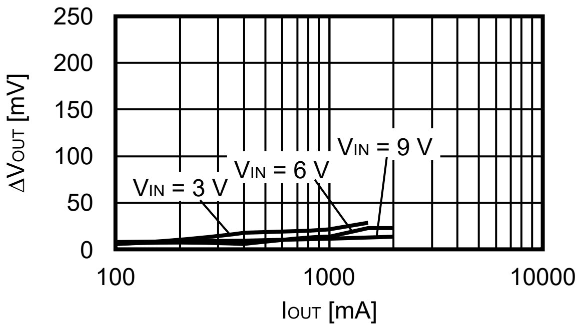
4. 1. 1 Efficiency (η) vs. Output current (I_{OUT})



4. 1. 2 Output voltage (V_{OUT}) vs. Output current (I_{OUT})

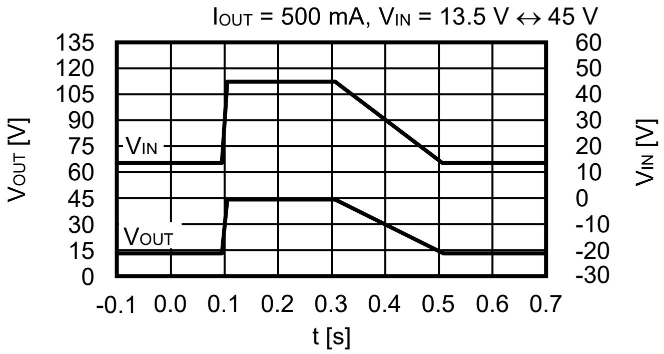


4. 1. 3 Ripple voltage (ΔV_{OUT}) vs. Output current (I_{OUT})



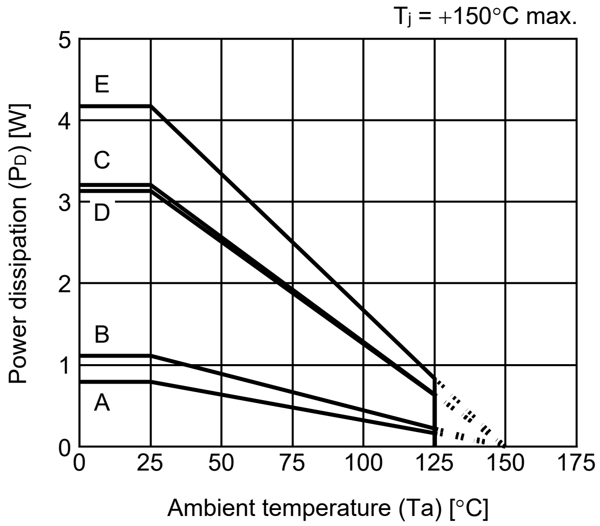
5. Load dump characteristics (Ta = +25°C)

5. 1 V_{OUT} = 12 V



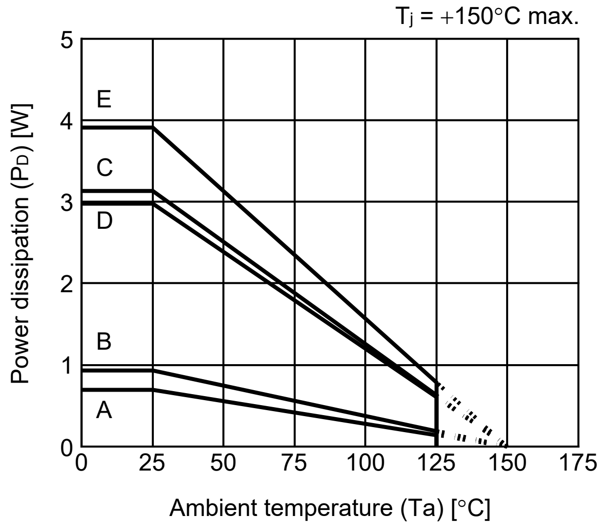
■ Power Dissipation

HTMSOP-8



Board	Power Dissipation (P_D)
A	0.79 W
B	1.11 W
C	3.21 W
D	3.13 W
E	4.17 W

HSNT-8(2030)

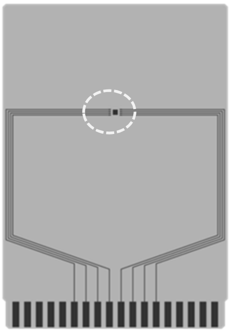


Board	Power Dissipation (P_D)
A	0.69 W
B	0.93 W
C	3.13 W
D	2.98 W
E	3.91 W

HTMSOP-8 Test Board

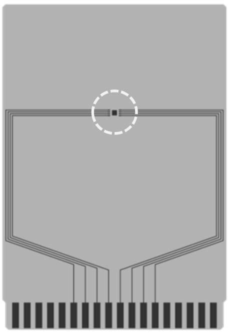
IC Mount Area

(1) Board A



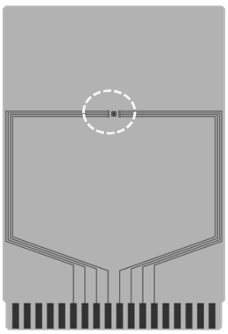
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

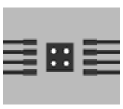


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



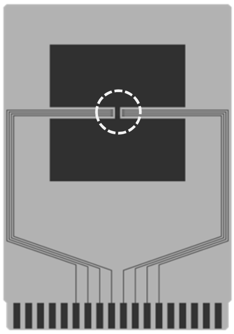
enlarged view

No. HTMSOP8-A-Board-SD-1.0

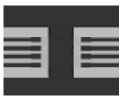
HTMSOP-8 Test Board

IC Mount Area

(4) Board D

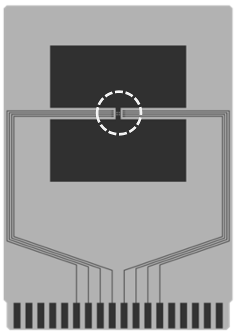


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

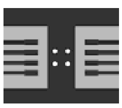


enlarged view

(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

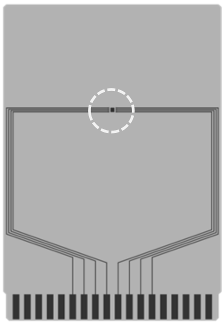


enlarged view

No. HTMSOP8-A-Board-SD-1.0

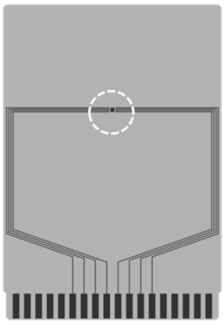
HSNT-8(2030) Test Board

(1) Board A



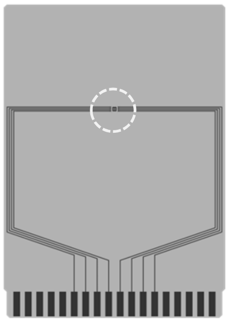
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B

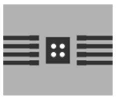


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



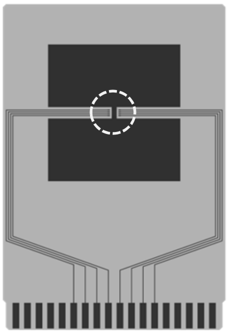
enlarged view

No. HSNT8-A-Board-SD-2.0

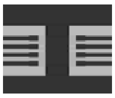
HSNT-8(2030) Test Board

IC Mount Area

(4) Board D

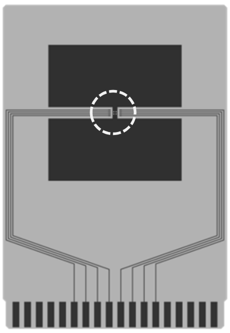


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-



enlarged view

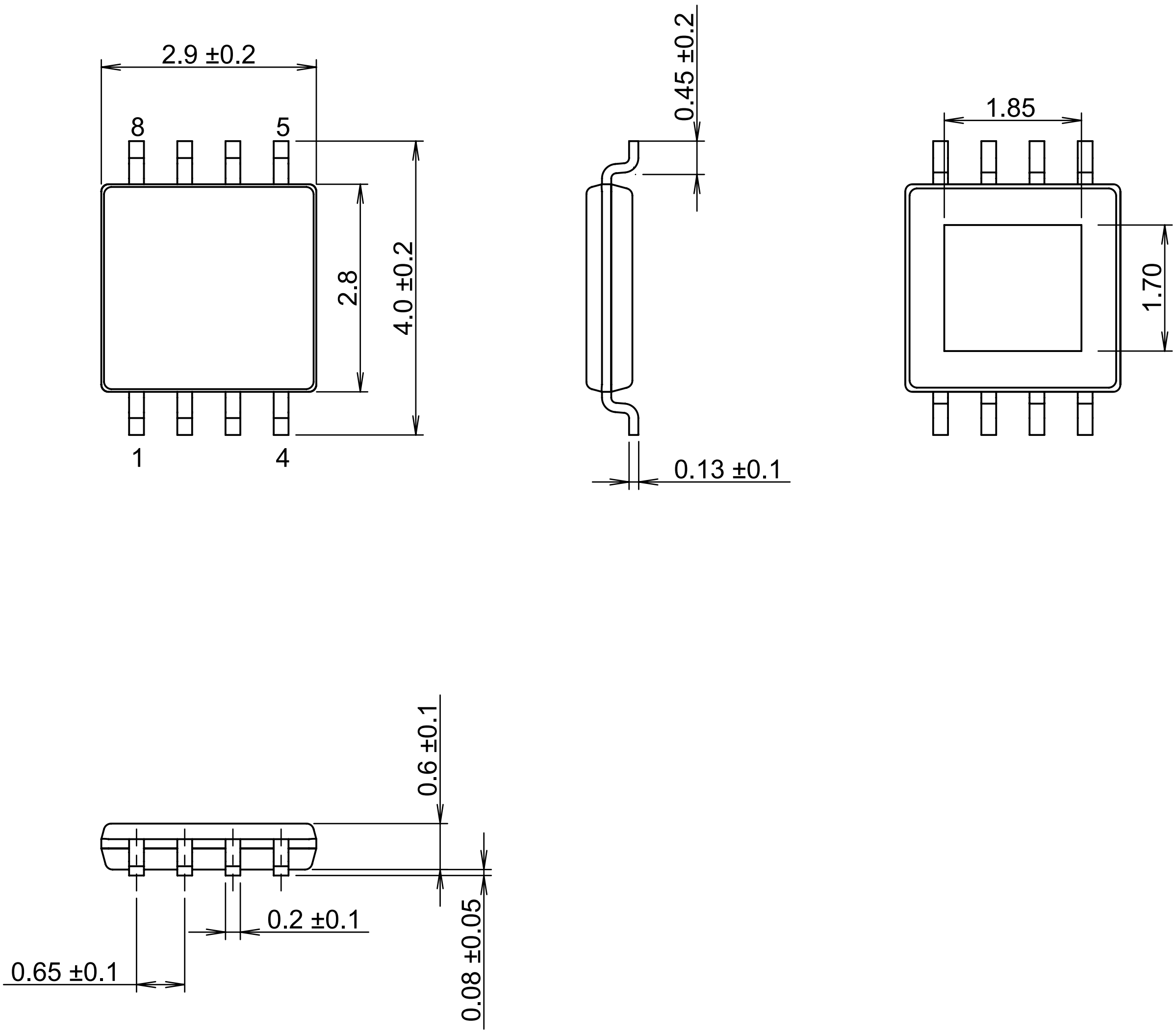
(5) Board E



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

enlarged view

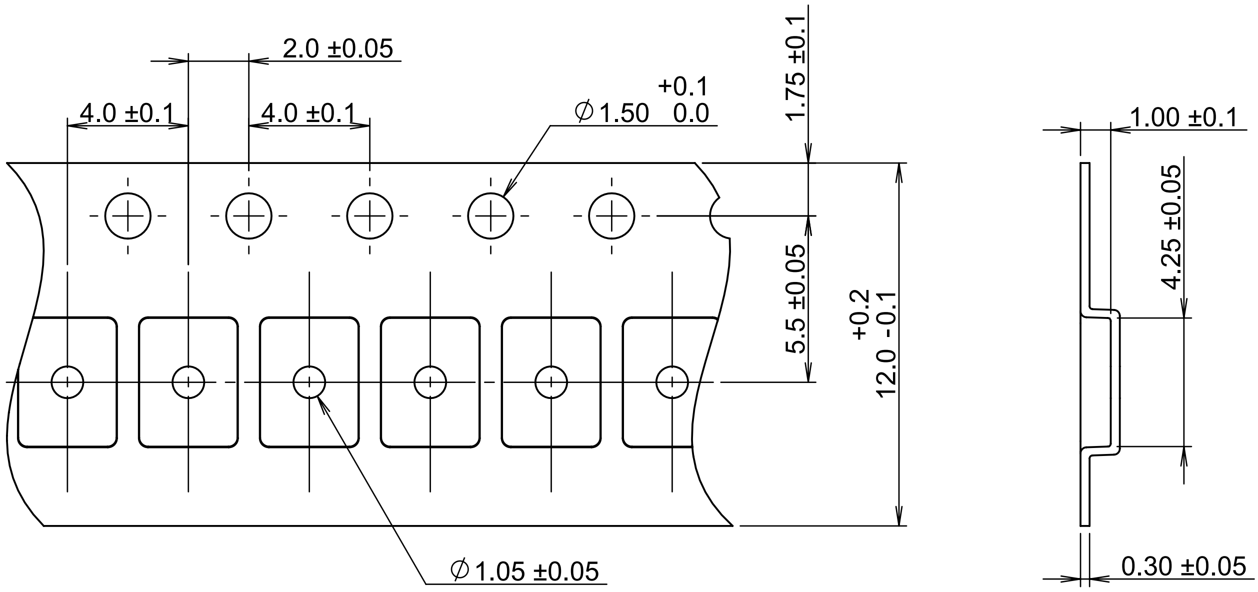
No. HSNT8-A-Board-SD-2.0

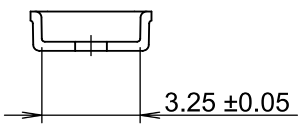


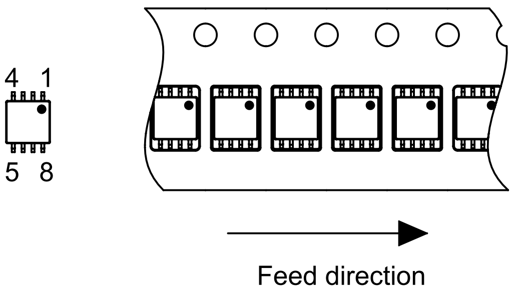
No. FP008-A-P-SD-2.0

TITLE	HTMSOP8-A-PKG Dimensions
No.	FP008-A-P-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



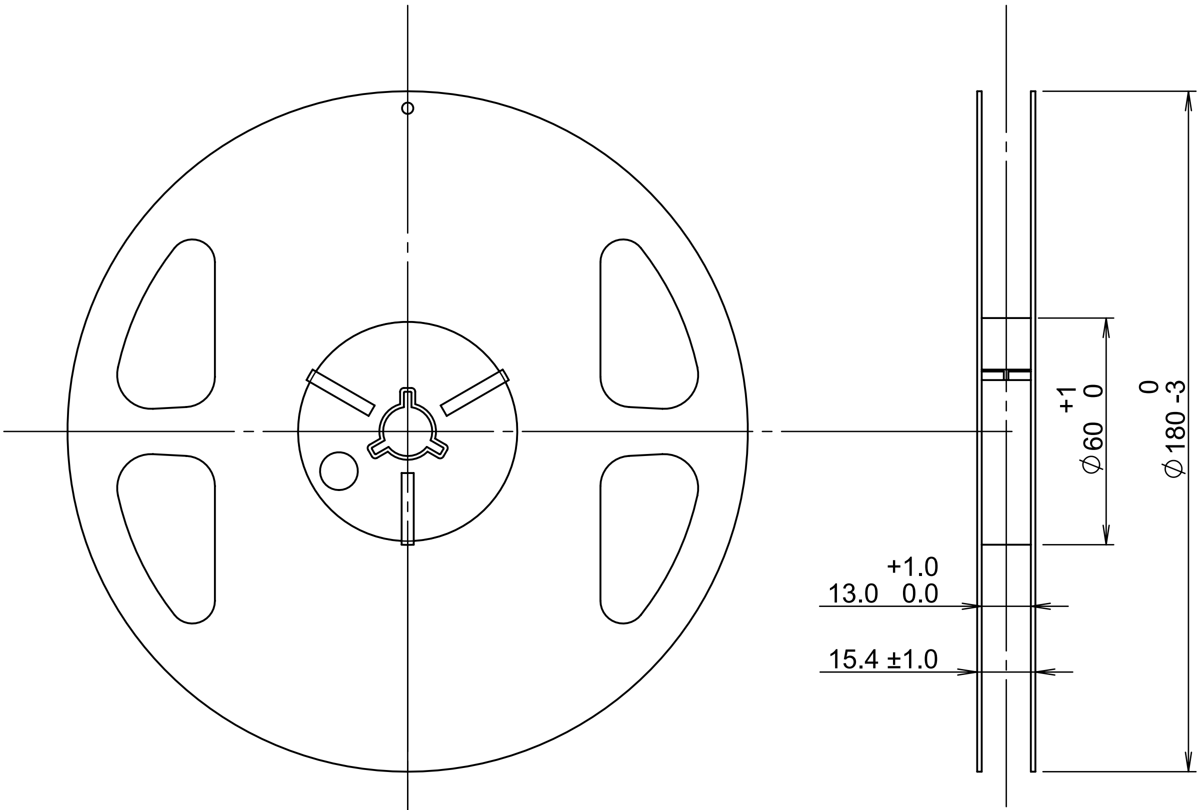




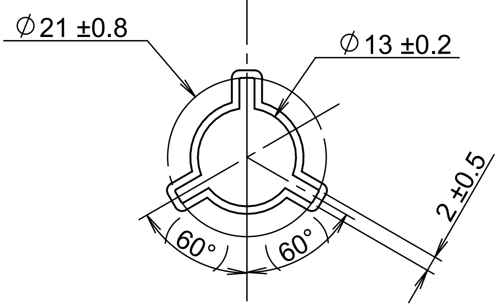
No. FP008-A-C-SD-1.0

TITLE	HTMSOP8-A-Carrier Tape
No.	FP008-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



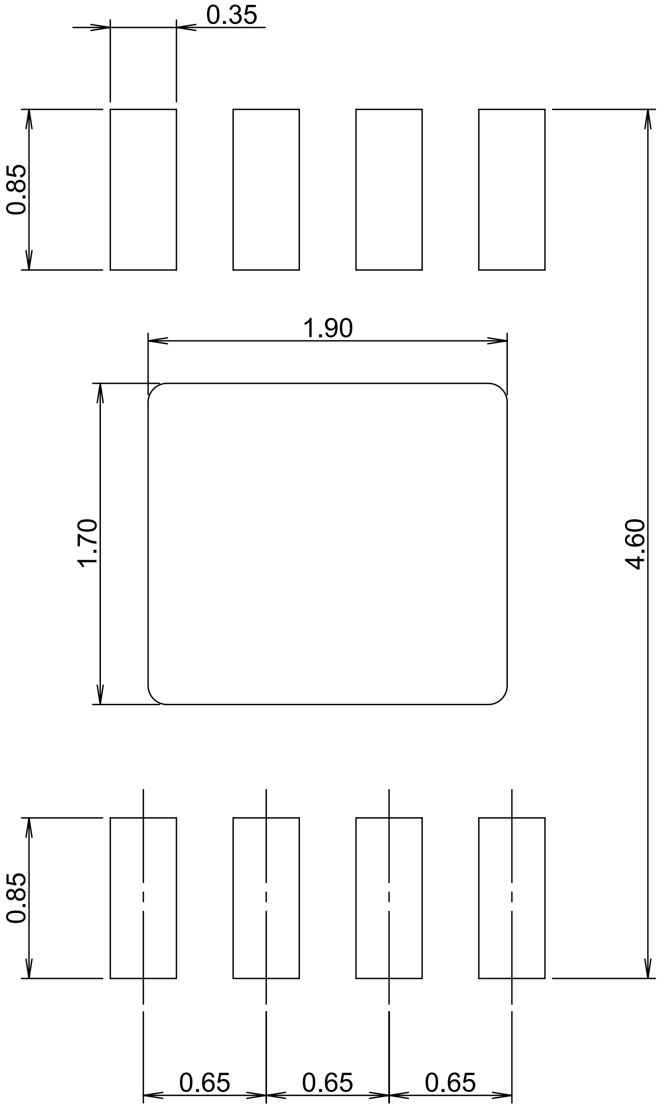
Enlarged drawing in the central part



No. FP008-A-R-SD-2.0

TITLE	HTMSOP8-A-Reel		
No.	FP008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		

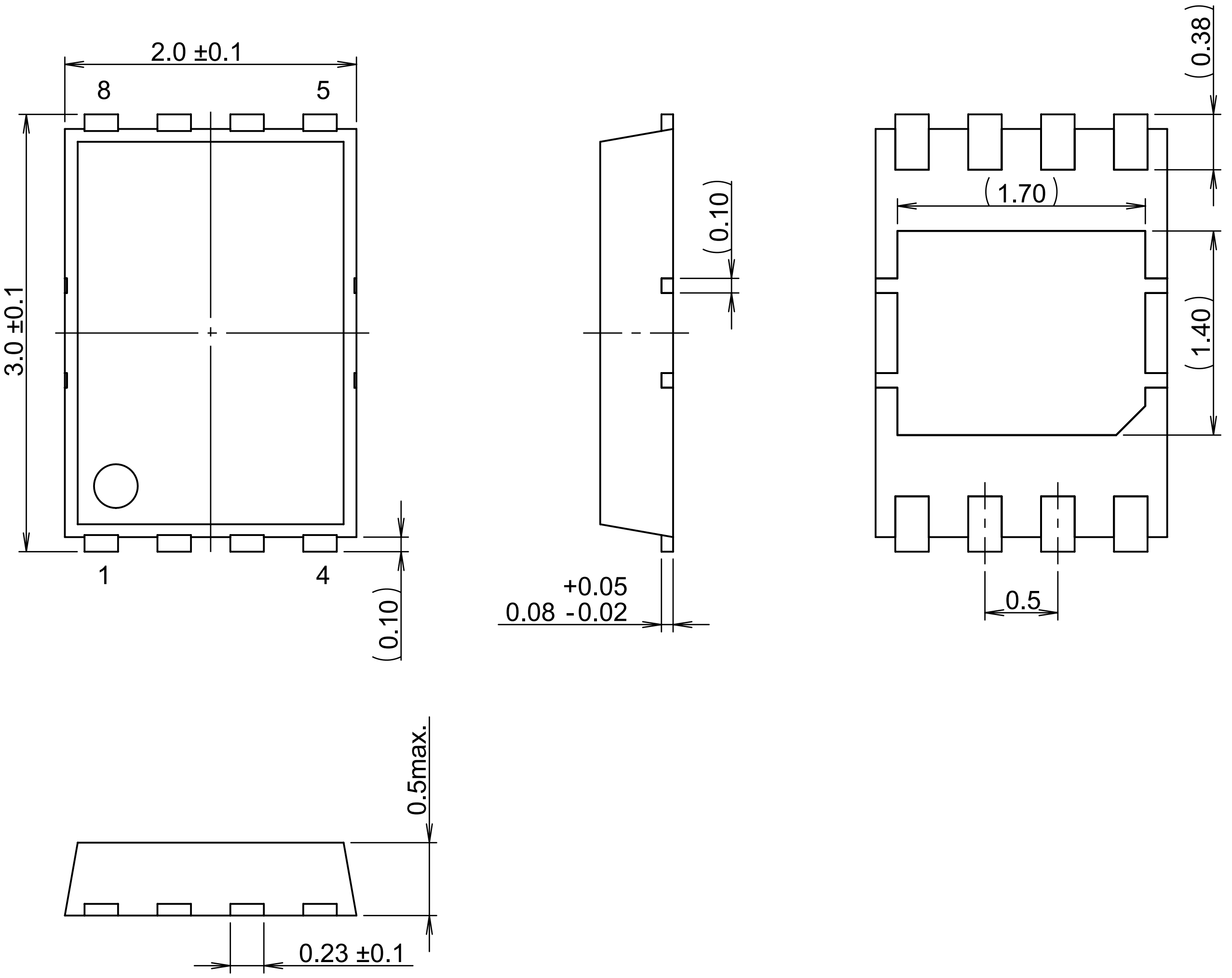
ABLIC Inc.



No. FP008-A-L-SD-2.0

TITLE	HTMSOP8-A -Land Recommendation
No.	FP008-A-L-SD-2.0
ANGLE	
UNIT	mm

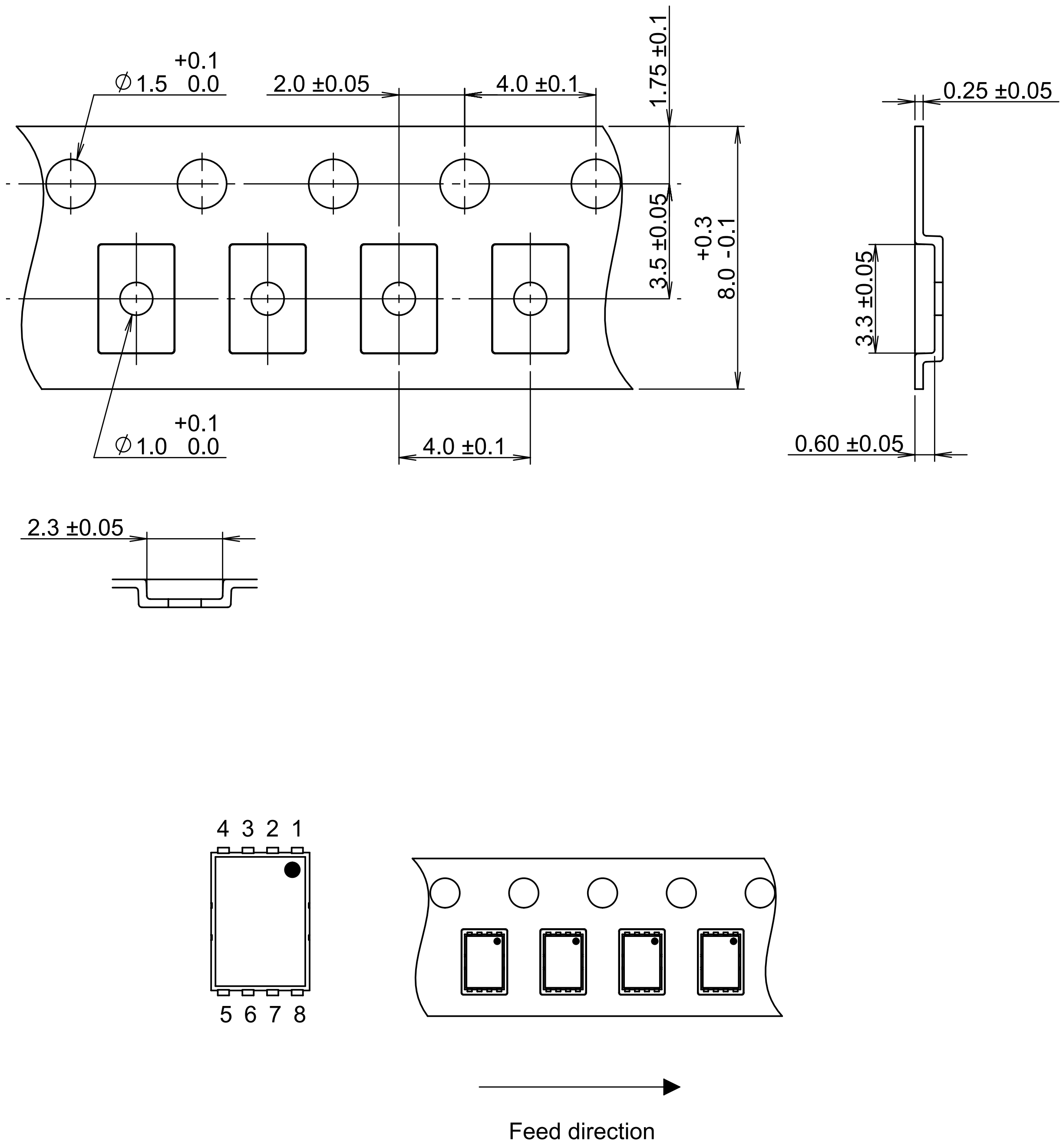
ABLIC Inc.



No. PP008-A-P-SD-3.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-3.0
ANGLE	
UNIT	mm

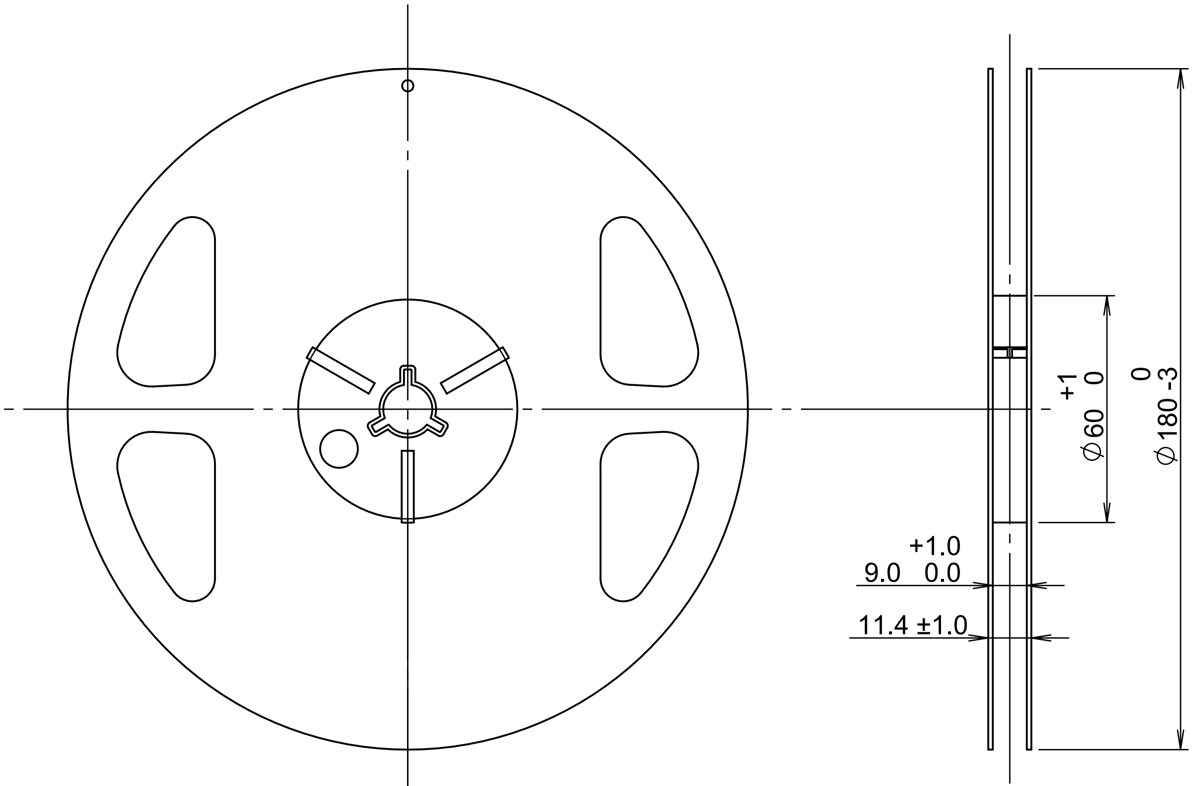
ABLIC Inc.



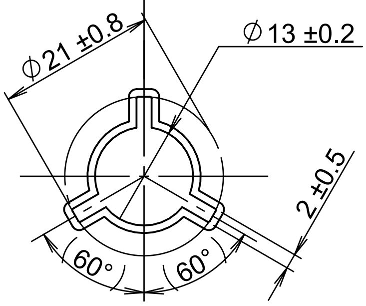
No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



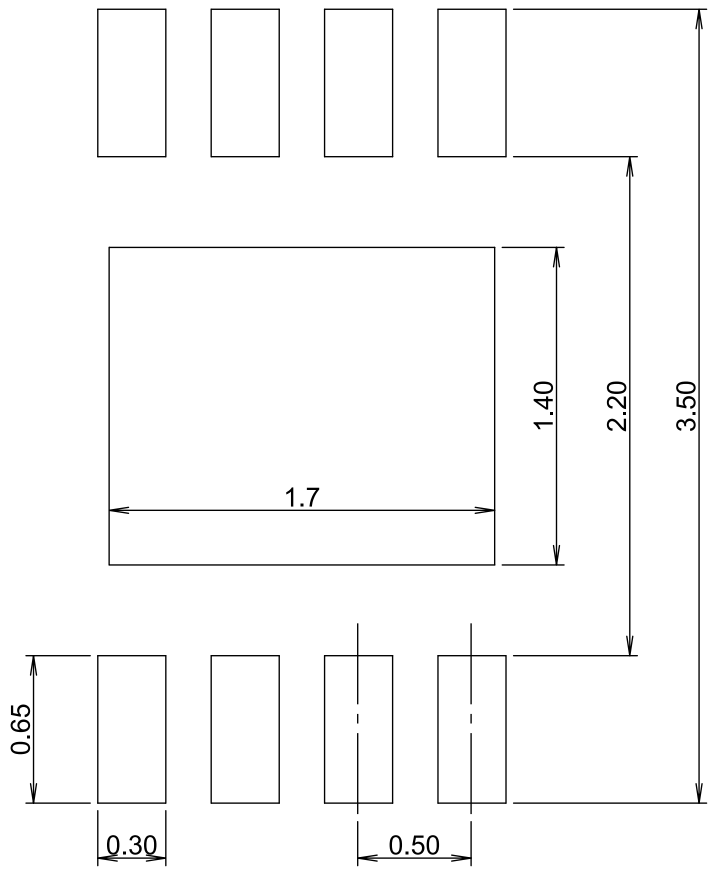
Enlarged drawing in the central part



No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		

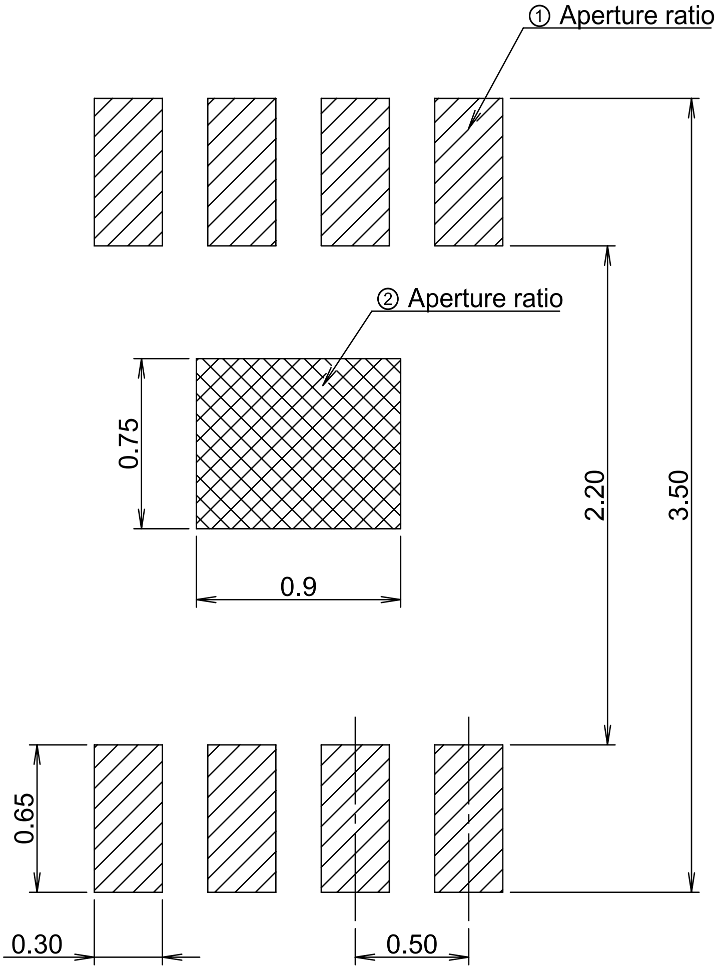
ABLIC Inc.



No. PP008-A-L-SD-2.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is approximately 30%.
③ Mask thickness: t0.12mm
④ Reflow atmosphere: Nitrogen atmosphere is recommended.
(Oxygen concentration: 1000ppm or less)

注意 ① リード実装部のマスク開口率：100%
② 放熱板実装のマスク開口率：約30%
③ マスク厚み：t0.12mm
④ リフロー雰囲気：窒素雰囲気(酸素濃度1000ppm以下)推奨

No. PP008-A-L-S1-2.0

TITLE	HSNT-8-A-Stencil Opening
No.	PP008-A-L-S1-2.0
ANGLE	
UNIT	mm

ABLIC Inc.

Disclaimers (Handling Precautions)

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