



# MP2984

## 36V, Synchronous Buck-Boost Controller with Current Monitoring, I<sup>2</sup>C Interface, and Adjustable OCP via IPWM

### DESCRIPTION

The MP2984 is a high-efficiency, synchronous, quad-switch, buck-boost controller that can regulate different output voltages across a wide input voltage ( $V_{IN}$ ) range. The output voltage ( $V_{OUT}$ ),  $V_{OUT}$  slew-rate, and output constant-current limit can be configured via the I<sup>2</sup>C interface. The MP2984 is suitable for USB power delivery (PD) applications in USB Type-C power supplies.

The MP2984 uses valley current control in buck mode and peak current control in boost mode to provide fast load transient response and smooth buck-boost mode transient. Forced continuous conduction mode (FCCM) and a configurable current limit support flexible design for various applications.

Full protection features include configurable over-current protection (OCP), over-voltage protection (OVP), and  $V_{IN}$  under-voltage lockout (UVLO) hysteresis.

The MP2984 is available in a QFN-32 (4mmx4mm) package.

### FEATURES

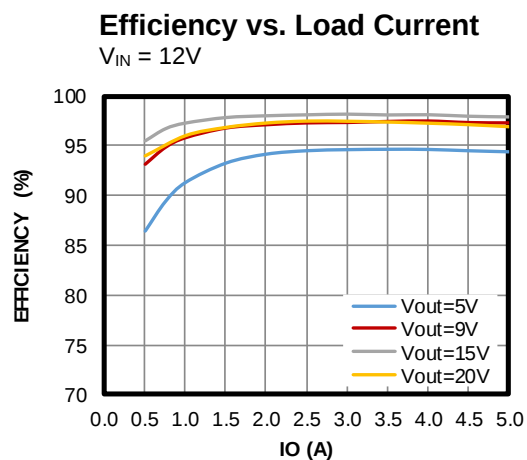
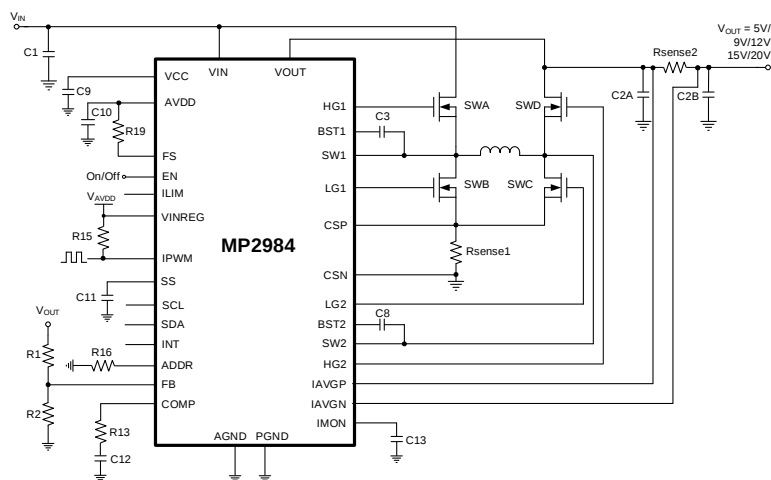
- Wide 5V to 36V Operating  $V_{IN}$  Range
- Wide 6V to 36V Start-Up Input Voltage ( $V_{IN}$ ) Range
- Flexible Control via the I<sup>2</sup>C Interface:
  - 0.5V to 28V Output Voltage ( $V_{OUT}$ ) Range
  - 0.3V to 2.047V Reference Voltage ( $V_{REF}$ ) Range with 1mV Step
  - Selectable  $V_{OUT}$  Slew Rate
  - Configurable Constant-Current Limit
- Adjustable Current Limit with <50mA Steps via IPWM
- Output Current Monitoring (IMON)
- Configurable Soft-Start Time ( $t_{SS}$ )
- Switching Frequency ( $f_{SW}$ ) with Frequency Spread Spectrum for Reduced EMI
- Integrated  $V_{OUT}$  Discharge
- 200kHz, 300kHz, 400kHz, or 600kHz Selectable  $f_{SW}$
- Forced Continuous Conduction Mode (FCCM)
- Configurable  $V_{IN}$  Under-Voltage Lockout (UVLO) Hysteresis
- Minimum  $V_{IN}$  Regulation
- Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Over-Voltage Protection (OVP)
- OCP, OVP, OTP, and PNG Interrupt Indication
- Available in a QFN-32 (4mmx4mm) Package

### APPLICATIONS

- USB Power Delivery (PD)
- Industrial PC Power Supplies

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## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number | Package          | Top Marking | MSL Rating |
|-------------|------------------|-------------|------------|
| MP2984GR*   | QFN-32 (4mmx4mm) | See Below   | 1          |
| EVKT-MP2984 | Evaluation kit   |             |            |

\* For Tape & Reel, add suffix -Z (e.g. MP2984GR-Z).

## TOP MARKING

**MPSYWW**

**MP2984**

**LLLLLL**

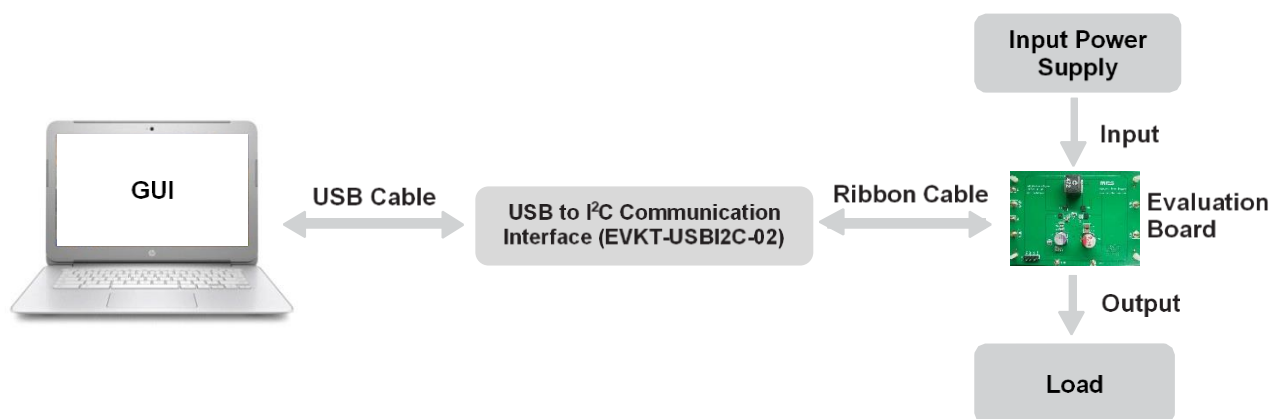
MPS: MPS prefix  
Y: Year code  
WW: Week code  
MP2984: Part number  
LLLLLL: Lot number

## EVALUATION KIT EVKT-MP2984

EVKT-MP2984 kit contents (items below can be ordered separately).

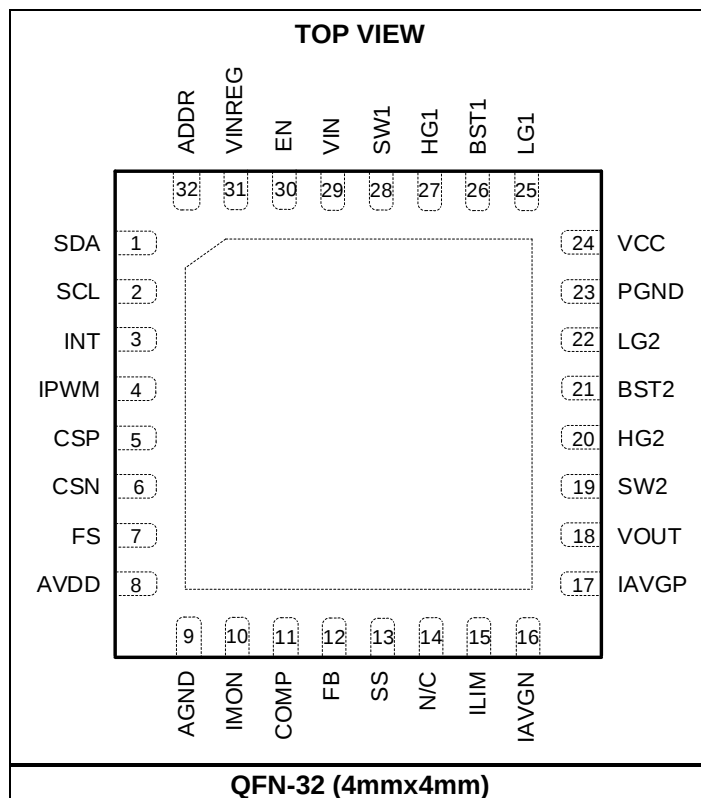
| # | Part Number        | Item                                                                                         | Quantity |
|---|--------------------|----------------------------------------------------------------------------------------------|----------|
| 1 | EV2984-R-00B       | MP2984GR evaluation board                                                                    | 1        |
| 2 | EVKT-USBI2C-02-BAG | Includes USB to I <sup>2</sup> C communication interface device, USB cable, and ribbon cable | 1        |

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**Figure 1: EVKT-MP2984 Evaluation Kit Set-Up**

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | SDA   | I <sup>2</sup> C data signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 2     | SCL   | I <sup>2</sup> C clock signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3     | INT   | <b>Interrupt for over-current (OC), over-temperature (OT), over-voltage (OV), and PNG fault events.</b> If a PNG event occurs in a default set-up, the INT pin is masked off. INT is an open-drain output. If an interrupt event occurs, INT is pulled low. INT recovers to its initial status once the fault is removed. If the IC is disabled, then INT is an open drain.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4     | IPWM  | <b>Current dimming pulse-width modulation (PWM) signal input.</b> If the output current limit (I <sub>OUT_LIMIT</sub> ) is configured via the I <sup>2</sup> C register, then the IPWM pin input signal duty cycle controls the average I <sub>OUT_LIMIT</sub> . Pull IPWM up to the AVDD pin internally via a 1MΩ resistor to set a 100% duty high-level voltage. It is recommended to connect an additional 100kΩ external pull-up resistor to IPWM.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 5     | CSP   | <b>Positive switching current-sense input.</b> Connect the CSP pin to the high side (HS) of the current-sense resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 6     | CSN   | <b>Negative switching current-sense input.</b> Connect the CSN pin to the low side (LS) of the current-sense resistor.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7     | FS    | <b>Switching frequency (f<sub>sw</sub>) bits default value setting.</b> During start-up, the two voltage levels on the FS pin set the default f <sub>sw</sub> values. The first FS voltage level is 0.51 x V <sub>AVDD</sub> to 0.68 x V <sub>AVDD</sub> , and the FSW bits are set to 00 (200kHz default f <sub>sw</sub> ). The second FS voltage level is 0.74 x V <sub>AVDD</sub> or greater, and the FSW bits are set to 10 (400kHz default f <sub>sw</sub> ). Do not float FS or connect FS to GND. For different voltage level settings, see the Electrical Characteristics section on page 9. Changing the FS voltage level after start-up does not change the FSW bit settings. After start-up, the FSW bits can be set via the I <sup>2</sup> C interface.                                                                                                                                      |
| 8     | AVDD  | <b>Internal control circuit bias supply.</b> Use a ≥2.2μF decoupling capacitor to decouple the AVDD pin.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 9     | AGND  | <b>Analog ground.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 10    | IMON  | <b>Current monitoring output.</b> The IMON pin outputs the voltage signal between the IAVGP and IAVGN pins. The MP2984 senses the average load current via a current-sense resistor to output this signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 11    | COMP  | <b>Internal error amplifier (EA) output.</b> For loop compensation, connect a capacitor and a resistor in series between the COMP and AGND pins.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 12    | FB    | <b>Output voltage (V<sub>OUT</sub>) feedback.</b> Connect a resistor divider between the VOUT and FB pins.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 13    | SS    | <b>Soft start (SS) setting.</b> Connect an external capacitor to the SS pin. SS also sets the hiccup mode off time.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 14    | NC    | <b>No connection.</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15    | ILIM  | <b>ILIM bits default value setting.</b> During start-up, the two voltage levels on the ILIM pin set the default current limit (I <sub>LIMIT</sub> ) values. At the first ILIM voltage level, the ILIM bits are set to 001 (32mV default I <sub>LIMIT</sub> ). At the second ILIM voltage level, the ILIM bits are set to 011 (45mV default I <sub>LIMIT</sub> ). At the third ILIM voltage level, the ILIM bits are set to 101 (56mV default I <sub>LIMIT</sub> ). At the fourth ILIM voltage level, the ILIM bits are set to 111 (68mV default I <sub>LIMIT</sub> ). In default set-up, float the ILIM pin to set the ILIMT bits to 111. For different voltage level settings, see the Electrical Characteristics section on page 9. Changing the ILIM voltage level after start-up does not change the ILIM bit settings. After start-up, the ILIM bits can be set via the I <sup>2</sup> C interface. |
| 16    | IAVGN | <b>Negative average current limit sense input.</b> Connect the IAVGN and IAVGP pins to the output rail's positive terminal to use IAVGN and IAVGP to set I <sub>OUT_LIMIT</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 17    | IAVGP | <b>Positive average current limit sense input.</b> Connect the IAVGN and IAVGP pins to the output rail's positive terminal to use IAVGN and IAVGP to set I <sub>OUT_LIMIT</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 18    | VOUT  | <b>V<sub>OUT</sub> voltage sense input.</b> The VOUT pin supplies power to the VCC pin based on the VCC power logic. Connect VOUT to the output capacitor (C <sub>OUT</sub> ).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19    | SW2   | <b>Converter boost switch node.</b> Connect the SW2 pin to SWD's source and SWC's drain.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## PIN FUNCTIONS (continued)

| Pin # | Name   | Description                                                                                                                                                                                             |
|-------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20    | HG2    | <b>Boost high-side MOSFET (HS-FET) gate driver.</b> Connect the HG2 pin to SWD's gate.                                                                                                                  |
| 21    | BST2   | <b>Boost HS-FET gate driver bootstrap power.</b> Connect a capacitor between the BST2 and SW2 pins. VCC or BST1 can supply BST2.                                                                        |
| 22    | LG2    | <b>Boost low-side MOSFET (LS-FET) gate driver.</b> Connect the LG2 pin to SWC's gate.                                                                                                                   |
| 23    | PGND   | <b>Power ground.</b> Gate driver current return pin.                                                                                                                                                    |
| 24    | VCC    | <b>Driver circuit and internal bias supply.</b> Use a $\geq 2.2\mu\text{F}$ ceramic decoupling capacitor to decouple VCC. Place this capacitor as close to VCC as possible. VOUT or VIN can supply VCC. |
| 25    | LG1    | <b>Buck LS-FET gate driver pin.</b> Connect LG1 to SWB's gate.                                                                                                                                          |
| 26    | BST1   | <b>Buck HS-FET gate driver bootstrap power.</b> Connect a capacitor between the BST1 and SW1 pins. VCC or BST2 can supply BST1.                                                                         |
| 27    | HG1    | <b>Buck HS-FET gate driver.</b> Connect directly to the gate of SWA.                                                                                                                                    |
| 28    | SW1    | <b>Converter buck switch node.</b> Connect to the source of SWA and the drain of SWB.                                                                                                                   |
| 29    | VIN    | <b>Power supply and voltage sense input.</b>                                                                                                                                                            |
| 30    | EN     | <b>Enable.</b> If not used, connect the EN pin to the input source for automatic start-up. EN can also configure V <sub>IN</sub> under-voltage lockout (UVLO) protection. Do not float EN.              |
| 31    | VINREG | <b>V<sub>IN</sub> regulation.</b> The VINREG pin sets the minimum operating V <sub>IN</sub> during switching. Connect VINREG to AVDD if not used.                                                       |
| 32    | ADDR   | <b>I<sup>2</sup>C slave address setting.</b> The ADDR pin sets the ENPWR bit's default value.                                                                                                           |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                 |                                       |
|-------------------------------------------------|---------------------------------------|
| VIN, EN                                         | -0.3V to +40V                         |
| VOUT, IAVGP, IAVGN                              | -0.3V to +30V                         |
| VCC                                             | -0.3V to +8.5V                        |
| SW1, SW2                                        | -1V to +40V (-5V to +45V for <20ns)   |
| LG1, LG2                                        | -0.3V to +10V (-2V to +11V for <20ns) |
| BST1, HG1                                       | -0.3V to V <sub>SW1</sub> + 8.5V      |
| BST2, HG2                                       | -0.3V to V <sub>SW2</sub> + 8.5V      |
| All other pins                                  | -0.3V to +6.5V                        |
| Continuous power dissipation <sup>(2) (5)</sup> | 4.4W                                  |
| Junction temperature                            | 150°C                                 |
| Lead temperature                                | 260°C                                 |
| Storage temperature                             | -65°C to +150°C                       |

## Recommended Operating Conditions <sup>(3)</sup>

|                                                           |                 |
|-----------------------------------------------------------|-----------------|
| Start-up voltage (V <sub>SU</sub> )                       | 6V to 36V       |
| Operating input voltage (V <sub>IN</sub> ) <sup>(4)</sup> | 5V to 36V       |
| Output voltage (V <sub>OUT</sub> )                        | 0.5V to 28V     |
| Operating junction temp (T <sub>J</sub> )                 | -40°C to +125°C |

## Thermal Resistance

|                             | $\theta_{JA}$ | $\theta_{JC}$ |
|-----------------------------|---------------|---------------|
| EV2984-R-00B <sup>(5)</sup> | 28            | 8             |
| JESD51-7 <sup>(6)</sup>     | 42            | 9             |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- This value is the operating V<sub>IN</sub> after V<sub>OUT</sub> has been regulated at  $\geq 5\text{V}$ , and the VCC load is < 10mA.
- Measured on the MPS evaluation board EV2984-R-00B, 91.4mmx66mm, 6-layer PCB, 20z-10z-10z-10z-10z-20z.
- The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to 125°C <sup>(7)</sup>, typical values are tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                        | Symbol                       | Condition                                                                                                  | Min   | Typ   | Max   | Units                 |
|------------------------------------------------------------------|------------------------------|------------------------------------------------------------------------------------------------------------|-------|-------|-------|-----------------------|
| Power Supply                                                     |                              |                                                                                                            |       |       |       |                       |
| Operating VCC voltage                                            | V <sub>CC</sub>              | V <sub>IN</sub> = 6V or V <sub>OUT</sub> = 6V, 0mA to 20mA on VCC                                          | 5.1   | 5.95  | 6     | V                     |
|                                                                  |                              | V <sub>IN</sub> = 12V or V <sub>OUT</sub> = 12V, 0mA to 60mA on VCC                                        | 6.7   | 7.2   | 7.7   | V                     |
| VIN under-voltage lockout (UVLO) rising threshold <sup>(8)</sup> | V <sub>IN_UVLO_RISING</sub>  | V <sub>IN</sub> rising                                                                                     | 5     | 5.5   | 5.9   | V                     |
| VCC UVLO falling threshold <sup>(8)</sup>                        | V <sub>CC_UVLO_FALLING</sub> | V <sub>CC</sub> falling                                                                                    | 3.8   | 4.3   | 4.8   | V                     |
| VCC power source threshold                                       | V <sub>IN_VCC</sub>          | V <sub>OUT</sub> = 12V, V <sub>IN</sub> ramps up from 5V to 10V                                            | 8.1   | 8.8   | 9.5   | V                     |
|                                                                  | V <sub>OUT_VCC</sub>         | V <sub>IN</sub> = 12V, V <sub>OUT</sub> ramps up from 5V to 10V                                            | 8.1   | 8.8   | 9.5   | V                     |
| AVDD voltage                                                     | V <sub>AVDD</sub>            | V <sub>IN</sub> = 12V, 0mA to 5mA                                                                          | 4.7   | 5.2   | 5.6   | V                     |
| Shutdown current                                                 | I <sub>SD</sub>              | Measured on the VIN and VOUT pins, V <sub>EN</sub> = 0V                                                    |       |       | 5     | μA                    |
|                                                                  |                              | ENPWR bit = 0, V <sub>IN</sub> = 12V, V <sub>OUT</sub> = 0V, measured on the VIN pin, V <sub>EN</sub> = 2V | 300   | 450   | 600   | μA                    |
| Enable (EN) Control                                              |                              |                                                                                                            |       |       |       |                       |
| EN start-up threshold voltage                                    | V <sub>EN_SU</sub>           | V <sub>EN</sub> rising, switching                                                                          | 1.25  | 1.35  | 1.45  | V                     |
| V <sub>EN</sub> high threshold                                   | V <sub>EN_HIGH</sub>         | V <sub>EN</sub> rising, micro-power                                                                        |       |       | 1.1   | V                     |
| V <sub>EN</sub> low threshold                                    | V <sub>EN_LOW</sub>          | V <sub>EN</sub> falling, micro-power                                                                       | 0.4   |       |       | V                     |
| EN start-up hysteresis current                                   | I <sub>EN_HYS</sub>          | V <sub>EN</sub> > V <sub>EN_SU</sub> , EN source current                                                   | 3.2   | 4.7   | 6.2   | μA                    |
| EN current                                                       | I <sub>EN</sub>              | V <sub>EN</sub> = 0V, 3.3V                                                                                 |       | 0.01  |       | μA                    |
| ENPWR start-up delay <sup>(9)</sup>                              | t <sub>DELAY_ENPWR</sub>     | From ENPWR = 1 to switching, C <sub>SS</sub> = 47nF                                                        |       | 1     |       | ms                    |
| Feedback (FB) Control                                            |                              |                                                                                                            |       |       |       |                       |
| FB reference voltage                                             | V <sub>REF</sub>             | VREF bits = 7FFH, T <sub>J</sub> = 25°C                                                                    | -1    | 2.047 | +1    | % of V <sub>REF</sub> |
|                                                                  |                              | VREF bits = 7FFH, T <sub>J</sub> = -40°C to 125°C                                                          | -2    | 2.047 | +2    |                       |
|                                                                  |                              | VREF bits = 1F4H, T <sub>J</sub> = 25°C                                                                    | -2    | 0.5   | +2    |                       |
|                                                                  |                              | VREF bits = 1F4H, T <sub>J</sub> = -40°C to 125°C                                                          | -3    | 0.5   | +3    |                       |
| FB current                                                       | I <sub>FB</sub>              | V <sub>FB</sub> = 0.52V                                                                                    |       |       | 200   | nA                    |
| Error amplifier (EA) transconductance                            | G <sub>EA</sub>              | V <sub>FB</sub> = V <sub>REF</sub> + 10mV, V <sub>COMP</sub> = 2.5V                                        |       | 1220  |       | μA/V                  |
| COMP to Current Sense Gain <sup>(9)</sup>                        | G <sub>CS</sub>              | ΔV <sub>CS</sub> / ΔV <sub>COMP</sub>                                                                      |       | 200   |       | mV/V                  |
| SS Charge Current                                                | I <sub>CHG_SS</sub>          | During soft start and overload recovery                                                                    | 2     | 6     | 10    | μA                    |
| SS Discharge Current                                             | I <sub>DSG_SS</sub>          | After hiccup protection is triggered                                                                       |       | 1     |       | μA                    |
| V <sub>REF</sub> slew rate                                       | t <sub>SR</sub>              | SR = 00                                                                                                    | 25    | 38    | 51    | mV/ms                 |
|                                                                  |                              | SR = 11                                                                                                    | 130   | 150   | 170   | mV/ms                 |
| VINREG voltage                                                   | V <sub>VINREG</sub>          | T <sub>J</sub> = 25°C                                                                                      | 1.188 | 1.2   | 1.212 | V                     |
|                                                                  |                              | T <sub>J</sub> = -40°C to 125°C                                                                            | 1.182 | 1.2   | 1.218 | V                     |
| VINREG current                                                   | I <sub>VINREG</sub>          | V <sub>VINREG</sub> = 1.25V                                                                                |       |       | 50    | nA                    |
| Current Limit                                                    |                              |                                                                                                            |       |       |       |                       |
| Buck valley current limit                                        | I <sub>LIMIT_VALLEY</sub>    |                                                                                                            | 113   | 133   | 153   | mV                    |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to 125°C <sup>(7)</sup>, typical values are tested at T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameter                                                           | Symbol                  | Condition                                                                                          | Min                                          | Typ  | Max  | Units                 |
|---------------------------------------------------------------------|-------------------------|----------------------------------------------------------------------------------------------------|----------------------------------------------|------|------|-----------------------|
| Boost peak current limit                                            | I <sub>LIMIT_PEAK</sub> |                                                                                                    | 130                                          | 150  | 170  | mV                    |
| Over-current protection (OCP) threshold <sup>(9)</sup>              | V <sub>OCP</sub>        |                                                                                                    |                                              | 60   |      | % of V <sub>REF</sub> |
| Constant-current limit                                              | I <sub>LIMIT_CC</sub>   | ILIM bits = 011, V <sub>IAVGN</sub> = 12V, V <sub>IAVGP</sub> ramps up                             | 40                                           | 45   | 50   | mV                    |
|                                                                     |                         | ILIM bits = 111, V <sub>IAVGN</sub> = 12V, V <sub>IAVGP</sub> ramps up                             | 62.5                                         | 68   | 73.5 | mV                    |
|                                                                     |                         | ILIM bits = 111, V <sub>IAVGN</sub> = 12V, T <sub>J</sub> = 25°C, V <sub>IAVGP</sub> ramps up      | -5%                                          | 68   | +5%  | mV                    |
| IPWM input high threshold                                           | V <sub>IPWM_HIGH</sub>  |                                                                                                    |                                              |      | 1.2  | V                     |
| IPWM input low threshold                                            | V <sub>IPWM_LOW</sub>   |                                                                                                    | 0.4                                          |      |      | V                     |
| IPWM to AVDD internal pull-up resistor                              | R <sub>IPWM</sub>       |                                                                                                    |                                              | 1    |      | MΩ                    |
| Current limit dimming                                               | I <sub>DIMMING</sub>    | 48% IPWM duty, 20kHz signal, T <sub>J</sub> = 25°C, ILIM bits = 111, measure load current limit    | 33                                           | 36   | 41   | mV                    |
|                                                                     |                         | IPWM duty = 71.5% 20kHz signal, T <sub>J</sub> = 25°C, ILIM bits = 111, measure load current limit | 48                                           | 51.5 | 57   | mV                    |
| CSP and CSN current bias                                            | I <sub>CS_BIAS</sub>    | V <sub>CSP</sub> = V <sub>CSN</sub> = 0V                                                           |                                              | 70   |      | μA                    |
| IAVGP and IAVGN current bias                                        | I <sub>AV_BIAS</sub>    | IAVGN = 5V, IAVGN = 20V, V <sub>IAVGP</sub> - V <sub>IAVGN</sub> = 40mV                            |                                              | 55   |      | μA                    |
| <b>Switching Frequency</b>                                          |                         |                                                                                                    |                                              |      |      |                       |
| Switching frequency                                                 | f <sub>SW</sub>         | FSW bits = 10, V <sub>OUT</sub> = 5V                                                               | 320                                          | 400  | 480  | kHz                   |
|                                                                     |                         | FSW bits = 00, V <sub>OUT</sub> = 5V                                                               | 140                                          | 200  | 260  | kHz                   |
| Frequency spread span <sup>(9)</sup>                                | f <sub>SS</sub>         | Dither bit = 1                                                                                     |                                              | ±6   |      | % of f <sub>SW</sub>  |
| Frequency spread spectrum (FSS) modulation frequency <sup>(9)</sup> | f <sub>SS_MOD</sub>     | Dither bit = 1                                                                                     |                                              | 2    |      | kHz                   |
| <b>Gate Driver</b>                                                  |                         |                                                                                                    |                                              |      |      |                       |
| Gate source current capability <sup>(9)</sup>                       | I <sub>HG_SOURCE</sub>  | V <sub>CC</sub> = 7.2V, 4.7nF load                                                                 |                                              | 0.7  |      | A                     |
|                                                                     | I <sub>LG_SOURCE</sub>  |                                                                                                    |                                              | 0.85 |      | A                     |
| Gate sink current capability <sup>(9)</sup>                         | I <sub>HG_SINK</sub>    | V <sub>CC</sub> = 7.2V, 4.7nF load                                                                 |                                              | 1.6  |      | A                     |
|                                                                     | I <sub>LG_SINK</sub>    |                                                                                                    |                                              | 2    |      | A                     |
| Low-side (LS) gate output high voltage                              | V <sub>LS_HIGH</sub>    |                                                                                                    | V <sub>CC</sub> - 0.05                       |      |      | V                     |
| LS gate output low voltage                                          | V <sub>LS_LOW</sub>     |                                                                                                    |                                              |      | 0.05 | V                     |
| High-side (HS) gate output high voltage                             | V <sub>HS_HIGH</sub>    |                                                                                                    | (V <sub>BST</sub> - V <sub>SW</sub> ) - 0.05 |      |      | V                     |
| HS gate output low voltage                                          | V <sub>HS_LOW</sub>     |                                                                                                    |                                              |      | 0.05 | V                     |
| Dead-time between HS gate and LS gate <sup>(9)</sup>                | t <sub>DEAD</sub>       |                                                                                                    |                                              | 30   |      | ns                    |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 12V, V<sub>EN</sub> = 2V, T<sub>J</sub> = -40°C to 125°C <sup>(7)</sup>, typical values are tested at T<sub>J</sub> = 25°C, unless otherwise noted.

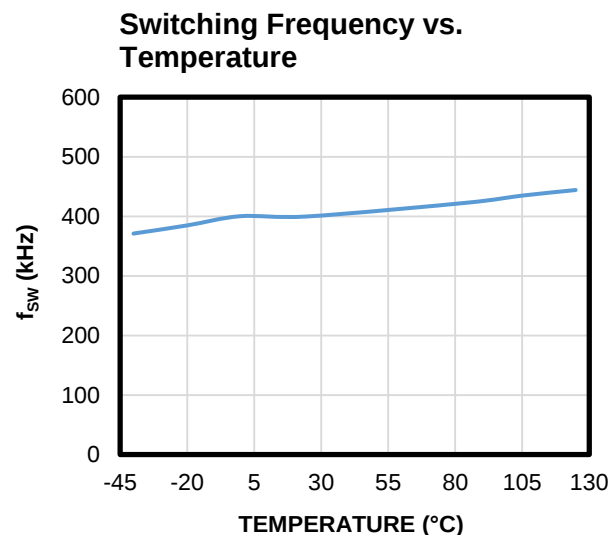
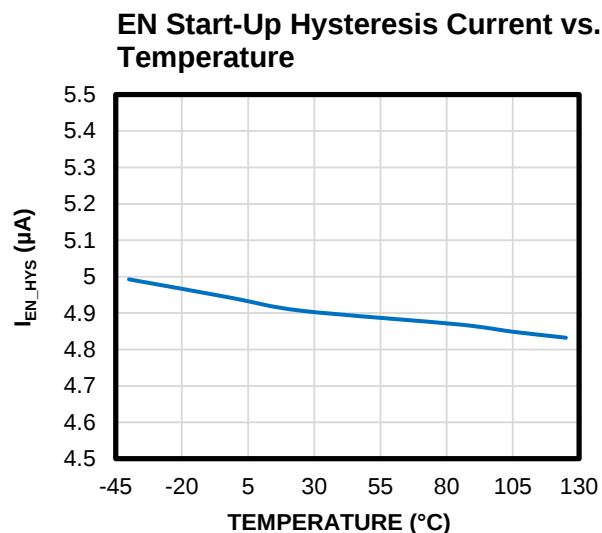
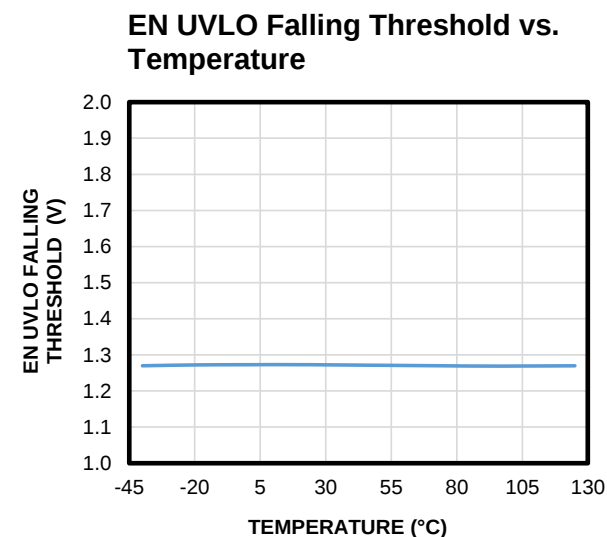
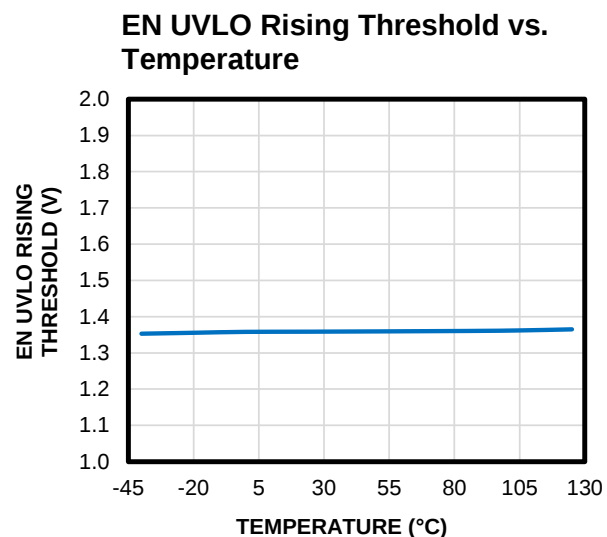
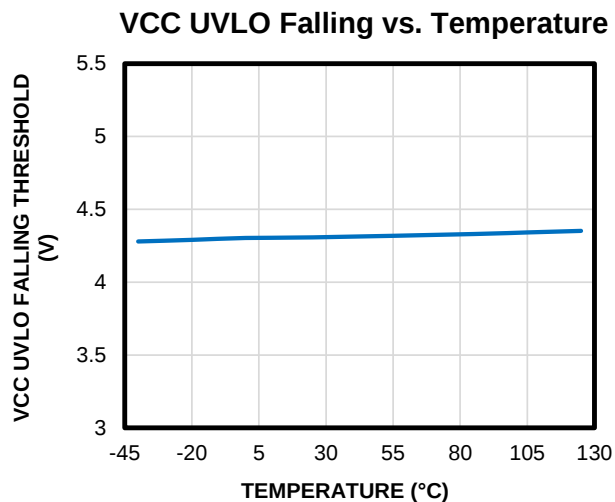
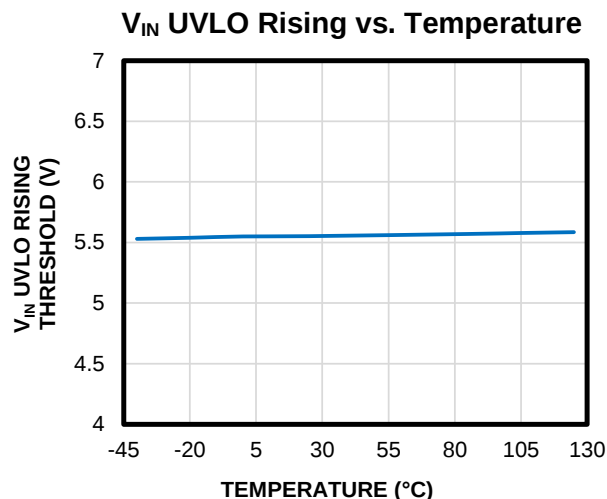
| Parameter                                    | Symbol                       | Condition                                    | Min   | Typ   | Max   | Units                 |
|----------------------------------------------|------------------------------|----------------------------------------------|-------|-------|-------|-----------------------|
| <b>Over-Voltage Protection (OVP)</b>         |                              |                                              |       |       |       |                       |
| FB OVP rising threshold                      | V <sub>OVP_RISING</sub>      |                                              | 119   | 127   | 135   | % of V <sub>REF</sub> |
| FB OVP falling threshold                     | V <sub>OVP_FALLING</sub>     |                                              | 104   | 111   | 118   | % of V <sub>REF</sub> |
| <b>Thermal Protection</b>                    |                              |                                              |       |       |       |                       |
| Thermal shutdown <sup>(9)</sup>              | T <sub>SD</sub>              |                                              |       | 150   |       | °C                    |
| Thermal shutdown hysteresis <sup>(9)</sup>   | T <sub>SD_HYS</sub>          |                                              |       | 25    |       | °C                    |
| <b>Power Good (PG)</b>                       |                              |                                              |       |       |       |                       |
| PG high threshold                            | V <sub>PG_FALLING_HIGH</sub> | PNG bit is set to 1, INT is pulled low       | 110   | 117   | 124   | % of V <sub>REF</sub> |
|                                              | V <sub>PG_RISING_HIGH</sub>  | PNG bit is reset to 0, INT is pulled high    | 101   | 106.5 | 112   |                       |
| PG low threshold                             | V <sub>PG_FALLING_LOW</sub>  | PNG bit set to 1, INT is pulled low          | 80    | 85.5  | 91    | % of V <sub>REF</sub> |
|                                              | V <sub>PG_RISING_LOW</sub>   | PNG bit resets to 0, INT is pulled high      | 85    | 91    | 97    |                       |
| PG delay (INT response to PNG fault)         | t <sub>DELAY_PG</sub>        | Low to high                                  |       | 10    |       | μs                    |
|                                              |                              | V <sub>OUT</sub> UVLO, high to low           |       | 2     |       | μs                    |
|                                              |                              | V <sub>OUT</sub> OVP, high to low            |       | 6.5   |       | ms                    |
| INT sink current capability                  | I <sub>SINK_INT</sub>        | 4mA sink                                     |       | 0.1   | 0.4   | V                     |
| INT leakage current                          | I <sub>LKG_INT</sub>         | V <sub>INT</sub> = 5V                        |       |       | 1     | μA                    |
| <b>I<sup>2</sup>C Interface</b>              |                              |                                              |       |       |       |                       |
| Input logic low voltage                      | V <sub>IN_LOW</sub>          | SCL, SDA                                     |       |       | 0.8   | V                     |
| Input logic high voltage                     | V <sub>IN_HIGH</sub>         | SCL, SDA                                     | 2     |       |       | V                     |
| Logic input current                          | I <sub>SCL_SDA_LKG</sub>     | SCL = 5V, SDA = 5V                           | -1    |       | +1    | μA                    |
| Output logic low voltage                     | V <sub>OUT_LOW</sub>         | SDA, 4mA sink                                |       |       | 0.4   | V                     |
| <b>ADDR Setting and ILIM Voltage Setting</b> |                              |                                              |       |       |       |                       |
| Voltage level 1 setting                      | ADDR1                        | Sets I <sup>2</sup> C address 60H (1100 000) |       |       | 0.23  | V <sub>AVDD</sub>     |
| Voltage level 2 setting                      | ADDR2                        | Sets I <sup>2</sup> C address 62H (1100 010) | 0.27  |       | 0.47  | V <sub>AVDD</sub>     |
| Voltage level 3 setting                      | ADDR3                        | Sets I <sup>2</sup> C address 64H (1100 100) | 0.51  |       | 0.68  | V <sub>AVDD</sub>     |
| Voltage level 4 setting                      | ADDR4                        | Sets I <sup>2</sup> C address 66H (1100 110) | 0.74  |       |       | V <sub>AVDD</sub>     |
| Pin to GND pull-down resistance              |                              | ADDR, ILIM pins                              |       | 2     |       | MΩ                    |
| <b>FS Pin Voltage Setting</b>                |                              |                                              |       |       |       |                       |
| Voltage level 1 setting                      | V <sub>FS_LEVEL1</sub>       | Sets FSW bits to 00                          | 0.51  |       | 0.68  | V <sub>AVDD</sub>     |
| Voltage level 2 setting                      | V <sub>FS_LEVEL2</sub>       | Sets FSW bits to 10                          | 0.74  |       |       | V <sub>AVDD</sub>     |
| <b>Current Monitoring</b>                    |                              |                                              |       |       |       |                       |
| IMON V <sub>OUT</sub> gain                   | G <sub>IMON</sub>            | I <sub>AVG</sub> sense voltage = 5mV         |       | 18.8  |       | V/V                   |
|                                              |                              | I <sub>AVG</sub> sense voltage = 55mV        | 16.92 | 18.8  | 20.68 | V/V                   |

### Notes:

- 7) Not tested in production. Guaranteed by over-temperature (OT) correlation.
- 8) The MP2984 has a minimum start-up voltage of 6, and its V<sub>IN</sub> UVLO falling threshold is lower than its VCC UVLO falling.
- 9) Guaranteed by engineer sample characterization.

# TYPICAL PERFORMANCE CHARACTERISTICS

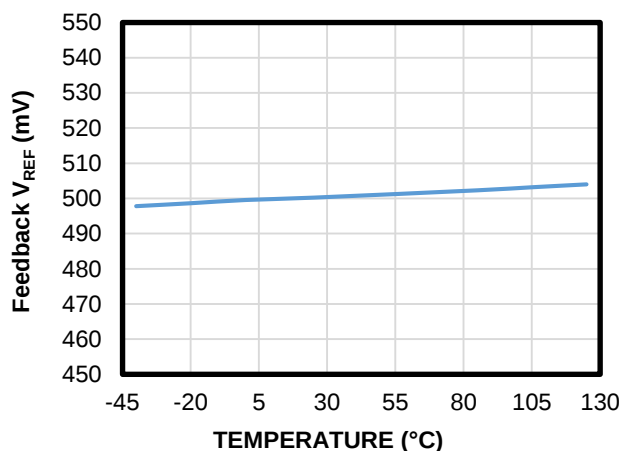
V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

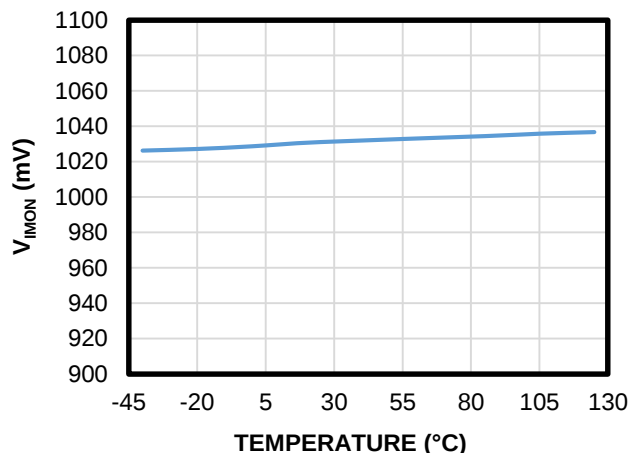
V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

**Feedback Reference Voltage vs. Temperature**

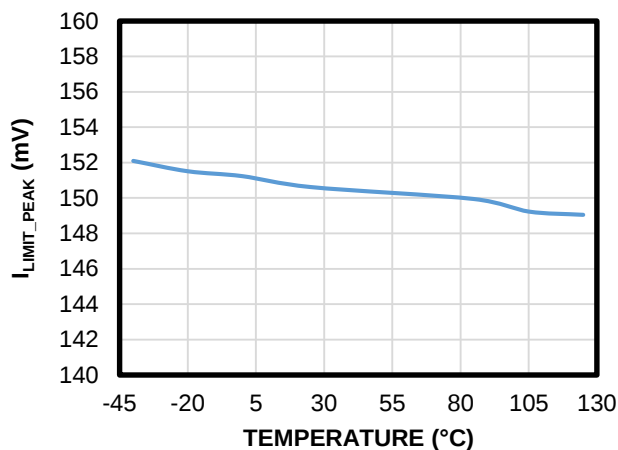


**IMON Voltage vs. Temperature**

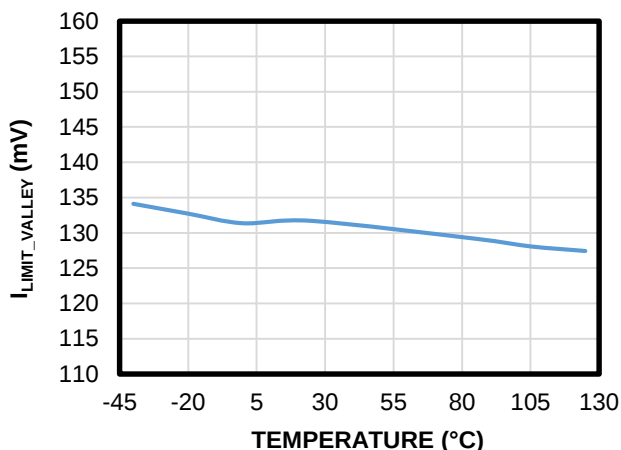
V<sub>IAVGP</sub> - V<sub>IAVGN</sub> = 55mV



**Boost Peak Current Limit vs. Temperature**

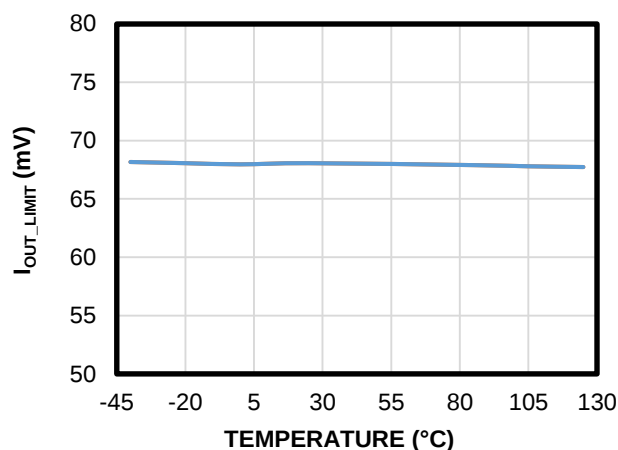


**Buck Valley Current Limit vs. Temperature**



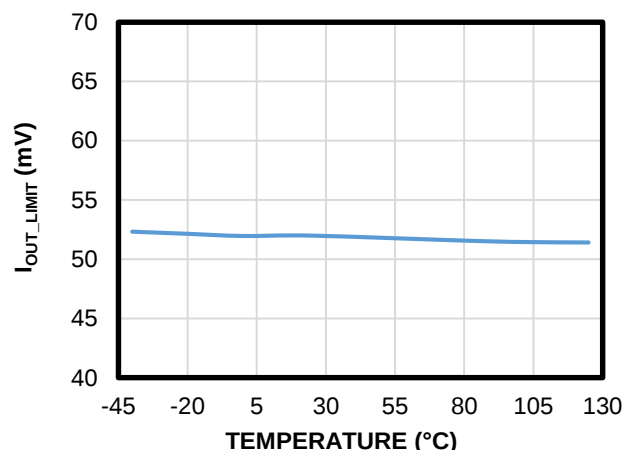
**Output Current Limit vs. Temperature**

ILIM bit = 111



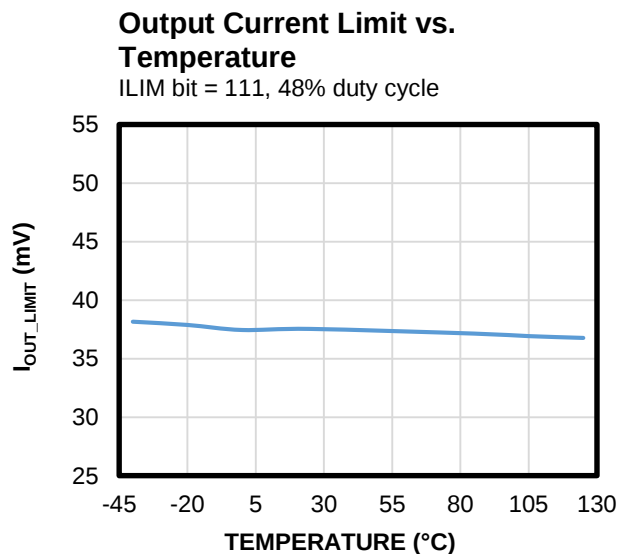
**Output Current Limit vs. Temperature**

ILIM bit = 111, 71.5% duty cycle



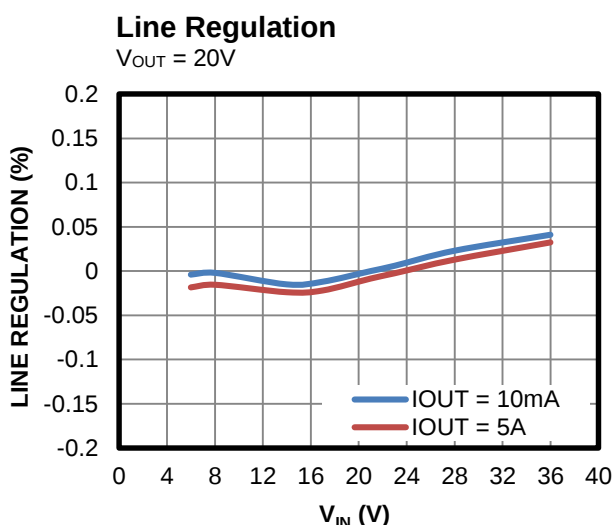
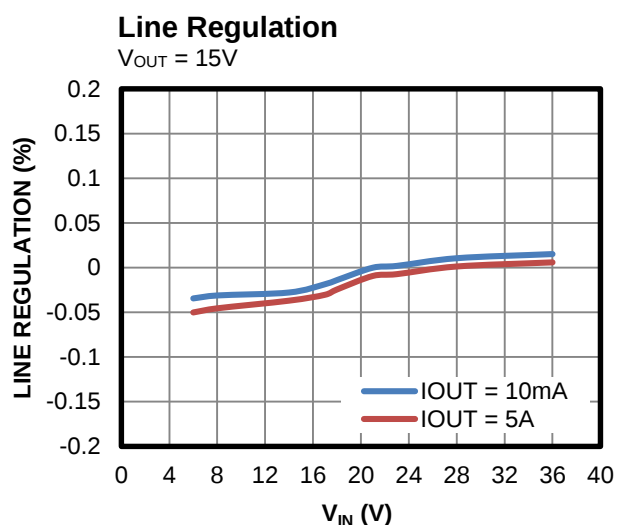
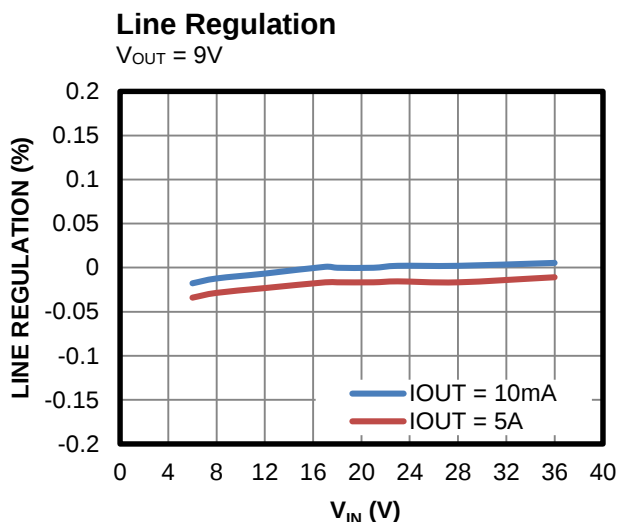
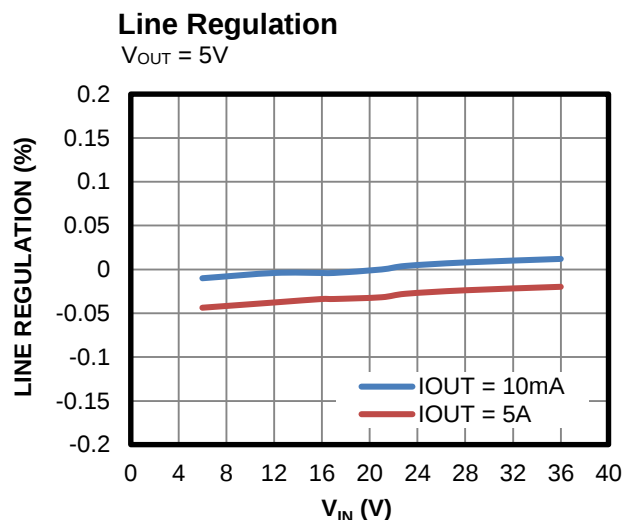
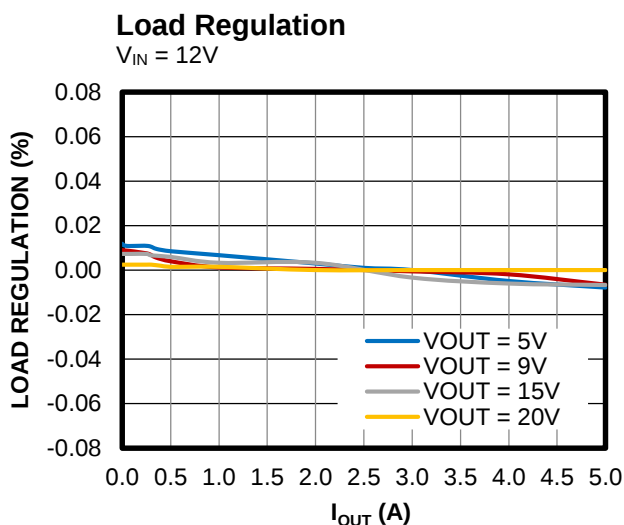
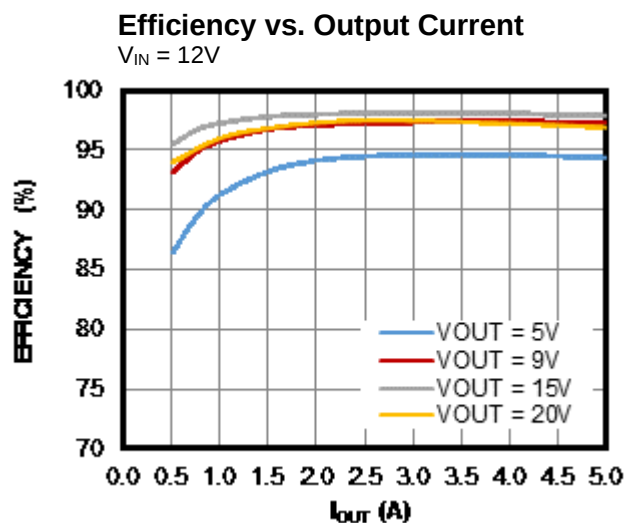
**TYPICAL PERFORMANCE CHARACTERISTICS** (*continued*)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

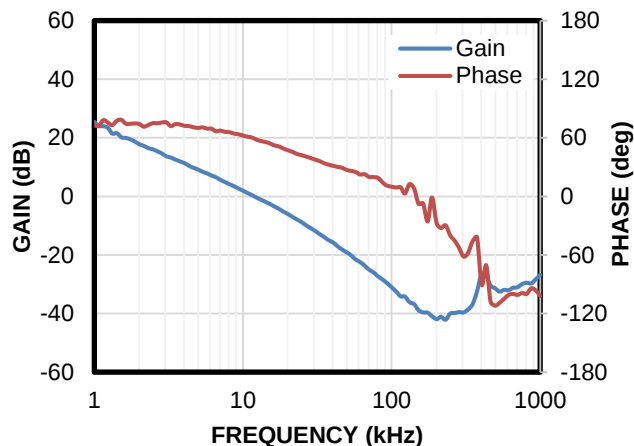


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $L = 4.7\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

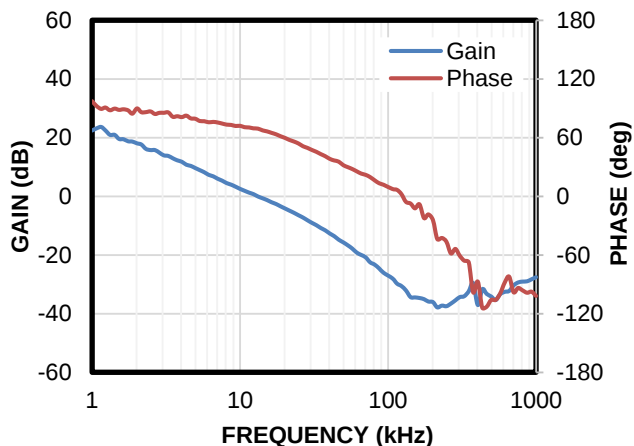
**Bode Plot**

$V_{OUT} = 5V$ ,  $I_{OUT} = 3A$ ,  $BW = 12.37kHz$ ,  
PM = 58.149°



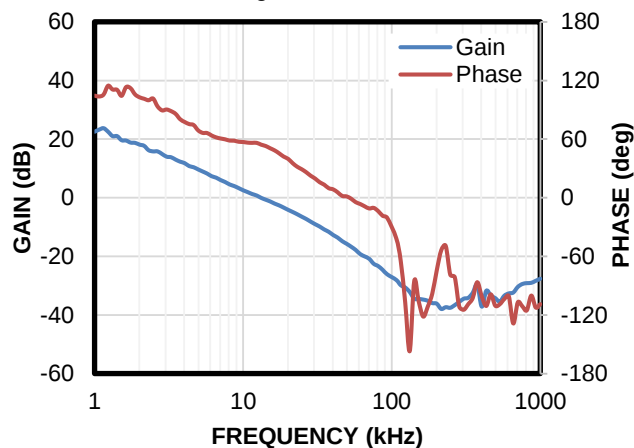
**Bode Plot**

$V_{OUT} = 9V$ ,  $I_{OUT} = 3A$ ,  $BW = 13.81kHz$ ,  
PM = 68.188°



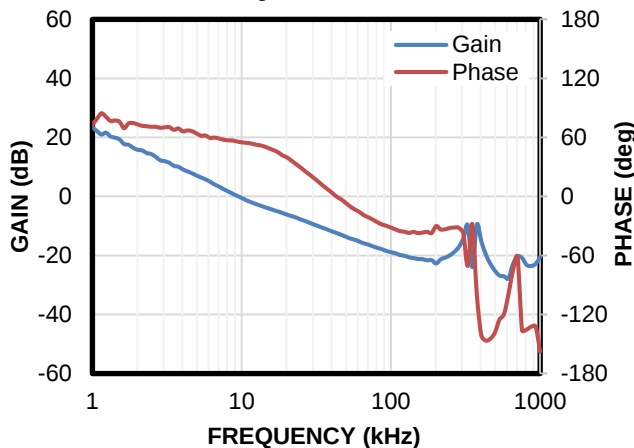
**Bode Plot**

$V_{OUT} = 15V$ ,  $I_{OUT} = 3A$ ,  $BW = 9.16 kHz$ ,  
PM = 57.613 deg



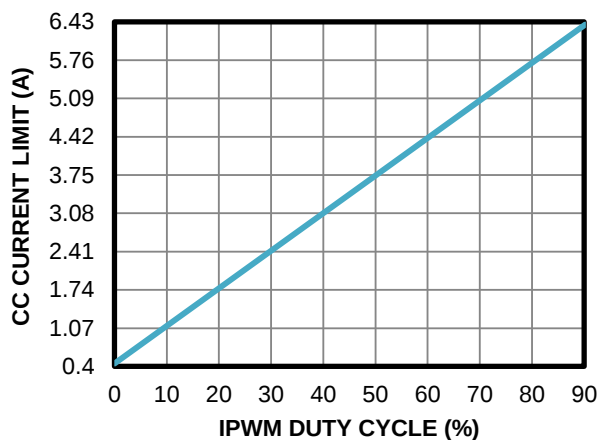
**Bode Plot**

$V_{OUT} = 20V$ ,  $I_{OUT} = 5A$ ,  $BW = 10 kHz$ ,  
PM = 54.907deg



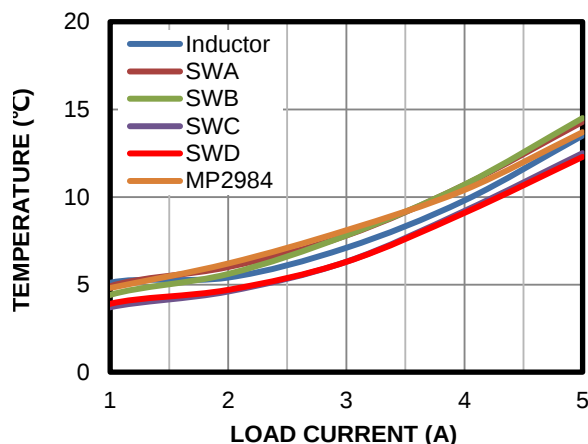
**Constant-Current Limit vs. IPWM Duty Cycle**

$I_{LIM} = 111$ ,  $R_{SENSE2} = 10m\Omega$



**Case Temperature Rise**

$V_{IN} = 12V$ ,  $V_{OUT} = 5V$ ,  $FSW$  bits = 10,  
tested on the EV2984-R-00B

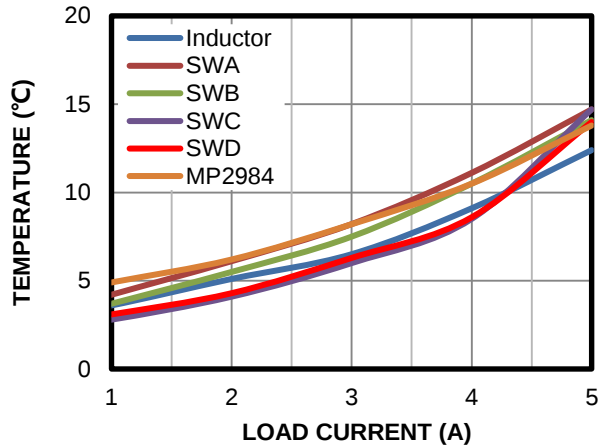


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

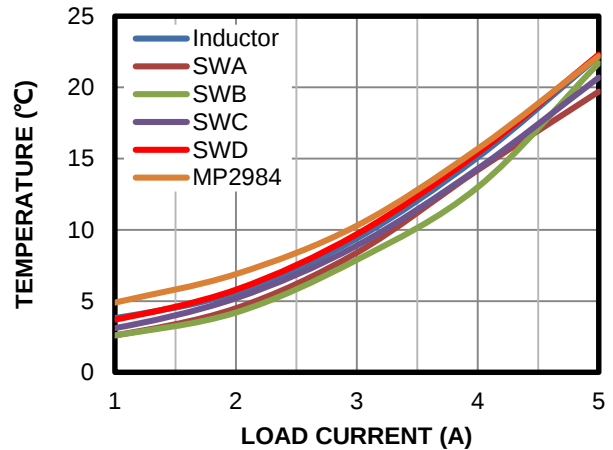
## Case Temperature Rise

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 9V, FSW bits = 10,  
tested on the EV2984-R-00B



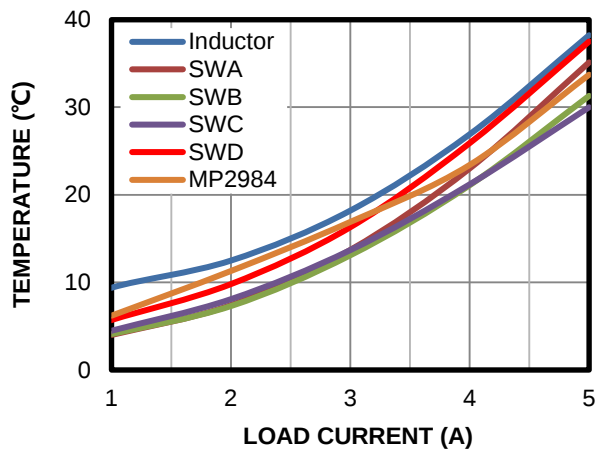
## Case Temperature Rise

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 15V, FSW bits = 10,  
tested on the EV2984-R-00B



## Case Temperature Rise

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 20V, FSW bits = 10,  
tested on the EV2984-R-00B

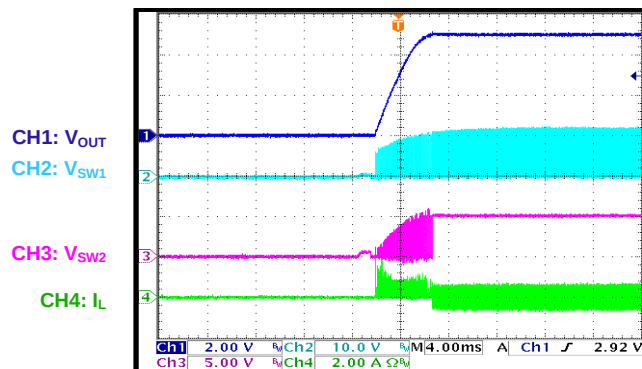


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

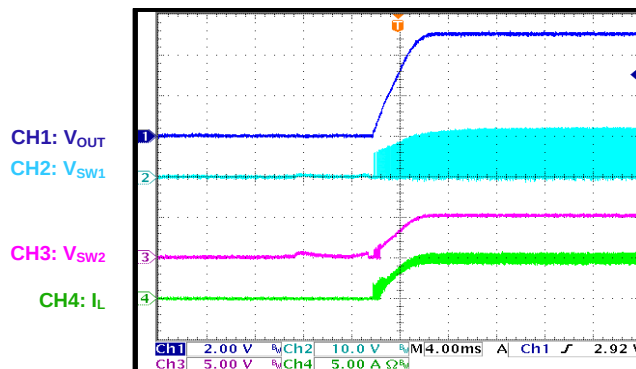
## Start-Up through VIN

I<sub>LOAD</sub> = 0A



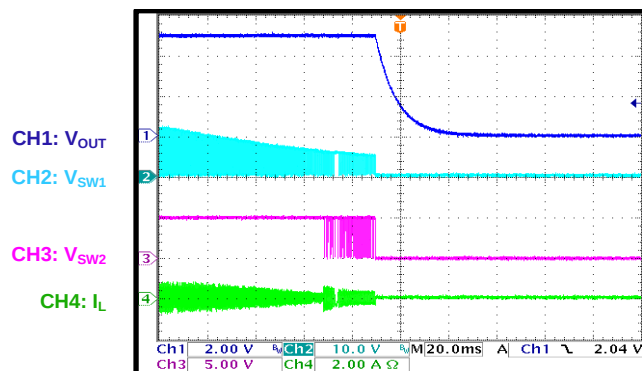
## Start-Up through VIN

I<sub>LOAD</sub> = 5A



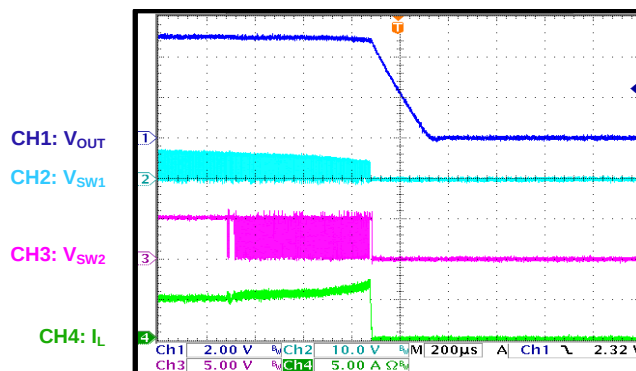
## Shutdown through VIN

I<sub>LOAD</sub> = 0A



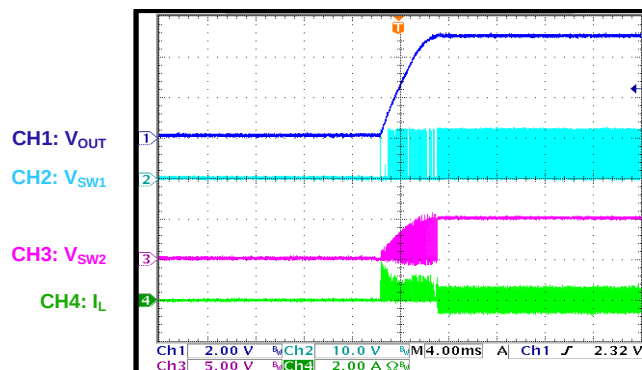
## Shutdown through VIN

I<sub>LOAD</sub> = 5A



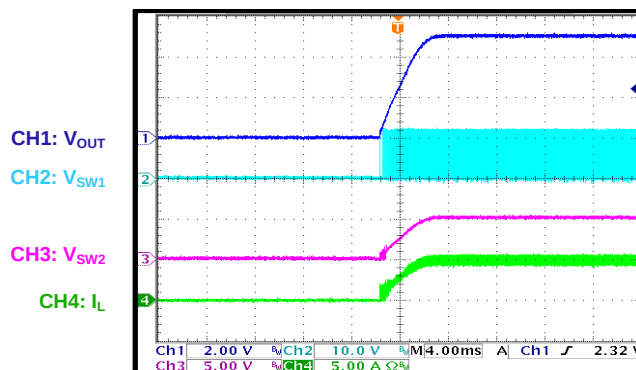
## ENPWR Enabled through the I<sup>2</sup>C

I<sub>LOAD</sub> = 0A



## ENPWR Enabled through the I<sup>2</sup>C

I<sub>LOAD</sub> = 5A



# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

## ENPWR Disabled through the I<sup>2</sup>C

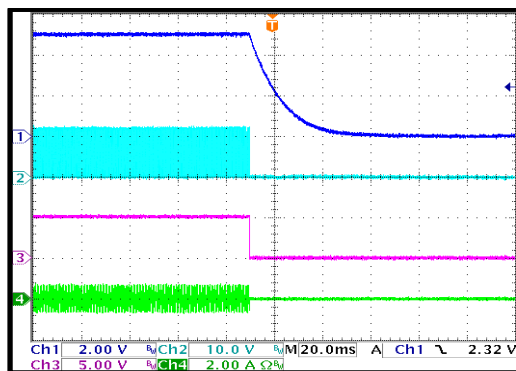
I<sub>LOAD</sub> = 0A

CH1: V<sub>OUT</sub>

CH2: V<sub>SW1</sub>

CH3: V<sub>SW2</sub>

CH4: I<sub>L</sub>



## ENPWR Disabled through the I<sup>2</sup>C

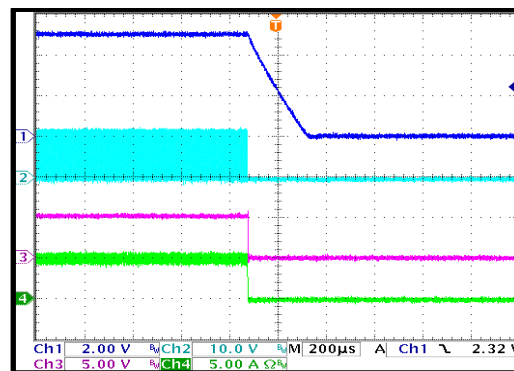
I<sub>LOAD</sub> = 5A

CH1: V<sub>OUT</sub>

CH2: V<sub>SW1</sub>

CH3: V<sub>SW2</sub>

CH4: I<sub>L</sub>



## Start-Up through EN

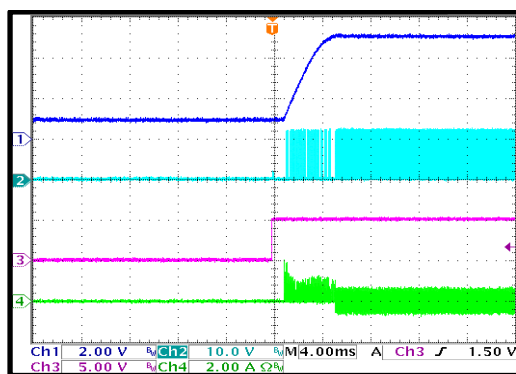
I<sub>LOAD</sub> = 0A

CH1: V<sub>OUT</sub>

CH2: V<sub>SW1</sub>

CH3: V<sub>SW2</sub>

CH4: I<sub>L</sub>



## Start-Up through EN

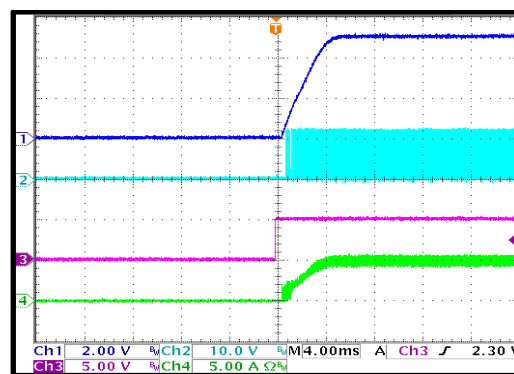
I<sub>LOAD</sub> = 5A

CH1: V<sub>OUT</sub>

CH2: V<sub>SW1</sub>

CH3: V<sub>SW2</sub>

CH4: I<sub>L</sub>



## Shutdown through EN

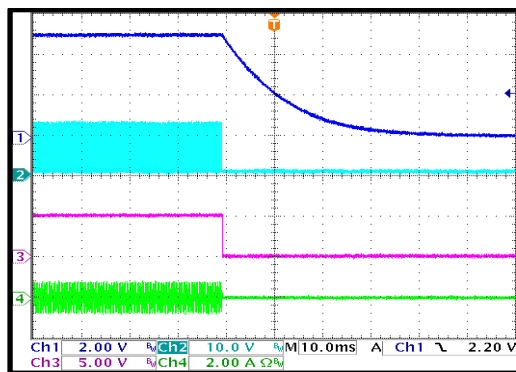
I<sub>LOAD</sub> = 0A

CH1: V<sub>OUT</sub>

CH2: V<sub>SW1</sub>

CH3: V<sub>SW2</sub>

CH4: I<sub>L</sub>



## Shutdown through EN

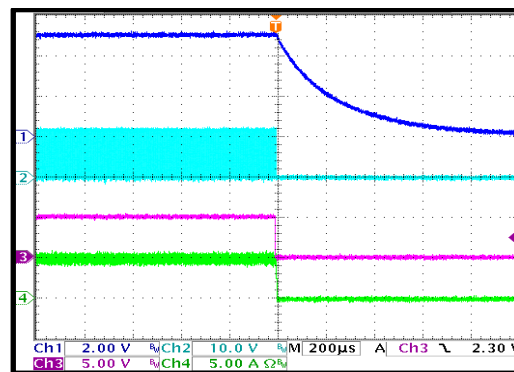
I<sub>LOAD</sub> = 5A

CH1: V<sub>OUT</sub>

CH2: V<sub>SW1</sub>

CH3: V<sub>SW2</sub>

CH4: I<sub>L</sub>

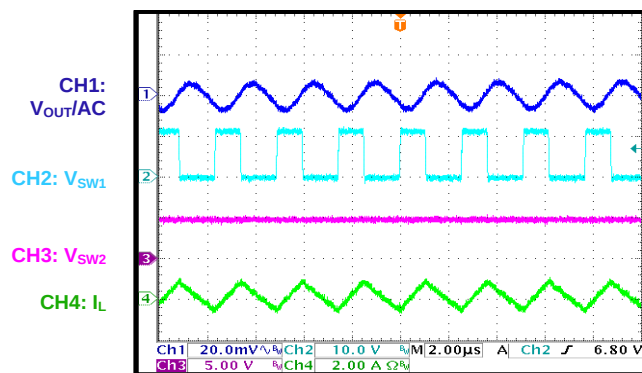


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

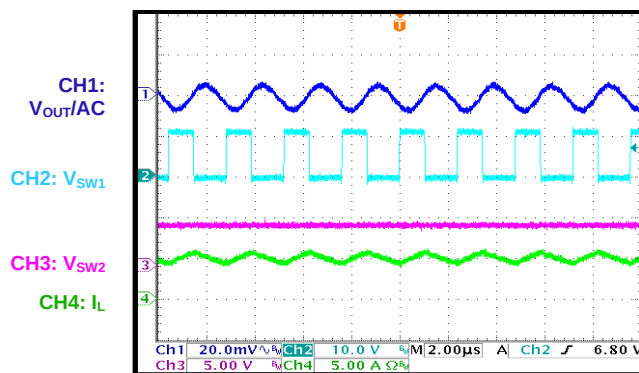
## Steady State

V<sub>OUT</sub> = 5V, I<sub>LOAD</sub> = 0A



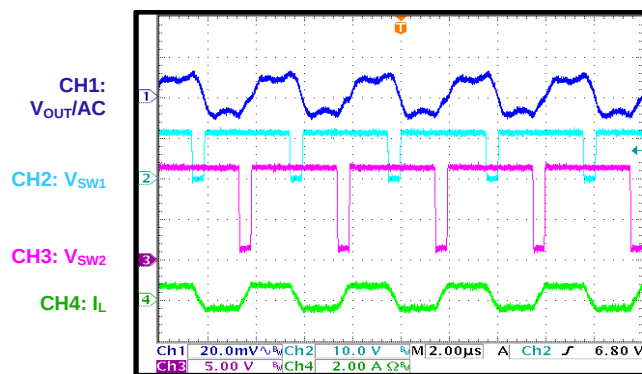
## Steady State

V<sub>OUT</sub> = 5V, I<sub>LOAD</sub> = 5A



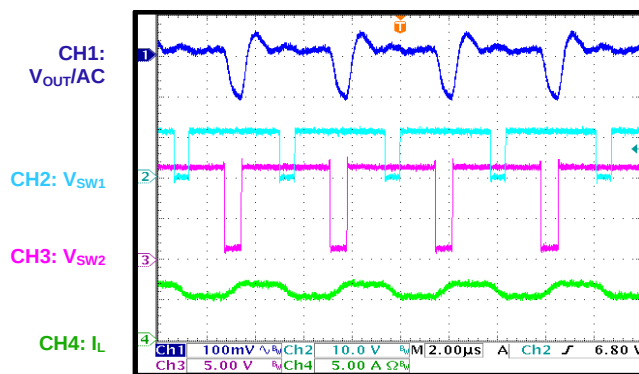
## Steady State

V<sub>OUT</sub> = 12V, I<sub>LOAD</sub> = 0A



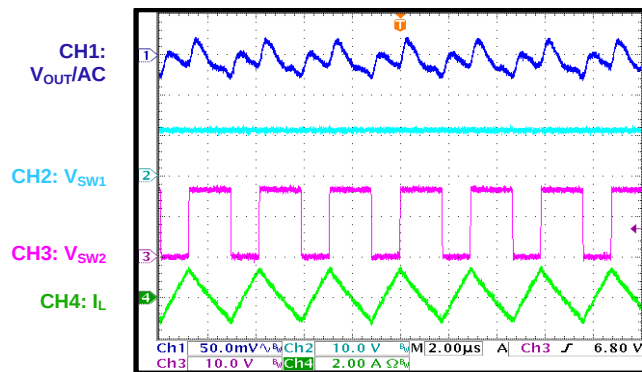
## Steady State

V<sub>OUT</sub> = 12V, I<sub>LOAD</sub> = 5A



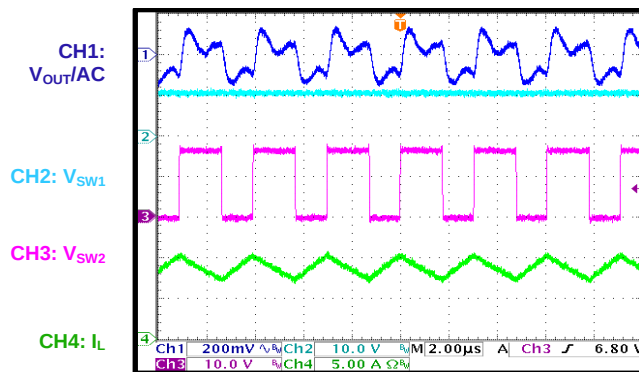
## Steady State

V<sub>OUT</sub> = 20V, I<sub>LOAD</sub> = 0A



## Steady State

V<sub>OUT</sub> = 20V, I<sub>LOAD</sub> = 5A

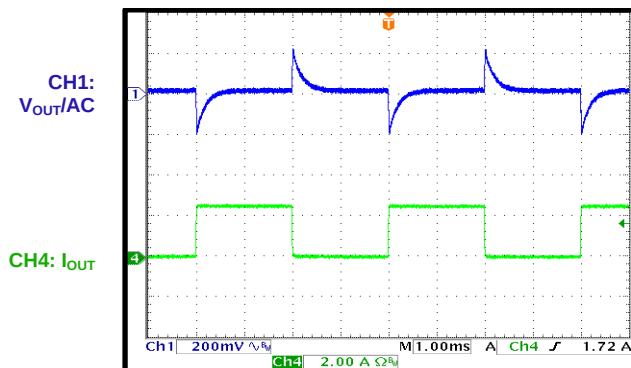


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

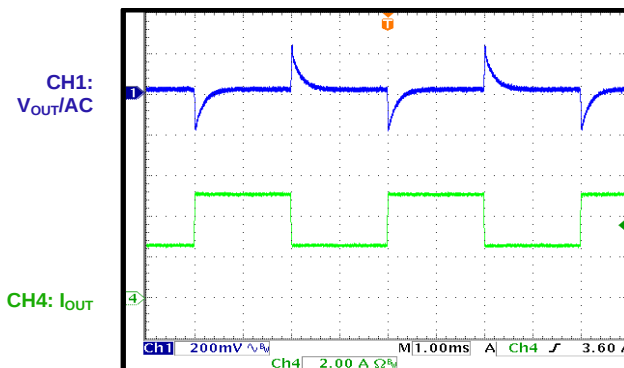
## Load Transient

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, I<sub>LOAD</sub> = 0A to 2.5A, 150mA/μs



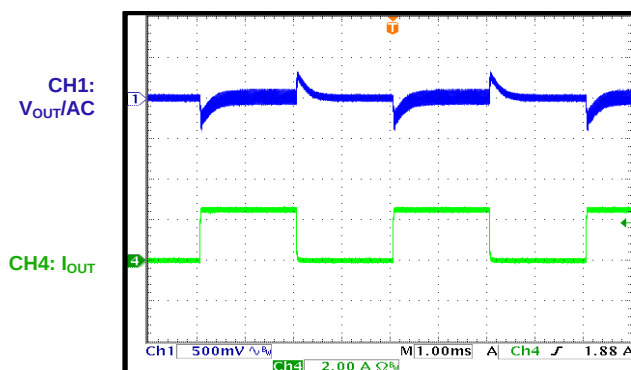
## Load Transient

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, I<sub>LOAD</sub> = 2.5A to 5A, 150mA/μs



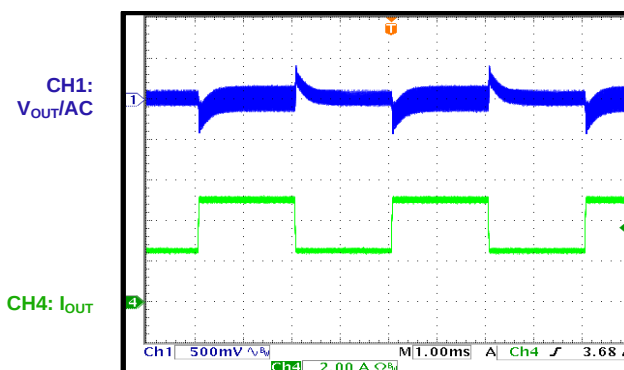
## Load Transient

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 20V, I<sub>LOAD</sub> = 0A to 2.5A, 150mA/μs



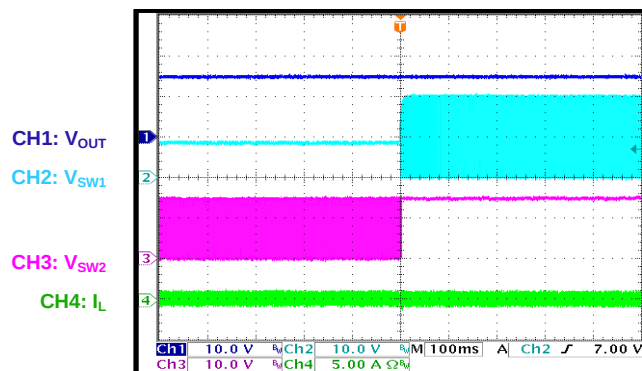
## Load Transient

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 20V, I<sub>LOAD</sub> = 2.5A to 5A, 150mA/μs



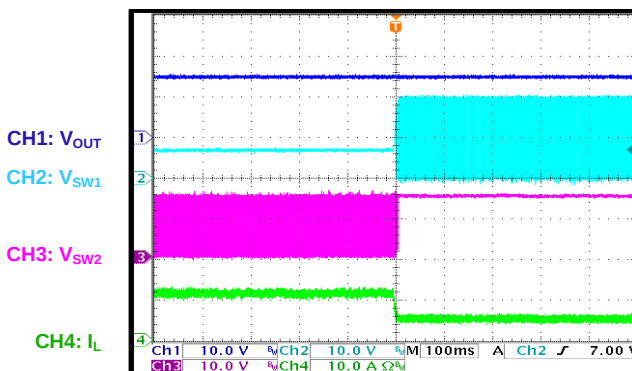
## V<sub>IN</sub> Transient

V<sub>IN</sub> = 9V to 20V, V<sub>OUT</sub> = 15V, I<sub>LOAD</sub> = 0A



## V<sub>IN</sub> Transient

V<sub>IN</sub> = 9V to 20V, V<sub>OUT</sub> = 15V, I<sub>LOAD</sub> = 5A

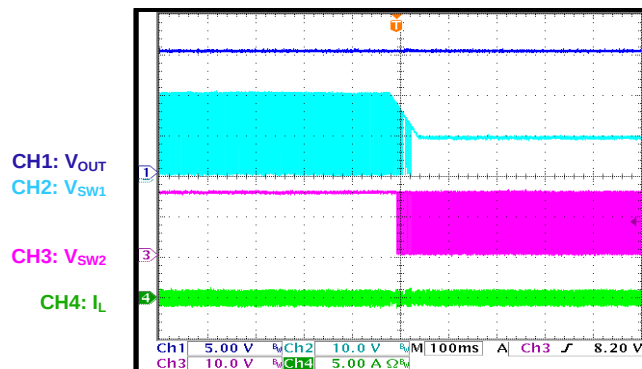


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

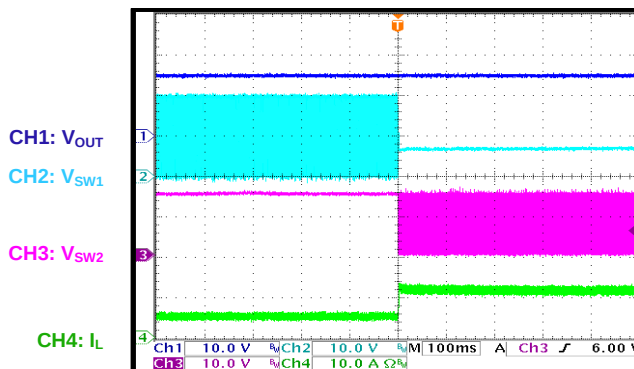
## V<sub>IN</sub> Transient

V<sub>IN</sub> = 9V to 20V, V<sub>OUT</sub> = 15V, I<sub>LOAD</sub> = 0A



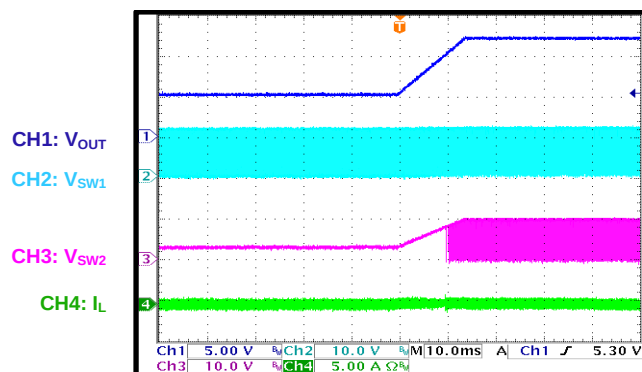
## V<sub>IN</sub> Transient

V<sub>IN</sub> = 20V to 9V, V<sub>OUT</sub> = 15V, I<sub>LOAD</sub> = 5A



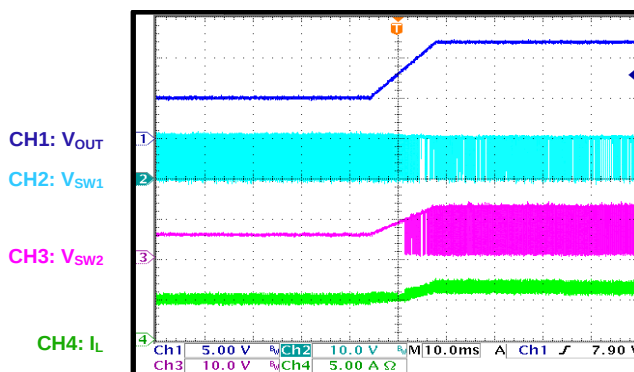
## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 5V to 12V, I<sub>OUT</sub> = 0A



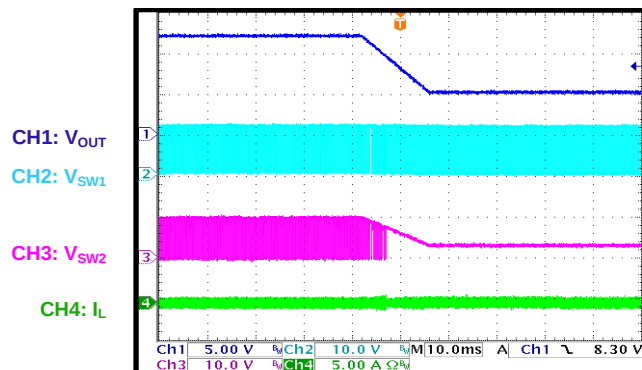
## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 5V to 12V, I<sub>OUT</sub> = 5A



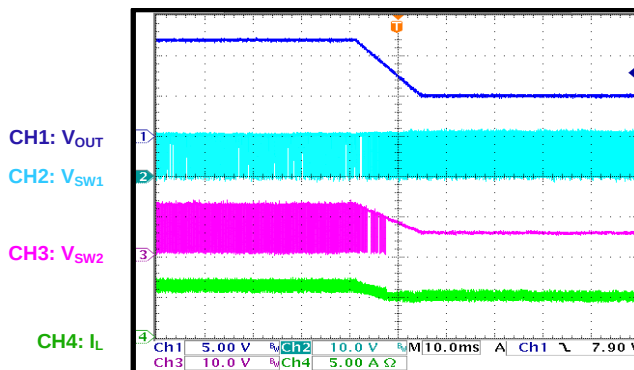
## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 12V to 5V, I<sub>LOAD</sub> = 0A



## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 12V to 5V, I<sub>LOAD</sub> = 5A

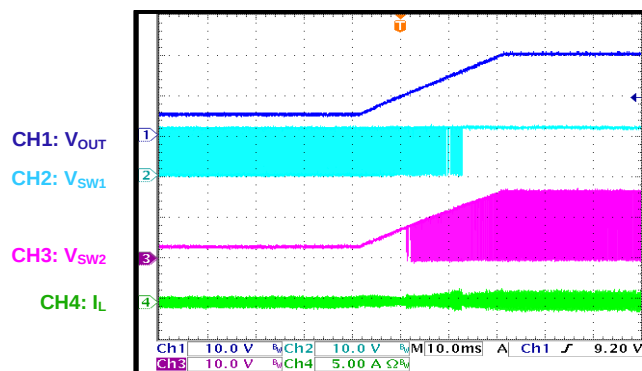


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

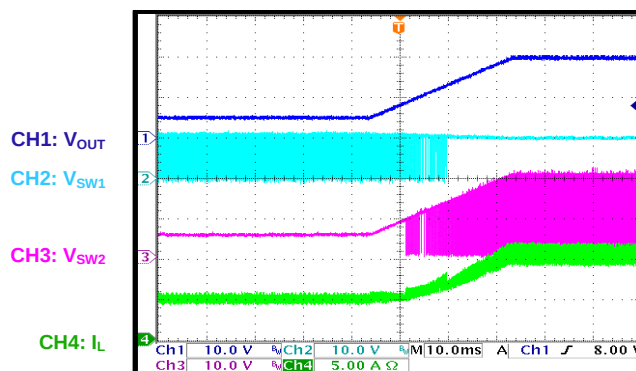
## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 5V to 20V, I<sub>LOAD</sub> = 0A



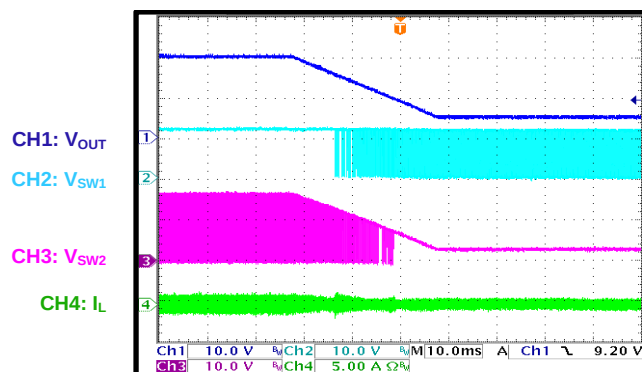
## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 5V to 20V, I<sub>LOAD</sub> = 5A



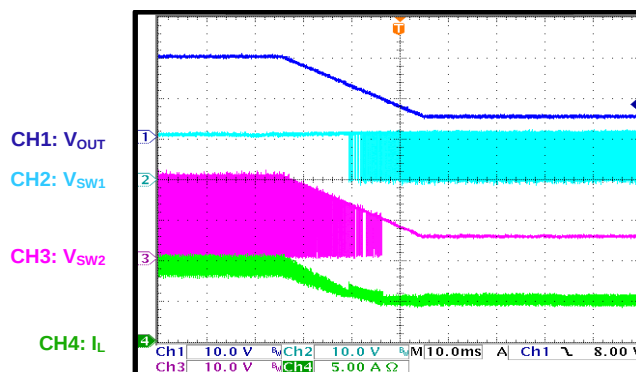
## V<sub>OUT</sub> Transient

V<sub>OUT</sub> = 20V to 5V, I<sub>LOAD</sub> = 5A

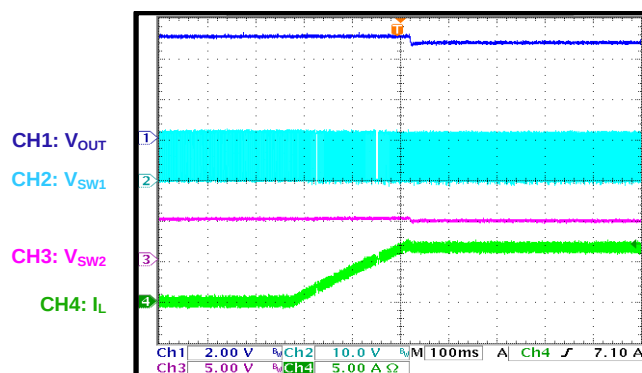


## V<sub>OUT</sub> Transient

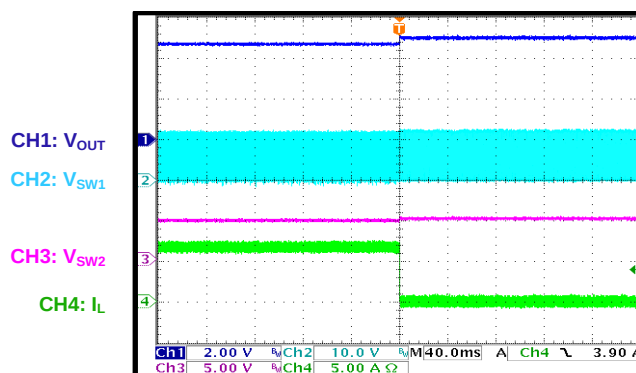
V<sub>OUT</sub> = 20V to 5V, I<sub>LOAD</sub> = 5A



## OCP Entry



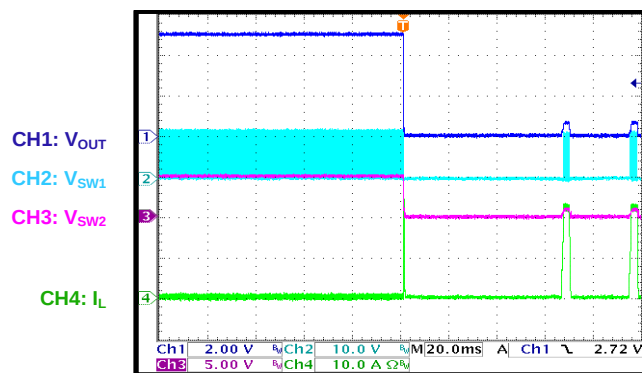
## OCP Recovery



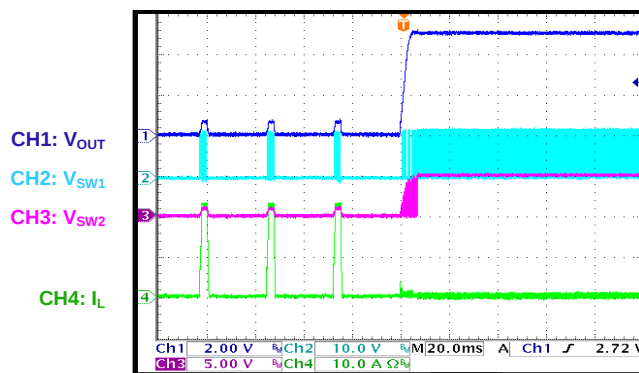
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V, L = 4.7μH, T<sub>A</sub> = 25°C, unless otherwise noted.

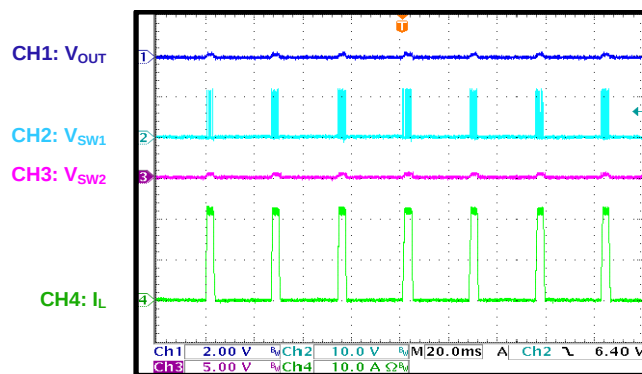
## SCP Entry



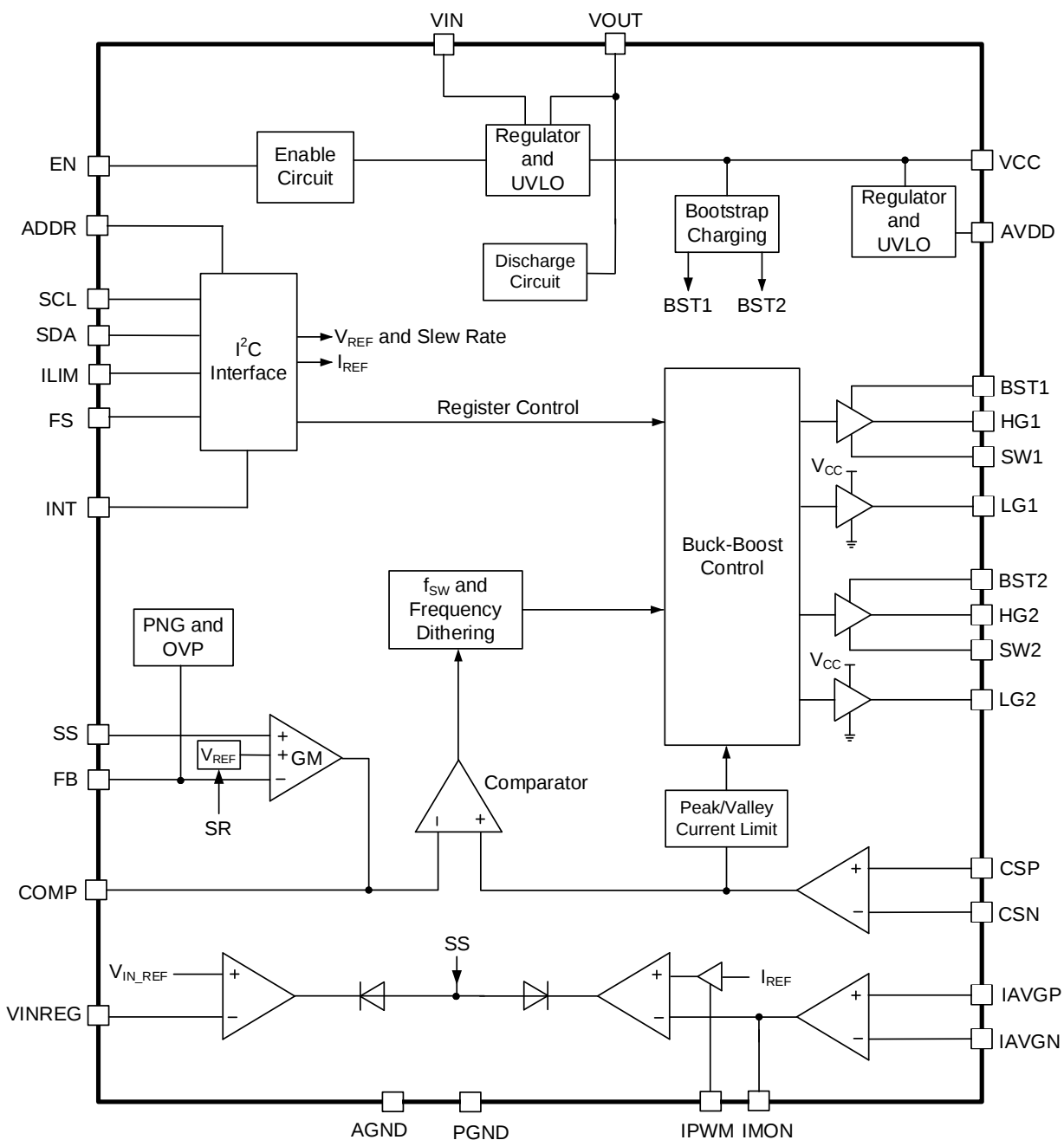
## SCP Recovery



## SCP Steady State



# FUNCTIONAL BLOCK DIAGRAM



**Figure 2: Functional Block Diagram**

## OPERATION

The MP2984 is a high-efficiency, quad-switch, synchronous buck-boost controller. The device operates with fixed frequency in buck mode, boost mode, and buck-boost mode. Buck-boost control provides high efficiency across the entire input voltage ( $V_{IN}$ ) range and smooth transient between modes.

### Buck-Boost Operation

The MP2984 can regulate outputs above, below, or equal to  $V_{IN}$ . Figure 3 shows a one-inductor, four-switch power structure buck-boost topology.

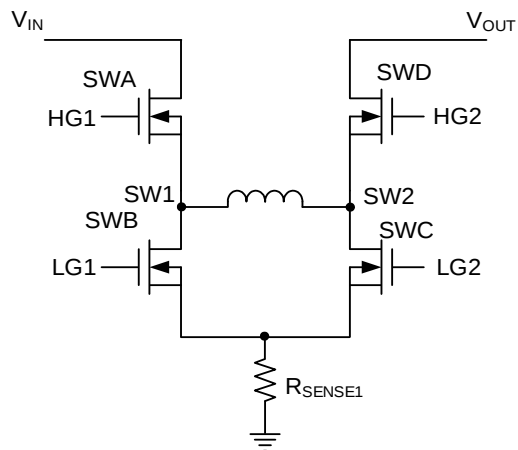


Figure 3: Buck-Boost Topology

In a buck-boost topology, the device can operate in buck mode, boost mode, or buck-boost mode with different  $V_{IN}$  inputs (see Figure 4).

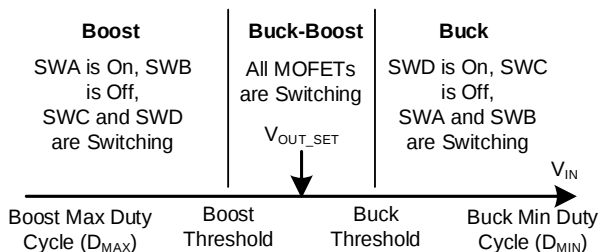


Figure 4: Buck-Boost Operating Range

### Buck Mode ( $V_{IN} > V_{OUT}$ )

If  $V_{IN}$  exceeds the output voltage ( $V_{OUT}$ ), the device operates in buck mode. The SWA and SWB MOSFETs are switching during buck regulation. The SWC MOSFET is off, and the SWD MOSFET remains on to conduct the inductor current ( $I_L$ ).

During each buck mode cycle, SWA turns on once the feedback (FB) voltage ( $V_{FB}$ ) drops below the reference voltage ( $V_{REF}$ ). Once SWA

turns off, SWB turns on to conduct  $I_L$  until  $I_L$  rises and triggers the COMP control signal. The converter regulates  $V_{OUT}$  by repeating this operation.

### Boost Mode ( $V_{IN} < V_{OUT}$ )

If  $V_{IN}$  drops below  $V_{OUT}$ , the device operates in boost mode. In boost mode, SWC and SWD switch during boost regulation. Once SWB is off, SWA remains on to conduct  $I_L$ .

In each boost mode cycle, SWC turns on to conduct  $I_L$  until  $I_L$  rises and triggers the COMP control signal. SWC turns off and SWD turns on during the current freewheel. Then SWC turns on and off repeatedly to regulate  $V_{OUT}$  in boost mode.

### Buck-Boost Mode ( $V_{IN} \approx V_{OUT}$ )

If  $V_{IN} \approx V_{OUT}$ , the converter cannot provide enough power to the load in buck mode due to SWA's minimum off time ( $t_{OFF\_MIN}$ ). Additionally, the converter can supply too much power to load in boost mode due to SWC's minimum on time ( $t_{ON\_MIN}$ ). Under these conditions, the MP2984 operates in buck-boost mode to regulate  $V_{OUT}$ . Figure 5 shows the buck-boost mode waveform.

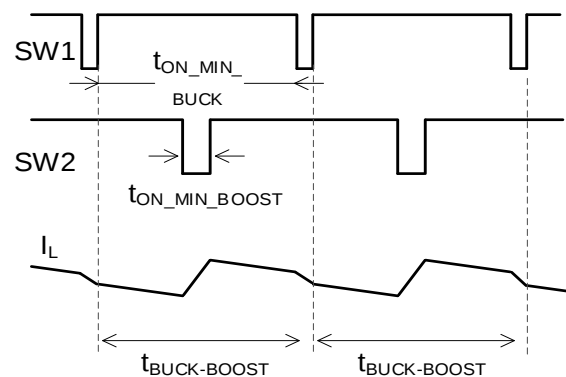


Figure 5: Buck-Boost Mode Waveform

If  $V_{IN} \approx V_{OUT}$ , then the device operates in buck-boost mode, and a boost switch is inserted during each buck switching period. The MOSFET start-up sequence is described below:

1. SWA and SWD start up.
2. SWA and SWC start up.
3. SWA and SWD start up.
4. SWB and SWD start up.
5.  $I_L$  reaches the COMP voltage ( $V_{COMP}$ ), and can supply enough current to the output.

## Power Supply

The MP2984's internal circuit is powered by AVDD (5.2V). The gate drivers are powered by VCC (7.2V). V<sub>IN</sub> and V<sub>OUT</sub> regulate the VCC voltage (V<sub>CC</sub>). VCC powers the AVDD voltage (V<sub>AVDD</sub>).

If V<sub>IN</sub> is supplied and V<sub>EN</sub> is high, the MP2984 regulates V<sub>CC</sub> at 7.2V and V<sub>AVDD</sub> to 5.2V. If V<sub>AVDD</sub> exceeds the UVLO threshold and ENPWR is high, then the part starts switching and regulates V<sub>OUT</sub> via soft-start control. If V<sub>IN</sub> and V<sub>OUT</sub> both exceed 8.8V, VCC is powered by the lower of the two voltage sources to reduce power loss. Otherwise, VCC is powered by the higher voltage power source to ensure that there is enough V<sub>CC</sub>. The VCC and BST pins have separate UVLO protections that keeps the gate signal off. Ensure that VCC and BST have enough voltage to restart the part after UVLO is triggered. This does not apply to AVDD UVLO.

The MP2984 operates from a wide 6V to 36V V<sub>IN</sub> range. If VCC is powered by V<sub>OUT</sub> after start-up, the part operates until V<sub>IN</sub> drops below 5V.

If the device is shut down through AVDD\_UVLO or the EN signal, then the I<sup>2</sup>C interface cannot respond to the host and COMP is pulled low. The V<sub>CC</sub>, V<sub>AVDD</sub>, and the bootstrap (BST) voltage (V<sub>BST</sub>) drop slowly with leakage, and all logic is off.

## Start-Up

The MP2984 initiates soft start (SS) to start-up the IC. The soft-start circuit charges the SS pin, and the soft-start voltage (V<sub>SS</sub>) ramps up slowly from 0V. The soft-start current (I<sub>SS</sub>) is then fed to the error amplifier (EA) to control V<sub>OU</sub>. After V<sub>SS</sub> exceeds V<sub>REF</sub> (set by the VREF bits), SS is complete, and the part enters closed-loop regulation. In steady state, V<sub>SS</sub> should rise and clamp at 0.6V > V<sub>REF</sub>, unless a protection has been triggered.

After start-up, the MP2984 typically enables buck switching since V<sub>OUT</sub> is lower than V<sub>IN</sub>. If there is a V<sub>OUT</sub> voltage bias, the part should not switch until V<sub>SS</sub> exceeds V<sub>FB</sub>. V<sub>FB</sub> is proportional to the V<sub>OUT</sub> voltage bias. During SS, the IC operates in automatic pulse-width modulation (PFM) mode. Over-voltage protection (OVP) and over-current protection (OCP) with hiccup mode are not functional during SS.

## Enable (EN) and Configurable Under-Voltage Lockout (UVLO) Protection

The EN pin enables and disables the MP2984. If the EN voltage (V<sub>EN</sub>) exceeds its high threshold (>1.1V), then some of the MP2984's internal circuitry starts up. This is called micro-power mode. If V<sub>EN</sub> exceeds its start-up threshold (1.35V), then the IC starts up and all functions are enabled. If V<sub>EN</sub> drops below its low threshold (<1.28V), switching is disabled.

If V<sub>EN</sub> drops below 0.4V, the MP2984 shuts down. After shutdown, the part sinks a small current from the input power (typically <1μA). EN is compatible with voltages up to 40V. For automatic start-up, connect the EN and VIN pins. During EN shutdown, the I<sup>2</sup>C interface resets to its default value after a 200ms discharge time (t<sub>DISCHARGE</sub>).

The MP2984 features a configurable UVLO hysteresis. During start-up, the EN pin sources a 4.7μA current (see Figure 6) once V<sub>EN</sub> exceeds 1.35V. V<sub>IN</sub> has to decrease in order to overcome the current source and to stop switching after the IC starts up. The V<sub>IN</sub> switching turn-on threshold (see Figure 6) can be calculated with Equation (1):

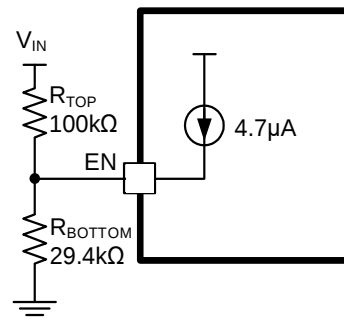
$$V_{IN\_ON}(V) = V_{EN\_ON}(V) \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) = 5.95V \quad (1)$$

The V<sub>IN</sub> switching turn-off threshold be calculated with Equation (2):

$$V_{IN\_OFF}(V) = V_{EN\_OFF}(V) \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) - 4.7\mu A \quad (2)$$

$$\times R_{TOP}(k\Omega) \div 1000 = 5.16V$$

Where V<sub>EN\_ON</sub> is about 1.35V (typically), and V<sub>EN\_OFF</sub> is about 1.28V.



**Figure 6: Configurable V<sub>IN</sub> UVLO**

## Forced Continuous Conduction Mode (FCCM)

The MP2984 can operate in forced continuous conduction mode (FCCM). The buck on time ( $t_{ON\_BUCK}$ ) and boost off time ( $t_{OFF\_BOOST}$ ) are determined by an internal circuit. This is to have the part operate with a fixed switching frequency ( $f_{SW}$ ), based on the  $V_{IN} / V_{OUT}$  ratio. If the load decreases, then the input current ( $I_{LIMIT}$ ) drops, which may cause  $I_L$  to go negative from  $V_{OUT}$  to  $V_{IN}$  during SWD's on time ( $t_{ON}$ ). This forces  $I_L$  to operate with a fixed  $f_{SW}$  in FCCM, which produces a low  $V_{OUT}$  ripple.

## Switching Current Limit

The MP2984 senses the LS-FET current through a current-sense resistor ( $R_{SENSE1}$ ) in the loop control. This allows the device to provide valley current limiting in buck mode and peak current limiting in boost mode, during each cycle-by-cycle switching period. In buck mode, the next period does not start until  $I_L$  drops to the valley current limit, so the device may fold back the frequency when the valley current limit is triggered. The buck current limit is fixed at 133mV and the boost current limit is fixed at 150mV. For example, if  $R_{SENSE1} = 5m\Omega$ , the buck current limit is  $133mV/5m\Omega = 26.6A$ , and the boost current limit is  $150mV/5m\Omega = 30A$ .

The switching current limit can be configured by the external sense resistor. The SWB and SWC current signal is internally blanked for about 180ns to enhance noise rejection.

Under over-current (OC) conditions, the MP2984 runs with a cycle-by-cycle current limit. The device may initiate hiccup protection or a latch-off protection based on OCP\_MODE.

In hiccup mode, the device turns off once  $V_{FB}$  drops below 60% of  $V_{REF}$ , and triggers the switching current limit after the SS period. The device recovers after a fixed off time, which is configured by the SS capacitor discharge period.

In latch-off mode, the MP2984 turns off if  $V_{FB}$  drops below 60% of  $V_{REF}$ , and triggers the switching current limit after the SS period. The device recovers after the next power cycle.

If hiccup and latch-off protection are disabled, the device continues switching with the cycle-by-cycle current limit. Hiccup and latch-off protections are masked during soft start.

## Average Current Limit

The IAVGP and IAVGN pins sense the output current. A current-sense resistor ( $R_{SENSE2}$ ) can be connected to the VOUT line to control the average output current limit. Once the sensed signal exceeds the current limit reference voltage, one internal EA pulls down  $V_{SS}$ . Eventually,  $V_{SS}$  replaces  $V_{REF}$  to control COMP instead of  $V_{REF}$ , and the inductor current is limited by COMP to transfer less energy to output. The SS pin keeps  $V_{OUT}$  low until the average load current drops.

If the switching current is regulated by the average current limit, and it does not trigger a cycle-by-cycle current limit, the MP2984 does not run hiccup or latch-off protection, even if the average current limit is reached. This allows the device to maintain a constant current charge.

The ILIM bits provide 8 selectable current limits, and the external IPWM pin provides high-resolution current limit adjusting.

If the IPWM pin is high or floating, the average output current limit is determined by both ILIM bits setting and  $R_{SENSE2}$ .

Another method to set the average output current limit is by multiplying the value set by the ILIM bit by the IPWM duty cycle. When the ILIM bits are set to 111 and the current limit is configured by the IPWM pin, the current limit threshold (OCP\_LIMIT) can be calculated with Equation (3):

$$OCP\_LIMIT (mV) = 65.8mV \times DUTY + 4.49mV \quad (3)$$

Where OCP\_LIMIT is the average load current limit configured by the IPWM pin (when the ILIM bits = 111), and DUTY is IPWM pin input signal duty cycle, which can be between 0 and 0.9.

The real output current limit (in A) is determined by  $OCP\_LIMIT / R_{SENSE2}$ .

For example, if the IPWM signal duty cycle is 48%, the final average output current limit is about 36mV. The IPWM signal frequency can be between 5kHz and 100kHz. It is recommended to have a 20kHz frequency signal. For USB PD applications, it is recommended for  $R_{SENSE2}$  to be 10m $\Omega$ .

## Overload Protection (OLP) and Short-Circuit Protection (SCP)

If an overload (OL) fault occurs, the MP2984 limits  $I_{OUT}$  via  $I_{LIMIT}$  loop regulation. If the  $I_{LIMIT}$  is disabled, then  $I_{OUT}$  is limited cycle-by-cycle. If the IC is operating in boost mode during cycle-by-cycle current limiting, then the SWC peak current ( $I_{PEAK}$ ) is limited. If the IC is operating in buck mode, then SWB remains on until  $I_L$  reaches  $I_{LIMIT\_VALLEY}$ . The next cycle begins once  $I_L$  reaches  $I_{LIMIT\_VALLEY}$ . Therefore,  $I_L$  can be controlled in all operation modes.

### Output Voltage Regulation

The MP2984 regulates  $V_{OUT}$  via the FB pin.  $V_{FB}$  is compared to the internal  $V_{REF}$ .  $V_{REF}$  can be between 300mV to 2.047V, depending on the VREF register bit settings. The EA output on COMP controls  $I_L$  to  $V_{OUT}$ .

### Switching Frequency ( $f_{SW}$ ) and Frequency Spread Spectrum (FSS)

The MP2984 configures the switching frequency ( $f_{SW}$ ) via the 2-bit FSW register.  $f_{SW}$  can be set to 200kHz, 300kHz, 400kHz, or 600kHz via the 2-bit FSW register. For most applications, it is recommended to set  $f_{SW}$  to 400kHz.

The MP2984 features frequency spread spectrum (FSS) and frequency dithering. Set the Dither bit to 1 (0x02h, bit D[4]) to enable FSS and frequency dithering. Set the Dither bit = 0 to disable FSS and frequency dithering. FSS reduces the peak emissions at certain frequencies.

The MP2984 uses a 2kHz triangle wave to modulate the internal oscillator. The frequency span of the spread spectrum is  $\pm 6\%$ .

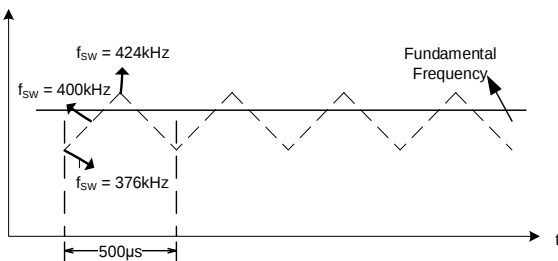


Figure 7: Frequency Spread Spectrum

FSS can operate with a 200kHz, 300kHz, 400kHz, or 600kHz  $f_{SW}$ .

### Gate Driver and Bootstrap (BST) Power

The MP2984 provides four N-channel power MOSFET gate drivers for the H-bridge MOSFETs (see Figure 3 on page 24). Each driver is capable of sourcing and sinking currents. In buck mode, LG1 and HG1 are switching while HG2 remains on. In boost mode, LG2 and HG2 are switching while HG1 remains on. LG1 and LG2 are powered by  $V_{CC}$ , while HG1 and HG2 are powered by  $V_{BST1}$  and  $V_{BST2}$ .

Capacitors between BST1 and SW1, as well as BST2 to SW2 are necessary to supply power, which can be supplied via an internal diode from VCC or from charging each other.

### Over-Voltage Protection (OVP)

The MP2984 monitors the feedback voltage ( $V_{FB}$ ). If  $V_{FB}$  exceeds 127% of  $V_{REF}$  and the OVP\_MODE bits are set to 01, then the IC discharges the output capacitor ( $C_{OUT}$ ) via an internal discharge resistor. Discharging stops once  $V_{FB}$  drops to 111% of the regulation voltage. If the OVP\_MODE bits are set to 00, then there is no logic available to stop switching, even if  $V_{FB}$  is above the OVP threshold. If the OVP\_MODE bits are set to 10, the IC latches off once  $V_{OUT}$  reaches 127% of  $V_{REF}$ .

### Interrupt (INT)

The interrupt (INT) pin is an open-drain output that indicate an interrupt signal for the following fault conditions : over-current fault (OC), over-voltage (OV) fault, over-temperature (OT) fault, and  $V_{OUT}$  is not within its normal range.

If OCP, output OVP, or thermal shutdown is triggered, the corresponding register bit (OCP, bit D[1], OVP, bit D[2], or OTP, bit D[4]) is set to 1. INT pulls low to indicate an interrupt signal, depending on the related mask register setting. If the device is off, then INT is an open drain.

### Current Monitor Output (IMON)

The MP2984 senses the average  $I_{LOAD}$  via a current-sense resistor, and outputs a voltage signal on the IMON pin. The signal is amplified by the voltage difference between the IAVGP and IAVGN pins ( $V_{IAVGP} - V_{IAVGN}$ ). Connect a small capacitor connected between the IMON and AGND pins. The IMON voltage ( $V_{IMON}$ ) can be calculated with Equation (4):

$$V_{IMON} \text{ (mV)} = \text{Gain} \times I_{OUT} \text{ (A)} \times R_{SENSE2} \text{ (m}\Omega\text{)} \quad (4)$$

Where Gain is typically 18.8mV/V, and  $R_{SENSE2}$  is the average load's current-sense resistor.

### Configurable Soft-Start Time ( $t_{SS}$ )

The SS pin sets the soft-start time ( $t_{SS}$ ).  $t_{SS}$  can be estimated with Equation (5):

$$t_{SS} \text{ (ms)} = C_{SS} \text{ (nF)} \times V_{REF} \text{ (V)} / I_{SS} \text{ (}\mu\text{A)} \quad (5)$$

Where the  $I_{SS}$  charge current is about 6 $\mu$ A, the soft-start capacitor ( $C_{SS}$ ) is 47nF, and  $V_{REF}$  is 0.5V. This means that  $t_{SS}$  is about 3.9ms.

### Slew Rate Control and Output Discharge

The internal SR bits set the  $V_{OUT}$  slew rate. Four The  $V_{REF}$  slew rate (rising and falling) can be set to 38mV/ms, 50mV/ms, 75mV/ms, or 150mV/ms.

During voltage transient, the discharge path is function once GO\_BIT is set to 1. The discharge path is disabled once GO\_BIT resets to 0 (e.g. after the  $V_{REF}$  change is complete). If  $V_{OUT}$  is not discharged to the target voltage before the  $V_{REF}$  change is complete (e.g. due to a large  $C_{OUT}$ ), then the OVP discharge function or the DISCHG bit can be used to continue discharging  $V_{OUT}$ .

$V_{OUT}$  can be discharged via the following:

- GO\_BIT = 1. The discharge path is enabled, then GO\_BIT resets to 0 after a 20ms delay.
- The DISCHG bit = 1.
- OVP\_MODE bits = 01, and  $V_{FB}$  exceeds 127% of  $V_{REF}$ .
- The ENPWR bit is off. The discharge path is enabled for 200ms.
- The EN pin is off. The discharge path is enabled for 200ms.
- If  $V_{IN}$  UVLO protection is triggered and some residual  $V_{AVDD}$  remains, then the discharge path is enabled for 200ms. This discharge path may be disabled if the  $V_{AVDD}$  drops.

### Current Limit Control (ILIM)

During start-up, the ILIM pin status is latched to the register status, and the ILIM pin sets the default ILIM bit values. After start-up, the pin status change should not affect the register status, unless the pin status is changed or the part shuts down.

### Frequency Control (FS)

During start-up, the FS pin status is latched to the register status, and the FS pin sets the

default FSW bit values. After start-up, the pin status change should not affect the register status, unless the pin status is changed or the part shuts down.

### V<sub>IN</sub> Regulation Loop (VINREG)

The VINREG pin sets the minimum operating  $V_{IN}$ . If  $V_{IN}$  drops to the set voltage level, then SS is pulled down to decrease  $I_{OUT}$  and maintain  $V_{IN}$ . If  $V_{IN}$  drops below the VINREG threshold, the IC stops converting power to  $V_{OUT}$ .

### Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures. If the junction temperature ( $T_J$ ) exceeds 150°C, then the MP2984 shuts down. Once  $T_J$  drops below 125°C, then the IC initiates a SS to resume normal operation. If thermal shutdown is triggered and the INT pin is not masked, the INT pin is pulled low.

### I<sup>2</sup>C Interface

The I<sup>2</sup>C interface has four device addresses (defined as 1100xxx) that are set via a resistor divider between the ADDR and AVDD pins. This address is 7 bits long, and is followed by an 8th read/write (R/W) data direction bit. A 1 indicates a read (R) command, and a 0 indicates a write (W) command (R = 1 and W = 0). The 7-bit address acts as a slave address, and can support both standard mode (100kbps) communication and fast mode (400kbps) communication.

Table 1 shows the configurable device address settings. The ADDR pin also affects the ENPWR bit default value.

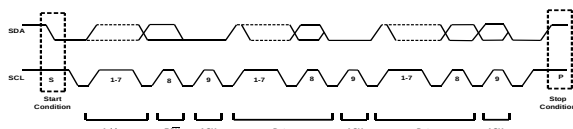
**Table 1: Device Address Setting**

| Device Address    | R <sub>TOP</sub> | R <sub>BOT</sub> | Default ENPWR |
|-------------------|------------------|------------------|---------------|
| 60h<br>(1100 000) | -                | 0 $\Omega$       | 1             |
| 62h<br>(1100 010) | 100k $\Omega$    | 59k $\Omega$     | 1             |
| 64h<br>(1100 100) | 68k $\Omega$     | 100k $\Omega$    | 0             |
| 66h<br>(1100 110) | 0 $\Omega$       | -                | 0             |

For more details, see I<sup>2</sup>C Registers section on page 31.

## I<sup>2</sup>C Data Transfer

Every byte on the SDA line should be 8 bits long. Each byte should be followed by an acknowledge (ACK) bit. The ACK clock pulse is generated by the master address. The transmitter releases the SDA line (SDA = high) during the ACK clock pulse. The SDA line is pulled down by the receiver during the ACK clock pulse to stabilize the SDA line (SDA = low) during the high period of this clock pulse.



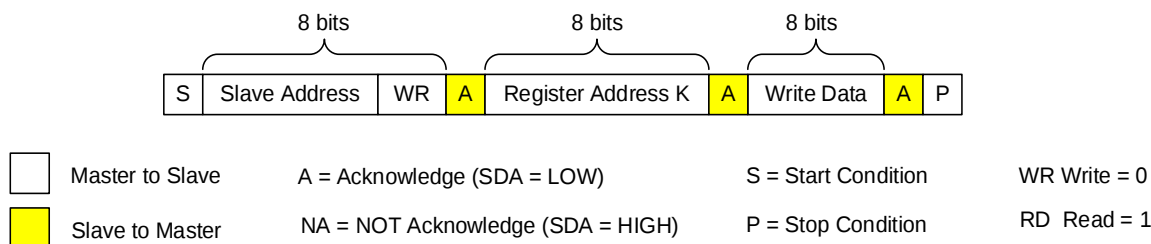
**Figure 8: Complete Data Transfer**

Figure 8 shows the complete data transfer format. After a start (S) condition, a slave address is sent. This address is 7 bits long, and is followed by an 8th data direction bit (R/W). A

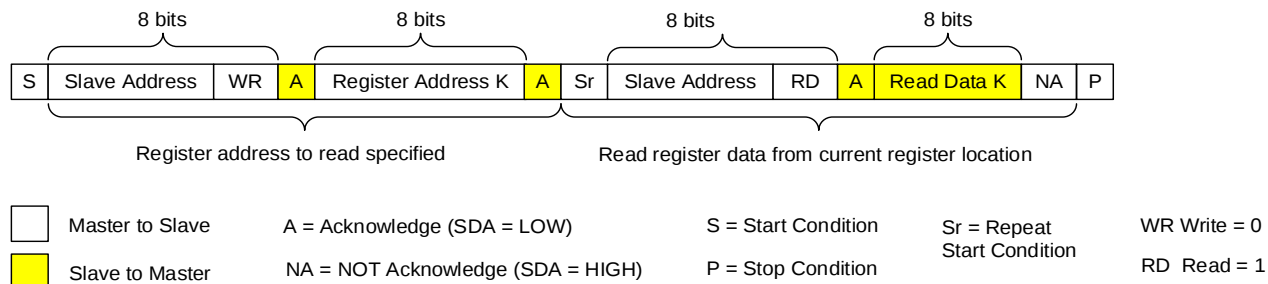
0 indicates a transmission (W), and a 1 indicates a request for data (R). A data transfer is always terminated by a stop (P) condition, which is generated by the master. If a master needs to communicate on the bus, then the master can generate a repeated start (S) condition and address another slave without having to generate a stop (P) condition.

The MP2984 includes a full I<sup>2</sup>C slave controller. The I<sup>2</sup>C slave complies with the I<sup>2</sup>C specification requirements. For a single data updated, the I<sup>2</sup>C slave requires a start (S) condition, valid I<sup>2</sup>C address, register address byte, and data byte. After receiving each byte, the MP2984 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the MP2984. The MP2984 then performs an update on the falling edge of the LSB byte.

Figure 9 and Figure 10 show examples of the I<sup>2</sup>C read and write commands.



**Figure 9: I<sup>2</sup>C Write Example**



**Figure 10: I<sup>2</sup>C Read Example**

## REGISTER DESCRIPTION

### Register Map

| Address | Register         | Type | D7     | D6  | D5     | D4     | D3        | D2                       | D1       | D0    | Reset State               |
|---------|------------------|------|--------|-----|--------|--------|-----------|--------------------------|----------|-------|---------------------------|
| 0x00    | REF_LSB          | R/W  | N/A    | N/A | N/A    | N/A    | N/A       | VREF_L                   |          |       | 0000 0100                 |
| 0x01    | REF_MSB          | R/W  | VREF_H |     |        |        |           |                          |          |       | 0011 1110                 |
| 0x02    | CONTROL_1        | R/W  | SR     |     | DISCHG | DITHER | PNG_LATCH | RESERVED <sup>(10)</sup> | GO_BIT   | ENPWR | 0100 010x <sup>(11)</sup> |
| 0x03    | CONTROL_2        | R/W  | FSW    |     | N/A    | BB_FSW | OCP_MODE  |                          | OVP_MODE |       | xx00 0101 <sup>(11)</sup> |
| 0x04    | ILIM             | R/W  | N/A    | N/A | N/A    | N/A    | N/A       | ILIM                     |          |       | 0000 1xxx <sup>(11)</sup> |
| 0x05    | INTERRUPT_STATUS | R/W  | N/A    | N/A | N/A    | OTP    | CC        | OVP                      | OCP      | PNG   | 0000 0000                 |
| 0x06    | INTERRUPT_MASK   | R/W  | N/A    | N/A | N/A    | M_OTP  | M_CC      | M_OVP                    | M_OCP    | M_PNG | 0000 0001                 |

#### Notes:

10) Reserved bits should not be set to a different value in application.

11) "x" means the value is determined by the external pin set during start-up. Refer to below register function description for details.

### Feedback Reference Data Format<sup>(12)</sup>

| Name           | VREF                            |    |    |    |    |                     |     |     |     |     |     |     |     |                     |     |     |
|----------------|---------------------------------|----|----|----|----|---------------------|-----|-----|-----|-----|-----|-----|-----|---------------------|-----|-----|
| Format         | Direct, unsigned binary integer |    |    |    |    |                     |     |     |     |     |     |     |     |                     |     |     |
| Register Name  | N/A                             |    |    |    |    | VREF_H, bits D[7:0] |     |     |     |     |     |     |     | VREF_L, bits D[2:0] |     |     |
| Bit            | 15                              | 14 | 13 | 12 | 11 | 10                  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2                   | 1   | 0   |
| Access         | N/A                             |    |    |    |    | R/W                 | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W                 | R/W | R/W |
| Function       | N/A                             |    |    |    |    | Data bit is high    |     |     |     |     |     |     |     | Data bit is low     |     |     |
| Default (0.5V) | N/A                             |    |    |    |    | 500 integer         |     |     |     |     |     |     |     |                     |     |     |

#### Note:

12) There are 11 bits that can set V<sub>REF</sub>. If V is an 11-bit, unsigned binary integer of VREF, bits[10:0], then V<sub>FB</sub> = V / 1000.

## I<sup>2</sup>C REGISTERS

### Register 0x00: REF\_LSB (Read/Write)

| Bits   | Name   | Default | Description                                                                  |
|--------|--------|---------|------------------------------------------------------------------------------|
| D[2:0] | VREF_L | 100     | Feedback (FB) reference voltage (V <sub>REF</sub> ) lower 3 bits. LSB = 1mV. |

### Register 0x01: REF\_MSB (Read/Write)

| Bits   | Name   | Default    | Description                                   |
|--------|--------|------------|-----------------------------------------------|
| D[7:0] | VREF_H | 0011, 1110 | FB V <sub>REF</sub> higher 8 bits. LSB = 8mV. |

### Register 0x02: CONTROL (Read/Write)

| Bits   | Name | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[7:6] | SR   | 01      | Sets the V <sub>OUT</sub> slew rate. The SR control is only functional once soft start (SS) is complete. During the SS time (t <sub>SS</sub> ), the output voltage (V <sub>OUT</sub> ) slew rate is controlled by SS. V <sub>OUT</sub> slew rate = V <sub>REF</sub> slew rate x feedback ratio. Where the feedback ratio is (R1 + R2) / R2.<br>00: 38mV/ms slew rate<br>01: 50mV/ms slew rate<br>10: 75mV/ms slew rate<br>11: 150mV/ms slew rate |

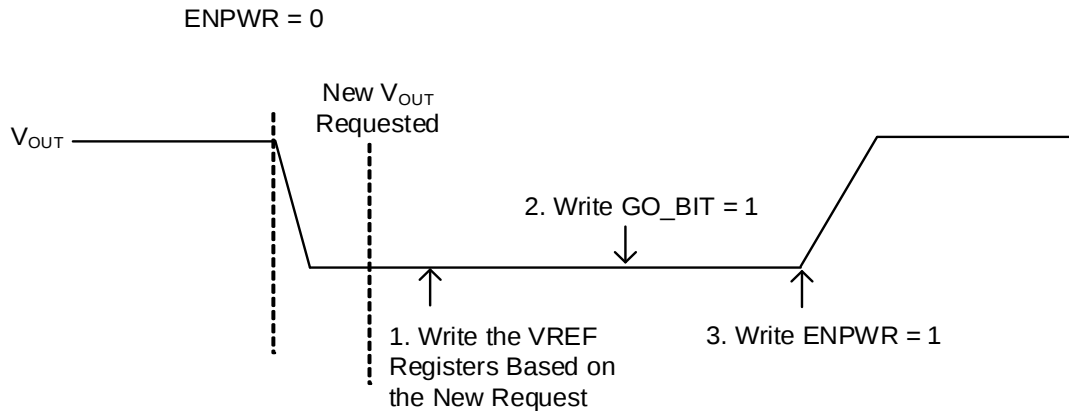
| Bits | Name      | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|-----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[5] | DISCHG    | 0       | <p>Enables the output discharge path. The DISCHG bit is functional even if the ENPWR bit is low.</p> <p>0: If this bit is set to 0, then the discharge path is disabled<br/>1: If this bit is set to 1, then V<sub>OUT</sub> is discharged via an internal resistor</p> <p>This bit does not affect the output discharge function for the following conditions: V<sub>OUT</sub> is set via the I<sup>2</sup>C, ENPWR is off, the EN pin is off, output over-voltage protection (OVP) is triggered (OVP_MODE enables the discharge path), and V<sub>IN</sub> under-voltage lockout (UVLO) protection is triggered. If GO_BIT = 1, then the discharge path is enabled. After a 20ms delay, GO_BIT resets to 0 and the discharge path is disabled. For most applications, it is recommended to set a low slew rate so that V<sub>OUT</sub> can follow V<sub>REF</sub> via the internal discharge current. If V<sub>OUT</sub> cannot follow V<sub>REF</sub> due to a large output capacitor (C<sub>OUT</sub>), then an additional 20ms of discharge time is added.</p> |
| D[4] | DITHER    | 0       | <p>Enables frequency dithering.</p> <p>0: If this bit is set to 0, then frequency dithering is disabled<br/>1: If this bit is set to 1, then frequency dithering is enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| D[3] | PNG_LATCH | 0       | <p>Resets the PNG status bit. For more details, see the PNG bit description on page 34.</p> <p>0: PNG bit status recovers to 0 once V<sub>OUT</sub> is within to its normal voltage range<br/>1: PNG bit status latches at 1 once V<sub>OUT</sub> exceeds the power good voltage (V<sub>PG</sub>) range</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| D[2] | RESERVED  | 1       | Reserved. Do not write a different value to this bit in application.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| D[1] | GO_BIT    | 0       | <p>Enables the V<sub>REF</sub> output change function. Write the VREF_L and VREF_H registers, and then write GO_BIT to 1. V<sub>REF</sub> and V<sub>OUT</sub> are determined by the new V<sub>REF</sub> value. The host reads GO_BIT to determine whether V<sub>REF</sub> scaling is complete. The output discharge path is enabled once GO_BIT = 1, regardless of what the DISCHRG bit's setting. Once GO_BIT resets to 0, output discharge continues. The discharge path is disabled after a 20ms delay.</p> <p>0: V<sub>OUT</sub> cannot be adjusted<br/>1: V<sub>OUT</sub> is determined by the VREF registers. Once V<sub>REF</sub> the level set by the VREF bits, then GO_BIT resets to 0. This setting prevents false V<sub>OUT</sub> scaling</p>                                                                                                                                                                                                                                                                                                          |
| D[0] | ENPWR     | x       | <p>Enables the MP2984's power MOSFETs. ENPWR's default value is determined by the ADDR pin setting. For more details, see Table 1 on page 28. If ENPWR is reset to 0, then the VREF bits are reset to 0011 1110 100 (0.5V). The VREF bits should only reset one time, so that once ENPWR = 0, V<sub>REF</sub> can adjust to the value set by the I<sup>2</sup>C. After ENPWR = 0, output discharge is functional for 200ms.</p> <p>0: Power MOSFETs are disabled<br/>1: Power MOSFETs are enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

### I<sup>2</sup>C V<sub>REF</sub> Sequence for USB Power Delivery (PD) Applications

If the sink device is unplugged, then the PD controller sets ENPWR to 0 in order to disable the bus voltage (V<sub>BUS</sub>). Once the sink device is attached again, the PD controller uses the following sequence to set V<sub>BUS</sub> to 5V:

1. Write the VREF bits based on the new V<sub>OUT</sub>.
2. Write GO\_BIT = 1, and keep ENPWR = 0. This can set V<sub>REF</sub> to the target value.
3. To enable V<sub>OUT</sub>, write ENPWR = 1.

Figure 11 shows the request sequence for a new V<sub>OUT</sub>.



**Figure 11: New V<sub>OUT</sub> Request Sequence**

### Register 0x03: CONTROL\_2 (Read/Write)

| Bits   | Name     | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[7:6] | FSW      | 00, 10  | Sets the switching frequency (f <sub>sw</sub> ) slew rate. FSW's default value is determined by the FS pin setting during start-up. For different voltage level settings, see the Electrical Characteristics section on page 9.<br>00: 200kHz slew rate<br>01: 300kHz slew rate<br>10: 400kHz slew rate<br>11: 600kHz slew rate                                                                                                                                                                                                                                                                         |
| D[4]   | BB_FSW   | 0       | Sets the buck-boost f <sub>sw</sub> .<br>0: Sets the buck-boost f <sub>sw</sub> to 40% of the base f <sub>sw</sub><br>1: Sets buck-boost f <sub>sw</sub> to 80% of the base f <sub>sw</sub>                                                                                                                                                                                                                                                                                                                                                                                                             |
| D[3:2] | OCP_MODE | 01      | Sets the mode once the current reaches the cycle-by-cycle valley current limit (I <sub>LIMIT_VALLEY</sub> ) in buck mode or the cycle-by-cycle peak current limit (I <sub>LIMIT_PEAK</sub> ) in boost mode.<br>00: No hiccup mode or latch-off protection; inductor current (I <sub>L</sub> ) is limited cycle-by-cycle<br>01: The part enters hiccup mode once the current reaches I <sub>LIMIT</sub> ; V <sub>FB</sub> < 60% of V <sub>REF</sub> , t <sub>SS</sub> is controlled by the SS discharge path<br>10: OCP is triggered; the part initiates a SS to resume normal operation<br>11: Reserved |

| Bits   | Name     | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[1:0] | OVP_MODE | 01      | <p>Sets the mode once the voltage exceeds the OVP threshold (127% of V<sub>REF</sub>).</p> <p>00: No protection or discharge after OVP; V<sub>OUT</sub> is regulated by COMP<br/> 01: V<sub>OUT</sub> is discharged via an internal resistor. The IC stops switching once V<sub>FB</sub> exceeds 127% of V<sub>REF</sub>, and recovers once V<sub>FB</sub> drops below 111% of V<sub>REF</sub><br/> 10: Over-voltage (OV) fault has occurred, and OVP is triggered (latch-off protection); no discharge after OVP<br/> 11: Reserved</p> |

**Register 0x04: ILIM (Read/Write)**

| Bits   | Name | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|--------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[2:0] | ILIM | N/A     | <p>Average I<sub>LIMIT</sub>. The average I<sub>LIMIT</sub> can configure the output current limit (I<sub>OUT_LIMIT</sub>). ILIM's default value is determined by the ILIM pin setting during start-up. Float the ILIM pin to set the ILIM bits to 111. For different voltage level settings, see the Electrical Characteristics section on page 9.</p> <p>000: 26mV I<sub>LIMIT</sub>, 2.6A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 001: 32mV I<sub>LIMIT</sub>, 3.2A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 010: 38mV I<sub>LIMIT</sub>, 3.8A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 011: 45mV I<sub>LIMIT</sub>, 4.5A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 100: 50mV I<sub>LIMIT</sub>, 5A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 101: 56mV I<sub>LIMIT</sub>, 5.6A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 110: 62mV I<sub>LIMIT</sub>, 6.2A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub><br/> 111: 68mV I<sub>LIMIT</sub>, 6.8A I<sub>LIMIT</sub> with 10mΩ R<sub>SENSE2</sub></p> |

**Register 0x05: INTERRUPT\_STATUS (Read/Write)**

| Bits | Name | Default | Description                                                                                                                                                                                                                                                                 | Reset Conditions                                                                                                               |
|------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|
| D[4] | OTP  | 0       | <p>Indicates whether an over-temperature (OT) fault has occurred.</p> <p>0: No fault has occurred<br/> 1: OT fault has occurred; the IC enters over-temperature protection (OTP)</p>                                                                                        | <p>These bit are latched once triggered. Write 0xFF to the register to reset the interrupt status and the INT pin's state.</p> |
| D[3] | CC   | 0       | <p>Indicates the output average current limit.</p> <p>0: No fault has occurred<br/> 1: The output current exceeds the average current limit reference, and V<sub>OUT</sub> drops</p>                                                                                        |                                                                                                                                |
| D[2] | OVP  | 0       | <p>Indicates whether an output OV fault has occurred.</p> <p>0: No fault has occurred<br/> 1: OV fault has occurred; the IC enters OVP, and I<sub>OUT_LIMIT</sub> exceeds the I<sub>LIMIT</sub> reference so that V<sub>OUT</sub> drops below the OVP falling threshold</p> |                                                                                                                                |
| D[1] | OCP  | 0       | <p>Indicates whether over-current protection (OCP) has been triggered.</p> <p>0: No fault has occurred<br/> 1: OCP is triggered; V<sub>FB</sub> &lt; 60% of V<sub>REF</sub>, and SS is complete</p>                                                                         |                                                                                                                                |

| Bits | Name | Default | Description                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                       |
|------|------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[0] | PNG  | 0       | <p>Indicate whether V<sub>OUT</sub> is within its normal range (0.5V to 28V). The PNG_LATCH bit controls the PNG reset behavior.</p> <p>0: V<sub>OUT</sub> is within its normal range (output power is good)<br/> 1: V<sub>OUT</sub> is outside of its normal range (output power is not good); the IC indicates once V<sub>OUT</sub> is within 0.5V to 28V</p> | <p>If PNG_LATCH = 0, then this bit indicates an instantaneous value and INT indicates an instantaneous state.</p> <p>If PNG_LATCH = 1, then this bit is latched once triggered. Write 0xFF to the register to reset the interrupt status and the INT pin's state.</p> |

**Register 0x06: INTERRUPT\_MASK (Read/Write)**

| Bits | Name  | Default | Description                                                                                                                                                                                   |
|------|-------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| D[4] | M_OTP | 0       | <p>Determines when an OTP mask bit is masked or not masked. The settings listed below are similar for other mask bits.</p> <p>0: Not masked<br/> 1: Masked (only the INT input is masked)</p> |
| D[3] | M_CC  | 0       | <p>Determines when a CC mask bit is masked or not masked.</p> <p>0: Not masked<br/> 1: Masked (only the INT input is masked); the CC bit cannot be masked</p>                                 |
| D[2] | M_OVP | 0       | <p>Determines when an OVP mask bit is masked or not masked.</p> <p>0: Not masked<br/> 1: Masked (only the INT input is masked)</p>                                                            |
| D[1] | M_OCP | 0       | <p>Determines when an OCP mask bit is masked or not masked.</p> <p>0: Not masked<br/> 1: Masked (only the INT input is masked)</p>                                                            |
| D[0] | M_PNG | 1       | <p>Determines when a PNG mask bit is masked or not masked.</p> <p>0: Not masked<br/> 1: Masked (only the INT input is masked)</p>                                                             |

## APPLICATION INFORMATION

### Output Voltage Setting

The default V<sub>OUT</sub> is set via the FB resistor divider. The default V<sub>REF</sub> is 0.5V. The bottom resistor in the resistor divider is typically between 1kΩ and 50kΩ. The top resistor (R1) in the resistor divider can be calculated with Equation (6):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (6)$$

The I<sup>2</sup>C interface can also select V<sub>REF</sub> to set V<sub>OUT</sub>.

### Selecting the Inductor

The inductor selection is based on the operation mode (buck mode, boost mode, or buck-boost mode). The buck mode inductance (I<sub>L\_BUCK</sub>) can be calculated with Equation (7):

$$I_{L\_BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Where ΔI<sub>L</sub> is the peak-to-peak inductor ripple current.

Choose ΔI<sub>L</sub> to be about 30% to 50% of the maximum load current (I<sub>LOAD\_MAX</sub>).

In boost mode, the inductor should be determined by ΔI<sub>L</sub>. Choose ΔI<sub>L</sub> to be about 30% to 50% of the maximum input current (I<sub>IN\_MAX</sub>). The boost mode inductance (I<sub>L\_BOOST</sub>) can be calculated with Equation (8):

$$I_{L\_BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (8)$$

The maximum input current (I<sub>IN\_MAX</sub>) can be calculated with Equation (9):

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{LOAD\_MAX}}{V_{IN} \times \eta} \quad (9)$$

Where ΔI<sub>L</sub> is about 30% to 50% of I<sub>IN\_MAX</sub>, and η is the efficiency.

A larger inductor reduces ΔI<sub>L</sub>; however, a larger inductor takes up more space and can reduce the converter's achievable bandwidth by moving the right half-plane zero to a lower frequency. Choose an inductor that matches the specific application requirements.

### Selecting the Input Capacitor (C<sub>IN</sub>)

In buck mode, the converter has a discontinuous input current (I<sub>IN</sub>), and requires a capacitor to supply AC current to the converter while maintaining the DC V<sub>IN</sub>. (In boost mode, the converter has a continuous I<sub>IN</sub>.) It is recommended to use ceramic capacitors placed as close to VIN as possible for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and small temperature coefficients. Choose a capacitor with a ripple current rating greater than the maximum input ripple current (ΔI<sub>IN</sub>). The buck mode input ripple current (I<sub>CIN\_RMS</sub>) can be estimated with Equation (10):

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (10)$$

The worst-case condition in buck mode occurs at V<sub>IN</sub> = 2 × V<sub>OUT</sub>, which can be calculated with Equation (11):

$$I_{CIN\_RMS} = \frac{I_{OUT}}{2} \quad (11)$$

For simplification, choose an input capacitor (C<sub>IN</sub>) with an RMS current rating greater than half of I<sub>LOAD\_MAX</sub>.

C<sub>IN</sub> determines the converter's (ΔV<sub>IN</sub>). If there is a ΔV<sub>IN</sub> in the system, choose a C<sub>IN</sub> that meets the system specification.

In buck mode, ΔV<sub>IN</sub> can be estimated with Equation (12):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (12)$$

The worst-case condition occurs at V<sub>IN</sub> = 2 × V<sub>OUT</sub>, which can be calculated with Equation (13):

$$\Delta V_{IN} = \frac{1}{4} \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (13)$$

### Selecting the Output Capacitor (C<sub>OUT</sub>)

In boost mode, the converter has a discontinuous output voltage (I<sub>OUT</sub>). The output

capacitor (C<sub>OUT</sub>) should be capable of reducing the output voltage ripple (ΔV<sub>OUT</sub>).

A higher C<sub>OUT</sub> may be required to lower ΔV<sub>OUT</sub> and transient response. Ceramic capacitors with low ESR are recommended for their small size and low output voltage ripple. For ceramic capacitors, the capacitance dominates the impedance at f<sub>SW</sub> and causes the majority of ΔV<sub>OUT</sub>. For simplification, (ΔV<sub>OUT</sub>) can be estimated with Equation (14):

$$\Delta V_{OUT} = \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{LOAD}}{C_{OUT} \times f_{SW}} \quad (14)$$

For hybrid, polymer, or electrolytic capacitors, the ESR dominates the impedance at f<sub>SW</sub>. For simplification, ΔV<sub>OUT</sub> can be estimated with Equation (15):

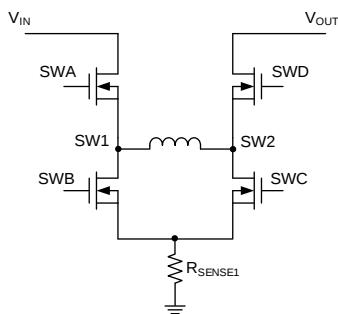
$$\Delta V_{OUT} = \frac{\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times I_{LOAD}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (15)$$

For 100W USB PD applications, it is recommended to use a 100μF polymer capacitor and four 22μF ceramic capacitors.

Choose a C<sub>OUT</sub> that satisfies the ΔV<sub>OUT</sub> and load transient requirements of the design. Capacitance derating should be taken into consideration when designing high V<sub>OUT</sub> applications.

### Selecting the External MOSFETs

The MP2984 requires four external N-channel power MOSFETs (see Figure 12). SWA and SWD are the top two MOSFETs. SWB and SWC are the bottom two MOSFETs. In buck mode, SWA and SWB are switching, and SWD is on. In boost mode, SWC and SWD are switching, and SWA is on.



**Figure 12: Buck-Boost Topology**

The critical parameters for selecting a MOSFET are listed below:

- **Maximum drain-to-source voltage (V<sub>DS\_MAX</sub>):** SWA and SWB have to withstand the maximum V<sub>IN</sub> and transient spikes at SW1. It is recommended to set the SWA and SWB V<sub>DS\_MAX</sub> to 1.5 x V<sub>IN</sub>. SWC and SWD have to withstand V<sub>OUT</sub> and transient spikes at SW2. It is recommended to set the SWC and SWD V<sub>DS\_MAX</sub> to ≥1.5 x V<sub>OUT</sub>.
- **Maximum continuous drain current (I<sub>D\_MAX</sub>):** SWA, SWB, SWC, and SWD have to withstand the maximum inductor current (I<sub>L\_MAX</sub>) and the peak inductor current (I<sub>L\_PEAK</sub>) while switching.
- **Voltage threshold (V<sub>TH</sub>):** The gate driver voltages are supplied by VCC. The MOSFET gate plateau voltages should not exceed the minimum V<sub>CC</sub>; otherwise, the MOSFETs may not enhance fully during start-up or OL conditions.
- **Total gate charge (Q<sub>G</sub>):** All MOSFETs Q<sub>G</sub> should be below 50nC (at 7.2V gate condition). If two MOSFETs in parallel, then each MOSFETs' Q<sub>G</sub> should be below 25nC.
- **Drain-source on resistance (R<sub>DS(ON)</sub>):** A lower R<sub>DS(ON)</sub> improves a MOSFET's temperature rise management and increases efficiency. See the MOSFET descriptions and Equations 16–24 for R<sub>DS(ON)</sub> selection.

### SWA MOSFET

In boost mode, SWA is on, and the SWA conduction power loss (P<sub>CON\_LOSS\_SWA</sub>) can be calculated with Equation (16):

$$P_{CON\_LOSS\_SWA} = \left(I_{OUT} \times \frac{V_{OUT}}{V_{IN}}\right)^2 \times R_{DS(ON)\_SWA} \quad (16)$$

If the MOSFET's junction-to-ambient thermal resistance is 50°C/W (determined by the board's power dissipation), and the maximum acceptant temperature rise is 50°C, then the maximum power loss (P<sub>CON\_LOSS</sub>) is 1W. P<sub>CON\_LOSS\_SWA</sub> can be calculated with Equation (17):

$$P_{CON\_LOSS\_SWA} < 1W \quad (17)$$

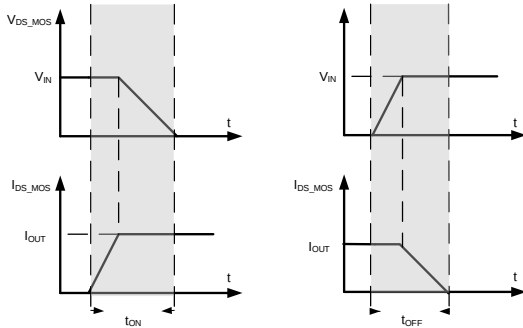
In buck mode, P<sub>CON\_LOSS\_SWA</sub> can be calculated with Equation (18):

$$P_{CON\_LOSS\_SWA} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DS(ON)\_SWA} \quad (18)$$

The SWA switching loss ( $P_{SW\_LOSS\_SWA}$ ) can be calculated with Equation (19):

$$P_{SW\_LOSS\_SWA} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{ON} + t_{OFF}) \times f_{SW} \quad (19)$$

The MOSFET on time ( $t_{ON}$ ) and off time ( $t_{OFF}$ ) are based on Figure 13.



**Figure 13: Switch On Time and Switch Off Time**

#### SWB MOSFET

In buck mode, the SWB conduction loss ( $P_{CON\_LOSS\_SWB}$ ) can be calculated with Equation (20):

$$P_{CON\_LOSS\_SWB} = (1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 \times R_{DS(ON)\_SWB} \quad (20)$$

#### SWC MOSFET

In boost mode, SWB is off, and the SWC conduction loss ( $P_{CON\_LOSS\_SWC}$ ) can be calculated with Equation (21):

$$P_{CON\_LOSS\_SWC} = (1 - \frac{V_{IN}}{V_{OUT}}) \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DS(ON)\_SWC} \quad (21)$$

In boost mode, the SWC switching loss ( $P_{SW\_LOSS\_SWC}$ ) can be calculated with Equation (22):

$$P_{SW\_LOSS\_SWC} = \frac{1}{2} \times V_{OUT} \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}}) \times (t_{ON} + t_{OFF}) \times f_{SW} \quad (22)$$

#### SWD MOSFET

In buck mode, SWD is on, and the SWD power loss ( $P_{CON\_LOSS\_SWD}$ ) can be calculated with Equation (23):

$$P_{CON\_LOSS\_SWD} = I_{OUT}^2 \times R_{DS(ON)\_SWD} \quad (23)$$

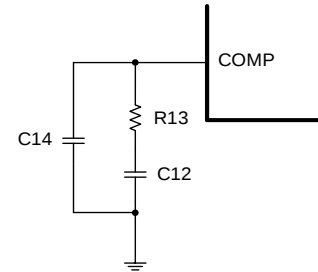
In boost mode, the SWD conduction loss can be calculated with Equation (24):

$$P_{CON\_LOSS\_SWD} = (\frac{V_{IN}}{V_{OUT}}) \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DS(ON)\_SWD} \quad (24)$$

The dead time ( $t_{DEAD}$ ) and the LS-FET switching loss can be ignored.

#### Compensation Components

The COMP pin controls the system stability and transient response. COMP is the output of the internal error amplifier (EA). A capacitor and resistor in series sets a pole and a zero to control the control the system's characteristics.



**Figure 14: COMP External Compensation**

External compensation sets one pole ( $F_{P1}$ ) and one zero ( $F_{Z1}$ ) (see Figure 14).  $F_{P1}$  can be calculated with Equation (25):

$$F_{P1} = \frac{1}{2\pi \times C14 \times R13} \quad (25)$$

$F_{Z1}$  can be calculated with Equation (26):

$$F_{Z1} = \frac{1}{2\pi \times C12 \times R13} \quad (26)$$

In buck mode, the voltage feedback loop DC gain ( $A_{VDC}$ ) can be calculated with Equation (27):

$$A_{VDC} = R_{LOAD} \times \frac{G_{CS}}{R_{SENSE1}} \times A_{V-EA} \times \frac{V_{FB}}{V_{OUT}} \quad (27)$$

Where  $G_{V\_EA}$  is the EA voltage gain (300V/V),  $G_{CS}$  is the COMP to current-sense gain,  $R_{SENSE1}$  is the current-sense resistor, and  $R_{LOAD}$  is the load resistance.

The system has two important poles: one is from the compensation capacitor (C10) and the EA output resistor, and the other one is from  $C_{OUT}$  and the load resistor. The compensation capacitor pole ( $F_{P2}$ ) can be calculated with Equation (28):

$$F_{P2} = \frac{G_{EA}}{2\pi \times C_{12} \times G_{V\_EA}} \quad (28)$$

The EA output resistor pole ( $F_{P3}$ ) can be calculated with Equation (29):

$$F_{P3} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (29)$$

Where  $G_{EA}$  is the EA transconductance (1220 $\mu$ A/V).

The system may have another significant zero ( $F_{ESR}$ ) if  $C_{OUT}$  has a large capacitance or a high ESR value.  $F_{ESR}$  can be calculated with Equation (30):

$$F_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (30)$$

In boost mode,  $A_{VDC}$  can be calculated with Equation (31):

$$A_{VDC} = \frac{V_{IN} \times A_{V-EA} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R_{13}}{2 \times V_{OUT}^2 \times R_{SENSE1}} \quad (31)$$

There is also a right half-plane zero ( $F_{RHPZ}$ ) in boost mode.  $F_{RHPZ}$  can be calculated with Equation (32):

$$F_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \quad (32)$$

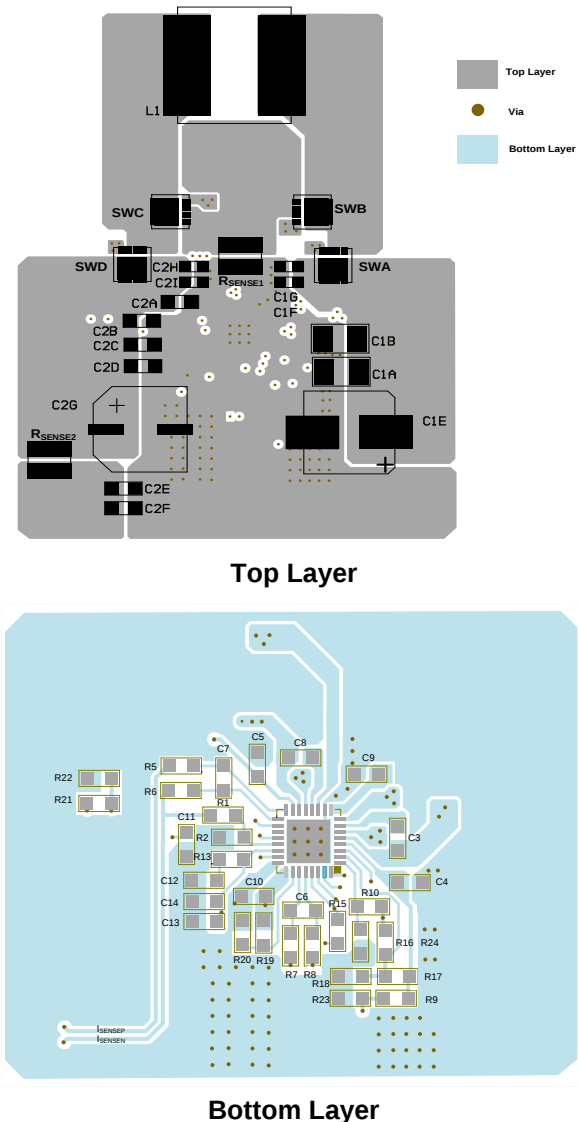
The right half-plane zero increases the gain and reduces the phase, which results in a smaller phase and gain margin. The worst-case condition occurs when  $V_{IN}$  is at its minimum and the  $V_{OUT}$  is at its maximum.

### PCB Layout Guidelines

Efficient layout is a critical for stable operation. Improper layout can result in reduced performance, increased EMI, resistive loss, and system instability. For the best results, refer to Figure 15 and follow the guidelines below:

1. In buck mode, place the input power loop ( $C_{IN}$ , SWA, and SWB), and the cycle-by-cycle current-sense resistor ( $R_{SENSE1}$ ) as close to each other as possible.
2. In boost mode, place the output power loop components — including the output filter capacitor ( $C_{OUT}$ ), the power MOSFETs (SWC and SWD), and the cycle-by-cycle current sense resistor ( $R_{SENSE1}$ ) — as close as possible.
3. Use wide copper traces and power loop vias to improve thermal dissipation.
4. Connect the exposed pad to GND, and place vias on the exposed pad for thermal dissipation.
5. Place small decoupling capacitors close to VIN, VOUT, and AGND.
6. Make the gate driver traces and return paths as direct as possible.
7. Keep the forward and return traces close together to minimize the inductance of the gate driver path. This can be accomplished by either running the traces side by side or on top of one another on adjacent layers.
8. Use Kelvin connections for  $R_{SENSE2}$  (for the average current sense) and R4 (for the cycle-by-cycle current). Run these lines in parallel from the  $R_{SENSE2}/R_{SENSE1}$  terminals to the IC pins. Avoid crossing noisy areas, such as SW1, SW2, or gate driver traces.
9. Place the filter capacitor for the current-sense signal as close to the IC's pins as possible.
10. Place the VCC and AVDD capacitors as close as possible to the VCC and AVDD pins.
11. Place the BST1 bootstrap capacitor close to the IC, and connect the capacitor directly to the BST1 and SW1 pins.

12. Place the BST2 bootstrap capacitor close to the IC, and connect the capacitor directly to the BST2 and SW2 pins.
13. Route the feedback loop far away from any noise sources. Place the FB dividers (R1 and R2) as close as possible to the FB and AGND pins.
14. Separate the power and signal paths so that no power or switching current flows through the AGND connections.
15. Connect the PGND and AGND traces near the PGND pin, the VCC capacitor's PGND connection, or near PGND's connection to R4.



**Figure 15: Recommended PCB Layout**

# TYPICAL APPLICATION CIRCUIT

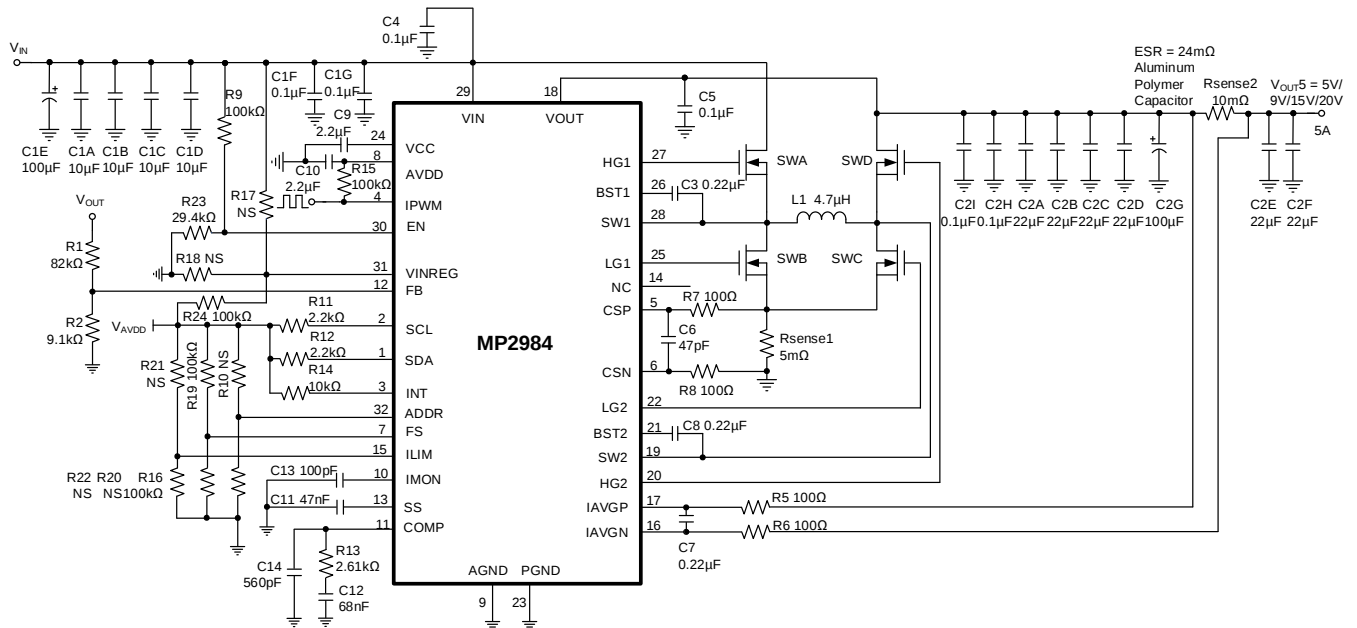
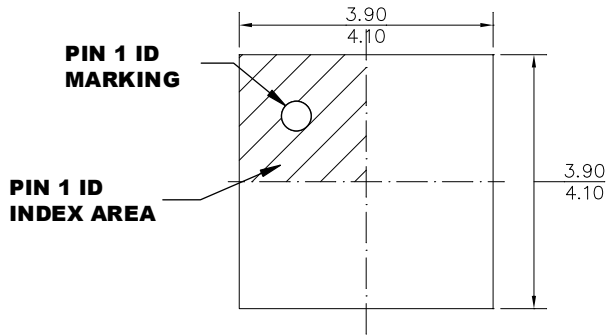


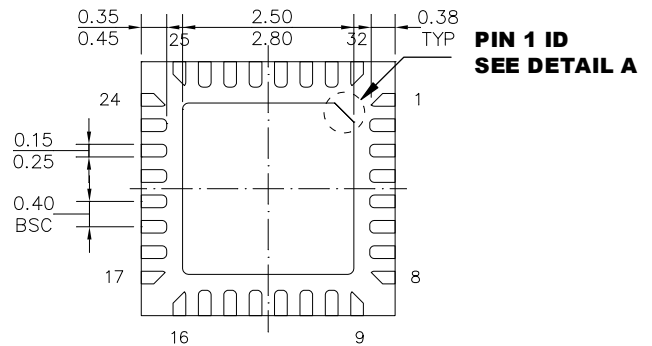
Figure 16: Typical Application Circuit (V<sub>IN</sub> = 12V, V<sub>OUT</sub> = 5V/9V/15V/20V for 100W USB PD)

# PACKAGE INFORMATION

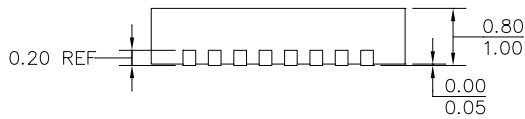
## QFN-32 (4mmx4mm)



**TOP VIEW**

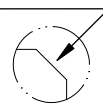


**BOTTOM VIEW**

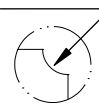


**SIDE VIEW**

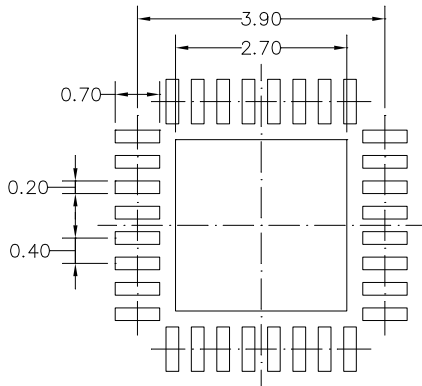
**PIN 1 ID OPTION A**  
0.30x45° TYP.



**PIN 1 ID OPTION B**  
R0.25 TYP.



**DETAIL A**

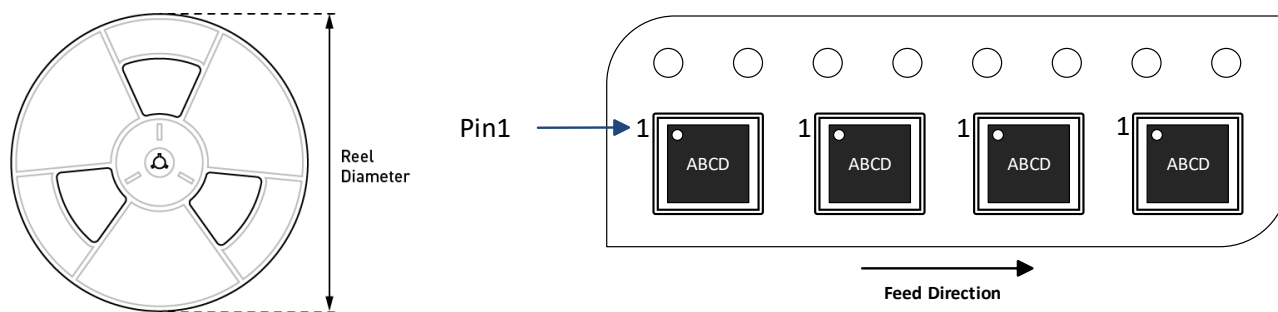


**RECOMMENDED LAND PATTERN**

## NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITIES SHALL BE 0.1 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------|---------------------|----------------|----------------|---------------|--------------------|--------------------|
| MP2984GR-Z  | QFN-32<br>(4mmx4mm) | 5000           | N/A            | 13in          | 12mm               | 8mm                |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 12/09/2021    | Initial Release | -             |

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