MICROCHIP

USB7205C

5-Port USB 3.2 Gen 2 Controller Hub

Highlights

- 5-Port USB 3.2 Gen 2 Smart Hub with:
  - Four Standard USB 3.2 Gen 2 downstream ports
  - One Standard USB 2.0 downstream port
  - Internal Hub Feature Controller enables:
    - USB to I^2C/SPI/I^2S/GPIO bridge endpoint support
    - USB to internal hub register write and read
- USB Link Power Management (LPM) support
- Programming of firmware image to external SPI memory device from USB host
- USB-IF Battery Charger revision 1.2 support on downstream ports (DCP, CDP, SDP)
- Enhanced OEM configuration options available through either OTP or external SPI memory
- Available in 100-pin (12 mm x 12 mm) VQFN RoHS compliant package
- Commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature range support

Target Applications

- Standalone USB Hubs
- Laptop Docks
- PC Motherboards
- PC Monitor Docks
- Multi-function USB 3.2 Gen 2 Peripherals

Key Benefits

- USB 3.2 Gen 2 compliant 10 Gbps, 5 Gbps, 480 Mbps, 12 Mbps, and 1.5Mbps operation
  - 5V tolerant USB 2.0 pins
  - 1.21V tolerant USB 3.2 Gen 2 pins
  - Integrated termination and pull-up/down resistors
- Supports battery charging of most popular battery powered devices on all ports
  - USB-IF Battery Charging rev. 1.2 support (DCP, CDP, SDP)
  - Apple® portable product charger emulation
  - Chinese YD/T 1591-2006/2009 charger emulation
  - European Union universal mobile charger support
  - Supports additional portable devices
- On-chip Microcontroller
  - Manages I/Os, VBUS, and other signals
- 96 kB RAM, 256 kB ROM
- 8 kB One-Time-Programmable (OTP) ROM
  - Includes on-chip charge pump
- Configuration programming via OTP Memory, SPI external memory or SMBus
- **FlexConnect**
  - The roles of the upstream and downstream ports are reversible on command
- **USB Bridging**
  - USB to I^2C, SPI, I^2S, and GPIO
- **PortSwap**
  - Configurable USB 2.0 differential pair signal swap
- **PHYBoost™**
  - Programmable USB transceiver drive strength for recovering signal integrity
- **VariSense™**
  - Programmable USB receive sensitivity
- **PortSplit**
  - USB 2.0 and USB 3.2 Gen 2 port operation can be split for custom applications using embedded USB 3.x devices in parallel with USB 2.0 devices
- Compatible with Microsoft Windows® 11, 10, 8, 7, XP, Apple OS X 10.4+, and Linux hub drivers
- Optimized for low-power operation and low thermal dissipation
- 100-pin VQFN package (12 mm x 12 mm)

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
ADC	Analog-to-Digital Converter
Byte	8 bits
CDC	Communication Device Class
CSR	Control and Status Registers
DFP	Downstream Facing Port
DWORD	32 bits
EOP	End of Packet
EP	Endpoint
FIFO	First In First Out buffer
FS	Full-Speed
FSM	Finite State Machine
GPIO	General Purpose I/O
HS	Hi-Speed
HSOS	High Speed Over Sampling
Hub Feature Controller	The Hub Feature Controller, sometimes called a Hub Controller for short is the internal processor used to enable the unique features of the USB Controller Hub. This is not to be confused with the USB Hub Controller that is used to communicate the hub status back to the Host during a USB session.
I^2C	Inter-Integrated Circuit
LS	Low-Speed
lsb	Least Significant Bit
LSB	Least Significant Byte
msb	Most Significant Bit
MSB	Most Significant Byte
N/A	Not Applicable
NC	No Connect
OTP	One Time Programmable
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer
PLL	Phase Lock Loop
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SDK	Software Development Kit
SMBus	System Management Bus
UFP	Upstream Facing Port
UUID	Universally Unique IDentifier
WORD	16 bits

1.2 Buffer Types

TABLE 1-2: BUFFER TYPES

Buffer Type	Description
I	Input.
IS	Input with Schmitt trigger.
O12	Output buffer with 12 mA sink and 12 mA source.
OD12	Open-drain output with 12 mA sink
PU	50 µA (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	50 µA (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
ICLK	Crystal oscillator input pin
OCLK	Crystal oscillator output pin
I/O-U	Analog input/output defined in USB specification.
I-R	RBIAS.
A	Analog.
AIO	Analog bidirectional.
P	Power pin.

1.3 Pin Reset States

The pin reset state definitions are detailed in Table 1-3. Refer to Section 3.1, 100- VQFN Pin Assignments for details on individual pin reset states.

TABLE 1-3: PIN RESET STATE LEGEND

Symbol	Description
AI	Analog input
AIO	Analog input/output
AO	Analog output
PD	Hardware enables pull-down
PU	Hardware enables pull-up
Y	Hardware enables function
Z	Hardware disables output driver (high impedance)
PU	Hardware enables internal pull-up
PD	Hardware enables internal pull-down

1.4 Reference Documents

1. *Universal Serial Bus Revision 3.2 Specification*, http://www.usb.org
2. *Battery Charging Specification*, Revision 1.2, Dec. 07, 2010, http://www.usb.org
3. *I^2C-Bus Specification*, Version 1.1, http://www.nxp.com/documents/user_manual/UM10204.pdf
4. *I^2S-Bus Specification*, http://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
5. *System Management Bus Specification*, Version 1.0, http://smbus.org/specs

Note: Additional USB7205C resources can be found on the Microchip USB7205C product page at www.microchip.com/USB7205C.

2.0 INTRODUCTION

2.1 General Description

The Microchip USB7205C hub is a low-power, OEM configurable, USB 3.2 Gen 2 hub controller with 5 downstream ports and advanced features for embedded USB applications. The USB7205C is fully compliant with the Universal Serial Bus Revision 3.2 Specification and USB 2.0 Link Power Management Addendum. The USB7205C supports 10 Gbps SuperSpeed+ (SS+), 5 Gbps SuperSpeed (SS), 480 Mbps Hi-Speed (HS), 12 Mbps Full-Speed (FS), and 1.5 Mbps Low-Speed (LS) USB downstream devices on four standard USB 3.2 Gen 2 downstream ports and only legacy speeds (HS/FS/LS) on one standard USB 2.0 downstream port.

The USB7205C supports the legacy USB speeds (HS/FS/LS) through a dedicated USB 2.0 hub controller that is the culmination of seven generations of Microchip hub feature controller design and experience with proven reliability, interoperability, and device compatibility. The SuperSpeed hub controller operates in parallel with the USB 2.0 controller, decoupling the 10/5 Gbps SS+/SS data transfers from bottlenecks due to the slower USB 2.0 traffic.

The USB7205C enables OEMs to configure their system using "Configuration Straps." These straps simplify the configuration process assigning default values to USB 3.2 Gen 2 ports and GPIOs. OEMs can disable ports, enable battery charging and define GPIO functions as default assignments on power up removing the need for OTP or external SPI ROM.

The USB7205C supports downstream battery charging. The USB7205C integrated battery charger detection circuitry supports the USB-IF Battery Charging (BC1.2) detection method and most Apple devices. The USB7205C provides the battery charging handshake and supports the following USB-IF BC1.2 charging profiles:

- DCP: Dedicated Charging Port (Power brick with no data)
- CDP: Charging Downstream Port (1.5A with data)
- SDP: Standard Downstream Port (0.5A[USB 2.0]/0.9A[USB 3.2] with data)

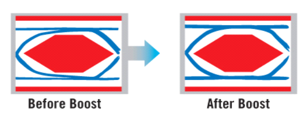
Additionally, the USB7205C includes many powerful and unique features such as:

The Hub Feature Controller, an internal USB device dedicated for use as a USB to I^2C/SPI/GPIO interface that allows external circuits or devices to be monitored, controlled, or configured via the USB interface.

FlexConnect, which provides flexible connectivity options. One of the USB7205C's downstream ports can be reconfigured to become the upstream port, allowing master capable devices to control other devices on the hub.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration. in a compromised system environment.



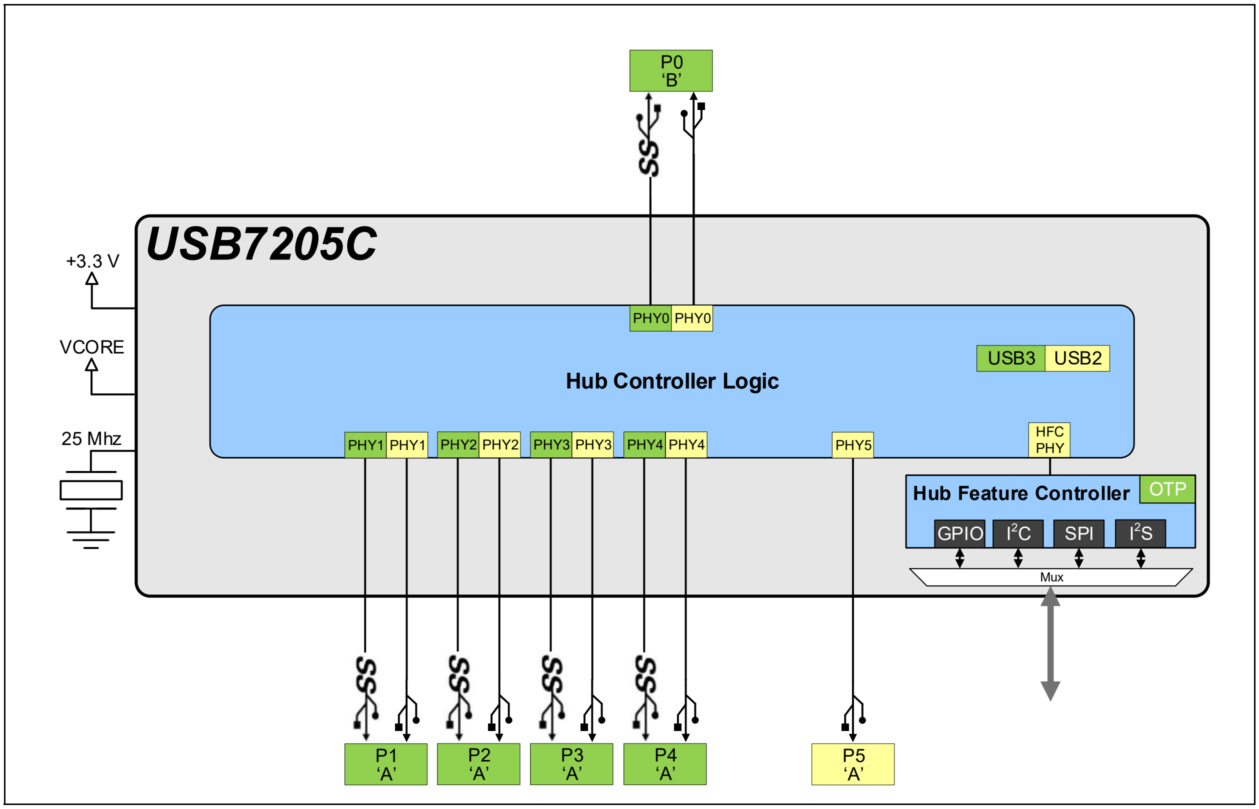
VariSense, which controls the Hi-Speed USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

Port Split, which allows for the USB 3.2 Gen 2 and USB 2.0 portions of downstream ports 3 and 4 to operate independently and enumerate two separate devices in parallel in special applications.

The USB7205C can be configured for operation through internal default settings. Custom OEM configurations are supported through external SPI ROM or OTP ROM. All port control signal pins are under firmware control in order to allow for maximum operational flexibility and are available as GPIOs for customer specific use.

The USB7205C is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the USB7205C in an upstream Type-B application is shown in Figure 2-1.

FIGURE 2-1: USB7205C INTERNAL BLOCK DIAGRAM - UPSTREAM TYPE- APPLICATION

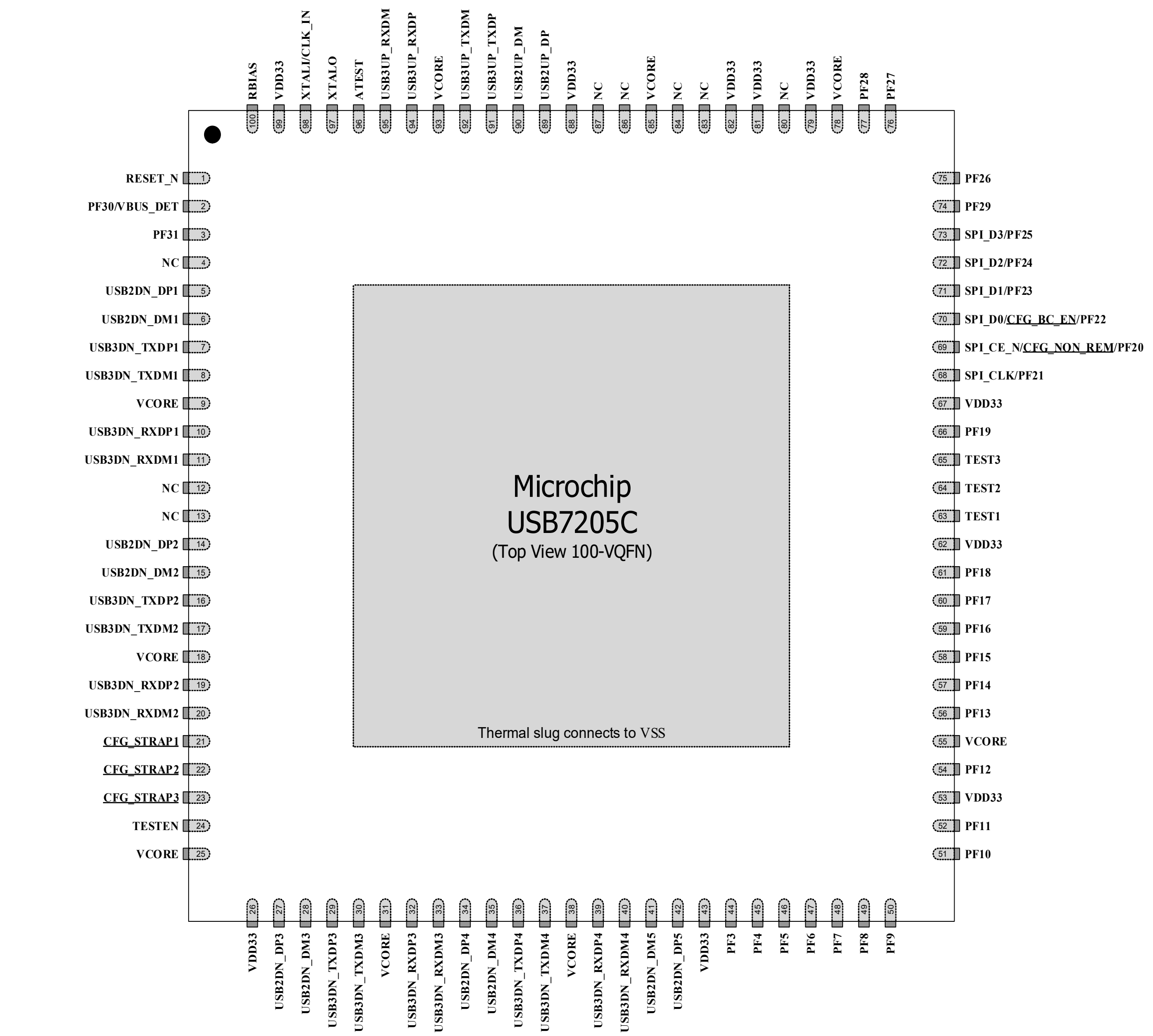


Note:	All port numbering in this document is LOGICAL port numbering with the device in the default configuration. LOGICAL port numbering is the numbering as communicated to the USB host. It is the end result after any port number remapping or port disabling. The PHYSICAL port number is the port number with respect to the physical PHY on the chip. PHYSICAL port numbering is fixed and the settings are not impacted by LOGICAL port renumbering/remapping. Certain port settings are made with respect to LOGICAL port numbering, and other port settings are made with respect to PHYSICAL port numbering. Refer to the “Configuration of USB7202/USB7206/USB725x” application note for details on the LOGICAL vs. PHYSICAL mapping and additional configuration details.

3.0 PIN DESCRIPTIONS

3.1 100- VQFN Pin Assignments

FIGURE 3-1: USB7205C 100-VQFN PIN ASSIGNMENTS



Note:	Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load.

TABLE 3-1: USB7205C 100-VQFN PIN ASSIGNMENTS

Pin Num	Pin Name	Reset	Pin Num	Pin Name	Reset
1	RESET_N	Z	51	PF10	PD
2	PF30/VBUS_DET	Z	52	PF11	PD
3	PF31	Z	53	VDD33	Z
4	NC	AI	54	PF12	PD
5	USB2DN_DP1	AIO PD	55	VCORE	Z
6	USB2DN_DM1	AIO PD	56	PF13	PD
7	USB3DN_TXDP1	AO PD	57	PF14	PD
8	USB3DN_TXDM1	AO PD	58	PF15	PD
9	VCORE	Z	59	PF16	PD
10	USB3DN_RXDP1	AI PD	60	PF17	PD
11	USB3DN_RXDM1	AI PD	61	PF18	Z
12	NC	AI	62	VDD33	Z
13	NC	AI	63	TEST1	Z
14	USB2DN_DP2	AIO PD	64	TEST2	Z
15	USB2DN_DM2	AIO PD	65	TEST3	Z
16	USB3DN_TXDP2	AO PD	66	PF19	Z
17	USB3DN_TXDM2	AO PD	67	VDD33	Z
18	VCORE	Z	68	SPI_CLK/PF21	Z
19	USB3DN_RXDP2	AI PD	69	SPI_CE_N/CFG_NON_REM/PF20	PU
20	USB3DN_RXDM2	AI PD	70	SPI_D0/CFG_BC_EN/PF22	Z
21	CFG_STRAP1	Z	71	SPI_D1/PF23	Z
22	CFG_STRAP2	Z	72	SPI_D2/PF24	Z
23	CFG_STRAP3	Z	73	SPI_D3/PF25	Z
24	TESTEN	Z	74	PF29	Z
25	VCORE	Z	75	PF26	Z
26	VDD33	Z	76	PF27	Z
27	USB2DN_DP3	AIO PD	77	PF28	Z
28	USB2DN_DM3	AIO PD	78	VCORE	Z
29	USB3DN_TXDP3	AO PD	79	VDD33	Z
30	USB3DN_TXDM3	AO PD	80	NC	AI
31	VCORE	Z	81	VDD33	Z
32	USB3DN_RXDP3	AI PD	82	VDD33	Z
33	USB3DN_RXDM3	AI PD	83	NC	AI
34	USB2DN_DP4	AIO PD	84	NC	AI
35	USB2DN_DM4	AIO PD	85	VCORE	Z
36	USB3DN_TXDP4	AO PD	86	NC	AI
37	USB3DN_TXDM4	AO PD	87	NC	AI
38	VCORE	Z	88	VDD33	Z
39	USB3DN_RXDP4	AI PD	89	USB2UP_DP	AIO Z
40	USB3DN_RXDM4	AI PD	90	USB2UP_DM	AIO Z
41	USB2DN_DM5	AIO PD	91	USB3UP_TXDP	AO PD
42	USB2DN_DP5	AIO PD	92	USB3UP_TXDM	AO PD
43	VDD33	Z	93	VCORE	Z
44	PF3	Z	94	USB3UP_RXDP	AI PD
45	PF4	Z	95	USB3UP_RXDM	AI PD
46	PF5	Z	96	ATEST	AO
47	PF6	Z	97	XTALO	AO
48	PF7	Z	98	XTALI/CLK_IN	AI
49	PF8	Z	99	VDD33	Z
50	PF9	Z	100	RBIAS	AI
Exposed Pad (VSS) must be connected to ground.					

3.2 Pin Descriptions

This section contains descriptions of the various USB7205C pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signal. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

The "If Unused" column provides information on how to terminate pins if they are unused in a customer design.

Buffer type definitions are detailed in Section 1.2, Buffer Types.

TABLE 3-1: PIN DESCRIPTIONS

Name	Symbol	Buffer Type	Description	If Unused
USB 3.2 Gen 2 Interfaces				
Upstream USB 3.2 Gen 2 TX D+	**USB3UP_TXDP**	I/O-U	Upstream USB 3.2 Gen 2 Transmit Data Plus.	Float
Upstream USB 3.2 Gen 2 TX D-	**USB3UP_TXDM**	I/O-U	Upstream USB 3.2 Gen 2 Transmit Data Minus.	Float
Upstream USB 3.2 Gen 2 RX D+	**USB3UP_RXDP**	I/O-U	Upstream USB 3.2 Gen 2 Receive Data Plus.	Weak pull-down to GND
Upstream USB 3.2 Gen 2 RX D-	**USB3UP_RXDM**	I/O-U	Upstream USB 3.2 Gen 2 Receive Data Minus.	Weak pull-down to GND
Downstream Ports 1-4 USB 3.2 Gen 2 TX D+	**USB3DN_TXDP[1:4]**	I/O-U	Downstream SuperSpeed+ Transmit Data Plus, ports 1 through 4.	Float
Downstream Ports 1-4 USB 3.2 Gen 2 TX D-	**USB3DN_TXDM[1:4]**	I/O-U	Downstream SuperSpeed+ Transmit Data Minus, ports 1 through 4.	Float
Downstream Ports 1-4 USB 3.2 Gen 2 RX D+	**USB3DN_RXDP[1:4]**	I/O-U	Downstream SuperSpeed+ Receive Data Plus, ports 1 through 4.	Weak pull-down to GND
Downstream Ports 1-4 USB 3.2 Gen 2 RX D-	**USB3DN_RXDM[1:4]**	I/O-U	Downstream SuperSpeed+ Receive Data Minus, ports 1 through 4.	Weak pull-down to GND
USB 2.0 Interfaces				
Upstream USB 2.0 D+	**USB2UP_DP**	I/O-U	Upstream USB 2.0 Data Plus (D+).	Mandatory Note 3-6
Upstream USB 2.0 D-	**USB2UP_DM**	I/O-U	Upstream USB 2.0 Data Minus (D-).	Mandatory Note 3-6
Downstream Port 5 USB 2.0 D+	**USB2DN_DP5**	I/O-U	Downstream USB 2.0 Port 5 Data Plus (D+).	Float

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description	If Unused
Downstream Port 4 USB 2.0 D+	**USB2DN_DP4**	I/O-U	Downstream USB 2.0 Port 4 Data Plus (D+).	Float
Downstream Port 3 USB 2.0 D+	**USB2DN_DP3**	I/O-U	Downstream USB 2.0 Port 3 Data Plus (D+).	Float
Downstream Port 2 USB 2.0 D+	**USB2DN_DP2**	I/O-U	Downstream USB 2.0 Port 2 Data Plus (D+).	Float
Downstream Port 1 USB 2.0 D+	**USB2DN_DP1**	I/O-U	Downstream USB 2.0 Port 1 Data Plus (D+).	Float
Downstream Port 5 USB 2.0 D-	**USB2DN_DM5**	I/O-U	Downstream USB 2.0 Port 5 Data Minus (D-)	Float
Downstream Port 4 USB 2.0 D-	**USB2DN_DM4**	I/O-U	Downstream USB 2.0 Port 4 Data Minus (D-)	Float
Downstream Port 3 USB 2.0 D-	**USB2DN_DM3**	I/O-U	Downstream USB 2.0 Port 3 Data Minus (D-)	Float
Downstream Port 2 USB 2.0 D-	**USB2DN_DM2**	I/O-U	Downstream USB 2.0 Port 2 Data Minus (D-)	Float
Downstream Port 1 USB 2.0 D-	**USB2DN_DM1**	I/O-U	Downstream USB 2.0 Port 1 Data Minus (D-)	Float
Detect Upstream VBUS Power	**VBUS_DET**	I	The Microchip hub monitors **VBUS_DET** to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the hub. For self-powered applications with a permanently attached host, this pin should be pulled up, typically to VDD33. **VBUS_DET** is a 3.3V input. A resistor divider must be used when connecting to 5V of USB power.	Pull up
SPI Interface				
SPI Clock	**SPI_CLK**	I/O-U	SPI clock. If the SPI interface is enabled, this pin must be driven low during reset.	Weak pull-down to GND

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description	If Unused
SPI Data 3-0	**SPI_D[3:0]**	I/O-U	SPI Data 3-0. If the SPI interface is enabled, these signals function as Data 3 through 0. **Note 3-1** **SPI_D0** operates as the **CFG_BC_EN** strap if external SPI memory is not used. It must be terminated with the selected strap resistor to 3.3V or GND. **SPI_D[1:3]** should be connected to GND through a weak pull-down.	Note 3-1
SPI Chip Enable	**SPI_CE_N**	I/O12	Active low SPI chip enable input. If the SPI interface is enabled, this pin must be driven high in powerdown states. **Note 3-2** Operates as the **CFG_NON_REM** strap if external SPI memory is not used. It must be terminated with the selected strap resistor to 3.3V or GND.	Note 3-2
Miscellaneous				
Programmable Function Pins	**PF[31:3]**	I/O12	Programmable function pins. **Note 3-3** If unused: depends on the configured pin function. Refer to Section 3.3.3, PF[31:3] Configuration (CFG_STRAP[2:1])	Note 3-3
Test 1	**TEST1**	A	Test 1 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.	Pull to 3.3V through a 10 kΩ resistor
Test 2	**TEST2**	A	Test 2 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.	Pull to 3.3V through a 10 kΩ resistor
Test 3	**TEST3**	A	Test 3 pin. This signal is used for test purposes and must always be pulled-up to 3.3V via a 10 kΩ resistor.	Pull to 3.3V through a 10 kΩ resistor
Reset Input	**RESET_N**	IS	This active low signal is used by the system to reset the device.	Mandatory Note 3-6

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description	If Unused
Bias Resistor	**RBIAS**	I-R	A 12.0 kΩ ±1.0% resistor is attached from ground to this pin to set the transceiver's internal bias settings. Place the resistor as close the device as possible with a dedicated, low impedance connection to the ground plane.	Mandatory Note 3-6
Test	**TESTEN**	I/O12	Test pin. This signal is used for test purposes and must always be connected to ground.	Connect to GND
Analog Test	**ATEST**	A	Analog test pin. This signal is used for test purposes and must always be left unconnected.	Float
External 25 MHz Crystal Input	**XTALI**	ICLK	External 25 MHz crystal input	Mandatory Note 3-6
External 25 MHz Reference Clock Input	**CLK_IN**	ICLK	External reference clock input. The device may alternatively be driven by a single-ended clock oscillator. When this method is used, **XTALO** should be left unconnected.	Mandatory Note 3-6
External 25 MHz Crystal Output	**XTALO**	OCLK	External 25 MHz crystal output	Float (only if single-ended clock is connected to **CLK_IN**)
No Connect	**NC**	-	No connect. For proper operation, this pin must be left unconnected.	No connect
Configuration Straps				
Non-Removable Ports Configuration Strap	**CFG_NON_REM**	I	Non-Removable Ports Configuration Strap. This configuration strap controls the number of reported non-removable ports. See Note 3-7. **Note 3-4** Mandatory if external SPI memory is not used for firmware execution. If external SPI memory is used for firmware execution, then configuration strap resistor should be omitted.	Note 3-4

TABLE 3-1: PIN DESCRIPTIONS (CONTINUED)

Name	Symbol	Buffer Type	Description	If Unused
Battery Charging Configuration Strap	CFG_BC_EN	I/O12	Battery Charging Configuration Strap. This configuration strap controls the number of BC 1.2 enabled downstream ports. See Note 3-7. **Note 3-5** Mandatory if external SPI memory is not used for firmware execution. If external SPI memory is used for firmware execution, then configuration strap resistor should be omitted.	Mandatory Note 3-6
Device Mode Configuration Straps 3-1	CFG_STRAP[3:1]	I	Device Mode Configuration Straps 3-1. These configuration straps are used to select the device's mode of operation. See Note 3-7.	Mandatory Note 3-6
Power/Ground				
+3.3V I/O Power Supply Input	VDD33	P	+3.3 V power supply input.	Mandatory Note 3-7
Digital Core Power Supply Input	VCORE	P	Digital core power supply input.	Mandatory Note 3-7
Ground	VSS	P	Common ground. The exposed pad must be connected to the ground plane with a via array.	Mandatory Note 3-7

Note 3-6 Configuration strap values are latched on Power-On Reset (POR) and the rising edge of **RESET_N** (external chip reset). Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor when connected to a load. For additional information, refer to Section 3.3, Configuration Straps and Programmable Functions.

Note 3-7 Pin use is mandatory. Cannot be left unused.

3.3 Configuration Straps and Programmable Functions

Configuration straps are multi-function pins that are used during Power-On Reset (POR) or external chip reset (RESET_N) to determine the default configuration of a particular feature. The state of the signal is latched following deassertion of the reset. Configuration straps are identified by an underlined symbol name. This section details the various device configuration straps and associated programmable pin functions.

Note: The system designer must guarantee that configuration straps meet the timing requirements specified in Section 5.6.2, Power-On and Configuration Strap Timing and Section 5.6.3, Reset and Configuration Strap Timing. If configuration straps are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

3.3.1 NON-REMOVABLE PORT CONFIGURATION (CFG_NON_REM)

The CFG_NON_REM configuration strap is used to configure the non-removable port settings of the device to one of five settings. These modes are selected by the configuration of an external resistor on the CFG_NON_REM pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-2.

TABLE 3-2: CFG_NON_REM RESISTOR ENCODING

CFG_NON_REM Resistor Value	Setting
200 kΩ Pull-Down	All ports removable
200 kΩ Pull-Up	Port 1 non-removable
10 kΩ Pull-Down	Ports 1, 2 non-removable
10 kΩ Pull-Up	Ports 1, 2, 3 non-removable
10 Ω Pull-Down	Ports 1, 2, 3, 4 non-removable
10 Ω Pull-Up	Ports 1, 2, 3, 4, 5 non-removable

3.3.2 BATTERY CHARGING CONFIGURATION (CFG_BC_EN)

The CFG_BC_EN configuration strap is used to configure the battery charging port settings of the device to one of six settings. These modes are selected by the configuration of an external resistor on the CFG_BC_EN pin. The resistor options are a 200 kΩ pull-down, 200 kΩ pull-up, 10 kΩ pull-down, 10 kΩ pull-up, 10 Ω pull-down, and 10 Ω pull-up, as shown in Table 3-3.

TABLE 3-3: CFG_BC_EN RESISTOR ENCODING

CFG_BC_EN Resistor Value	Setting
200 kΩ Pull-Down	Battery charging not enable on any port
200 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Port 1
10 kΩ Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2
10 kΩ Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3
10 Ω Pull-Down	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4
10 Ω Pull-Up	BC1.2 DCP and CDP battery charging enabled on Ports 1, 2, 3, 4, 5

3.3.3 PF[31:3] CONFIGURATION (CFG_STRAP[2:1])

The USB7205C provides 29 programmable function pins (PF[31:3]). These pins can only be configured to 1 predefined configuration via the CFG_STRAP[2:1] pins. This configuration is selected via external resistors on the CFG_STRAP[2:1] pins, as detailed in Table 3-4. Resistor values and combinations not detailed in Table 3-4 are reserved and should not be used.

Note: CFG_STRAP3 is not used and must be pulled-down to ground via a 200 kΩ resistor.

TABLE 3-4: CFG_STRAP[2:1] RESISTOR ENCODING

Mode	CFG_STRAP2 Resistor Value	CFG_STRAP1 Resistor Value
Configuration 3	200 kΩ Pull-Down	10 kΩ Pull-Down

Note: Configurations 1 and 2 are not used in the USB7205C.

A summary of the configuration pin assignments is provided in Table 3-5. For details on behavior of each programmable function, refer to Table 3-6.

TABLE 3-5: PF[31:3] FUNCTION ASSIGNMENT

Pin	Configuration 3
PF3	I2S_SDI
PF4	I2S_SDO
PF5	I2S_SCK
PF6	I2S_LRCK
PF7	I2S_MCLK
PF8	NC
PF9	NC
PF10	PRT_CTL3_U3
PF11	PRT_CTL4_U3
PF12	NC
PF13	NC
PF14	PRT_CTL4
PF15	PRT_CTL3
PF16	PRT_CTL2
PF17	PRT_CTL1
PF18	MSTR_I2C_CLK
PF19	MIC_DET
PF20	SPI_CE_N
PF21	SPI_CLK
PF22	SPI_D0
PF23	SPI_D1
PF24	SPI_D2
PF25	SPI_D3
PF26	SLV_I2C_CLK
PF27	SLV_I2C_DATA
PF28	PRT_CTL5
PF29	GPIO93
PF30	VBUS_DET
PF31	MSTR_I2C_DATA

Note: The default **PF*x*** pin functions can be overridden with additional configuration by modification of the pin mux registers. These changes can be made during the SMBus configuration stage, by programming to OTP memory, or during runtime (after hub has attached and enumerated) by register writes via the SMBus slave interface or USB commands to the internal Hub Feature Controller Device.

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS

Function	Buffer Type	Description	If Unused
Master SMBus/I^{2}C Interface			
MSTR_I2C_CLK	I/O12	Bridging Master SMBus/I^{2}C controller clock (SMBus/I^{2}C controller 1). External 1k-10k pull-up resistors to 3.3V are required if the I^{2}C Master Interface is to be used.	Weak pull-down to GND
MSTR_I2C_DATA	I/O12	Bridging Master SMBus/I^{2}C controller data (SMBus/I^{2}C controller 1). External 1k-10k pull-up resistors to 3.3V are required if the I^{2}C Master Interface is to be used.	Weak pull-down to GND
Slave SMBus/I^{2}C Interface			
SLV_I2C_CLK	I/O12	Slave SMBus/I^{2}C controller clock (SMBus/I^{2}C controller 2). External 1k-10k pull-up resistors to 3.3V are required if the I^{2}C Slave Interface is to be used.	Weak pull-down to GND
SLV_I2C_DATA	I/O12	Slave SMBus/I^{2}C controller data (SMBus/I^{2}C controller 2). External 1k-10k pull-up resistors to 3.3V are required if the I^{2}C Slave Interface is to be used.	Weak pull-down to GND
I^{2}S Interface			
I2S_SDI	I	I^{2}S Serial Data In	Weak pull-down to GND
I2S_SDO	O12	I^{2}S Serial Data Out	Weak pull-down to GND
I2S_SCK	O12	I^{2}S Continuous Serial Clock	Weak pull-down to GND
I2S_LRCK	O12	I^{2}S Word Select / Left-Right Clock	Weak pull-down to GND
I2S_MCLK	O12	I^{2}S Master Clock	Weak pull-down to GND
MIC_DET	I	I^{2}S Microphone Plug Detect 0 = No microphone plugged into the audio jack 1 = Microphone plugged into the audio jack	Weak pull-down to GND

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description	If Unused
Miscellaneous			
PRT_CTL5	I/O12 (PU)	Port 5 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 5. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** This signal controls both the USB 2.0 and USB 3.2 portions of the port. **Note 3-1** This pin can be left unused only if Port 5 is disabled via strap/OTP/SMBus/SPI configuration.	Float (Note 3-1)
PRT_CTL4	I/O12 (PU)	Port 4 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 4. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.2 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only. **Note 3-2** This pin can be left unused only if Port 4 is disabled via strap/OTP/SMBus/SPI configuration.	Float (Note 3-2)
PRT_CTL3	I/O12 (PU)	Port 3 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 3. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.2 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only. **Note 3-3** This pin can be left unused only if Port 3 is disabled via strap/OTP/SMBus/SPI configuration.	Float (Note 3-3)

TABLE 3-6: PROGRAMMABLE FUNCTIONS DESCRIPTIONS (CONTINUED)

Function	Buffer Type	Description	If Unused
PRT_CTL2	I/O12 (PU)	Port 2 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 2. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.2 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only. **Note 3-4** This pin can be left unused only if Port 2 is disabled via strap/OTP/SMBus/SPI configuration.	Float (Note 3-1)
PRT_CTL1	I/O12 (PU)	Port 1 power enable / overcurrent sense When the downstream port is enabled, this pin is set as an input with an internal pull-up resistor applied. The internal pull-up enables power to the downstream port while the pin monitors for an active low overcurrent signal assertion from an external current monitor on USB port 1. This pin will change to an output and be driven low when the port is disabled by configuration or by the host control. **Note:** When PortSplit is disabled, this signal controls both the USB 2.0 and USB 3.2 portions of the port. When PortSplit is enabled, this signal controls the USB 2.0 portion of the port only. **Note 3-5** This pin can be left unused only if Port 1 is disabled via strap/OTP/SMBus/SPI configuration.	Float (Note 3-1)
PRT_CTL4_U3	O12	Port 4 USB 3.2 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.2 portion of the downstream port 4 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.2 device.	Float
PRT_CTL3_U3	O12	Port 3 USB 3.2 PortSplit power enable This signal is an active high control signal used to enable to the USB 3.2 portion of the downstream port 3 when PortSplit is enabled. When PortSplit is disabled, this pin is not used. **Note:** This signal should only be used to control an embedded USB 3.2 device.	Float
GPIO93	I/O12	General Purpose Input/Output	Weak pull-down to GND

3.4 Physical and Logical Port Mapping

The USB72xx family of devices are based upon a common architecture, but all have different modifications and/or pin bond outs to achieve the various device configurations. The base chip is composed of a total of 5 USB3 PHYs and 6 USB2 PHYs. These PHYs are physically arranged on the chip in a certain way, which is referred to as the PHYSICAL port mapping.

The actual port numbering is remapped by default in different ways on each device in the family. This changes the way that the ports are numbered from the USB host's perspective. This is referred to as LOGICAL mapping.

The various configuration options available for these devices may, at times, be with respect to PHYSICAL mapping or LOGICAL mapping. Each individual configuration option which has a PHYSICAL or LOGICAL dependency is declared as such within the register description.

The PHYSICAL vs. LOGICAL mapping is described for all port related pins in Table 3-7. A system design in schematics and layout is generally performed using the pinout in Section 3.1, 100- VQFN Pin Assignments, which is assigned by the default LOGICAL mapping. Hence, it may be necessary to cross reference the PHYSICAL vs. LOGICAL look up tables when determining the hub configuration.

Note: The MPLAB Connect tool makes configuration simple; the settings can be selected by the user with respect to the LOGICAL port numbering. The tool handles the necessary linking to the PHYSICAL port settings. Refer to Section 6.0, Device Configuration for additional information.

TABLE 3-7: USB7205C PHYSICAL VS. LOGICAL PORT MAPPING

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER						
		0	1	2	3	4	5	0	1	2	3	4	6
5	USB2DN_DP1		X						X				
6	USB2DN_DM1		X						X				
7	USB3DN_TXDP1		X						X				
8	USB3DN_TXDM1		X						X				
10	USB3DN_RXDP1		X						X				
11	USB3DN_RXDM1		X						X				
14	USB2DN_DP2			X						X			
15	USB2DN_DM2			X						X			
16	USB3DN_TXDP2			X						X			
17	USB3DN_TXDM2			X						X			
19	USB3DN_RXDP2			X						X			
20	USB3DN_RXDM2			X						X			
27	USB2DN_DP3				X						X		
28	USB2DN_DM3				X						X		
29	USB3DN_TXDP3				X						X		
30	USB3DN_TXDM3				X						X		
32	USB3DN_RXDP3				X						X		
33	USB3DN_RXDM3				X						X		
34	USB2DN_DP4					X						X	
35	USB2DN_DM4					X						X	
36	USB3DN_TXDP4					X						X	
37	USB3DN_TXDM4					X						X	
39	USB3DN_RXDP4					X						X	
40	USB3DN_RXDM4					X						X	
41	USB2DN_DM5						X						X

TABLE 3-7: USB7205C PHYSICAL VS. LOGICAL PORT MAPPING (CONTINUED)

Device Pin	Pin Name (as in datasheet)	LOGICAL PORT NUMBER						PHYSICAL PORT NUMBER					
		0	1	2	3	4	5	0	1	2	3	4	6
42	USB2DN_DP5						X						X
89	USB2UP_DP	X						X					
90	USB2UP_DM	X						X					
91	USB3UP_TXDP	X						X					
92	USB3UP_TXDM	X						X					
94	USB3UP_RXDP	X						X					
95	USB3UP_RXDM	X						X					

4.0 FUNCTIONAL DESCRIPTIONS

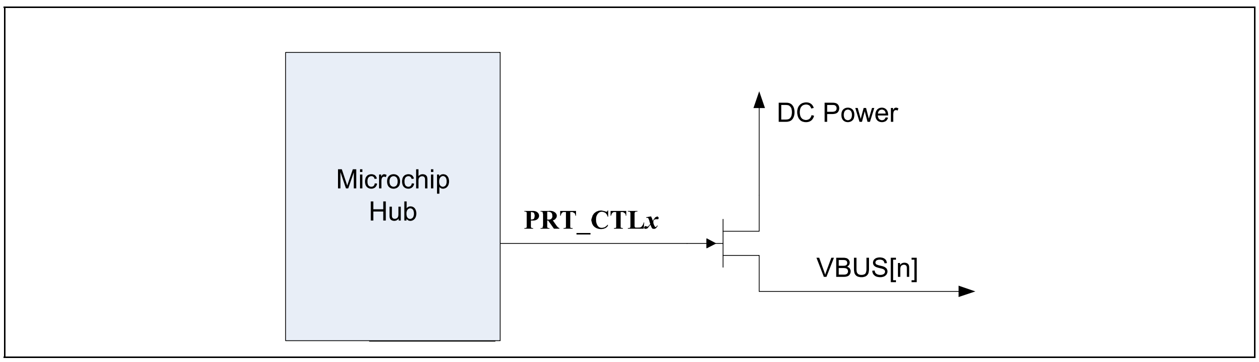
This section details various USB7205C functions, including:

- Downstream Battery Charging
- Port Power Control
- PortSplit
- FlexConnect
- USB to GPIO Bridging
- USB to I2C Bridging
- USB to SPI Bridging
- Link Power Management (LPM)
- Resets

4.1 Downstream Battery Charging

The device can be configured by an OEM to have any of the downstream ports support battery charging. The hub's role in battery charging is to provide acknowledgment to a device's query as to whether the hub system supports USB battery charging. The hub silicon does not provide any current or power FETs or any additional circuitry to actually charge the device. Those components must be provided externally by the OEM.

FIGURE 4-1: BATTERY CHARGING EXTERNAL POWER SUPPLY



If the OEM provides an external supply capable of supplying current per the battery charging specification, the hub can be configured to indicate the presence of such a supply from the device. This indication, via the **PRT_CTL*x*** pins, is on a per port basis. For example, the OEM can configure two ports to support battery charging through high current power FETs and leave the other two ports as standard USB ports.

The port control signals are assigned to programmable pins (**PF*x***) and therefore the device must be programmed into specific configurations to enable the signals. Refer to Section 3.3.3, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

For detailed information on utilizing the battery charging feature, refer to the application note "*USB Battery Charging with Microchip USB720x and USB725x Hubs*", which can be found on the Microchip USB7205C product page www.microchip.com/USB7205C.

4.2 Port Power Control

Port power and over-current sense share the same pin (**PRT_CTLx**) for each port. These functions can be controlled directly from the USB hub, or via the processor.

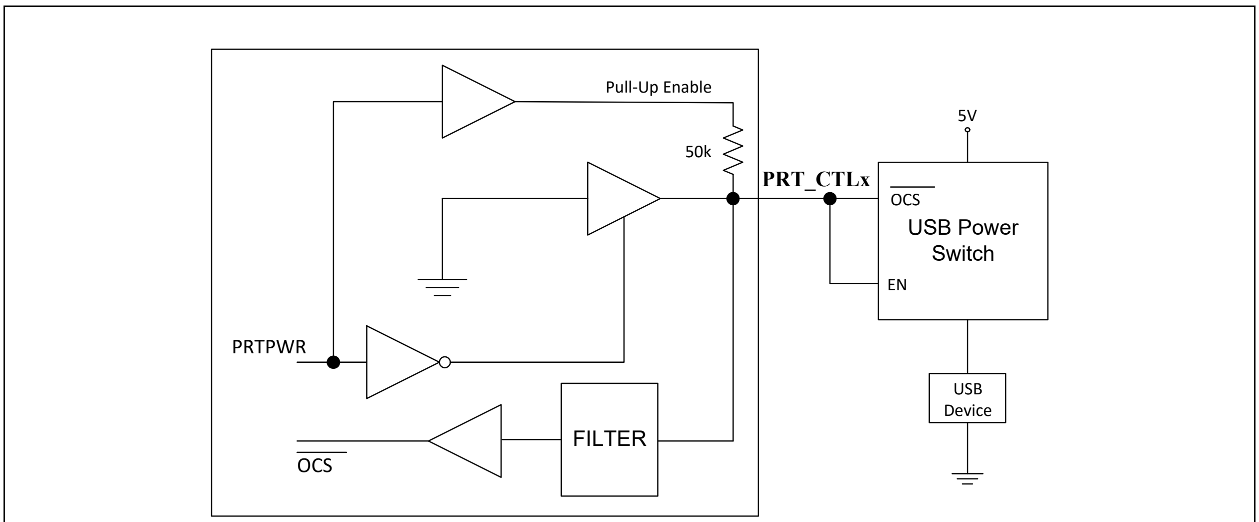
Note:	The **PRT_CTLx** function is assigned to programmable function pins (**PFx**) via configuration straps. Refer to Section 3.3.3, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

4.2.1 PORT POWER CONTROL USING USB POWER SWITCH

When operating in combined mode, the device will have one port power control and over-current sense pin for each downstream port. When disabling port power, the driver will actively drive a '0'. To avoid unnecessary power dissipation, the pull-up resistor will be disabled at that time. When port power is enabled, it will disable the output driver and enable the pull-up resistor, making it an open drain output. If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmidt trigger input will recognize that as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions such as low voltage while the device is powering up.

Note:	An external power switch is the required implementation for Type-C ports due to the requirement that VBUS on Type-C ports must be discharged to 0V when no device is attached to the port.

FIGURE 4-2: PORT POWER CONTROL WITH USB POWER SWITCH

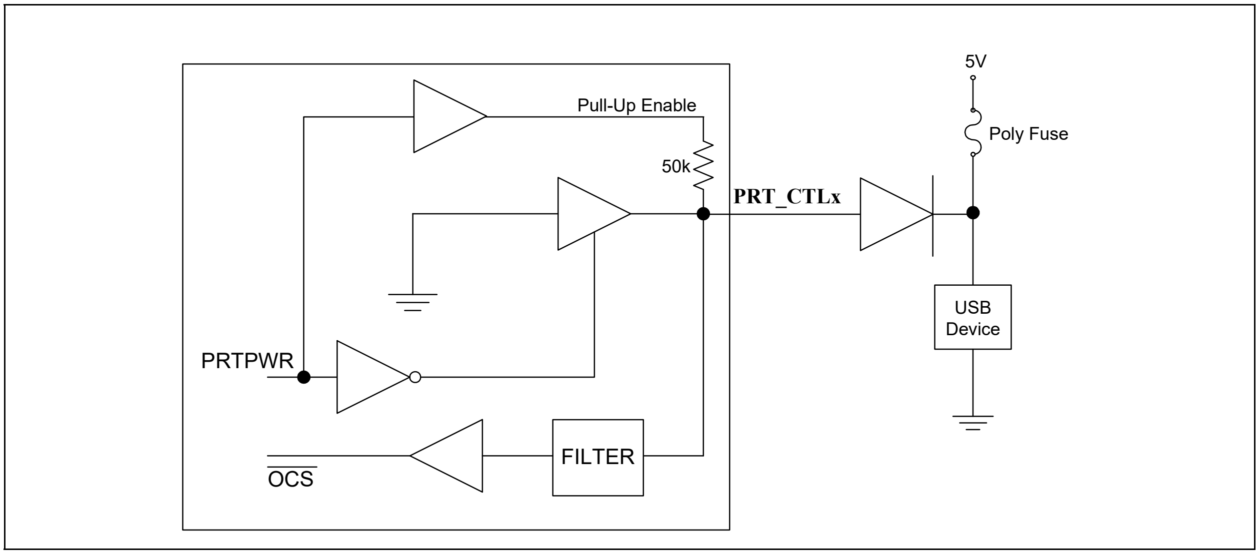


4.2.2 PORT POWER CONTROL USING POLY FUSE

When using the device with a poly fuse, there is no need for an output power control. A single port power control and over-current sense for each downstream port is still used from the Hub's perspective. When disabling port power, the driver will actively drive a '0'. This will have no effect as the external diode will isolate pin from the load. When port power is enabled, it will disable the output driver and enable the pull-up resistor. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to 0 volts. The anode of the diode will be at 0.7 volts, and the Schmidt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

Note:	Type-C ports may not utilize a Poly-Fuse port power implementation due to the requirements that VBUS on Type-C ports must be discharged to 0V when no device is attached to the port.

FIGURE 4-3: PORT POWER CONTROL USING A POLY FUSE



4.3 PortSplit

The PortSplit feature allows the USB 2.0 and USB 3.2 PHYs associated with a downstream port to be operationally separated. The intention of this feature is to allow a system designer to connect an embedded USB 3.x device to the USB 3.2 PHY, while allowing the USB 2.0 PHY to be used as either a standard USB 2.0 port or with a separate embedded USB 2.0 device. PortSplit can be configured via OTP/SMBus. By default, all ports are configured to non-split mode.

When PortSplit is disabled on a specific port, the corresponding **PRT_CTL*x*** pin controls both the USB 2.0 and USB 3.2 portions of the port (port power and overcurrent condition). When PortSplit is enabled on a specific port, the corresponding **PRT_CTL*x*** pin controls the USB 2.0 portion of the port, and the corresponding **PRT_CTL*x*_U3** pin controls the USB 3.2 portion of the port.

4.4 FlexConnect

The device allows the upstream port to be swapped with a downstream port (all downstream ports except the last), enabling another USB port to assume the role of USB host at any time during hub operation. This host role exchange feature is called FlexConnect. Additionally, the USB 2.0 ports can be flexed independently of the USB 3.2 ports.

This functionality can be used in two primary ways:

1. **Host Swapping:** This functionality can be achieved through a hub wherein a host and device can agree to swap the host/device relationship; The host becomes a device, and the device becomes a host.
2. **Host Sharing:** A USB ecosystem can be shared between multiple hosts. Note that only 1 host may access to the USB tree at a time.

FlexConnect can be enabled through any of the following three methods:

- **I²C Control:** The embedded I²C slave can be used to control the state of the FlexConnect feature through basic write/read operations.
- **USB Command:** FlexConnect can be initiated via a special USB command directed to the hub's internal Hub Feature Controller device.
- **Direct Pin Control:** Any available GPIO pin on the hub can be assigned the role of a FlexConnect control pin.

Note:	Direct Pin Control is only available in certain configurations. Refer to Section 3.3.3, PF[31:3] Configuration (CFG_STRAP[2:1]) for additional information.

For detailed information on utilizing the FlexConnect feature, refer to the application note "*USB720x/USB725x FlexConnect Operation*", which can be found on the Microchip USB7205C product page at www.microchip.com/USB7205C.

4.5 USB to GPIO Bridging

The USB to GPIO bridging feature provides system designers expanded system control and potential BOM reduction. General Purpose Input/Outputs (GPIOs) may be used for any general 3.3V level digital control and input functions.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Set the direction of the GPIO (input or output)
- Enable a pull-up resistor
- Enable a pull-down resistor
- Read the state
- Set the state

For detailed information on utilizing the USB to GPIO bridging feature, refer to the application note "*USB to GPIO Bridging with Microchip USB720x and USB725x Hubs*", which can be found on the Microchip USB7205C product page at www.microchip.com/USB7205C.

4.6 USB to I^{2}C Bridging

The USB to I^{2}C bridging feature provides system designers expanded system control and potential BOM reduction. The use of a separate USB to I^{2}C device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to I^{2}C device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Configure I^{2}C Pass-Through Interface
- I^{2}C Write
- I^{2}C Read

For detailed information on utilizing the USB to I^{2}C bridging feature, refer to the application note "*USB to I^{2}C Bridging with Microchip USB720x and USB725x Hubs*", which can be found on the Microchip USB7205C product page at www.microchip.com/USB7205C.

4.7 USB to SPI Bridging

The USB to SPI bridging feature provides system designers expanded system control and potential BOM reduction. The use of a separate USB to SPI device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to SPI device is implemented.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable SPI Pass-Through Interface
- SPI Write/Read
- Disable SPI Pass-Through Interface

For detailed information on utilizing the USB to SPI bridging feature, refer to the application note "*USB to SPI Bridging with Microchip USB720x and USB725x Hubs*", which can be found on the Microchip USB7205C product page at www.microchip.com/USB7205C.

4.8 Link Power Management (LPM)

The device supports the L0 (On), L1 (Sleep), and L2 (Suspend) link power management states. These supported LPM states offer low transitional latencies in the tens of microseconds versus the much longer latencies of the traditional USB suspend/resume in the tens of milliseconds. The supported LPM states are detailed in Table 4-1.

TABLE 4-1: LPM STATE DEFINITIONS

State	Description	Entry/Exit Time to L0
L2	Suspend	Entry: ~3 ms Exit: ~2 ms (from start of RESUME)
L1	Sleep	Entry: <10 µs Exit: <50 µs
L0	Fully Enabled (On)	—

4.9 Resets

The device includes the following chip-level reset sources:

- Power-On Reset (POR)
- External Chip Reset (RESET_N)
- USB Bus Reset

4.9.1 POWER-ON RESET (POR)

A power-on reset occurs whenever power is initially supplied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset per the specifications listed in Section 5.6.2, Power-On and Configuration Strap Timing.

4.9.2 EXTERNAL CHIP RESET (RESET_N)

A valid hardware reset is defined as assertion of RESET_N, after all power supplies are within operating range, per the specifications in Section 5.6.3, Reset and Configuration Strap Timing. While reset is asserted, the device (and its associated external circuitry) enters Standby Mode and consumes minimal current.

Assertion of RESET_N causes the following:

1. The PHY is disabled and the differential pairs will be in a high-impedance state.
2. All transactions immediately terminate; no states are saved.
3. All internal registers return to the default state.
4. The external crystal oscillator is halted.
5. The PLL is halted.

Note: All power supplies must have reached the operating levels mandated in Section 5.2, Operating Conditions**, prior to (or coincident with) the assertion of RESET_N.

4.9.3 USB BUS RESET

In response to the upstream port signaling a reset to the device, the device performs the following:

1. Sets default address to 0.
2. Sets configuration to Unconfigured.
3. Moves device from suspended to active (if suspended).
4. Complies with the USB Specification for behavior after completion of a reset sequence.

The host then configures the device in accordance with the USB Specification.

Note: The device does not propagate the upstream USB reset to downstream devices.

5.0 OPERATIONAL CHARACTERISTICS

5.1 Absolute Maximum Ratings*

Digital Core Supply Voltage (**VCORE**) (Note 1) . . . . -0.5V to +1.25V

+3.3V Supply Voltage (**VDD33**) (Note 1) . . . . -0.5V to +4.6V

Positive voltage on input signal pins, with respect to ground (Note 2) . . . . +4.6V

Negative voltage on input signal pins, with respect to ground . . . . -0.5V

Positive voltage on **XTALI/CLK_IN**, with respect to ground . . . . +3.63V

Positive voltage on USB DP/DM signal pins, with respect to ground . . . . +6.0V

Positive voltage on USB 3.2 Gen 2 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** signal pins, with respect to ground 1.25V

Storage Temperature . . . . -55°C to +150°C

Junction Temperature . . . . +125°C

Lead Temperature Range . . . . Refer to JEDEC Spec. J-STD-020

HBM ESD Performance . . . . +/-3.5 kV

Note 1: When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Note 2: This rating does not apply to the following pins: All USB DM/DP pins, **XTAL1/CLK_IN**, and **XTALO**.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 5.2, Operating Conditions**, Section 5.5, DC Specifications, or any other applicable section of this specification is not implied.

5.2 Operating Conditions**

Digital Core Supply Voltage (**VCORE**) . . . . +1.09V to +1.21V

+3.3V Supply Voltage (**VDD33**) . . . . +3.0V to +3.6V

Input Signal Pins Voltage (Note 2) . . . . -0.3V to +3.6V

XTALI/CLK_IN Voltage . . . . -0.3V to +3.6V

USB 2.0 DP/DM Signal Pins Voltage . . . . -0.3V to +5.5V

USB 3.2 Gen 2 **USB3UP_*xxxx*** and **USB3DN_*xxxx*** Signal Pins Voltage . . . . -0.3V to +1.21V

Ambient Operating Temperature in Still Air (T_A) . . . . Note 3

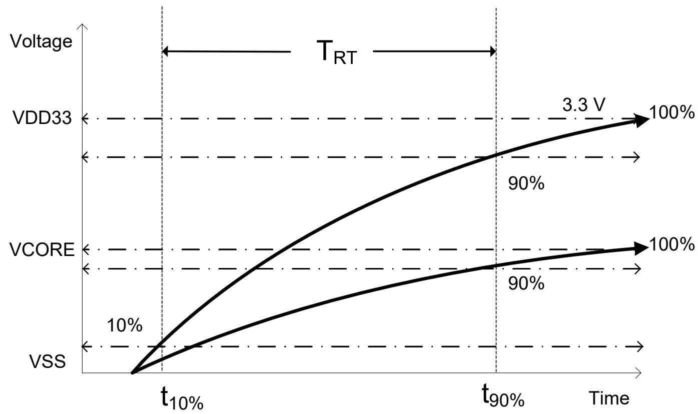
Digital Core Supply Voltage Rise Time (T_{RT} in Figure 5-1) . . . . 5 ms

+3.3V Supply Voltage Rise Time (T_{RT} in Figure 5-1) . . . . 5 ms

Note 3: 0°C to +70°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section. Do not drive input signals without power supplied to the device.

FIGURE 5-1: SUPPLY RISE TIME MODEL



Note:	The Power Supply Rise time requirement does not apply if the **RESET_N** signal is held low during power on and released after power levels rise and stabilize above the power on thresholds, or if the **RESET_N** signal is toggled after power supplies become stable.

5.3 Package Thermal Specifications

TABLE 5-1: 100-VQFN PACKAGE THERMAL PARAMETERS

Symbol	°C/W	Velocity (Meters/s)
Θ_{JA}	19	0
	16	1
	14	2.5
Ψ_{JT}	0.1	0
	0.1	1
Ψ_{JB}	9	0
Θ_{JC}	1.3	0
	1.3	1
Θ_{JB}	10	—

Note:	Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESDN51. For industrial applications, the USB7205C requires multi-layer 2S4P PCB power dissipation.

5.4 Power Consumption

This section details the power consumption of the device as measured during various modes of operation. Power dissipation is determined by temperature, supply voltage, and external source/sink requirements.

TABLE 5-2: DEVICE POWER CONSUMPTION

	Typical (mA) @ 25°C		Typical Power
	VCORE (1.15V)	VDD33 (3.3V)	(mW)
Global Suspend	5.4	2.3	14
VBUS Off	5.3	6.4	27
Reset	4.2	—	5
Data for Calculating Active Transfer Current			
Upstream Port Link Speed Base Currents			
SS+ Current	410	30.8	—
SS Current	370	27.3	—
HS Current	58	19.7	—
Additional Current Per Enabled Port			
SS+ Current	179	11.1	—
SS Current	143	9.1	—
HS Current	1	10.8	—
Example Active Data Transfer Current Calculation: 1 SS+ Port and 2 HS Ports			
Active Data Transfer Current (mA @ 3.3V)	{30.8} + {1 * 11.1} + {2 * 10.8} = 63.5		
Active Data Transfer Current (mA @ 1.15V)	{410} + {1 * 179} + {2 * 1} = 591		

Note: In the Active Idle and Active Data Transfer sections of Table 5-2, the various port configurations are indicated via the following acronyms:

SS+ = USB 3.2 SuperSpeed+ (Gen 2)

SS = USB 3.2 SuperSpeed (Gen 1)

HS = USB 2.0 High Speed

5.5 DC Specifications

TABLE 5-3: I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Units	Notes
I Type Input Buffer						—
Low Input Level	V_{IL}	—	—	0.9	V	
High Input Level	V_{IH}	2.1	—	—	V	
IS Type Input Buffer						—
Low Input Level	V_{IL}	—	—	0.9	V	
High Input Level	V_{IH}	2.1	—	—	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	100	160	240	mV	
O12 Type Output Buffer						
Low Output Level	V_{OL}	—	—	0.4	V	I_{OL} = 12 mA
High Output Level	V_{OH}	**VDD33**-0.4	—	—	V	I_{OH} = -12 mA
OD12 Type Output Buffer						
Low Output Level	V_{OL}	—	—	0.4	V	I_{OL} = 12 mA
ICLK Type Input Buffer (XTALI Input)						Note 4
Low Input Level	V_{IL}	—	—	0.35	V	
High Input Level	V_{IH}	1.1	—	—	V	
IO-U Type Buffer (See Note 5)	—	—	—	—	—	Note 5

Note 4: **XTALI** can optionally be driven from a 25 MHz singled-ended clock oscillator.

Note 5: Refer to the USB 3.2 Gen 2 Specification for USB DC electrical characteristics.

5.6 AC Specifications

This section details the various AC timing specifications of the device.

5.6.1 POWER SUPPLY AND RESET_N SEQUENCE TIMING

There is no specific requirement for power sequencing of **VDD33** and **VCORE** for device operation. Figure 5-2 illustrates the recommended power supply sequencing for ensuring long term reliability of the device. **VCORE** should rise after or at the same time as **VDD33**. Similarly, **RESET_N** and/or **VBUS_DET** should rise after or at the same time as **VDD33**. **VBUS_DET** and **RESET_N** do not have any other timing dependencies. The rise times for **VCORE** and **VDD33** are provided in Section 5.2, Operating Conditions** and Figure 5-1.

FIGURE 5-2: POWER SUPPLY AND RESET_N SEQUENCE TIMING

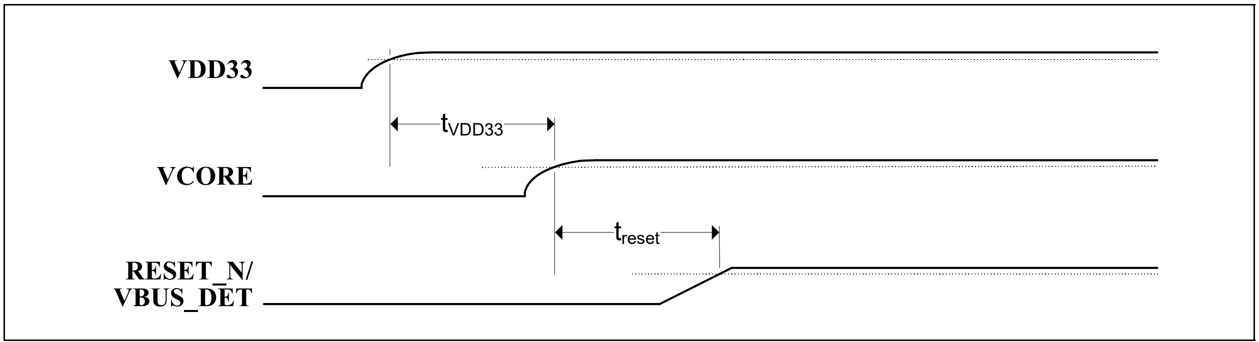


TABLE 5-4: POWER SUPPLY AND RESET_N SEQUENCE TIMING

Symbol	Description	Min	Typ	Max	Units
t_{VDD33}	**VDD33** to **VCORE** rise delay	0	—	—	ms
t_{reset}	**VDD33** to **RESET_N/VBUS_DET** rise delay	0	—	—	ms

5.6.2 POWER-ON AND CONFIGURATION STRAP TIMING

Figure 5-3 illustrates the configuration strap valid timing requirements in relation to power-on, for applications where **RESET_N** is not used at power-on. In order for valid configuration strap values to be read at power-on, the following timing requirements must be met. The operational levels (V_{opp}) for the external power supplies are detailed in Section 5.2, Operating Conditions**.

FIGURE 5-3: POWER-ON CONFIGURATION STRAP VALID TIMING

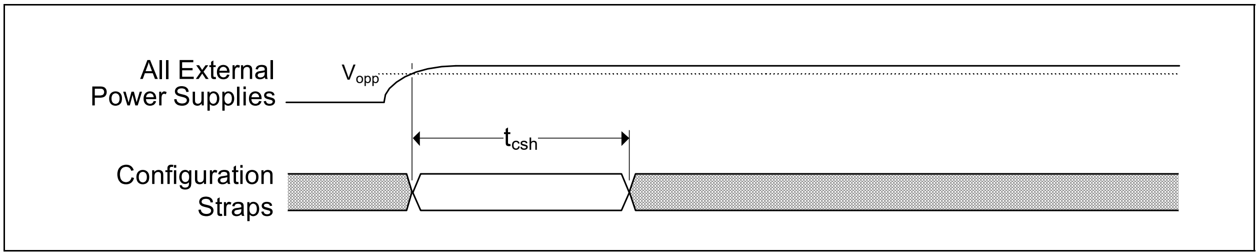


TABLE 5-5: POWER-ON CONFIGURATION STRAP LATCHING TIMING

Symbol	Description	Min	Typ	Max	Units
t_{csh}	Configuration strap hold after external power supplies at operational levels	1	—	—	ms

Device configuration straps are also latched as a result of **RESET_N** assertion. Refer to Section 5.6.3, Reset and Configuration Strap Timing for additional details.

5.6.3 RESET AND CONFIGURATION STRAP TIMING

Figure 5-4 illustrates the **RESET_N** pin timing requirements and its relation to the configuration strap pins. Assertion of **RESET_N** is not a requirement. However, if used, it must be asserted for the minimum period specified. Refer to Section 4.9, Resets for additional information on resets. Refer to Section 3.3, Configuration Straps and Programmable Functions for additional information on configuration straps.

FIGURE 5-4: RESET_N CONFIGURATION STRAP TIMING

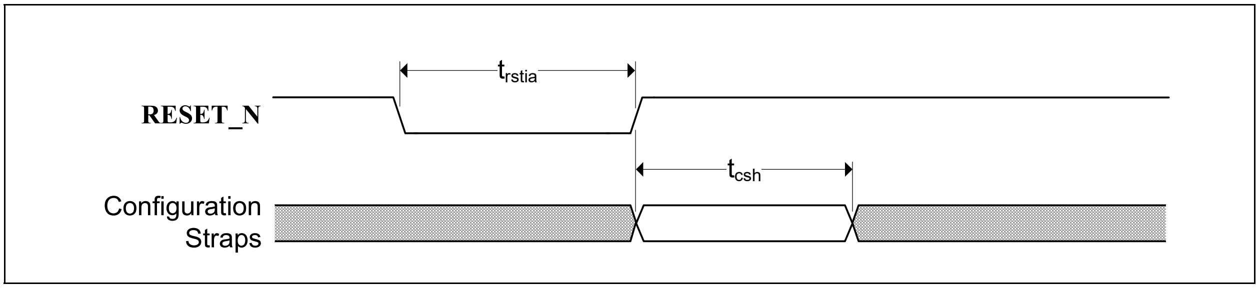


TABLE 5-6: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Units
t_{rstia}	**RESET_N** input assertion time	5	—	—	µs
t_{csh}	Configuration strap pins hold after **RESET_N** deassertion	1	—	—	ms

Note: The clock input must be stable prior to **RESET_N** deassertion.

Configuration strap latching and output drive timings shown assume that the Power-On reset has finished first otherwise the timings in Section 5.6.2, Power-On and Configuration Strap Timing apply.

5.6.4 POWER-ON OR RESET TO SMBUS SLAVE READY TIMING

Figure 5-5 illustrates the SMBus Slave interface readiness in relation to power-on or de-assertion of **RESET_N**. In order to ensure reliable SMBus slave operation, the SMBus master must allow the bus to remain idle until t_{SMBUS_RDY} timing has been met. The operational levels (V_{opp}) for the external power supplies are detailed in Section 5.2, Operating Conditions**.

FIGURE 5-5: POWER-ON OR RESET TO SMBUS SLAVE READY TIMING

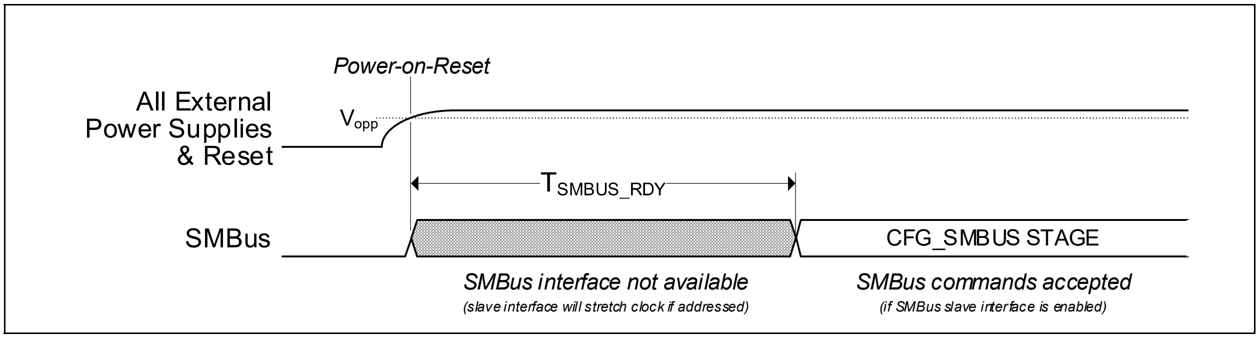


TABLE 5-7: POWER-ON OR RESET TO SMBUS SLAVE READY TIMING

Symbol	Description	Min	Typ	Max	Units
t_{SMBUS_RDY}	Power-on or **RESET_N** deassertion to SMBus ready	40	—	—	ms

5.6.5 USB ATTACH COMMAND TO SMBUS SLAVE READY TIMING

Figure 5-6 illustrates the SMBus Slave interface readiness in relation to ACK of the Slave interface to the “USB Attach with SMBus Runtime Access” (AA56h) from the SMBus Master. In order to ensure reliable SMBus slave operation, the SMBus master must allow the bus to remain idle after issuing the “USB Attach with SMBus Runtime Access” until t_{ATTACH_RDY} timing has been met.

Note:	When accessing SMBus during runtime, it is critical to force some clocks to stay on. If this step is not taken, the SMBus slave interface will not be accessible while the hub is placed into a Suspend state by the host.

FIGURE 5-6: USB ATTACH COMMAND TO SMBUS SLAVE READY TIMING

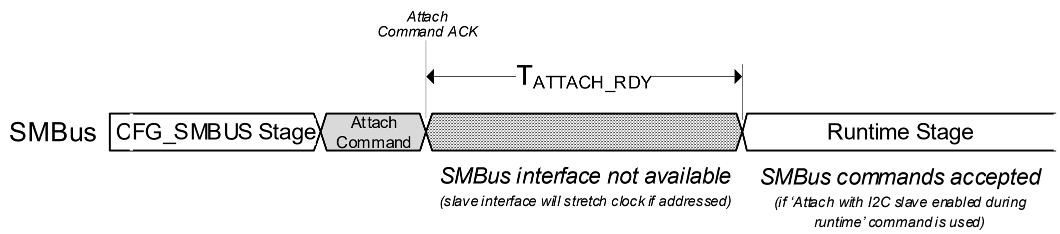


TABLE 5-8: USB ATTACH COMMAND TO SMBUS SLAVE READY TIMING

Symbol	Description	Min	Typ	Max	Units
t_{ATTACH_RDY}	USB Attach command to SMBus ready (Note 6)	11.5	—	—	ms

Note 6: The t_{ATTACH_RDY} values are preliminary and subject to change.

5.6.6 USB TIMING

All device USB signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *Universal Serial Bus Specification*. Please refer to the *Universal Serial Bus Revision 3.2 Specification*, available at http://www.usb.org/developers/docs.

5.6.7 SMBUS TIMING

All device SMBus signals conform to the voltage, power, and timing characteristics/specifications as set forth in the *System Management Bus Specification.* Please refer to the *System Management Bus Specification*, Version 1.0, available at http://smbus.org/specs.

5.6.8 I^{2}C TIMING

All device I^{2}C signals conform to the 100 kHz Standard-mode (Sm) and 400 kHz Fast Mode (Fm) voltage, power, and timing characteristics/specifications as set forth in the *I^{2}C-Bus Specification*. Please refer to the *I^{2}C-Bus Specification*, available at http://www.nxp.com/documents/user_manual/UM10204.pdf.

5.6.9 I^{2}S TIMING

All device I^{2}S signals conform to the voltage, power, and timing characteristics/specifications as set forth in the I^{2}S-Bus Specification. Please refer to the I^{2}S-Bus Specification, available at www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf

5.6.10 SPI/SQI MASTER TIMING

This section specifies the SPI/SQI master timing requirements for the device.

FIGURE 5-7: SPI/SQI MASTER TIMING

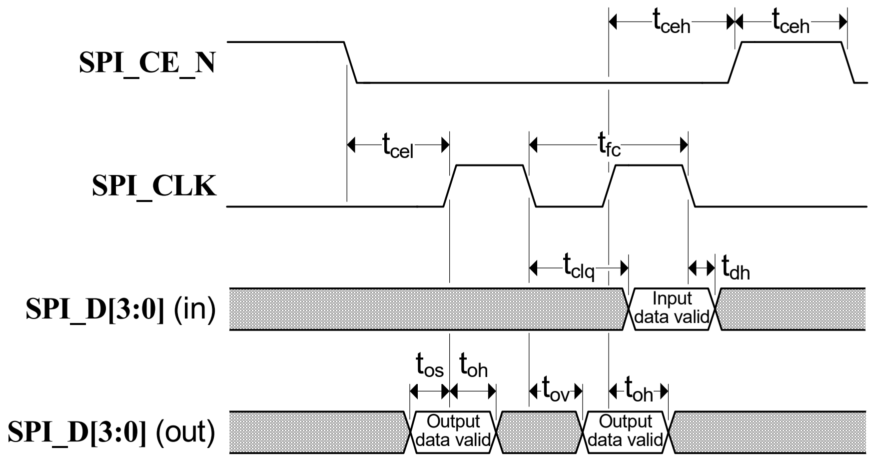


TABLE 5-9: SPI/SQI MASTER TIMING (30 MHZ OPERATION)

Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency	—	—	30	MHz
t_{ceh}	Chip enable (SPI_CE_N) high time	100	—	—	ns
t_{clq}	Clock to input data	—	—	13	ns
t_{dh}	Input data hold time	0	—	—	ns
t_{os}	Output setup time	5	—	—	ns
t_{oh}	Output hold time	5	—	—	ns
t_{ov}	Clock to output valid	4	—	—	ns
t_{cel}	Chip enable (SPI_CE_N) low to first clock	12	—	—	ns
t_{ceh}	Last clock to chip enable (SPI_CE_N) high	12	—	—	ns

TABLE 5-10: SPI/SQI MASTER TIMING (60 MHZ OPERATION)

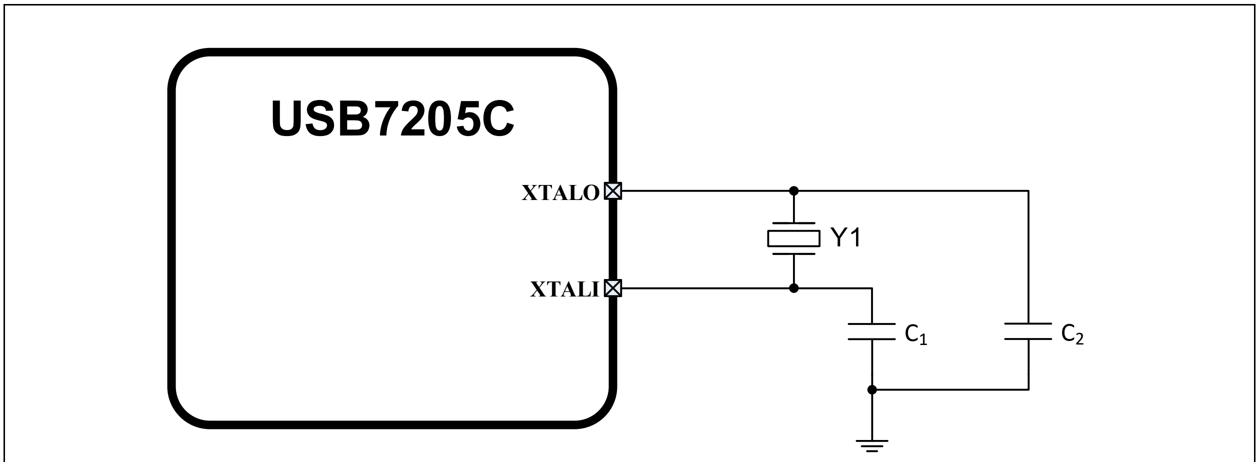
Symbol	Description	Min	Typ	Max	Units
t_{fc}	Clock frequency	—	—	60	MHz
t_{ceh}	Chip enable (SPI_CE_N) high time	50	—	—	ns
t_{clq}	Clock to input data	—	—	9	ns
t_{dh}	Input data hold time	0	—	—	ns
t_{os}	Output setup time	5	—	—	ns
t_{oh}	Output hold time	5	—	—	ns
t_{ov}	Clock to output valid	4	—	—	ns
t_{cel}	Chip enable (SPI_CE_N) low to first clock	12	—	—	ns
t_{ceh}	Last clock to chip enable (SPI_CE_N) high	12	—	—	ns

5.7 Clock Specifications

The device can accept either a 25 MHz crystal or a 25 MHz single-ended clock oscillator input. If the single-ended clock oscillator method is implemented, XTALO should be left unconnected and XTALI/CLK_IN should be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTALI/XTALO). The following circuit design (Figure 5-8) and specifications (Table 5-11) are required to ensure proper operation.

FIGURE 5-8: 25 MHZ CRYSTAL CIRCUIT



5.7.1 CRYSTAL SPECIFICATIONS

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTALI/XTALO). Refer to Table 5-11 for the recommended crystal specifications.

TABLE 5-11: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Units	Notes
Crystal Cut	AT, typ					—
Crystal Oscillation Mode	Fundamental Mode					—
Crystal Calibration Mode	Parallel Resonant Mode					—
Frequency	F_{fund}	—	25.000	—	MHz	—
Frequency Tolerance @ 25°C	F_{tol}	—	—	±50	PPM	—
Frequency Stability Over Temp	F_{temp}	—	—	±50	PPM	—
Frequency Deviation Over Time	F_{age}	—	±3 to 5	—	PPM	Note 7
Total Allowable PPM Budget		—	—	±100	PPM	—
Shunt Capacitance	C_O	—	7 typ	—	pF	—
Load Capacitance	C_L	—	20 typ	—	pF	—
Drive Level	P_W	100	—	—	µW	—
Equivalent Series Resistance	R_1	—	—	60	Ω	—
Operating Temperature Range	—	Note 8	—	Note 9	°C	—
XTALI/CLK_IN Pin Capacitance	—	—	3 typ	—	pF	Note 10
XTALO Pin Capacitance	—	—	3 typ	—	pF	Note 10

Note 7: Frequency Deviation Over Time is also referred to as Aging.

Note 8: 0 °C for commercial version, -40 °C for industrial version.

Note 9: +70 °C for commercial version, +85 °C for industrial version.

Note 10: This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XTALI/CLK_IN** pin, **XTALO** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

5.7.2 EXTERNAL REFERENCE CLOCK (**CLK_IN**)

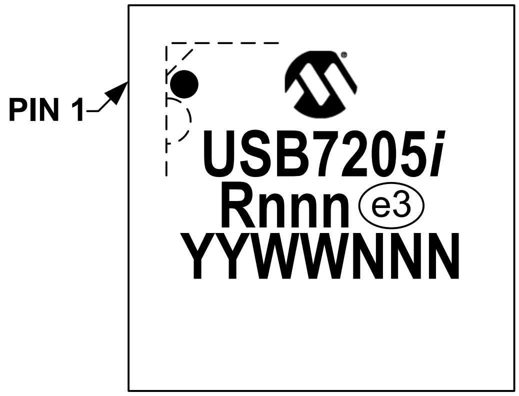
When using an external reference clock, the following clock characteristics are required:

- 25 MHz
- 50% duty cycle ±10%, ±100 ppm
- Jitter < 100 ps RMS

6.0 PACKAGE OUTLINE

6.1 Package Marking Information

100-VQFN (12x12 mm)



Legend:

i	Temperature range designator (Blank = commercial, *i* = industrial)
R	Product revision
nnn	Internal code
e3	Pb-free JEDEC® designator for Matte Tin (Sn)
YY	Year code (last two digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

* Standard device marking consists of Microchip part number, year code, week code and traceability code. For device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

6.2 100-VQFN Package Drawings

Note:	For the most current package drawings, see the Microchip Packaging Specification at: http://www.microchip.com/packaging.

FIGURE 6-1: 100-VQFN PACKAGE (DRAWING)

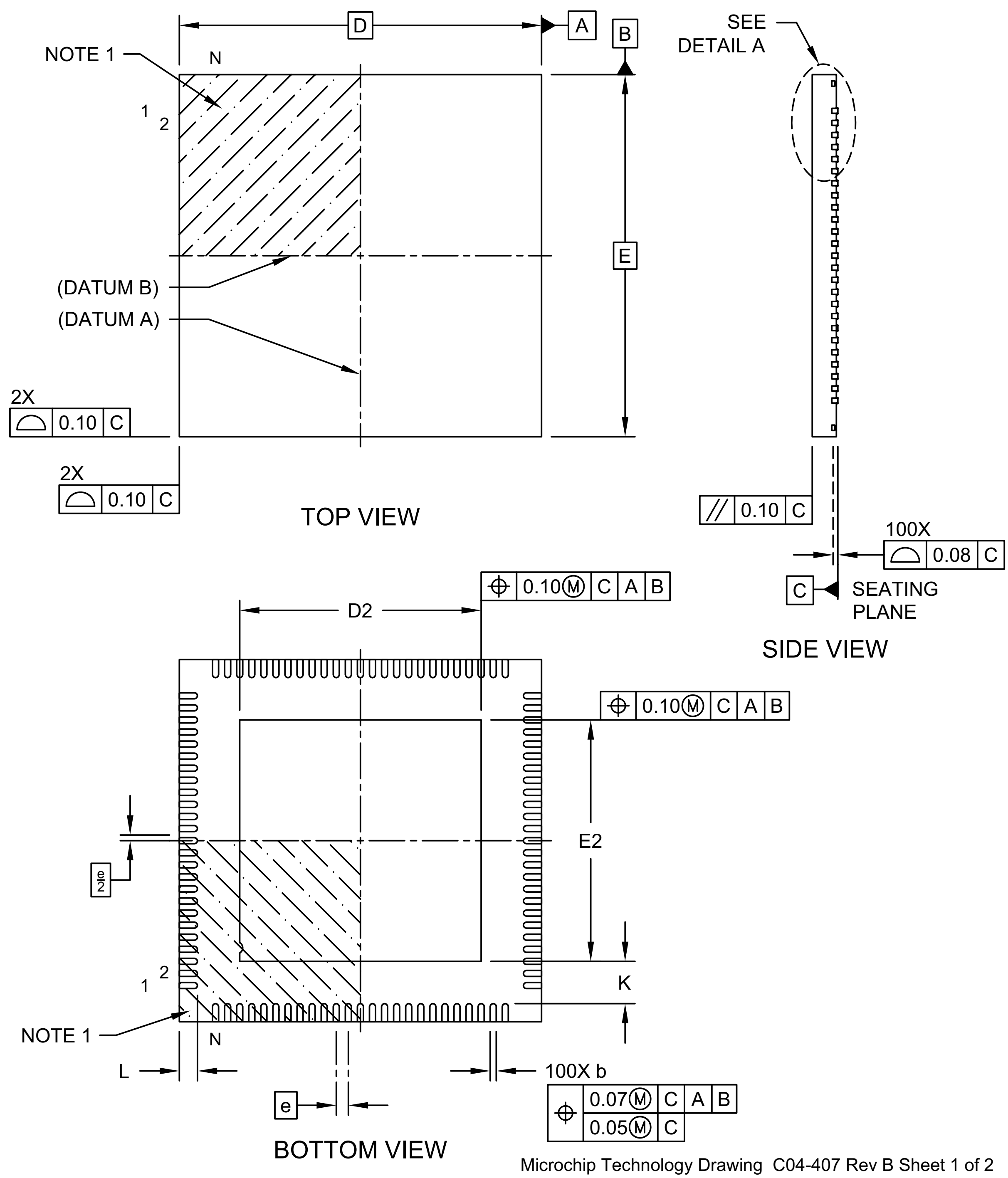


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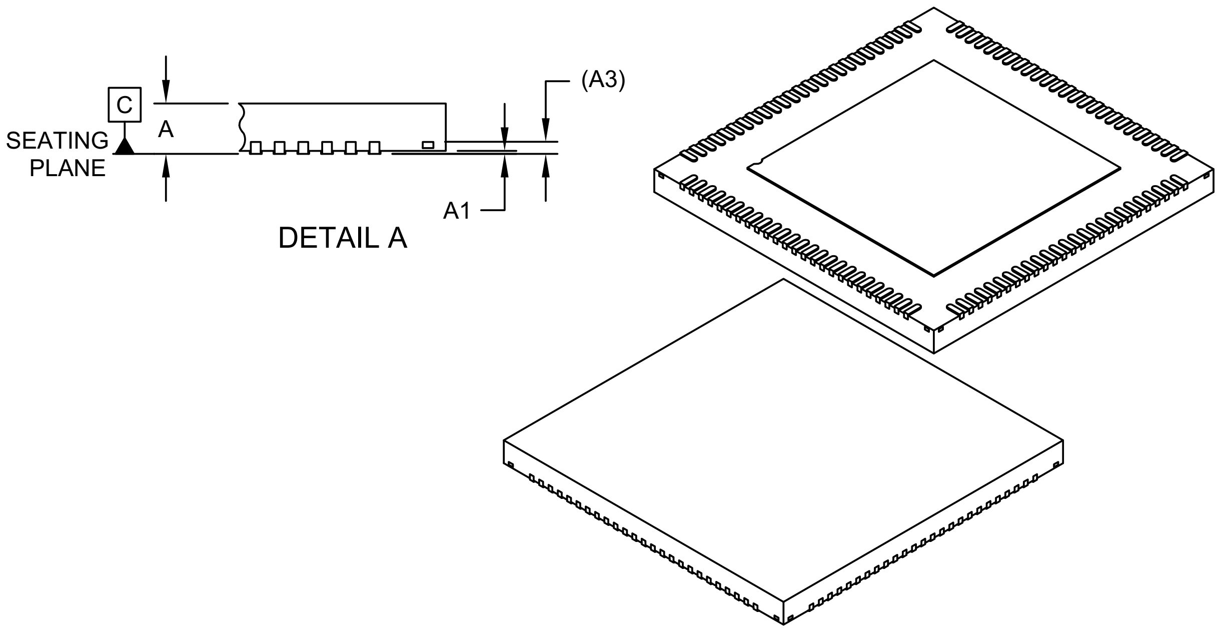
FIGURE 6-2: 100-VQFN PACKAGE (DIMENSIONS)



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		12.00 BSC	
Exposed Pad Length	D2	7.90	8.00	8.10
Overall Width	E		12.00 BSC	
Exposed Pad Width	E2	7.90	8.00	8.10
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	1.30	-	-

Notes:

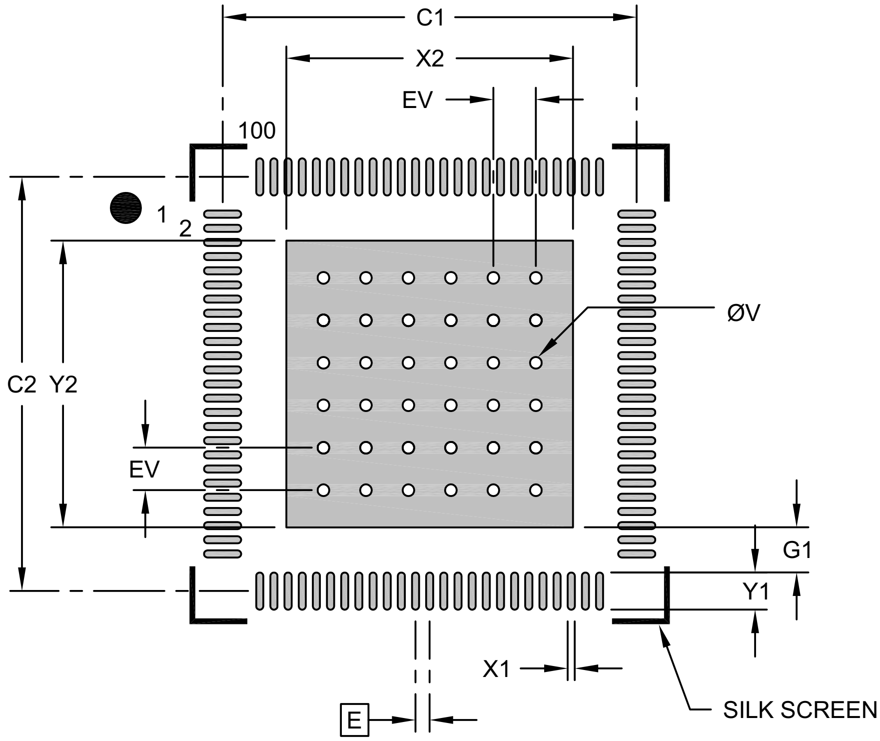
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-407 Rev B Sheet 2 of 2

FIGURE 6-3: 100-VQFN PACKAGE (LAND PATTERN)



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			8.10
Optional Center Pad Length	Y2			8.10
Contact Pad Spacing	C1		11.70	
Contact Pad Spacing	C2		11.70	
Contact Pad Width (X100)	X1			0.20
Contact Pad Length (X100)	Y1			1.05
Contact Pad to Center Pad (X100)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2407A

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
00005227D (09-29-25)	Cover	Added trademark symbol to PHYBoost™ and-VariSense™
	Figure 3-1, "USB7205C 100-VQFN Pin Assignments", Table 3-1, "Pin Descriptions", Section 3.3, Configuration Straps and Programmable Functions, Section 5.1.4, Configuration Strap Read Stage (CFG_STRAP)	Removal of Port Disable Configuration Strap options.
	Table 3-1, "Pin Descriptions"	The status of the USB 2.0 Interfaces Downstream Ports “If Unused” column has been updated from “Connect directly to 3.3V” to “Float”.
00005227C (01-15-25)	Throughout document.	Removal of 132-Pin Package option.
	Highlights	Added Celsius temperature ranges to description of Commercial and Industrial support.
	Key Benefits	Added Windows 11 compatibility.
	Table 3-1, "Pin Descriptions"	Description for pin VBUS_MON_UP removed.
	Table 3-1, "Pin Descriptions"	The following note for pin VBUS_DET has been removed: “Pull down will disable entire device chip.“
	Table 5-2, "Device Power Consumption"	Device Power Consumption number updated.
00005227B (05-22-24)	Section 4.0, Device Connections, Section 5.0, Modes of Operation, Section 6.0, Device Configuration, Section 7.0, Device Interfaces	Reinserted chapters not present in previous revision.
	Highlights	FlexConnect feature bullet changed from "The roles of the upstream and all downstream ports are reversible on command” to “The roles of the upstream and downstream ports are reversible on command”.

TABLE A-1: REVISION HISTORY (CONTINUED)

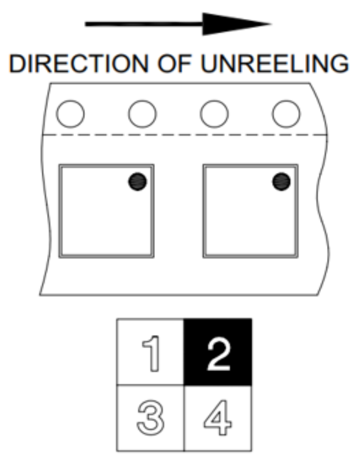
Revision Level & Date	Section/Figure/Entry	Correction
	Section 5.1.7, OTP Configuration Stage (CFG_OTP)	Section rewritten for clarity. Previously stated: “Once the SOC has indicated that it is done with configuration, all configuration data is combined in this stage. The default data, the SOC configuration data, and the OTP data are all combined in the firmware and the device is programmed.” Now states: “All configuration data from CFG_ROM, CFG_STRAP, CFG_SMBUS stages, and OTP or Pseudo OTP (when SPI firmware is used) are combined in this stage. If a register is modified in both the CFG_SMBUS stage and OTP/Pseudo OTP, the OTP data overwrites SMBus data when executing from ROM firmware, while SMBus data overwrites Pseudo OTP data when executing from SPI firmware. Note that when executing from SPI firmware, the internal OTP content is ignored except for USB2/USB3 UUID data and trim registers for PHY settings.”
	Figure 5-1	Updated to remove Configuration 1.
	Section 5.1.8, Hub Connect Stage (USB_ATTACH)	Section rewritten for clarity. Previously stated: “Once the hub registers are updated through default values, SMBus master, and OTP, the device firmware will enable attaching the USB host by setting the USB_ATTACH bit in the HUB_CMD_STAT register (for USB 2.0) and the USB3_HUB_ENABLE bit (for USB 3.2). The device will remain in the Hub Connect stage indefinitely.” Now states: “After updating the hub registers in CFG_OTP stage, the firmware enables the USB host attachment by setting the USB_ATTACH bit in the HUB_CMD_STAT register for USB 2.0 and the USB3_HUB_ENABLE bit for USB 3.2. The device remains in this USB_ATTACH stage indefinitely until it gets enumerated by a USB Host.”
	Section 4.4, FlexConnect	First sentence changed from “The device allows the upstream port to be swapped with any downstream port, enabling any USB port to assume the role of USB host at any time during hub operation” to “The device allows the upstream port to be swapped with a downstream port (all downstream ports except the last), enabling another USB port to assume the role of USB host at any time during hub operation.”
	Figure 5-5 and Figure 5-6	Changed “SOC_CFG” to “CFG_SMBUS” in both diagrams.
DS00005227A (12-13-23)		Initial Release

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	-	[X]	/	XXX
Device	Tape and Reel Option		Temperature Range		Package

Device:	USB7205C
Tape and Reel Option:	Blank = Standard packaging (tray) T = Tape and Reel (Note 1)
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)
Package:	KDX = 100-pin VQFN



Examples:

a) USB7205C/KDX
Tray, 0°C to +70°C, 100-pin VQFN

b) USB7205CT/KDX
Tape & reel, 0°C to +70°C, 100-pin VQFN

c) USB7205C-I/KDX
Tray, -40°C to +85°C, 100-pin VQFN

d) USB7205CT-I/KDX
Tape & reel, -40°C to +85°C, 100-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.