8-Bit I2C-Bus and SMBus Low Power I/O Port with Interrupt and Reset

Features

- Operation Power Supply Voltage from 2.3V to 5.5V
- 8-bit I^2C-bus GPIO with Interrupt and Reset
- 5V Tolerant I/Os
- Active Low Interrupt Output
- Active Low Reset Input
- Polarity Inversion Register
- Low Current Consumption
- 0Hz to 400KHz Clock Frequency
- Noise Filter on SCL/SDA Inputs
- Power-on Reset
- ESD Protection (4KV HBM and 1KV CDM)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions
- Packaging (Pb-free & Green available):
  - TSSOP-16 (L)
  - TQFN 4x4-16 (ZY)

Description

The DIODES™ PI4IOE5V9538 provides 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I^2C-bus/ SMBus applications. It includes the features such as higher driving capability, 5V tolerance, lower power supply, individual I/O configuration, and smaller packaging. It provides a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PI4IOE5V9538 consists of an 8-bit register to configure the I/Os as either inputs or outputs, and two 8-bit polarity registers to change the polarity of the input port register data. The data for each input or output is kept in the corresponding Input port or Output port register. All registers can be read by the system master.

The PI4IOE5V9538 open-drain interrupt output ($\overline{INT}$) is activated when any input state and is used to indicate the system master that an input state has changed.

The power-on reset sets the registers to their default values and initializes the device state machine. The Reset pin causes the same reset/initialization to occur without de-powering the device.

Two hardware pins (A0 and A1) vary the fixed I2C-bus address and allow up to four devices to share the same I2C-bus/SMBus.

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Configuration

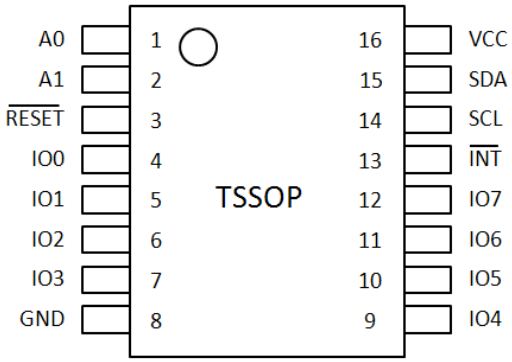


Figure 1: TSSOP-16 (Top View)

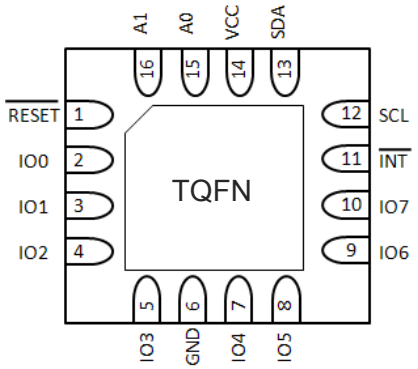


Figure 2: TQFN 4x4-16 (Top View)

Pin Description

TSSOP Pin#	TDFN Pin #	Name	Type	Description
1	15	A0	I	address input 0
2	16	A1	I	address input 1
3	1	$\overline{\text{RESET}}$	I	Reset pin
4	2	IO0	I/O	input/output 0
5	3	IO1	I/O	input/output 1
6	4	IO2	I/O	input/output 2
7	5	IO3	I/O	input/output 3
8	6	GND	G	supply ground
9	7	IO4	I/O	input/output 4
10	8	IO5	I/O	input/output 5
11	9	IO6	I/O	input/output 6
12	10	IO7	I/O	input/output 7
13	11	$\overline{\text{INT}}$	O	Interrupt output (open-drain)
14	12	SCL	I/O	Serial clock line
15	13	SDA	I/O	Serial data line
16	14	VCC	P	Power supply

* I = Input; O = Output; P = Power; G = Ground

Maximum Ratings

Power Supply	-0.5V to +6.0V
Voltage on an I/O Pin	GND-0.5V to +6.0V
Input Current	±20mA
Output Current on an I/O Pin	±50mA
Supply Current	85mA
Ground Supply Current	100mA
Total Power Dissipation	200mW
Operation Temperature	-40~85℃
Storage Temperature	-65~150℃
Maximum Junction Temperature ,Tj (max)	125℃

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Static Characteristics

VCC = 2.3 V to 5.5 V; GND = 0 V; Tamb= -40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
V_{CC}	Supply voltage		2.3	-	5.5	V
I_{CC}	Supply current	Operating mode; VCC = 5.5 V; no load; fSCL= 400 kHz	-	40	60	µA
		Operating mode; VCC = 2.3 V; no load; fSCL= 400 kHz		10	20	µA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; VI = GND; fSCL= 0 kHz; I/O = inputs	-	0.25	1	µA
I_{stb}	Standby current	Standby mode; VCC = 5.5 V; no load; VI = VCC; fSCL= 0 kHz; I/O = inputs		0.25	1	µA
V_{POR}	Power-on reset voltage [1]		-	1.16	1.41	V
Input SCL, Input/Output SDA						
V_{IL}	Low level input voltage		-0.5	-	+0.3VCC	V
V_{IH}	High level input voltage		0.7VCC	-	5.5	V
I_{OL}	Low level output current	V_{OL}=0.4V	3	7	-	mA
I_L	Leakage current	V_I=VCC=GND	-1	-	1	µA
C_i	Input capacitance	V_I =GND	-	5	10	pF
I/Os						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_{OL}	Low level output current	VCC = 2.3 V; V_{OL} = 0.5 V[2]	8	10	-	mA
		VCC = 2.3 V; V_{OL} = 0.7 V[2]	10	13	-	mA
		VCC = 3.0 V; V_{OL} = 0.5 V[2]	8	14	-	mA
		VCC = 3.0 V; V_{OL} = 0.7 V[2]	10	19	-	mA
		VCC = 4.5 V; V_{OL} = 0.5 V[2]	8	17	-	mA
		VCC =4.5 V; V_{OL} = 0.7 V[2]	10	24	-	mA
V_{OH}	High level output voltage	I_{OH}=-8mA;VCC=2.3V[3]	1.8	-	-	V
		I_{OH}=-10mA;VCC=2.3V[3]	1.7	-	-	V
		I_{OH}=-8mA;VCC=3.0V[3]	2.6	-	-	V
		I_{OH}=-10mA;VCC=3.0V[3]	2.5	-	-	V
		I_{OH}=-8mA;VCC=4.75V[3]	4.1	-	-	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
		I_{OH}=-10mA;VCC=4.75V[3]	4.0	-	-	V
I_{LI}	Input leakage current	VCC=3.6V; V_I=VCC=GND	-1	-	1	μA
C_i	Input capacitance		-	5	10	pF
Interrupt $\overline{INT}$						
I_{OL}	Low level output current	V_{OL}=0.4V	3	13	-	mA
I_{OH}	High level input voltage	V_{OL}=0.4V	-1		+1	μA
Select Inputs A0,A1 and $\overline{RESET}$						
V_{IL}	Low level input voltage		-0.5	-	+0.81	V
V_{IH}	High level input voltage		+1.8	-	5.5	V
I_L	Input leakage current	V_I=VCC=GND	-1		1	μA

Note:
[1]: VCC must be lowered to 0.2 V for at least 5 us in order to reset part.
[2]: Each I/O must be externally limited to a maximum of 25 mA and each octal (IO0 to IO7) must be limited to a maximum current of 100 mA for a device total of 200 mA.
[3]: The total current sourced by all I/Os must be limited to 160 mA.

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Standard mode I²C		Fast mode I²C		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{VD;ACK}$[1]	data valid acknowledge time		-	3.45	-	0.9	µs
$t_{HD;DAT}$[2]	data hold time		0	-	0	-	ns
$t_{VD;DAT}$	data valid time		-	3.45	-	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
t_f	fall time of both SDA and SCL signals		-	300	-	300	ns
t_r	rise time of both SDA and SCL signals		-	1000	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port Timing							
$t_{v(Q)}$	Data output valid time[4]		-	200	-	200	ns
$t_{su(D)}$	Data input set-up time		100	-	100	-	ns
$t_{h(D)}$	Data input hold time		1	-	1	-	µs
Interrupt Timing							
$t_{v(INT)}$	Valid time on pin $\overline{INT}$		-	4	-	4	µs
$t_{rst(INT)}$	Reset time on pin $\overline{INT}$		-	4	-	4	µs
$\overline{RESET}$ **Timing**							
$t_{w(rst)}$	Reset pulse width		25	-	25	-	ns
$t_{vrec(rst)}$	Reset recovery time[5]		0	-	0	-	ns
T_{rst}	Reset time		1	-	1	-	us

Note:
[1]: $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
[2]: $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
[3]: C_b = total capacitance of one bus line in pF.
[4]: $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.
[5]: To reset the device while actively communicating on the bus may cause glitches or errant STOP conditions. Upon reset, the full delay will be the sum of t_{rst} and RC time constant of SDA bus.

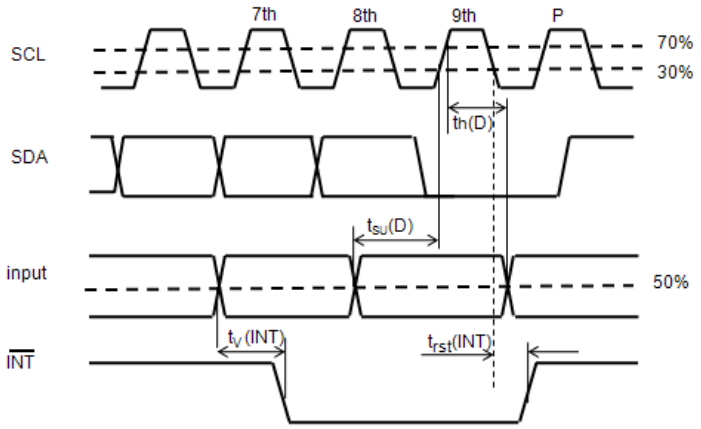
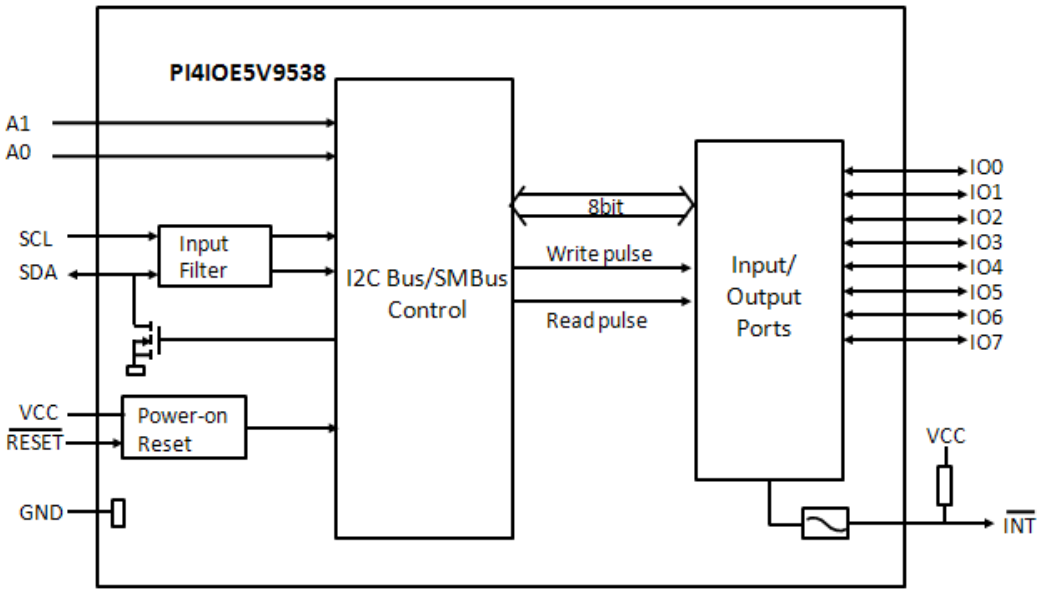


Figure 3: Timing Parameters for INT Signal

Block Diagram

Figure 4: Block Diagram of PI4IOE5V9538



Note: All I/Os are set to inputs at reset.

Details Description

a. Device Address

Table 1: Device Address

	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Address Byte	1	1	1	0	0	A1	A0	R/W

Note: Read "1", Write "0"

b. Registers

i. Command Byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Table 2: Command Byte

Command	Register
0	Input port register
1	Output port register
2	Polarity inversion register
3	Configuration register

ii. Register 0: Input Port Registers

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 2. Writes to this register have no effect.
The default value 'X' is determined by the externally applied logic level.

Table 3: Input Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	I7	I6	I5	I4	I3	I2	I1	I0
Default	X	X	X	X	X	X	X	X

iii. Register 1:Output Port Register

This register is an output-only port. It reflects the outgoing logic levels of the pins defined as outputs by Registers 3. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 4: Output Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	O7	O6	O5	O4	O3	O2	O1	O0
Default	1	1	1	1	1	1	1	1

iv. Register 2: Polarity Inversion Register

This register allows the user to invert the polarity of the Input port register data. If a bit in this register is set (written with '1'), the Input port data polarity is inverted. If a bit in this register is cleared (written with a '0'), the Input port data polarity is retained.

Table 5: Polarity Inversion Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	N7	N6	N5	N4	N3	N2	N1	N0
Default	0	0	0	0	0	0	0	0

v. Register 3: Configuration Registers

This register configures the directions of the I/O pins. If a bit in this register is set (written with '1'), the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared (written with '0'), the corresponding port pin is enabled as an output. At reset, the IOs are configured as inputs.

Table 6: Configuration Port 0 Register

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	1	1	1	1	1

c. Power-On Reset

When power is applied to VCC, an internal power-on reset holds the PI4IOE5V9538 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V9538 registers and SMBus state machine will initialize to their default states. Thereafter, VCC must be lowered below 0.2 V to reset the device. For a power reset cycle, VCC must be lowered below 0.2 V and then restored to the operating voltage.

d. RESET Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of tw(rst). The PI4IOE5V9538 registers and SMBus/I2C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH. This input requires a pull-up resistor to VDD if no active connection is used.

e. Interrupt Output

The open-drain interrupt output ($\overline{\text{INT}}$) is activated when one of the port pins changes state and the pin is configured as an input.

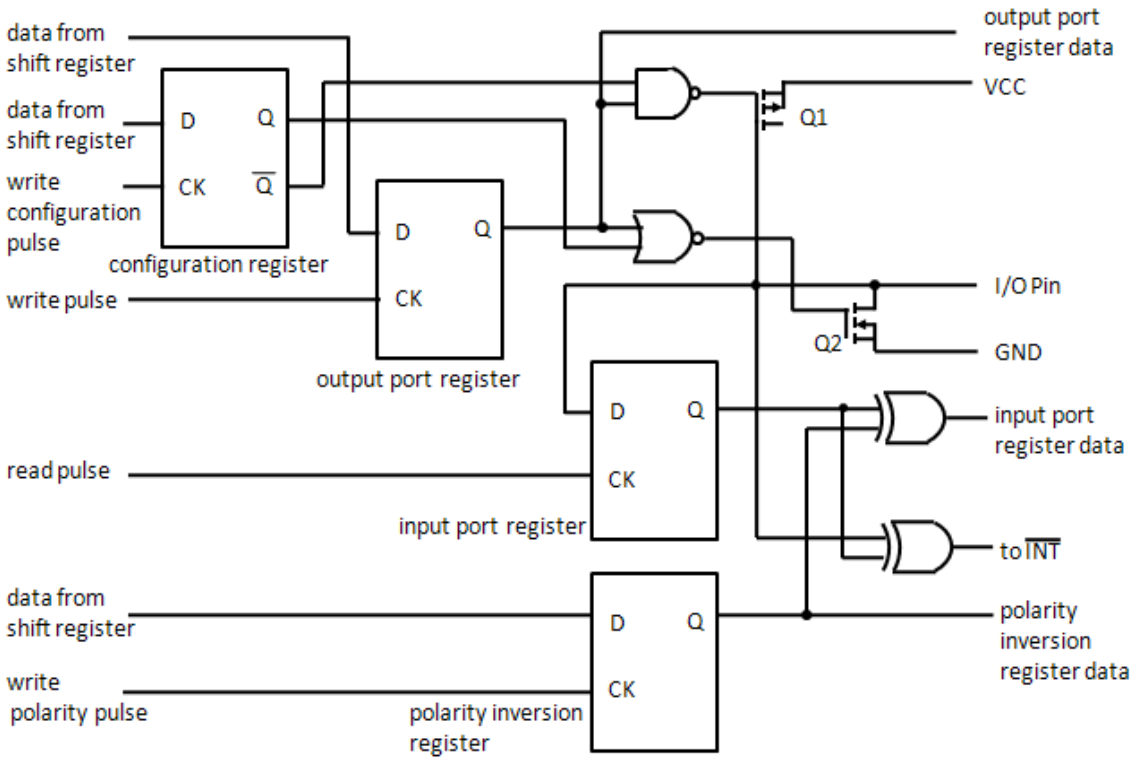
The interrupt is de-activated when the input returns to its previous state or the Input Port register is read.
Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the input Port register.

f. I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above VCC to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is on, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance path that exists between the pin and either VCC or GND.

Figure 5: Simplified Schematic of I/Os



After power-on reset, all registers return to default values.

g. Bus Transaction

Data is transmitted to the PI4IOE5V9538 using the Write mode as shown in Figure 6. Data is read from the PI4IOE5V9538 using the read mode as shown in Figure 8. These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

Figure 6: Write to Output Registers

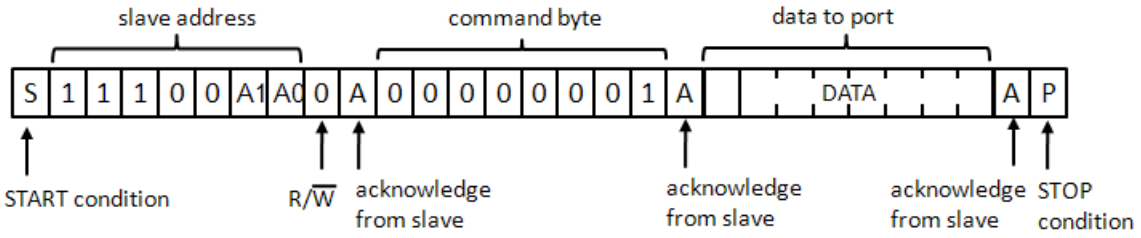


Figure 7: Write to Polarity Inversion Registers

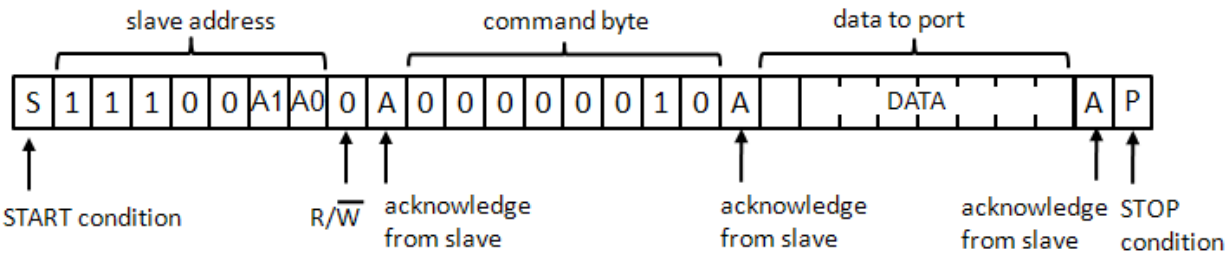
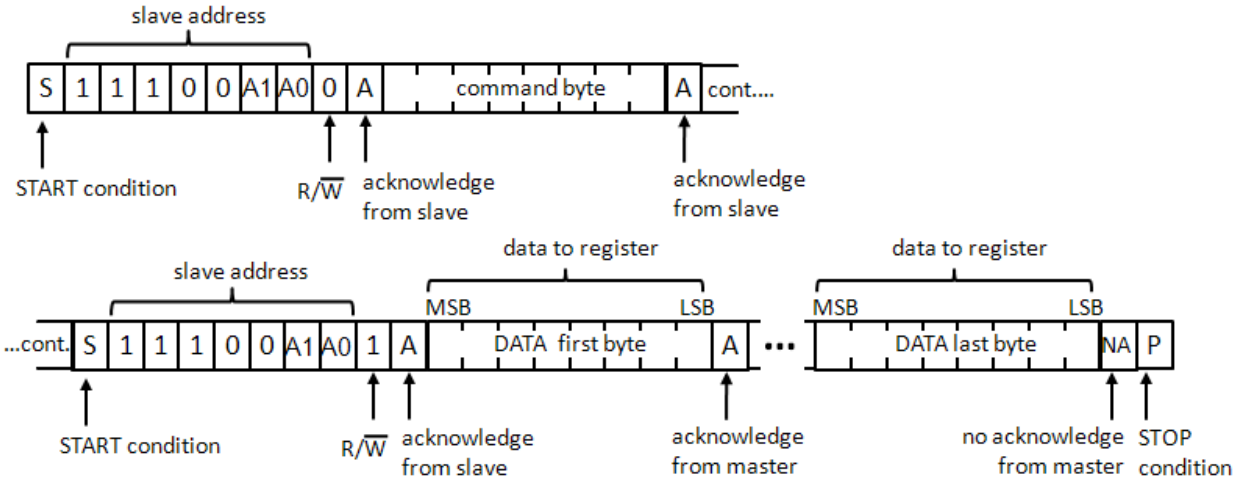
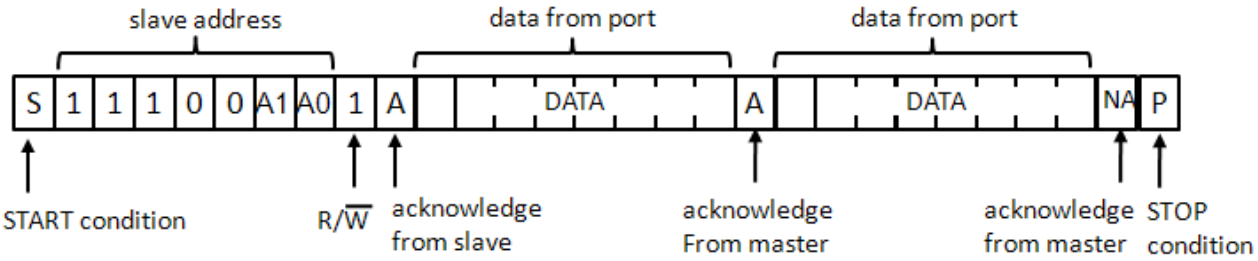


Figure 8: Read from Registers



Note: Transfer can be stopped at any time by a STOP condition.

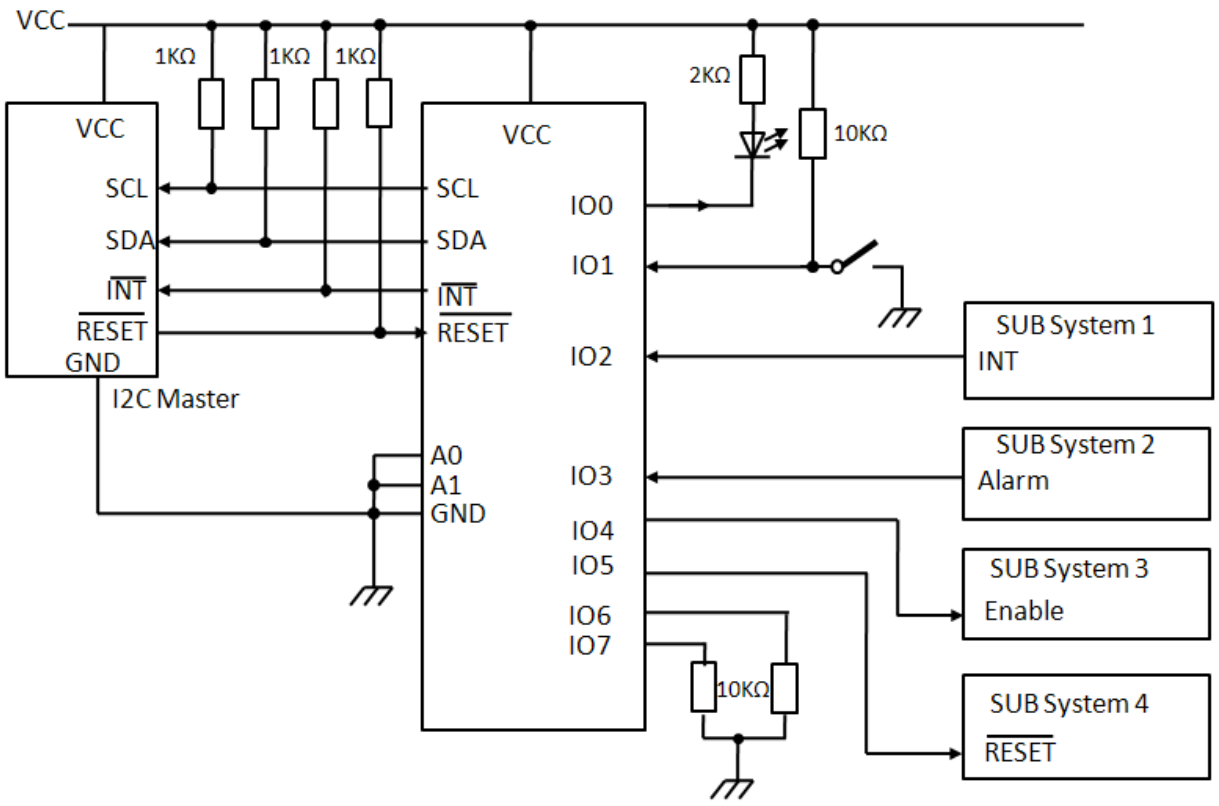
Figure 9: Read Input Port Register



Note: Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read Input Port register).

Application Design-in Information

Figure 10: Typical Application



IO0, IO4, IO5, IO6, IO7 configured as outputs.
IO1, IO2, IO3 configured as inputs.

Minimizing ICC when the I/Os are used to control LEDS

When the I/Os are used to control LEDs, they are normally connected to VCC through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than VCC. The supply current, ICC, increases as V_I becomes lower than VCC.

Designs need minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to VCC when the LED is off. Figure 11 shows a high value resistor in parallel with the LED. Figure 12 shows VCC less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above VCC and prevent additional supply current consumption when the LED is off.

Figure 11: High Value Resistor in Parallel with the LED

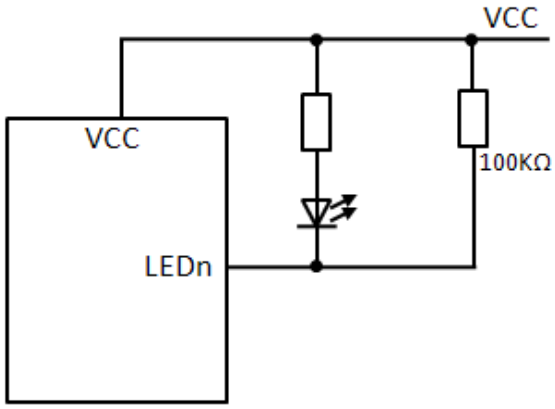
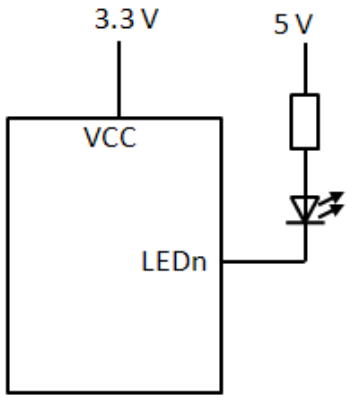


Figure 12: Device Supplied by a Lower Voltage



Part Marking

L Package

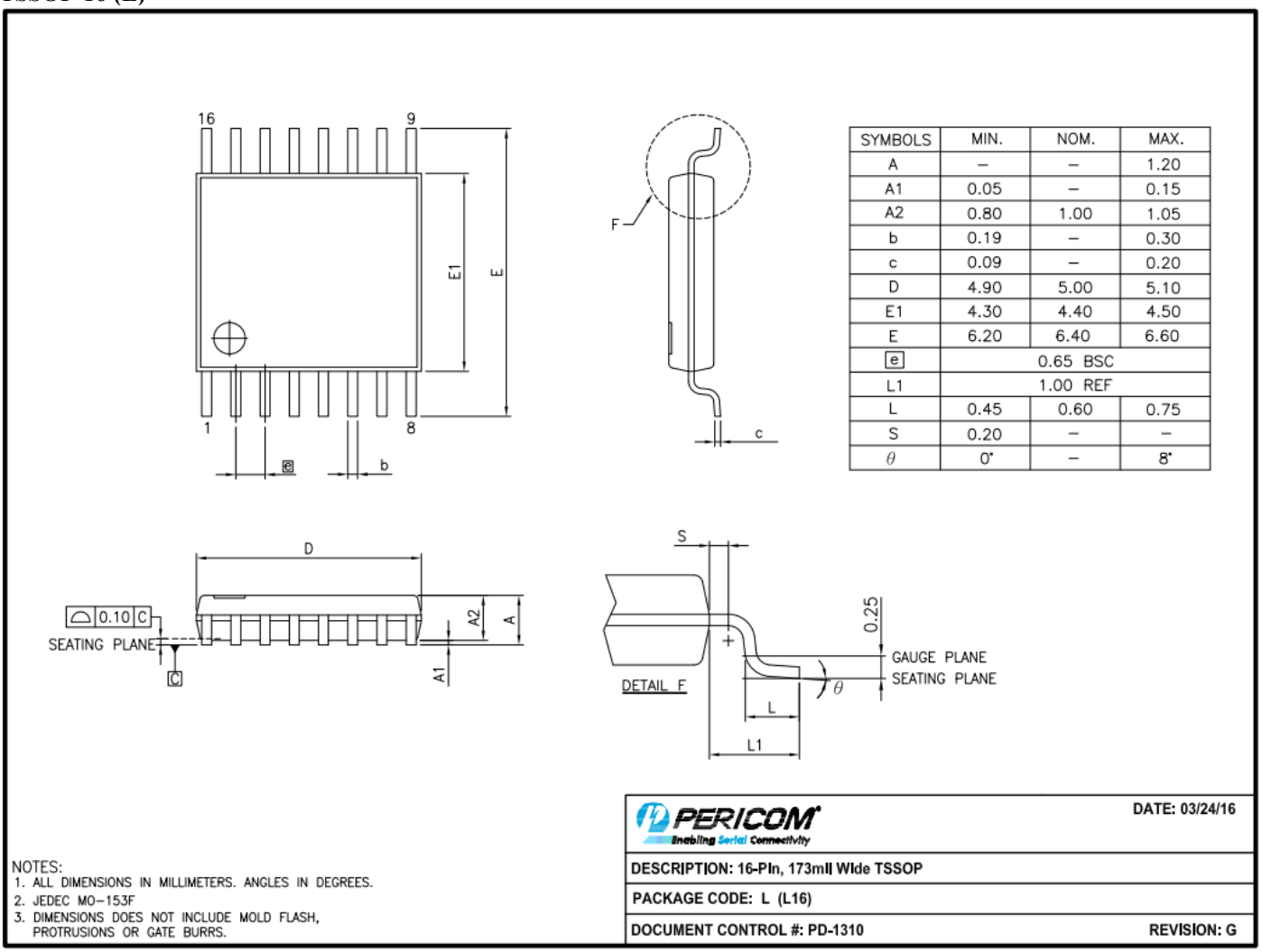
Z: Die Rev
Y: Year
W: Workweek
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above fab code means Cu wire

ZY Package

Z: Die Rev
Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Fab Site Code
Bar above 2nd "X" means Cu wire

Packaging Mechanical

TSSOP-16 (L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

NOTES:
1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.
2. JEDEC MO–153F
3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

PERICOM Enabling Serial Connectivity

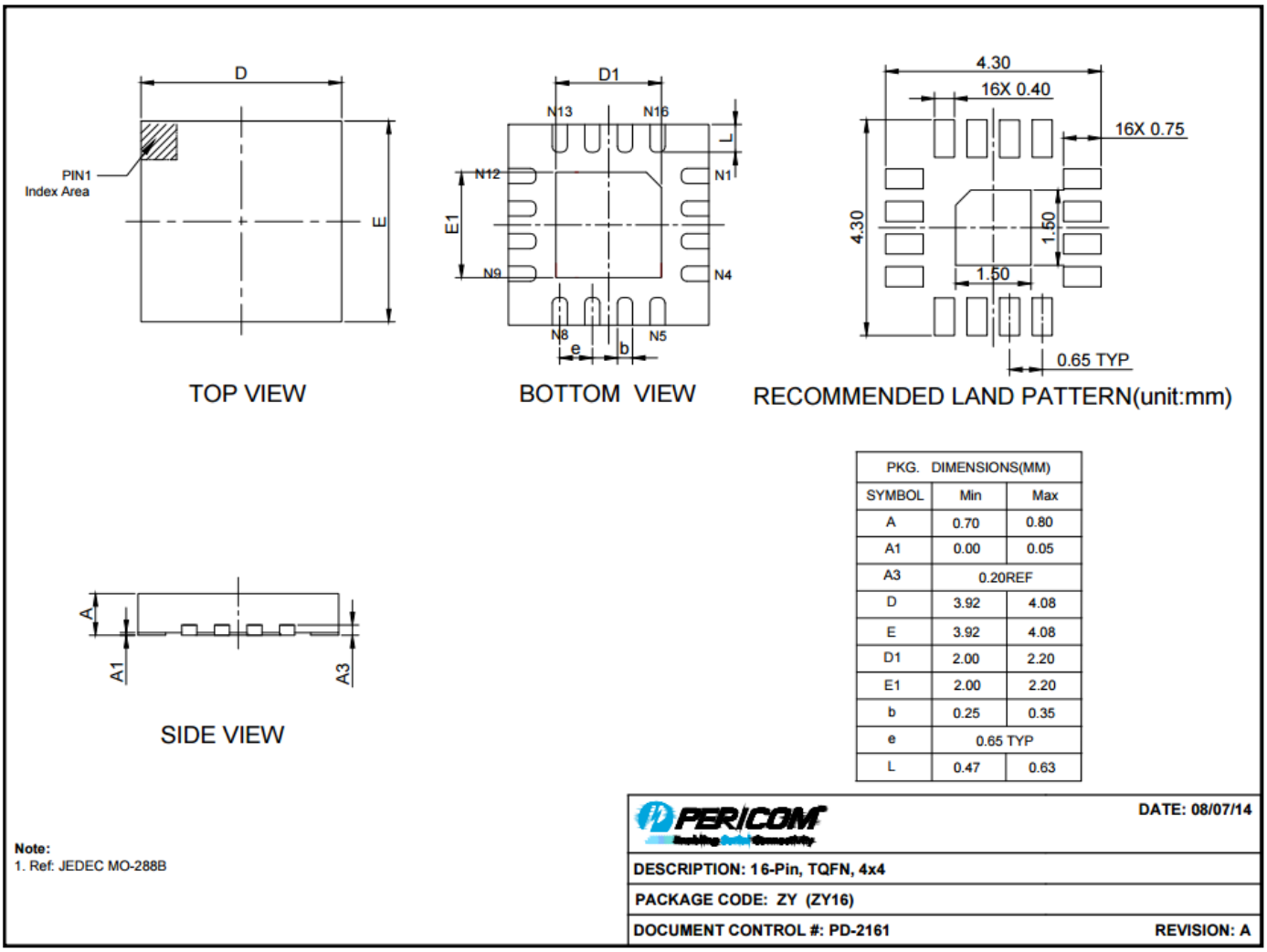
DATE: 03/24/16

DESCRIPTION: 16-Pin, 173mil Wide TSSOP

PACKAGE CODE: L (L16)

DOCUMENT CONTROL #: PD-1310 REVISION: G

TQFN-16 (ZY)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20REF	
D	3.92	4.08
E	3.92	4.08
D1	2.00	2.20
E1	2.00	2.20
b	0.25	0.35
e	0.65 TYP	
L	0.47	0.63

Note:
1. Ref: JEDEC MO-288B

PERICOM Semiconductor Corporation — DATE: 08/07/14

DESCRIPTION: 16-Pin, TQFN, 4x4

PACKAGE CODE: ZY (ZY16)

DOCUMENT CONTROL #: PD-2161 — REVISION: A

14-0209

For latest package info.
please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part Numbers	Package Code	Package
PI4IOE5V9538LEX	L	16-Pin,173 mil Wide (TSSOP)
PI4IOE5V9538ZYEX	ZY	16-Pin, 4x4 (TQFN) (Please contact the local Diodes sales)

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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