MP2703

26V Input, 1A, Linear Charger with Battery Diagnostics for 1 Cell or 2 Cells

DESCRIPTION

The MP2703 is a linear charger for 1-cell to 2-cell Li-ion, Li-polymer, $LiFePO_4$, and 2-cell to 6-cell NiMH batteries. The device can sustain a voltage up to 26V.

The MP2703 measures the battery voltage (V_{BATT}) and automatically charges the battery in four phases: trickle charge, pre-charge, constant-current (CC) fast charge, and constant-voltage charge.

The MP2703 provides a dedicated ISET pin to set the charge current by connecting a resistor between ISET and ground. The device also has a minimum input voltage limit (V_{IN_LIM}) to reduce the charge current when the input power is overloaded.

The MP2703 provides robust protections including input over-voltage protection (OVP), battery OVP, charge safety timer, and battery temperature protection, which is compliant with the JEITA standard.

The MP2703 integrates a battery diagnostic function. The BATTSNS pin provides an output that is proportional to the real V_{BATT}, which can be directly delivered to an external analog-to-digital converter (ADC) input for V_{BATT} measurements. In addition, an internal dummy load can be controlled to discharge the battery. An external microcontroller (MCU) can detect the battery impedance with the V_{BATT} measurement and discharge function above.

The MP2703 also provides two open-drain pins to indicate the input power status and charge status. The $\overline{ACOK}$ pin can indicate whether the input power is present. The $\overline{CHG}$ pin can indicate several charging states, including charging, termination, and fault events.

The MP2703 offers flexible one-time programmable (OTP) memory to configure a variety of charge parameters.

The MP2703 is available in a QFN-10 (2mmx2.5mm) package.

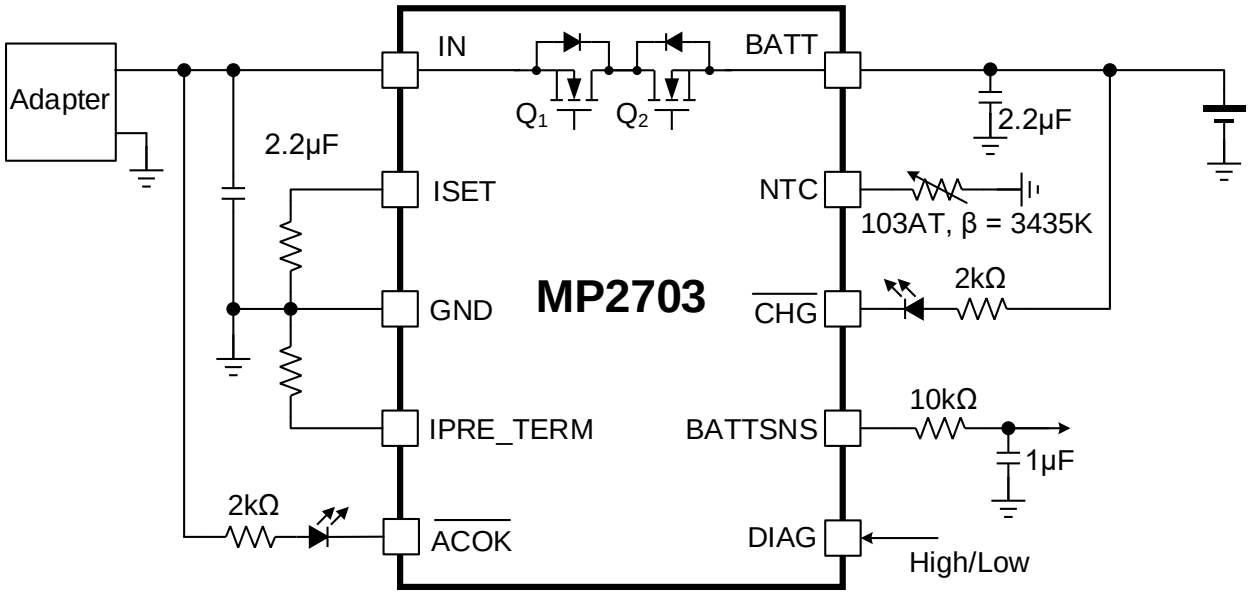
FEATURES

- Up to 26V of Sustainable Voltage
- Up to 1A of Configurable Charge Current via the ISET Pin
- ISET Pin Short-Circuit Protection (SCP)
- Configurable Pre-Charge Current
- Configurable Termination Current Threshold
- One-Time Programmable (OTP) Memory Selection for 3 Minimum Input Voltage Limit (V_{IN_LIM}) Levels
- OTP Selection for Battery Regulation Voltage from 2.4V to 4.5V Per Cell
- 0.5% Battery Regulation Voltage Accuracy
- OTP Selection for 1-Cell or 2-Cell Batteries
- Battery Voltage Monitoring Pin
- Battery Impedance Diagnostics
- Integrated Chip Junction Temperature (T_J) Regulation
- Battery Temperature Protection Compliant with JEITA Standard
- 100nA Battery Leakage Current in Shutdown Mode
- Down to 3mA Termination Current
- Charge Status and Fault Indication
- Input Power Indication
- Integrated Charge Safety Timer
- OTP for Miscellaneous Parameters
- Provides Option to Charge 2-Cell to 6-Cell NiMH Batteries
- Compatible with $LiFePO_4$ Batteries
- Available in a Compact QFN-10 (2mmx2.5mm) Package

APPLICATIONS

- Headphones
- Wearable Devices
- Emergency Calls

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2703GRP-xxxx**	QFN-10 (2mmx2.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP2703GRP-xxxx-Z).

**"xxxx" is the register setting option. The factory default code is "0000". This content can be viewed in the OTP register map. Contact an MPS FAE to obtain an "xxxx" value.

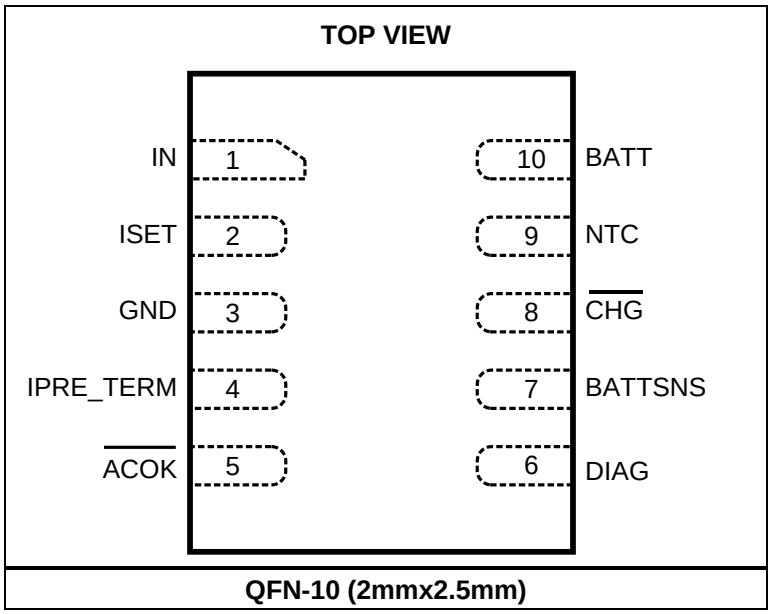
TOP MARKING

$\overline{\text{LBY}}$

LLL

LB: Product code of MP2703GRP-xxxx
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Type (1)	Description
1	IN	P	**Power input of the IC.** Place a 1μF to 10μF bypass capacitor between the IN and GND pins.
2	ISET	AI	**Charge current setting.** Connect a resistor between the ISET and GND pins to set the fast charge current, which should range between 20mA and 1A.
3	GND	P	**Ground terminal.**
4	IPRE_TERM	AI	**Pre-charge and termination current setting.** Connect a resistor between the IPRE_TERM and GND pins to set the pre-charge current (I_{PRE}) and termination current (I_{TERM}).
5	$\overline{ACOK}$	DO	**Input power status indication.** The $\overline{ACOK}$ pin is an open-drain output. If the input voltage (V_{IN}) exceeds its under-voltage lockout (UVLO) threshold (V_{IN_UVLO}) and the battery voltage (V_{BATT}), then $\overline{ACOK}$ pulls low.
6	DIAG	DI	**Diagnostic control.** The DIAG pin is active high. When this pin is enabled, an internal 95mA dummy load is added at the battery.
7	BATTSNS	AO	**Battery voltage sense.** The voltage at the BATTSNS pin is 1/4 (1-cell) or 1/8 (2-cell) of the real V_{BATT}.
8	$\overline{CHG}$	DO	**Charge status indication.** If the $\overline{CHG}$ pin pulls low, this indicates that charging is in progress. If $\overline{CHG}$ is an open drain, this indicates that there is either no charging or charging is complete.
9	NTC	AI	**Temperature-sense input.** Connect a negative temperature coefficient (NTC) thermistor between the NTC and GND pins. Pull the NTC pin to ground to disable charging.
10	BATT	P	**Battery terminal.** Place a 1μF to 10μF bypass capacitor between the BATT and GND pins.

Note:

1) AI refers to analog input, DI refers to digital input, DO refers to digital output, and P refers to power.

ABSOLUTE MAXIMUM RATINGS (2)

IN, $\overline{ACOK}$, $\overline{CHG}$ to GND .....-0.3V to +26V
BATT to GND.....- 0.3V to +26V
All other pins to GND .....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (3) 1.78W
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C
Storage temperature…. ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) (4)..... 1.5kV
Charged-device model (CDM) (5)..... 750V

Recommended Operating Conditions (6)

Input voltage (V_{IN}) .....Up to 13.5V
Input current (I_{IN}).....Up to 1A
Charge current (I_{CC}) .....Up to 1A
Battery voltage (V_{BATT}) .....Up to 9V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (7) θ_{JA} θ_{JC}

QFN-10 (2mmx2.5mm)..... 88 ..... 13... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can provide an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per ANSI/ESDA/JEDEC JS-001, all pins.
5) Per ANSI/ESDA/JEDEC JS-002, all pins.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40 to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristics						
Input voltage (V_{IN}) under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.4	3.6	3.8	V
V_{IN} UVLO threshold hysteresis	$V_{IN\_UV\_HYS}$	V_{IN} rising		340		mV
Input voltage vs. battery voltage headroom threshold	V_{HDRM}	V_{IN} rising, 1 cell		200		mV
		V_{IN} rising, 2 cells		240		mV
		V_{IN} falling, 1 cell	10	100	190	mV
		V_{IN} falling, 2 cells	20	130	240	mV
Input power good rising deglitch time	t_{VIN_GD}	V_{IN} rising		30		ms
V_{IN} over-voltage protection (OVP) threshold	V_{IN_OVP}	V_{IN} rising, 1 cell	5.8	6	6.2	V
		V_{IN} rising, 2 cells	13.8	14.4	15	V
V_{IN} OVP hysteresis	$V_{IN\_OV\_HYS}$	V_{IN} falling, 1 cell		220		mV
	$V_{IN\_OV\_HYS}$	V_{IN} falling, 2 cells		550		mV
V_{IN} OVP deglitch time	t_{VIN_OVP}	V_{IN} rising		100		µs
V_{IN} OVP recovery deglitch time		V_{IN} falling		30		ms
Input shutdown current	I_{IN_Q}	V_{IN} = 5V, charge disabled by pulling NTC to GND		290	335	µA
		V_{IN} = 5V, charge termination		490	585	µA
BATT leakage current in shutdown mode	I_{BATT_SHDN}	V_{BATT} = 4.2V (1 cell) / 8.4V (2 cells), V_{IN} = GND		0.1	1	µA
Battery quiescent current after termination	I_{BATT_Q}	V_{IN} = 5V, 1 cell, charge terminated		3.8	5	µA
		V_{IN} = 9V, 2 cells, charge terminated		5.6	7.2	µA
Battery Charger (T_A = 0°C to 70°C)						
IN to BATT on resistance	R_{ON_Q1+Q2}			370		mΩ
Trickle charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	0.9	1	1.1	V/cell
Trickle charge to pre-charge threshold hysteresis	$V_{BATT\_TC\_HYS}$	V_{BATT} falling		100		mV/cell

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40 to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Trickle charge current	I_{TC}	R_{ISET} = 550Ω	28	50	72	mA
		Minimum clamp	1	3	5.5	mA
Pre-charge to fast charge threshold	V_{BATT_PRE}	VBATT_PRE = 2.5V/cell	2.4	2.5	2.6	V/cell
		VBATT_PRE = 2.8V/cell	2.7	2.8	2.9	
		VBATT_PRE = 3V/cell	2.9	3	3.1	
		VBATT_PRE = 3.2V/cell	3.1	3.2	3.3	
Pre-charge to fast charge deglitch time	t_{PRE_CC}			30		ms
Fast charge to pre-charge deglitch time	t_{CC_PRE}			30		ms
Pre-charge current	I_{PRE}	IPRE_TERM floating, R_{ISET} = 1.1kΩ	88	100	112	mA
		IPRE_TERM floating, R_{ISET} = 550Ω	160	200	240	mA
		R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 1.1kΩ	75	100	125	mA
		R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 550Ω	145	202	258	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 1.1kΩ	32	50	66	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 550Ω	70	100	130	mA
		Minimum clamp	1	3	5.5	mA
Constant-current fast charge current	I_{CC}	R_{ISET} = 786Ω	665	700	735	mA
		R_{ISET} = 11kΩ	45	50	55	mA
		R_{ISET} = 27.5kΩ	15	20	25	mA
Over charge current protection	I_{OC}	R_{ISET} = 0Ω		1.25		A
Battery charge voltage regulation	V_{BATT_REG}	VBATT_REG = 3.6V/cell	3.582	3.6	3.618	V/cell
		VBATT_REG = 4.1V/cell	4.080	4.1	4.121	
		VBATT_REG = 4.2V/cell	4.179	4.2	4.221	
		VBATT_REG = 4.35V/cell	4.328	4.35	4.372	
		VBATT_REG = 4.5V/cell	4.478	4.5	4.523	
Battery charge termination threshold	I_{TERM}	R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 1.1kΩ	38	50	62	mA
		R_{IPRE_TERM} = 2.26kΩ, R_{ISET} = 550Ω	74	100	126	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 1.1kΩ	12	22	31	mA
		R_{IPRE_TERM} = 1.13kΩ, R_{ISET} = 550Ω	32	48	64	mA
		Minimum clamp	1	3	5.5	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40 to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Charge termination deglitch time	t_{TERM_DGL}			30		ms
Auto recharge voltage threshold	V_{RECH}	Lower than V_{BATT_REG}	135	200	265	mV/cell
Auto recharge voltage deglitch time	t_{RECH_DGL}			30		ms
Battery OVP threshold	V_{BATT_OVP}	Comparing with V_{BATT_REG}, V_{BATT} rising	85	150	215	mV/cell
Battery OVP threshold hysteresis	$V_{BATT\_OVP\_HYS}$	Comparing with V_{BATT_OVP}, V_{BATT} falling		30		mV/cell
Minimum Input Voltage Regulation (T_A = 0°C to 70°C)						
Minimum input voltage limit	V_{IN_LIM}	VIN_LIM = 4.375V/cell	4.25	4.37	4.49	V/cell
		VIN_LIM = 4.5V/cell	4.37	4.5	4.6	V/cell
		VIN_LIM = 4.75V/cell	4.63	4.75	4.87	V/cell
Thermal Protection						
Thermal shutdown rising threshold (7)	T_{J_SHDN}	T_J rising		160		°C
Thermal shutdown hysteresis (7)	$T_{J\_SHDN\_HYS}$			20		°C
Thermal regulation point (7)	T_{J_REG}			120		°C
Battery Diagnostics (T_A = 0°C to 70°C)						
Battery dummy load current	I_{BATT_DUMMY}	V_{BATT} = 4V	92.3	95	96.6	mA
Battery sense percentage	$V_{BATTSNS}$	V_{BATT} = 4V, 1 cell	24.5	25	25.5	%
		V_{BATT} = 8V, 2 cells	11.9	12.5	13.1	%
Battery Temperature Monitoring and Protection						
NTC biased current	I_{NTC}	T_A = 0°C to 70ºC	47.5	50	52	µA
Cold temperature threshold	V_{COLD}	V_{NTC} = 1V to 1.5V, VCOLD = 0°C	1363	1377	1391	mV
Hysteresis of cold temperature threshold	V_{COLD_HYS}	V_{NTC} = 1.5V to 1V, VCOLD = 0°C		90		mV
Cool temperature threshold	V_{COOL}	V_{NTC} = 0.5V to 1V, VCOOL = 10°C	893	902	915	mV
Hysteresis of cool temperature threshold	V_{COOL_HYS}	V_{NTC} = 1V to 0.5V, VCOOL = 10°C		34		mV
Warm temperature threshold	V_{WARM}	V_{NTC} = 0.5V to 0.2V, VWARM = 45°C	239	245	251	mV
Hysteresis of warm temperature threshold	V_{WARM_HYS}	V_{NTC} = 0.2V to 0.5V, VWARM = 45°C		11		mV

Note:

7) Guaranteed by design.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.7V, V_{BATT_REG} = 4.2V/cell, T_A = -40 to +125°C, unless otherwise noted.

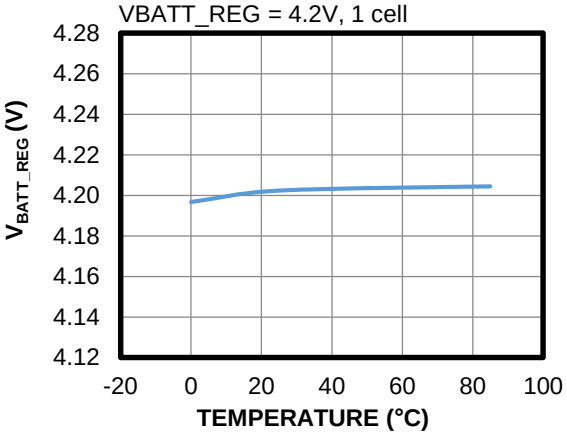
Parameter	Symbol	Condition	Min	Typ	Max	Units
Hot temperature threshold	V_{HOT}	V_{NTC} = 0.2 to 0.1V, VHOT = 60°C	138	151	157	mV
Hysteresis of hot temperature threshold	V_{HOT_HYS}	V_{NTC} = 0.1 to 0.2V, VHOT = 60°C		11		mV
NTC enable charge threshold		V_{NTC} = 0V to 0.15V	75	90	105	mV
NTC enable charge threshold hysteresis		V_{NTC} = 0.15V to 0V		15		mV
NTC bias current when charge is disabled by NTC pin		V_{NTC} = 0V	20	30	40	µA
NTC charge termination disable threshold		V_{NTC} rising	2.4	2.5	2.6	V
NTC charge termination disable threshold hysteresis		V_{NTC} falling		100		mV
NTC minimum bias current when NTC is floating	I_{NTC_FLT}	V_{NTC} = 3V	3	4.5	6	µA
NTC float voltage	V_{NTC_FLT}			3.6		V
Open-Drain Pin Characteristics						
$\overline{CHG}$ pin output voltage		I_{SINK} = 5mA			0.4	V
$\overline{ACOK}$ pin output voltage		I_{SINK} = 5mA			0.4	V
Logic Levels on the DIAG Pin						
Logic low input voltage					0.4	V
Logic high input voltage			1.6			V
Timing Characteristics (T_A = 0°C to 70°C)						
Charge timer	t_{TMR}	TMR_SET = 10 hours	8	10	12	hr
Trickle charge and pre-charge timer			0.8	1	1.2	hr

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

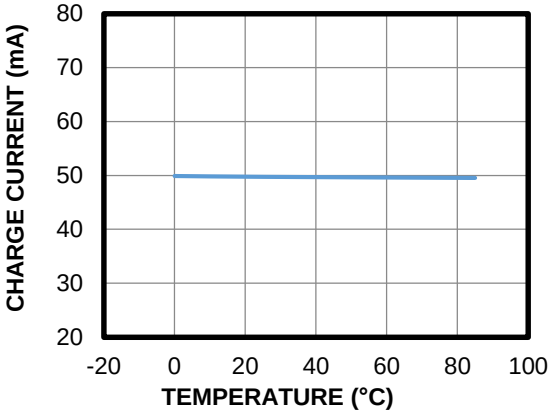
Battery Regulation Voltage vs. Temperature

VBATT_REG = 4.2V, 1 cell



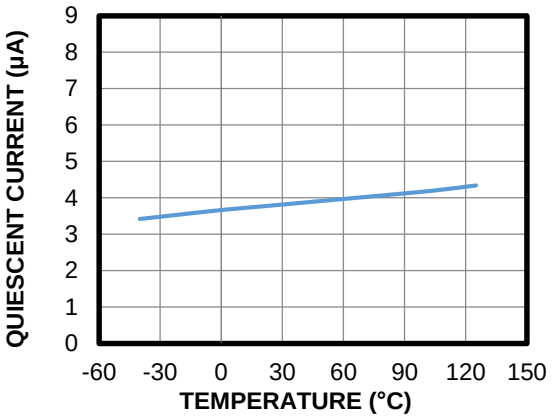
Charge Current vs. Temperature

I_{CC} = 50mA, V_{IN} = 5V, V_{BATT} = 3.8V



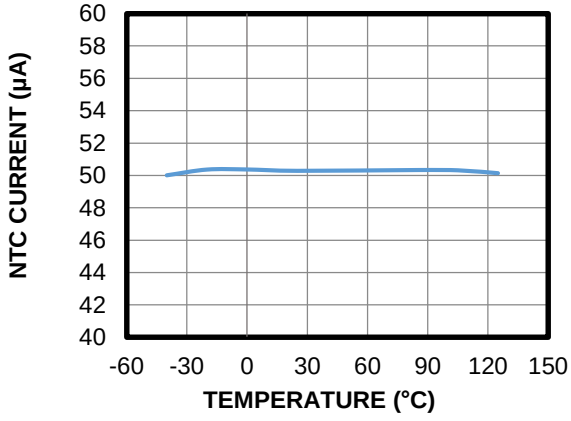
Battery Quiescent Current vs. Temperature

V_{IN} = 5V, 1 cell, charge termination



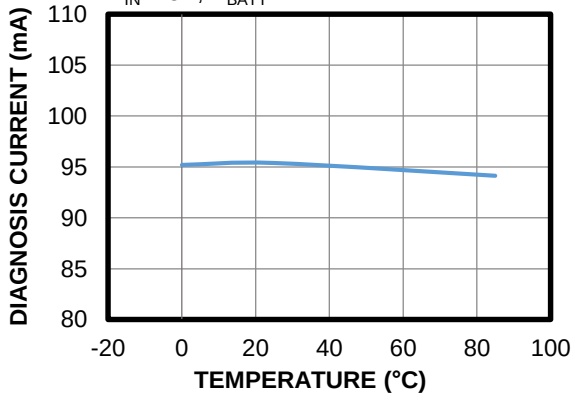
NTC Current vs. Temperature

V_{IN} = 5V, V_{BATT} = 4V



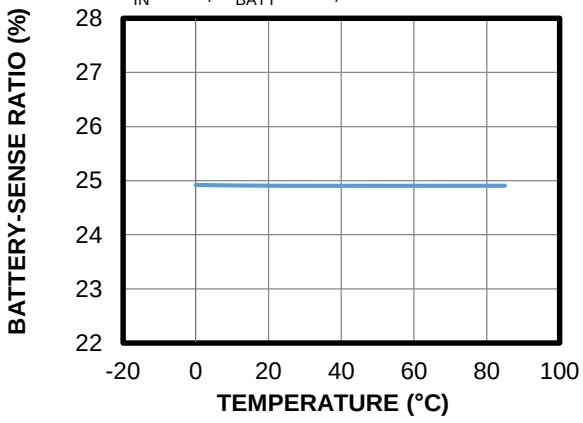
Battery Diagnosis Current vs. Temperature

V_{IN} = 5V, V_{BATT} = 4V



Battery-Sense Ratio vs. Temperature

V_{IN} = 5V, V_{BATT} = 4V, 1 cell

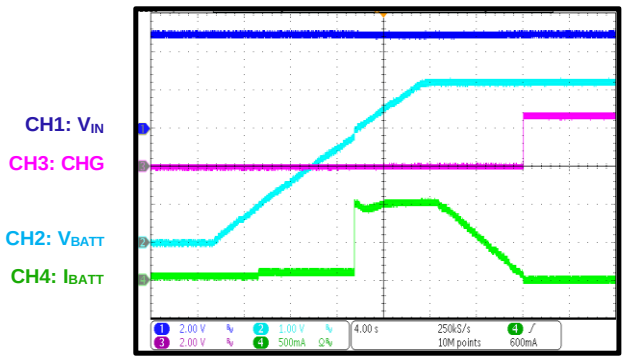


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

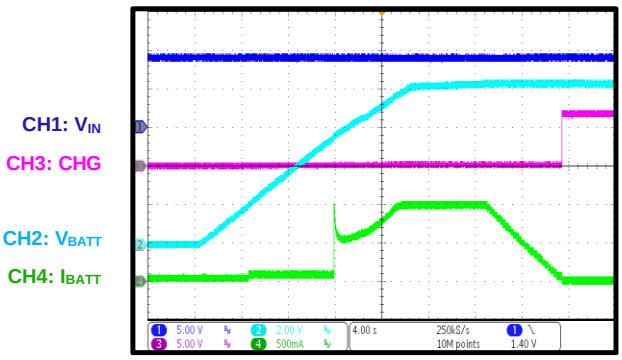
Battery Charge Profile

V_{IN} = 5V, I_{PRE} = 10%, I_{CC} = 1A, 1 cell



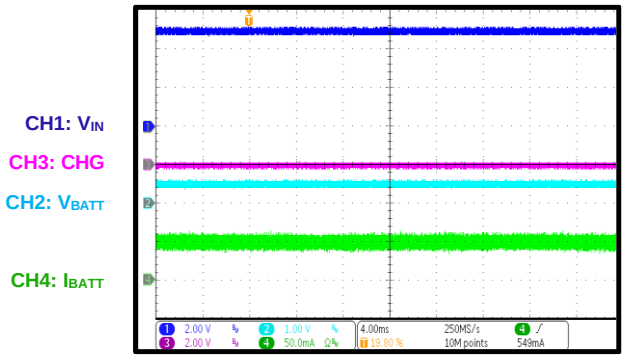
Battery Charge Profile

V_{IN} = 9V, I_{PRE} = 10%, I_{CC} = 1A, 2 cells



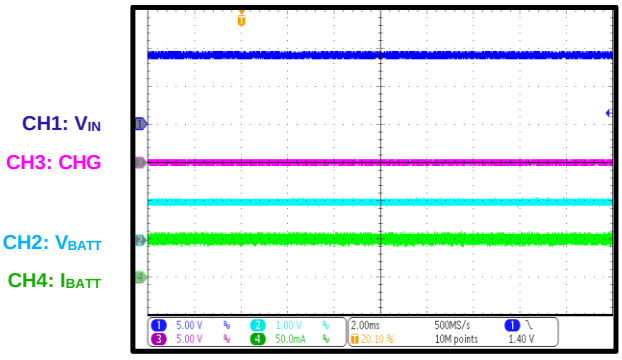
Trickle Charge

V_{IN} = 5V, V_{BATT} = 0.5V, I_{TC} = 50mA, 1 cell



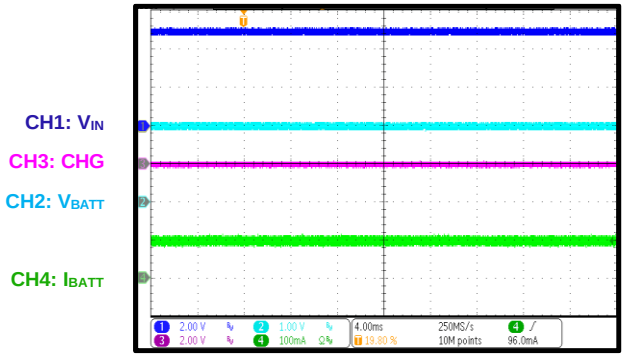
Trickle Charge

V_{IN} = 9V, V_{BATT} = 1V, I_{TC} = 50mA, 2 cells



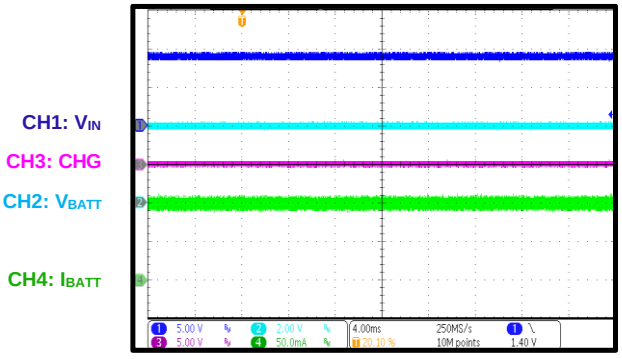
Pre-Charge

V_{IN} = 5V, V_{BATT} = 2V, I_{PRE} = 100mA, 1 cell



Pre-Charge

V_{IN} = 9V, V_{BATT} = 4V, I_{PRE} = 100mA, 2 cells

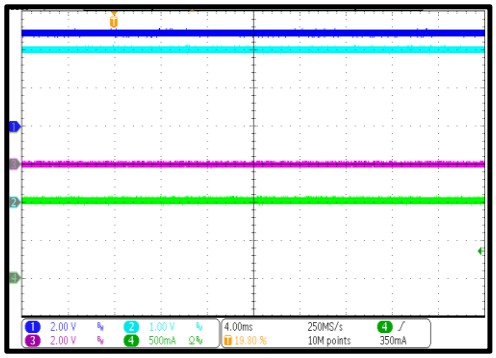


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

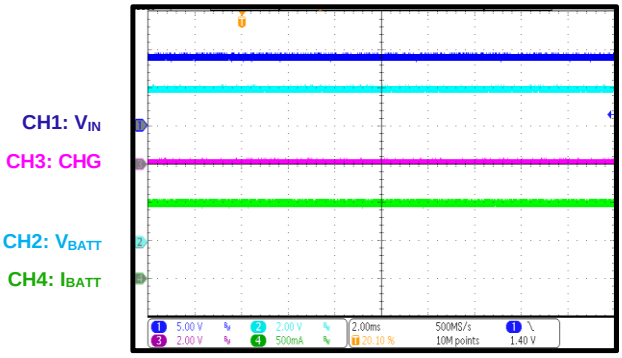
Constant-Current Charge

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



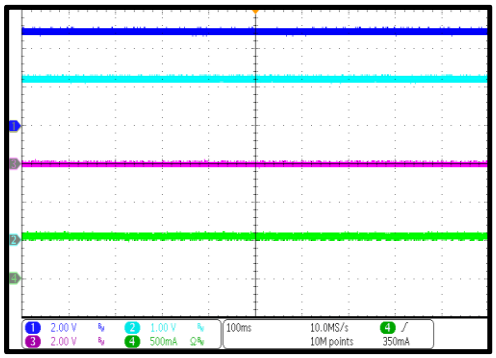
Constant-Current Charge

V_{IN} = 9V, V_{BATT} = 8V, I_{CC} = 1A, 2 cells



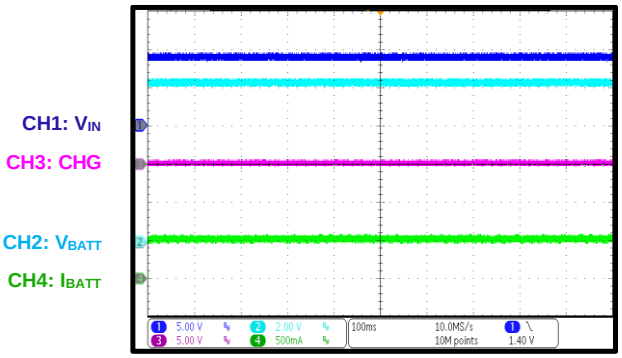
Constant Voltage Charge

V_{IN} = 5V, V_{BATT} = 4.185V, I_{CC} = 1A, 1 cell



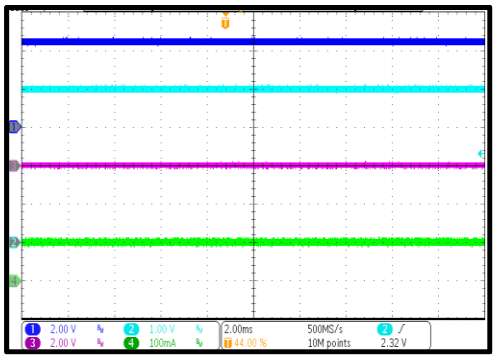
Constant Voltage Charge

V_{IN} = 9V, V_{BATT} = 8.389V, I_{CC} = 1A, 2 cells



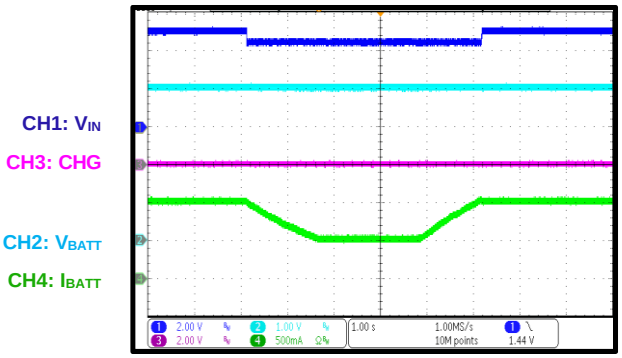
Input Voltage Limit Steady State

V_{IN} = 5V (0.1A), V_{IN_LIM} = 4.5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



Input Voltage Limit

V_{IN} = 5V (1A to 0.5A to 1A), V_{IN_LIM} = 4.5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell

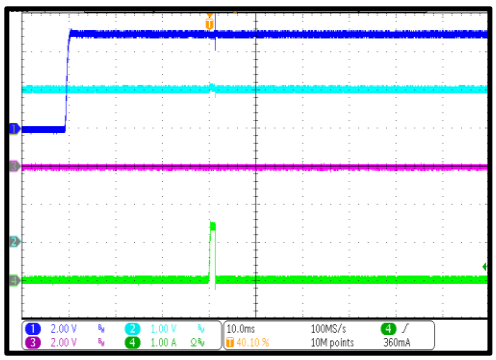


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, I_{CC} = 1A, V_{BATT} = full range, 1 cell, T_A = 25°C, unless otherwise noted.

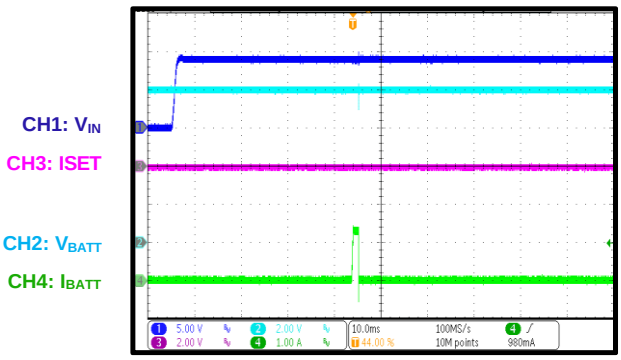
Start-Up with ISET Short

V_{IN} = 5V, V_{BATT} = 4V, ISET short, 1 cell



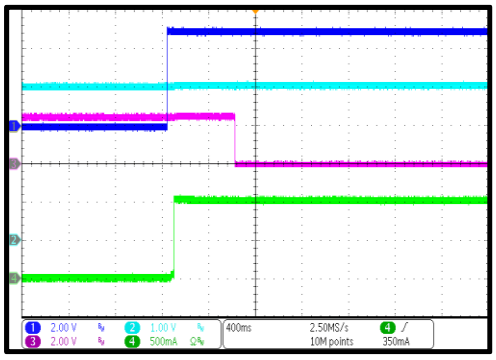
Start-Up with ISET Short

V_{IN} = 9V, V_{BATT} = 8V, ISET short, 2 cells



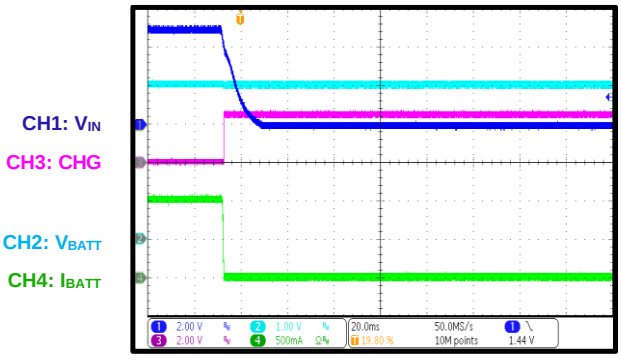
Start-Up

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



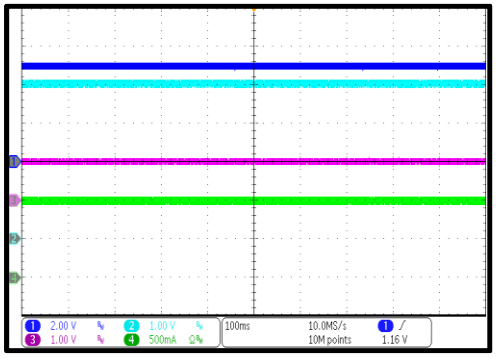
Shutdown

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



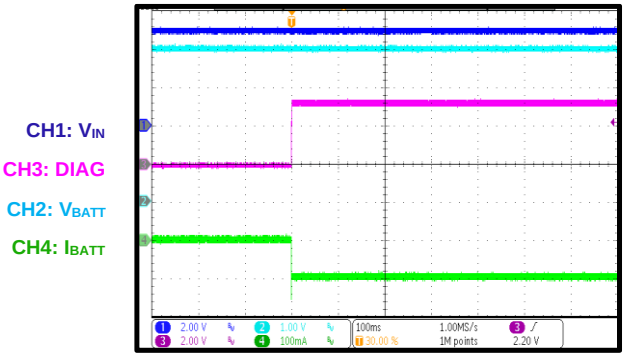
BATTSNS Output

V_{IN} = 5V, V_{BATT} = 4V, I_{CC} = 1A, 1 cell



Battery Dummy Load

V_{IN} = 5V, V_{BATT} = 4V, V_{NTC} = 0V, 1 cell



FUNCTIONAL BLOCK DIAGRAM

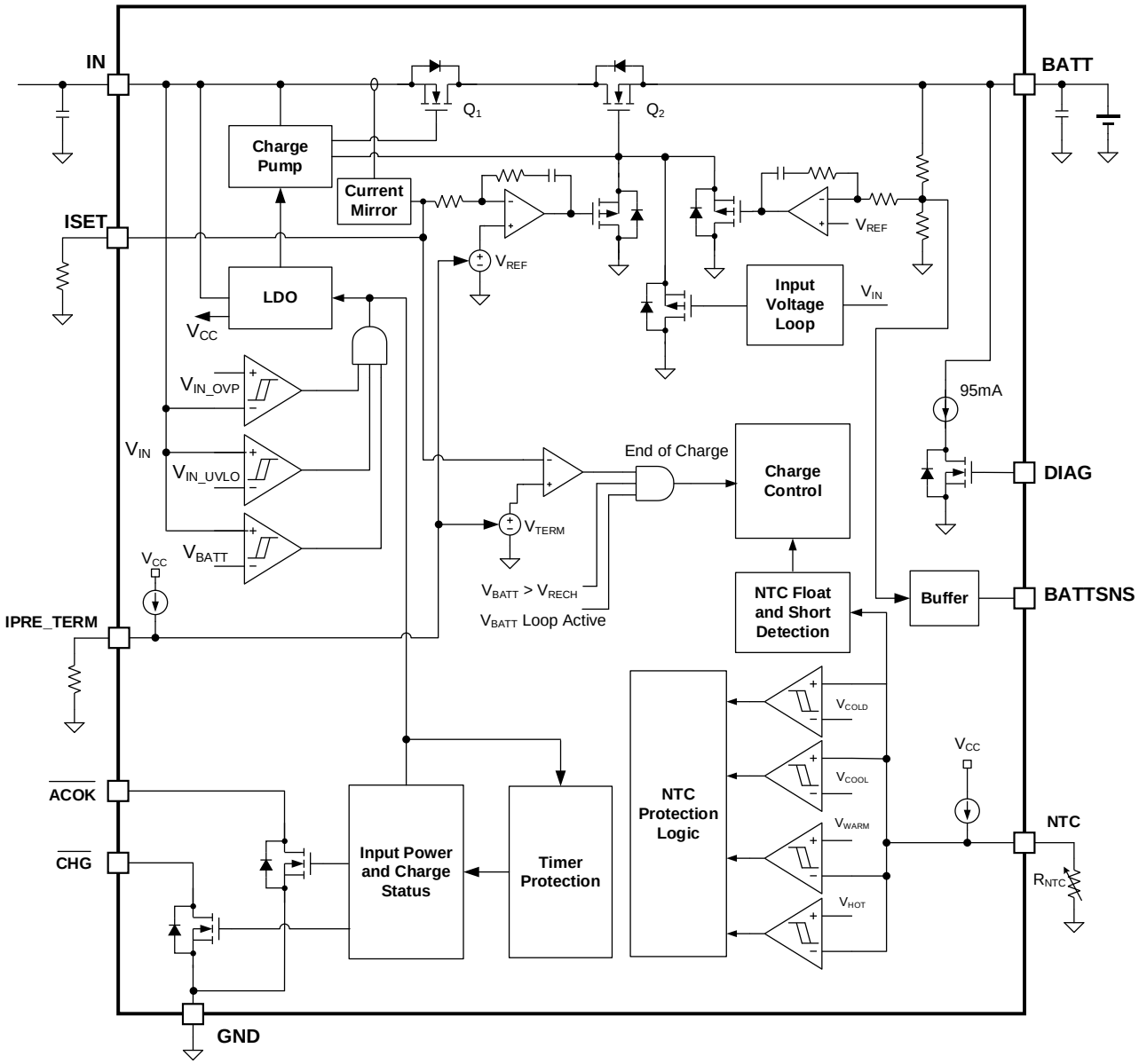


Figure 1: Functional Block Diagram

OPERATION

Introduction

The MP2703 is a linear charger for 1-cell to 2-cell Li-ion, Li-polymer, and $LiFePO_4$ battery applications, and 2-cell to 6-cell NiMH battery applications. The device can sustain an input voltage (V_{IN}) up to 26V and achieve up to 1A of charge current.

Power Supply

The IC is powered by the input. Once V_{IN} exceeds its under-voltage lockout (UVLO) threshold (V_{IN_UVLO}), the internal control and logic circuit starts to operate. If V_{IN} exceeds both V_{IN_UVLO} and the sum of the battery voltage (V_{BATT}) and the V_{IN} vs. V_{BATT} headroom threshold (V_{HDRM}) (V_{BATT} + V_{HDRM}), the MP2703 indicates power good (PG), and the $\overline{ACOK}$ pin is pulled down to GND.

Charge Cycle

When the input power is qualified as a good power supply, the IC checks V_{BATT} and provides four charging phases: trickle charge, pre-charge, constant-current (CC) fast charge, and constant-voltage charge (see Figure 2).

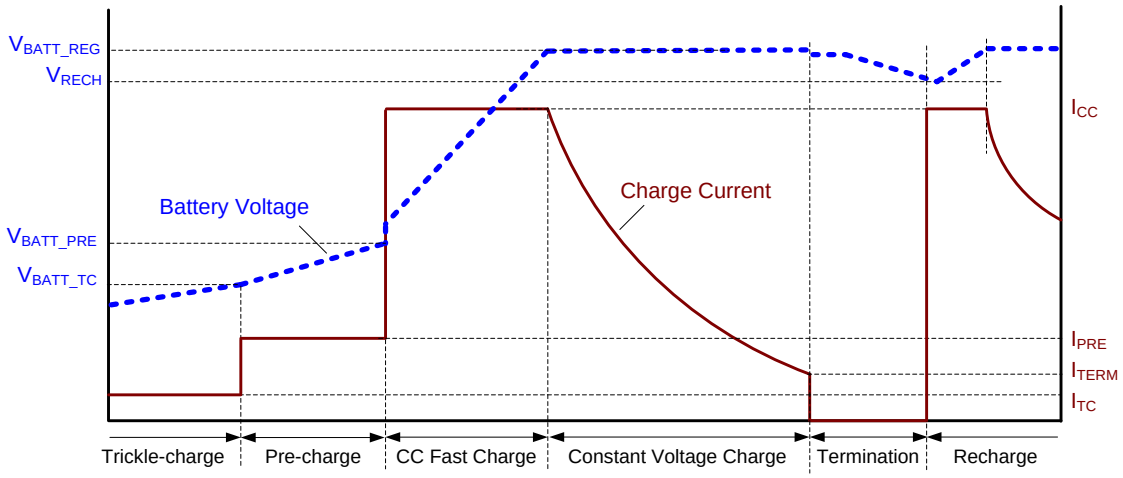


Figure 2: Charge Cycle Profile

Phase 1 (Trickle Charge)

If V_{BATT} is below the trickle charge to pre-charge threshold (V_{BATT_TC}), a trickle charging current is applied on the battery to reset the protection circuit in the battery pack. The trickle charge current (I_{TC}) is 5% of the set fast charge current (I_{CC}). Once 5% of I_{CC} drops below 3mA, I_{TC} is clamped at 3mA.

Phase 2 (Pre-Charge)

If V_{BATT} exceeds V_{BATT_TC} but remains below the pre-charge to fast charge threshold (V_{BATT_PRE}), the IC charges the battery with the pre-charge current (I_{PRE}). There are four one-time programmable (OTP) memory options available for V_{BATT_PRE}.

I_{PRE} is proportional to the fast charge current and this proportion can be configured via the IPRE_TERM pin.

Phase 3 (Constant-Current Fast Charge)

If V_{BATT} exceeds V_{BATT_PRE}, the IC enters the constant-current fast charge phase. I_{CC} can be set via the ISET pin.

Phase 4 (Constant-Voltage Charge)

If V_{BATT} rises to the battery charge regulation voltage (V_{BATT_REG}), the charge current starts to decrease. Once the charge current reaches the battery charge termination threshold (I_{TERM}), the charge cycle is considered complete after the charge termination deglitch time (t_{TERM_DGL}). If I_{TERM} is not reached before the safety charge timer expires, then the charge cycle stops and the corresponding timeout fault signal asserts.

Charge Termination

If V_{BATT} reaches the full voltage regulation threshold and the charge current is below I_{TERM}, charging is terminated after a deglitch time of 30ms. Charge termination can be disabled by floating the NTC pin.

Automatic Recharge

Once the battery charge cycle completes, the IC remains off. During this time, the external load consumes battery power or the battery self-discharges. A new charge cycle automatically begins once V_{BATT} drops below the automatic recharge threshold for the 30ms deglitch time. The safety charge timer resets when the automatic recharge cycle begins.

Minimum Input Voltage Limit (V_{IN_LIM})

The MP2703 also has a minimum input voltage limit (V_{IN_LIM}) regulation loop. If the charge current exceeds the input power supply's current rating, the MP2703 automatically reduces the charge current when V_{IN} reaches V_{IN_LIM}. There are three options for V_{IN_LIM}, set via the OTP.

Cell Selection

The MP2703 can support both 1-cell and 2-cell batteries. The battery cell counts can be set by via the OTP. See the One-Time Programmable (OTP) Memory Map section on page 20 for details.

For 2-cell applications, battery hot insertion or shorting is not allowed when V_{IN} is present and charging is enabled.

Battery Regulation Voltage

The MP2703 supports a variety of battery-full voltages, which can be set via the OTP. This voltage ranges between 2.4V/cell and 4.5V/cell, with 50mV per step.

Fast Charge Current Setting

An external resistor between ISET and GND pin configures the fast charge current (see Figure 3).

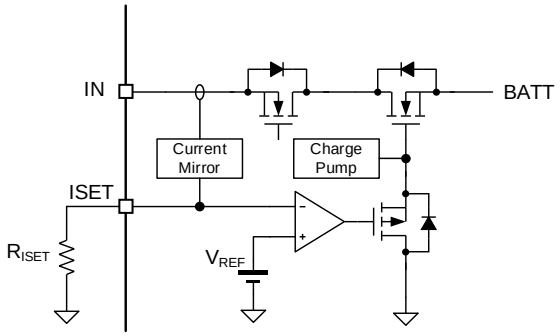


Figure 3: Functional Diagram Setting the Charge Current via the ISET Pin

The relationship between the fast charge current and R_{ISET} can be calculated with Equation (1):

$$V_{REF}=k\times I_{CC}\times R_{ISET} \quad (1)$$

Where *k* is the current mirror's sense gain. The expected I_{CC} can be estimated with Equation (2):

$$I_{CC}=\frac{V_{REF}/k}{R_{ISET}} \quad (2)$$

Where V_{REF} is 1.2V, and *k* is 2.18 x 10^{-3}.

Over-Current Protection (OCP)

The MP2703 provides OCP if the charge current is set too high by mistake. For example, if the ISET pin is shorted to GND, the charge current is clamped at 1.25A, and the MP2703 latches off after a 1ms deglitch time. The only way to reset the fault is to re-plug the input power or pull NTC to GND.

Pre-Charge Current Setting

Connect a resistor from the IPRE_TERM pin to GND to configure the ratio of I_{PRE} to I_{CC}.

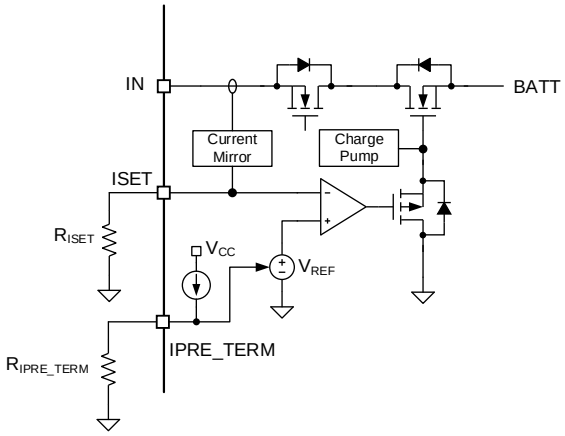


Figure 4: The Functional Diagram of Pre-charge Current Setting

The ratio of I_{PRE} to I_{CC} can be calculated with Equation (3):

$$I_{PRE} / I_{CC} = R_{IPRE\_TERM} / K_{PRE-CC} \quad (3)$$

Where K_{PRE-CC} is 112.36Ω/%.

For example, to set the proportion of I_{PRE} / I_{CC} to 10%, connect a 1.13kΩ resistor between the IPRE_TERM pin and ground.

Setting the Charge Termination Threshold

If V_{BATT} reaches the full voltage, the battery voltage loop is initiated and the charge current drops. Once the three conditions below are satisfied, charging terminates:

- The V_{BATT} loop is active.
- V_{BATT} exceeds the automatic recharge voltage threshold (V_{RECH}).
- The battery current (I_{BATT}) is below I_{TERM}.

I_{TERM} is also proportional to I_{CC}. This threshold (I_{TERM} / I_{CC}) can be configured via the resistor placed between IPRE_TERM and ground, and can be estimated with Equation (4):

$$I_{TERM} / I_{CC} = R_{IPRE\_TERM} / K_{TERM-CC} \quad (4)$$

Where $K_{TERM-CC}$ is 224.72Ω/%. For example, if R_{IPRE_TERM} is 1.13kΩ, then the proportion between I_{TERM} and I_{CC} is 5%.

When the IPRE_TERM pin is floating, I_{TERM} is fixed at 10% of the set I_{CC}.

Figure 5 shows the functional diagram to set I_{TERM}.

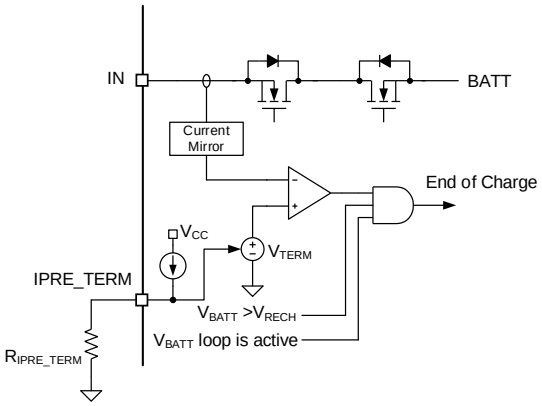


Figure 5: The Functional Diagram of Termination Current Threshold

Battery Temperature Monitor via the Negative Thermal Coefficient (NTC) Thermistor

Thermistor is the generic name for thermally sensitive resistors. Negative temperature coefficient (NTC) thermistors are typically called thermistors. Depending on the manufacturing method and structure, thermistors come in many shapes with characteristics for various purposes. Unless otherwise specified, the thermistor resistance values are classified at a standard temperature of 25°C. The thermistor resistance is solely a function of its absolute temperature.

Refer to the thermistor datasheet for the mathematic expression that relates the resistance and absolute temperature of a thermistor. The resistance at the absolute temperature T1 (R1) can be calculated with Equation (5):

$$R1 = R2 \times e^{\beta \times \left(\frac{1}{T1} - \frac{1}{T2}\right)} \quad (5)$$

Where R2 is the resistance at the absolute temperature (T2), and β is a constant that depends on the material of the thermistor.

The MP2703 continuously monitors the battery's temperature by measuring the NTC pin voltage (V_{NTC}), which is generated by a precise current flowing from the NTC pin through the NTC resistor (R_{NTC}) to ground.

The MP2703 compares V_{NTC} to an internal threshold to determine the fault type that occurs and takes different actions accordingly. The current from the NTC pin is only active when V_{IN} is present.

Figure 6 shows the functional diagram of the NTC protection circuit.

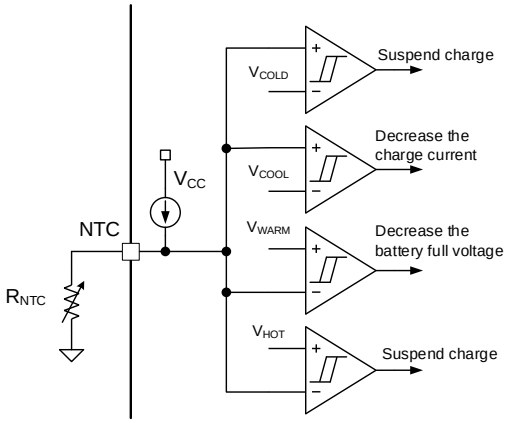


Figure 6: Functional Diagram of NTC Protection Circuit

To satisfy the JEITA requirements, the MP2703 provides four temperature thresholds: cold (0°C by default), cool (10°C by default), warm (45°C by default), and hot (60°C by default). For a given NTC thermistor, these temperatures correspond to V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}, respectively. If V_{NTC} is below V_{HOT}, or V_{NTC} exceeds V_{COLD}, then charging and the timers are suspended.

If V_{HOT} < V_{NTC} < V_{WARM}, or if V_{COOL} < V_{NTC} < V_{COLD}, then the charging behavior is configured via the OTP. The preset thresholds are defined based on a thermistor where β = 3435K. Figure 7 shows the NTC JEITA profile.

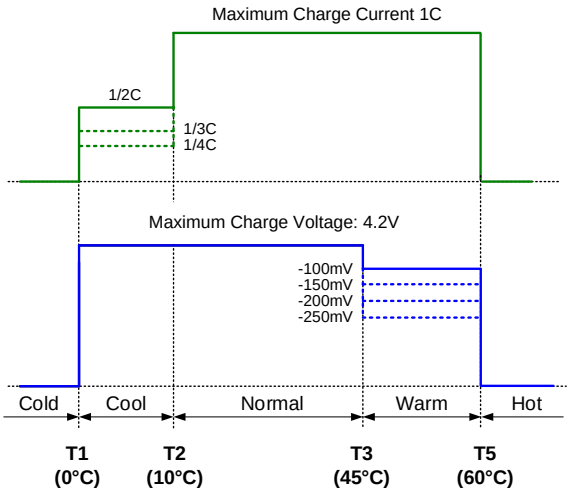


Figure 7: NTC JEITA Profile

Charge Enable Control

Charging can be disabled by pulling the NTC pin to GND. The $\overline{ACOK}$ pin stays low as long as a normal input is available. To enable charging, the following conditions must be met:

- The NTC pin is not pulled to GND.
- There is no NTC fault that could suspend charging.
- There is no timer fault.
- There is no thermal fault.

Floated NTC Mode

When the NTC pin is floated, V_{NTC} is 3.6V. Since this exceeds the 2.5V charge termination disable threshold, the charge termination and safety timer are disabled.

To avoid overlap between the termination disable threshold and the cold temperature threshold, an internal loop can decrease the NTC bias current when V_{NTC} exceeds 2V. This prevents a cold thermistor from setting V_{NTC} above 2.5V.

Input Over-Voltage Protection (OVP)

The MP2703 provides input OVP. When V_{IN} rises to the OVP threshold (V_{IN_OVP}), the MP2703 stops charging. When V_{IN} returns to its normal range, the MP2703 starts charging automatically.

The V_{IN_OVP} threshold is 6V for 1-cell applications and 14.4V for 2-cell applications.

Battery Over-Voltage Protection (OVP)

If V_{BATT} exceeds the battery OVP threshold (V_{BATT_OVP}), charging stops. If V_{BATT} is below the V_{BATT_OVP} falling threshold, the battery state transitions from battery OVP to charge termination.

Safety Charge Timer

The MP2703 provides a backup charge timer to ensure charge safety. When any new charge cycle starts, if the charging stays in trickle charge and pre-charge for 1 hour, or the entire charge process lasts for 10 hours (configurable via the OTP), charging automatically stops and the fault is reported. Once charging transitions from fast charge to pre-charge, the pre-charge timer resets.

After the safety timer expires, it can be reset by one of the actions below:

- Re-plug V_{IN}
- Pull the NTC pin to GND

Battery Dummy Load

The MP2703 integrates an internal 95mA dummy load on the BATT pin, which is controlled by the DIAG pin.

When V_{IN} is present, this dummy load is connected between BATT and GND if DIAG is high (see Figure 8).

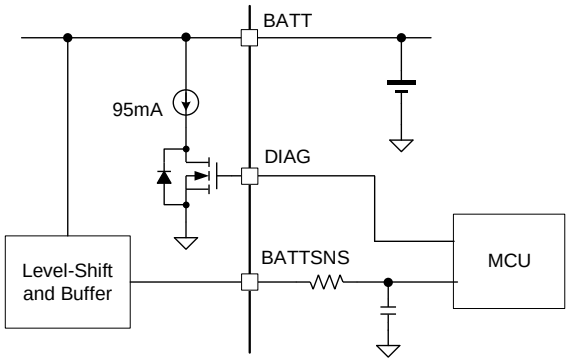


Figure 8: Dummy Load Control Function Block

Battery Voltage (V_{BATT}) Measurement

The MP2703 integrates a high-accuracy level-shift circuit to convert the high battery voltage to a lower value. This allows the MCU to measure this voltage directly. The voltage-sense gain is 1/4 for 1-cell applications and 1/8 for 2-cell applications.

This function is enabled when V_{IN} is present, The MCU measures V_{BATT} via the BATTSNS pin.

Battery Age Diagnosis

The internal battery dummy load and battery voltage measurement function can be used to diagnose the battery age.

When V_{IN} is present, the host should follow the steps below to diagnose a battery:

1. Pull the NTC pin low to disable the charge.
2. Measure V_{BATT} via BATTSNS.
3. Enable the dummy load by pulling the DIAG pin high.
4. Measure the BATSNS voltage again.
5. Disable the dummy load by pulling the DIAG pin low.
6. Re-enable charge by releasing the NTC pin.

The host can use the voltage difference between two measurements to estimate the battery's age.

Operation Indication

The MP2703 has two open-drain indicators to report the status of the input power and charging. Table 1 shows the truth table for the $\overline{ACOK}$ pin.

Table 1: $\overline{ACOK}$ Indication Truth Table

V_{IN} Status	$\overline{ACOK}$
V_{IN} UVLO	Hi-Z
V_{IN} OVP	Hi-Z
$V_{IN} < V_{BATT} + V_{HDRM}$	Hi-Z
Normal Input ($V_{IN} > V_{BATT} + V_{HDRM}$, and $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVP}$)	Low

For $\overline{CHG}$ indication, the $\overline{CHG}$ pin pulls low when charging is in progress. After charge termination, the $\overline{CHG}$ pin enters a high-impedance (Hi-Z) state. When charging is disabled by the NTC pin, the $\overline{CHG}$ pin is in Hi-Z. The $\overline{CHG}$ pin also can indicate certain fault events, such as an NTC fault, timer fault, and charge OCP.

After the input powers on or charging is enabled, there is a 600ms deglitch time for $\overline{CHG}$ indication, which is always Hi-Z during the blanking time (see Table 2).

Table 2: $\overline{CHG}$ Indication Truth Table

Charging Status	$\overline{CHG}$
Invalid input	High-Z
Charge disable by pulling NTC to ground	High-Z
Charge termination	High-Z
Charge in process	Low
NTC fault, Timer fault, Charge OCP	Blinking (1Hz)

Thermal Regulation and Thermal Shutdown

During the battery charging process, the MP2703 continuously monitors the internal junction temperature (T_J) to avoid overheating the chip. If the internal temperature reaches the thermal regulation threshold (T_{J_REG}), the MP2703 starts to reduce the charge current to prevent higher power dissipation.

If T_J reaches the thermal shutdown threshold (T_{J_SHDN}), the MP2703 stops charging immediately. Once T_J drops below the T_{J_SHDN} falling threshold, the device resumes normal operation.

One-Time Programmable (OTP) Memory

The MP2703 provides OTP memory to configure the default value of several parameters. See the One-Time Programmable (OTP) Memory Map section on page 20 for the configurable parameters. Contact MPS to obtain a custom OTP setting.

ONE-TIME PROGRAMMABLE (OTP) MEMORY MAP

REG00h: Battery Voltage Threshold Setting

This register sets the battery cells' information and battery regulation voltage for each cell.

Bits	Bit Name	Default	Description
7	CELLS	1'b0	Selects the battery cell. 0: 1 cell (default) 1: 2 cells
6	RESERVED	1'b0	Reserved.
5:0	VBATT_REG	6'b100100	Sets the battery regulation voltage. Range: 2.4V/cell (000000) to 4.5V/cell (101010) Offset: 2.4V/cell Step: 50mV/cell Default: 4.2V/cell (100100)

REG01h: Timer and Thermal Setting

This register sets the safety charge timer and internal junction temperature (T_J) regulation threshold.

Bits	Bit Name	Default	Description
7	TMR_PRE	1'b1	Sets the safety timer for trickle charge and pre-charge. 0: Disabled 1: 1 hour (default)
6	TMR_EN	1'b1	Enables safety timer control. 0: Disabled 1: Enabled (default)
5:3	TMR_SET	3'b010	Sets the safety timer for the entire charge process. Range: 2 hours (000) to 30 hours (111) Offset: 2 hours Step: 4 hours Default: 10 hours (010)
2	RESERVED	1'b0	Reserved.
1	TJ_REG	1'b1	Sets the T_J regulation loop. 0: 100°C 1: 120°C
0	RESERVED	1'b0	Reserved.

REG02h: Input Voltage Limit Setting

This register sets the input voltage limit (V_{IN_LIM}) loop threshold. If V_{IN} drops below this threshold, the charge current decreases to prevent V_{IN} from dropping further.

Bits	Bit Name	Default	Description
7:6	RESERVED	2'b00	Reserved.
5:4	VIN_LIM[1]	2'b10	Sets the V_{IN} limit. 00: Reserved 01: 4.375V/cell 10: 4.5V/cell (default) 11: 4.75V/cell
3:0	RESERVED	4'b0000	Reserved.

REG03h: JEITA Temperature Threshold Setting

This register sets the JEITA hot, warm, cool, and cold temperature thresholds.

Bits	Bit Name	Default	Description
7:6	VHOT	2'b10	Sets the hot falling threshold. 00: 0.208V (50°C) 01: 0.176V (55°C) 10: 0.151V (60°C, default) 11: 0.129V (65°C)
5:4	VWARM	2'b01	Sets the warm falling threshold. 00: 0.291V (40°C) 01: 0.245V (45°C, default) 10: 0.205V (50°C) 11: 0.176V (55°C)
3:2	VCOOL	2'b10	Sets the cool rising threshold. 00: 1.377V (0°C) 01: 1.111V (5°C) 10: 0.902V (10°C, default) 11: 0.737V (15°C)
1:0	VCOLD	2'b01	Sets the cold rising threshold. 00: 1.732V (-5ºC) 01: 1.377V (0°C, default) 10: 1.111V (+5°C) 11: 0.902V (+10°C)

REG04h: JEITA Protection Setting

This register sets the charging behavior within the JEITA warm and cool temperature windows.

Bits	Bit Name	Default	Description
7:6	WARM_ACT	2'b01	Sets the charge action when the NTC is warm. 00: No action. Charging stops when the NTC is hot 01: Reduce V_{BATT_REG} when the NTC is warm (default) 10: Reduce I_{CC} when the NTC is warm 11: Reduce both V_{BATT_REG} and I_{CC} when the NTC is warm
5:4	COOL_ACT	2'b10	Sets the charge action when the NTC is cool. 00: No action. Charging stops when NTC is cold 01: Reduce V_{BATT_REG} when the NTC is cool 10: Reduce I_{CC} when the NTC is cool (default) 11: Reduce both V_{BATT_REG} and I_{CC} when the NTC is cool
3:2	JEITA_VSET	2'b00	00: V_{BATT_REG} - 100mV/cell (default) 01: V_{BATT_REG} - 150mV/cell 10: V_{BATT_REG} - 200mV/cell 11: V_{BATT_REG} - 250mV/cell
1:0	JEITA_ISET	2'b00	00: 50% of I_{CC} (default) 01: 33% of I_{CC} 10: 25% of I_{CC} 11: 0% of I_{CC} (disable charge)

REG05h: Pre-Charge Threshold Setting

This register sets the pre-charge threshold.

Bits	Bit Name	Default	Description
7:2	RESERVED	6’b000000	Reserved.
1:0	VBATT_PRE	2’b01	Sets the pre-charge threshold. 00: 2.5V/cell 01: 2.8V/cell (default) 10: 3V/cell 11: 3.2V/cell

APPLICATION INFORMATION

Setting the Fast Charge Current

A resistor connected from ISET to GND sets I_{CC}. The relationship between I_{CC} and the setting resistor can be estimated with Equation (6):

$$I_{CC} = \frac{V_{REF} / k}{R_{ISET}} \quad (6)$$

Where V_{REF} is 1.2V, and *k* is 2.18 x 10^{-3}.

For example, to set I_{CC} to 1A, then R_{ISET} is calculated to be 550Ω.

Setting the Pre-Charge Current and Termination Current

The pre-charge current is set as a percentage of fast charge current by connecting a resistor from the IPRE_TERM pin to GND.

The ratio of I_{PRE} to I_{CC} can be calculated with Equation (7):

$$I_{PRE} / I_{CC} = R_{IPRE\_TERM} / K_{PRE\text{-}CC} \quad (7)$$

Where $K_{TERM\text{-}CC}$ is 112.36Ω/%. For example, if R_{IPRE_TERM} is 1.13kΩ, then the proportion between I_{TERM} and I_{CC} is 10%.

When the IPRE_TERM pin is floating, I_{TERM} is fixed at 20% of the set I_{CC}.

The termination current is fixed at 50% of the pre-charge current.

Setting the Battery Cell

The MP2703 supports 1-cell and 2-cell batteries, the battery cell number is configured via the OTP.

For 2-cell applications, battery hot insertion or shorting is not allowed when V_{IN} is present and charging is enabled.

Selecting the Input Capacitor

An input capacitor is required for stability. Connect a minimum 1μF capacitor between IN and GND for stable operation across full load current range. The capacitor's voltage rating should exceed the normal input voltage level. A low-ESR, X5R/X7R ceramic capacitor is recommended.

Selecting the BATT to GND Capacitor

The MP2703 requires that a capacitor be connected from BATT to GND. A minimum 1μF ceramic capacitor with X5R/X7R dielectrics is sufficient for most applications.

Selecting the NTC Resistor

The MP2703 supports a configurable JEITA, which is based on a precise 50μA current source flowing through the external NTC thermistor. To use this function, connect a 10kΩ NTC thermistor with a β = 3435K from the NTC pin to GND.

The JEITA threshold can be configured via the OTP.

If the NTC pin is not used, connect a fixed 10kΩ resistor from NTC to GND.

PCB Layout Guidelines

Place the external capacitors as close to the IC as possible to ensure the smallest input/output inductance and ground impedance.

TYPICAL APPLICATION CIRCUIT

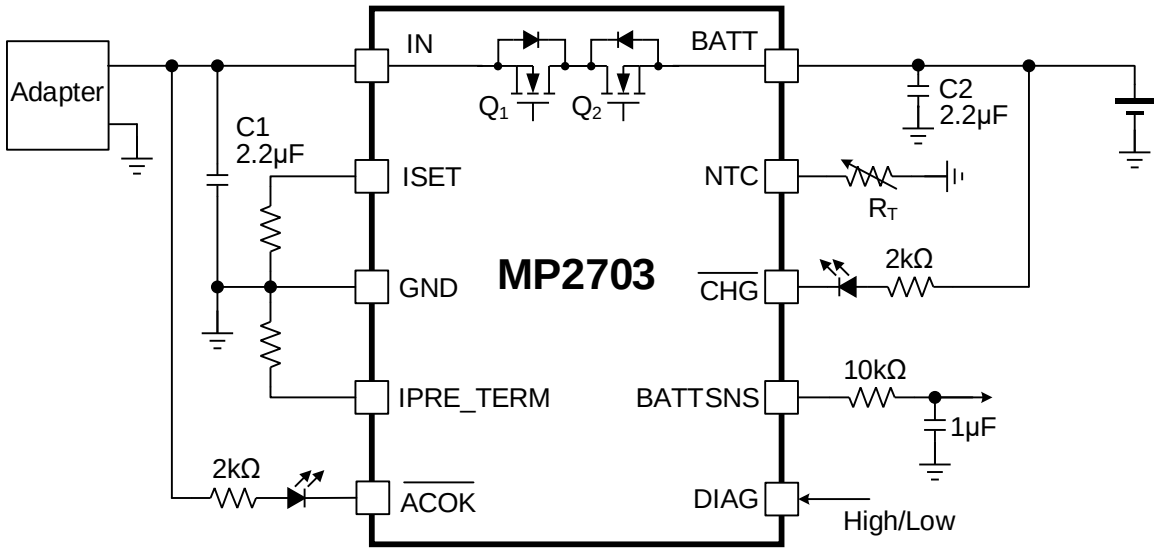


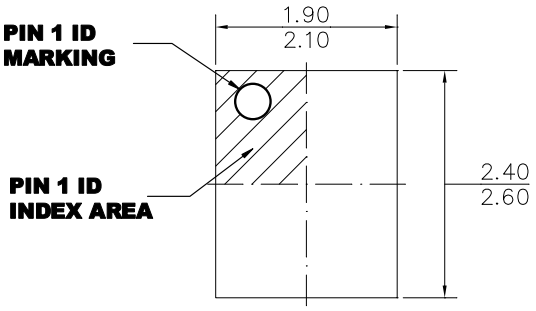
Figure 9: Typical Application Circuit

Table 3: Key BOM of Figure 9

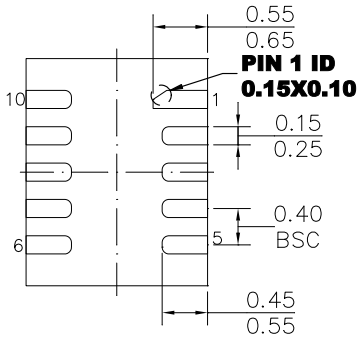
Qty	Ref	Value	Description	Package	Manufacturer
1	C1	2.2µF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	C2	2.2µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	R_T	10kΩ	β = 3435K	Any	Any

PACKAGE INFORMATION

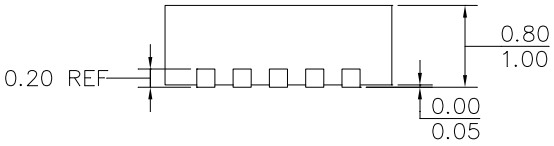
QFN-10 (2mmx2.5mm)



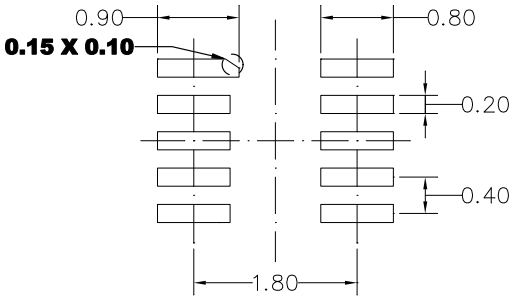
TOP VIEW



BOTTOM VIEW



SIDE VIEW

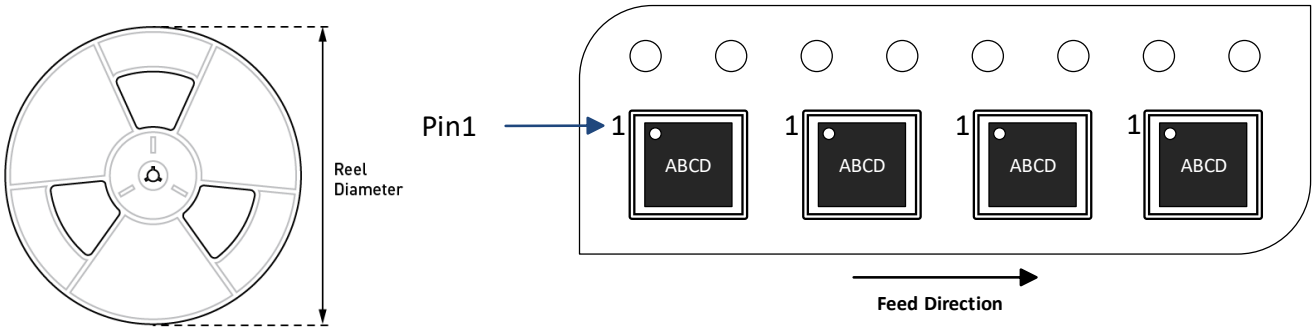


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2703GRP-xxxx-Z	QFN-10 (2mmx2.5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/12/2023	Initial Release	-