NCP5603

High Efficiency Charge Pump Converter

The NCP5603 is an integrated circuit dedicated to the medium power White LED applications. The power conversion is achieved by means of a charge pump structure, using two external ceramic capacitors, making the system extremely tiny. The device supplies a constant voltage to the load from a low battery voltage source. It is particularly suited for the High Efficiency LED used in low cost, low power applications, with high extended battery life.

Features

- Wide Battery Supply Voltage Range: 2.7 < V_{CC} < 5.5 V
- Automatic Operating Mode 1X, 1.5X and 2X Improves Efficiency
- Dimmable Output Current
- Up to 350 mA Output Pulsed Current
- Selectable Output Voltage
- High Efficiency Up To 90%
- Supports 2.5 kV ESD, Human Body Model
- Supports 200 V Machine Model ESD
- Low 40 mA Short Circuit Current
- Pb−Free Package is Available

Applications

- High Power LED
- Back Light Display
- High Power Flash

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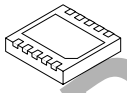
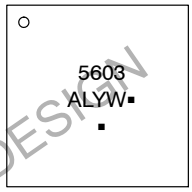
MARKING DIAGRAM

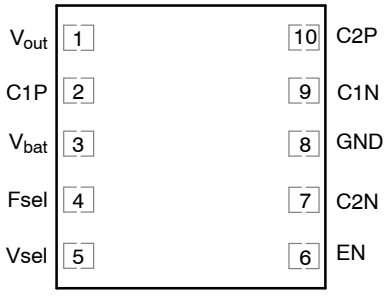


DFN10, 3x3
MN SUFFIX
CASE 485C



5603 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5603MNR2	DFN10	3000/ Tape & Reel
NCP5603MNR2G	DFN10 (Pb−Free)	3000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

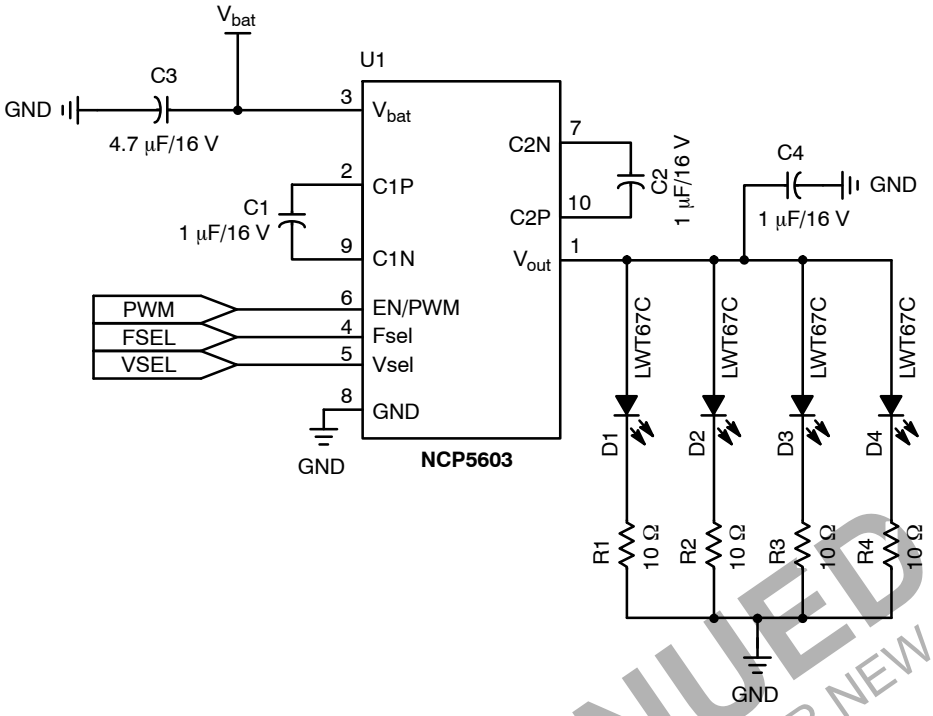


Figure 1. Typical Application

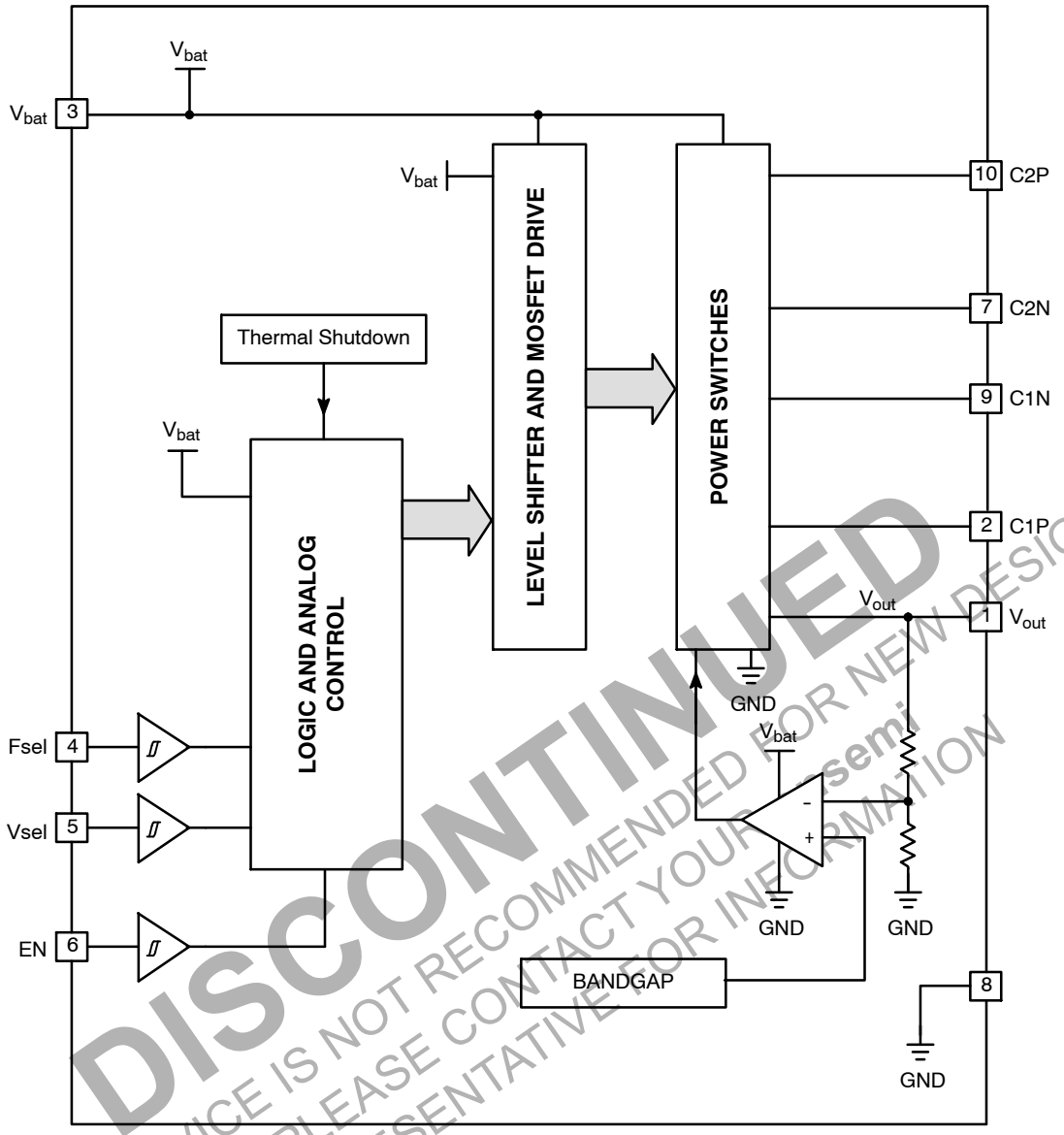


Figure 2. Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1	V_{out}	OUTPUT, PWR	This pin supplies the regulated voltage to the external LED. Since high current transients are present in this pin, care must be observed to avoid voltage spikes in the system. Good high frequency layout technique must be observed.
2	C1N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1P, pin 9. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.
3	V_{bat}	POWER	This pin shall be connected to the power source, and must be decoupled to Ground by a low ESR capacitor (2.2 μF/6.3 V ceramic or better (see Note 1)).
4	Fsel	INPUT, Digital	This pin is used to program the operating frequency: Fsel = 0 → Fop = 262 kHz Fsel = 1 → Fop = 650 kHz
5	Vsel	INPUT, Digital	This pin setup the output voltage: Vsel = 0 → V_{out} = 4.5 V Vsel = 1 → V_{out} = 5.0 V
6	EN/PWM	INPUT, Digital	This pin controls the activity of the NCP5603 chip: EN/PWM = Low → the chip is deactivated, the load is disconnected EN/PWM = High → the chip is activated and the load is connected to the regulated output current. The NCP5603 can operate either in a continuous mode (EN/PWM = High), or can be controlled by a PWM pulse applied to EN/PWM to dim the output light. When EN/PWM is Low, the external load is disconnected from the converter, providing a very low standby current. The pull down built−in resistance makes sure the chip is deactivated even if the EN/PWM pin is disconnected (see Note 2).
7	C2N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C2P, pin 10. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.
8	GND	GROUND	This pin combines the Signal ground and the Power ground and must be connected to the system ground. Using good quality ground plane is mandatory to avoid spikes on the logic signal lines.
9	C1P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1N, pin 2. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.
10	C2P	POWER	One side of the external charge pump capacitor is connected to this pin, associated with C2N, pin 7. Using low ESR ceramic capacitor is recommended to optimize the Charge Pump efficiency.

1. Using ceramic 16 V working voltage capacitors is recommended to compensate the DC bias effect encountered with such type of capacitors.
2. Any external impedance connected to pin 6 shall be 10 kΩ or higher.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{bat}	7.0	V
Power Supply Current	I_{bat}	800	mA
Digital Input Pins	V_{in}	−0.5 V < Vbat < Vbat +0.5 V < 6.0 V	V
Digital Input Pins	Iin	±5.0	mA
Output Voltage	V_{out}	5.5	V
ESD Capability (Note 3) Human Body Model Machine Model	V_{ESD}	 2.5 200	 kV V
DFN10, 3x3 Package Power Dissipation @ Tamb = +85°C Thermal Resistance, Junction−to−Air ($R_{\theta JA}$)	 P_{DS} $R_{\theta JA}$	 580 68.5	 mW °C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Latchup Current Maximum Rating		100 mA per JEDEC standard, JESD78	
Moisture Sensitivity Level (MSL)		1 per IPC/JEDEC standard, J−STD−020A	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.5 kV per JEDEC Standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC Standard: JESD22−A115.
4. The maximum package power dissipation limit must not be exceeded.

ELECTRICAL CHARACTERISTICS @ 2.85 V < Vbat < 5.5 V (−40°C to +85°C ambient temperature, unless otherwise noted).

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Power Supply	3	V_{bat}	2.85	–	5.5	V
Quiescent Current @ V_{bat} = 3.7 V, I_{out} = 0 μA	3	Iqsc				mA
@ Pulsed Clock Fop = 262 kHz			–	–	0.8	
@ Pulsed Clock Fop = 650 kHz			–	–	1.2	
@ Continuous Clock Fop = 262 kHz			–	1.0	–	
@ Continuous Clock Fop = 650 kHz			–	2.1	–	
Shutdown Current @ I_{out} = 0 mA, EN/PWM = L	3	I_{stdb}				μA
@ 2.85 < V_{bat} < 4.2 V			–	–	2.5	
@ V_{bat} = 5.5 V			–	–	4.0	
Output Voltage Regulation	3	V_{out}				V
@ Vsel = 1, 2.85 V < V_{bat} < 4.3 V			4.75	5.0	5.25	
@ Vsel = 0, 2.85 V < V_{bat} < 4.3 V			4.275	4.5	4.725	
Continuous DC Load Current (Note 7)	3	I_{out}				mA
Cin = 1.0 μF, C_{FLY} = 1.0 μF, Cout = 1.0 μF						
@ Vsel = 1, 3.2 V < V_{bat} < 4.3 V			–	–	160	
@ Vsel = 0, 3.2 V < V_{bat} < 4.3 V			–	–	200	
@ Vsel = 1, 2.85 V < V_{bat} < 4.3 V			–	–	80	
@ Vsel = 0, 2.85 V < V_{bat} < 4.3 V			–	–	120	
Pulsed Output Current	3	I_{FLH}				mA
Cin = 10 μF, C_{FLY} = 1.0 μF, Cout = 10 μF, V_{bat} = 3.6 V Pwidth = 500 ms, −40°C < T_A < +65°C			–	350	–	
Output Continuous Short Circuit Current, V_{out} = 0 V	3	Isch	–	40	100	mA
Operating Frequency (Note 5)		Fop				kHz
@ Fsel = 0, 2.85 V < V_{bat} < 4.5 V			210	262	320	
@ Fsel = 1, 2.85 V < V_{bat} < 4.5 V			500	650	1000	
Output Voltage Ripple (Note 6)	3	V_{PP}				mV
Fop = 262 kHz, I_{out} = 60 mA (Note 7)						
@ C_{out} = 1.0 μF			–	150	–	
@ C_{out} = 4.7 μF			–	25	60	
Digital Input High Level	4, 5, 6	V_{IH}	1.3	–	–	V
Digital Input Low level	4, 5, 6	V_{IL}	–	–	0.4	V
Output Power Efficiency		Pη				%
@ V_{bat} = 3.3 V, V_{out} = 5.0 V, I_{out} = 60 mA, Fop = 262 kHz			–	75	–	
@ V_{bat} = 3.9 V, V_{out} = 5.0 V, I_{out} = 160 mA, Fop = 650 kHz			–	84	–	
Thermal Shut Down Protection		T_{HSD}	–	160	–	°C
Hysteresis			–	20	–	

5. Temperature range guaranteed by design, not production tested.
6. Smaller footprint associated to lower working voltages (10 V or 6.3 V, size 0805 or 0602) can be used, but care must be observed to prevent DC bias effect on the capacitance final value. See capacitor manufacturer data sheets.
7. Ceramic X7R, ESR < 100 mΩ, SMD type capacitors are mandatory to achieve the I_{out} specifications. Depending upon the PCB layout, it might be necessary to use two 2.2 μF/6.3 V/ceramic capacitors in parallel, yielding an improved V_{out} noise over the temperature range. On the other hand, care must be observed to take into account the DC bias impact on the capacitance value. See ceramic capacitor manufacturer data sheets.
8. Digital inputs undershoot < − 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{bat}.

TYPICAL CHARACTERISTICS

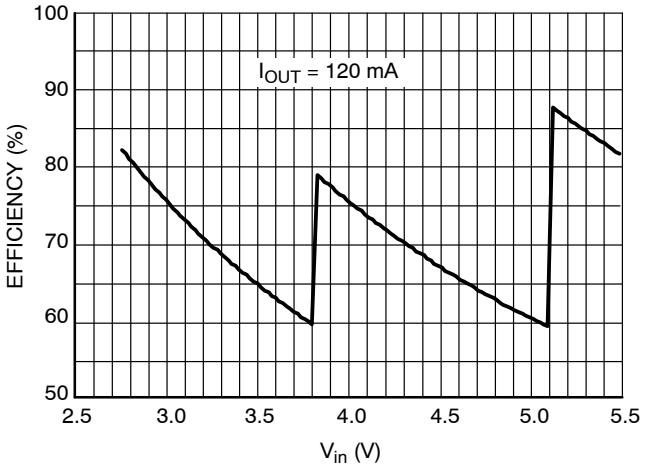


Figure 3. Operating Modes Transitions and Output Power Efficiency @ V_{out} = 4.5 V/262 kHz

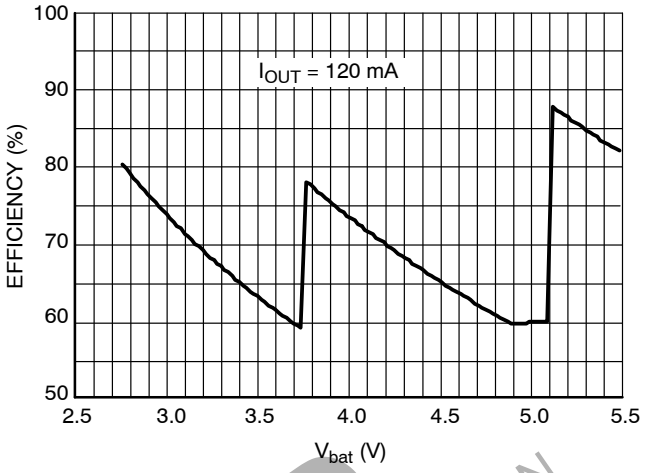


Figure 4. Operating Modes Transitions and Output Power Efficiency @ V_{out} = 4.5 V/650 kHz

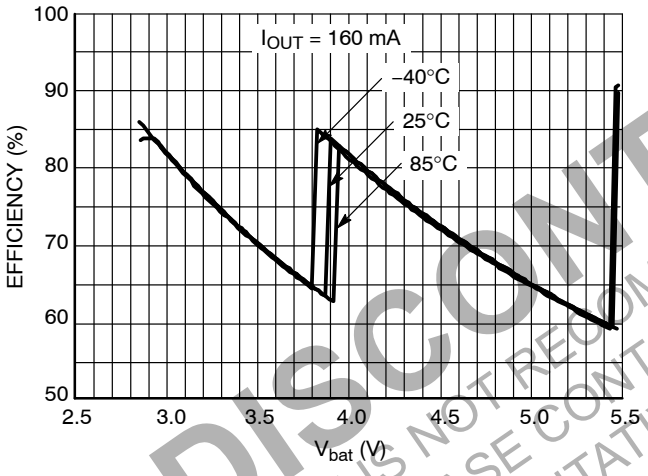


Figure 5. Operating Modes Transitions and Output Power Efficiency @ V_{out} = 5.0 V/650 kHz

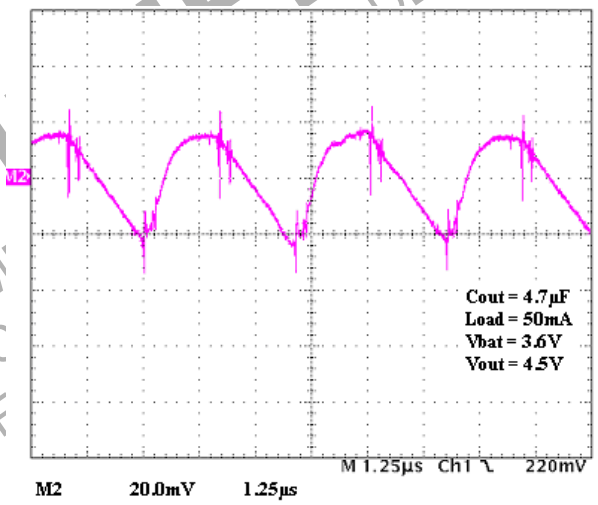


Figure 6. Typical Output Voltage Ripple

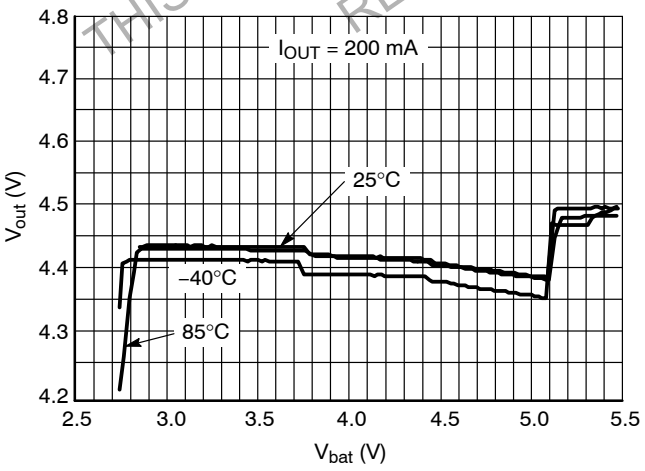
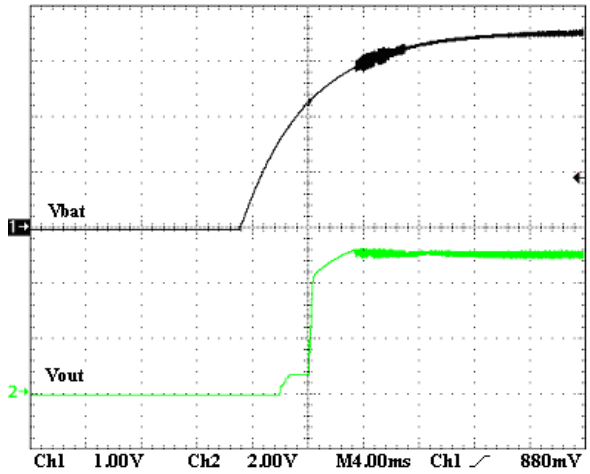


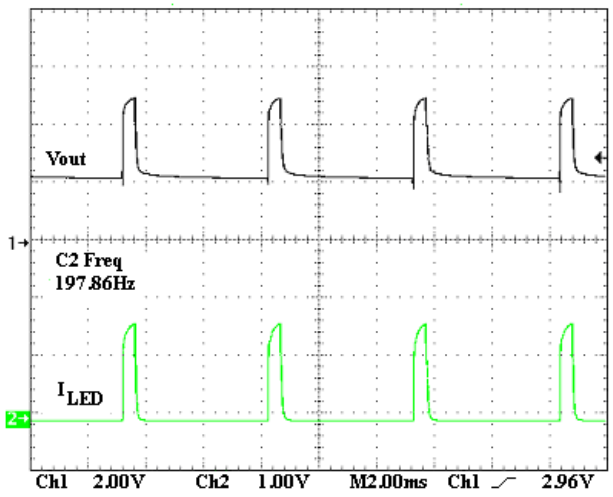
Figure 7. Typical Output Voltage Line Regulation



Test conditions: V_{bat} = 3.6 V, V_{out} = 5 V, Load = 4*LW87S, I_{LED} = 25mA

Figure 8. Output Voltage Startup from Scratch

TYPICAL CHARACTERISTICS



Test conditions: V_{bat} = 3.6 V, V_{out} = 5 V, Load = 4*LW87S, I_{LED} = 25mA

Figure 9. Typical PWM Dimming

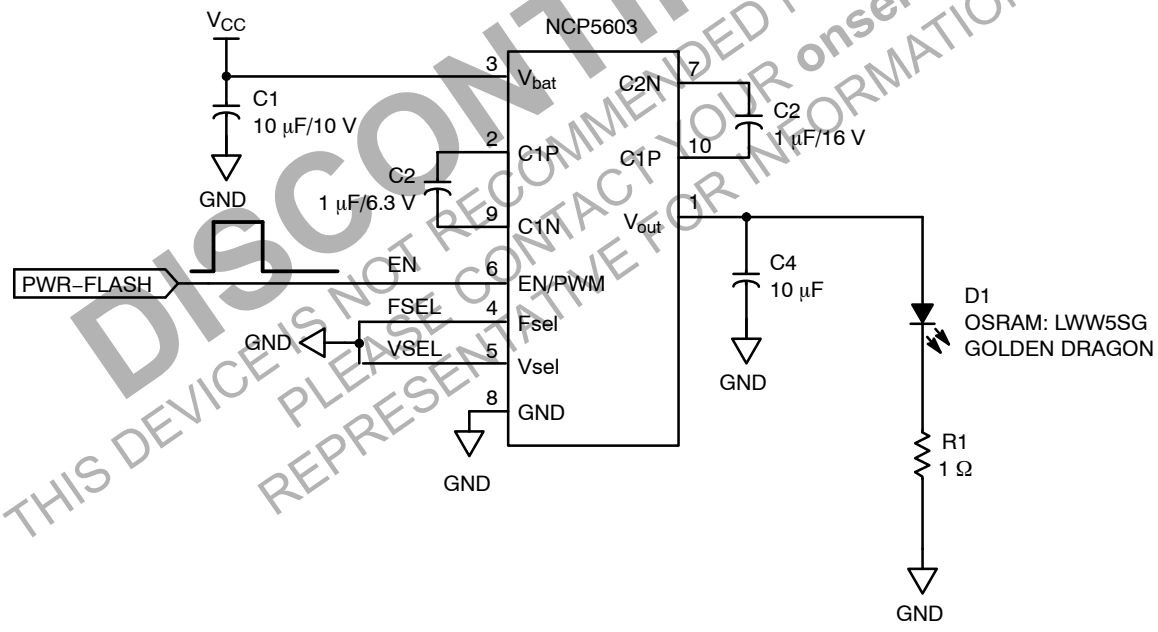


Figure 10. Typical High Power Flash Circuit

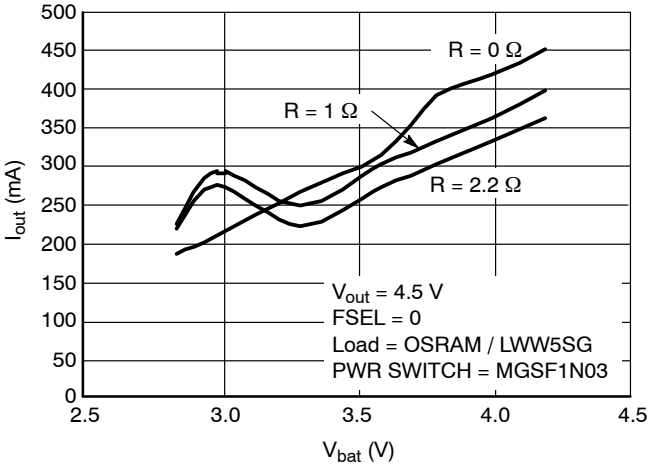


Figure 11. NCP5603 Output Current

Table 1. Ceramic Preferred Capacitors

Manufacturer	Type/Series	Format	Value
TDK	C3216X5R1C475MT	1206	4.7 μF / 16 V
TDK	C2012X5R1C225MT	0805	2.2 μF / 16 V
TDK	C2012X5R1C105MT	0805	1.0 μF / 16 V

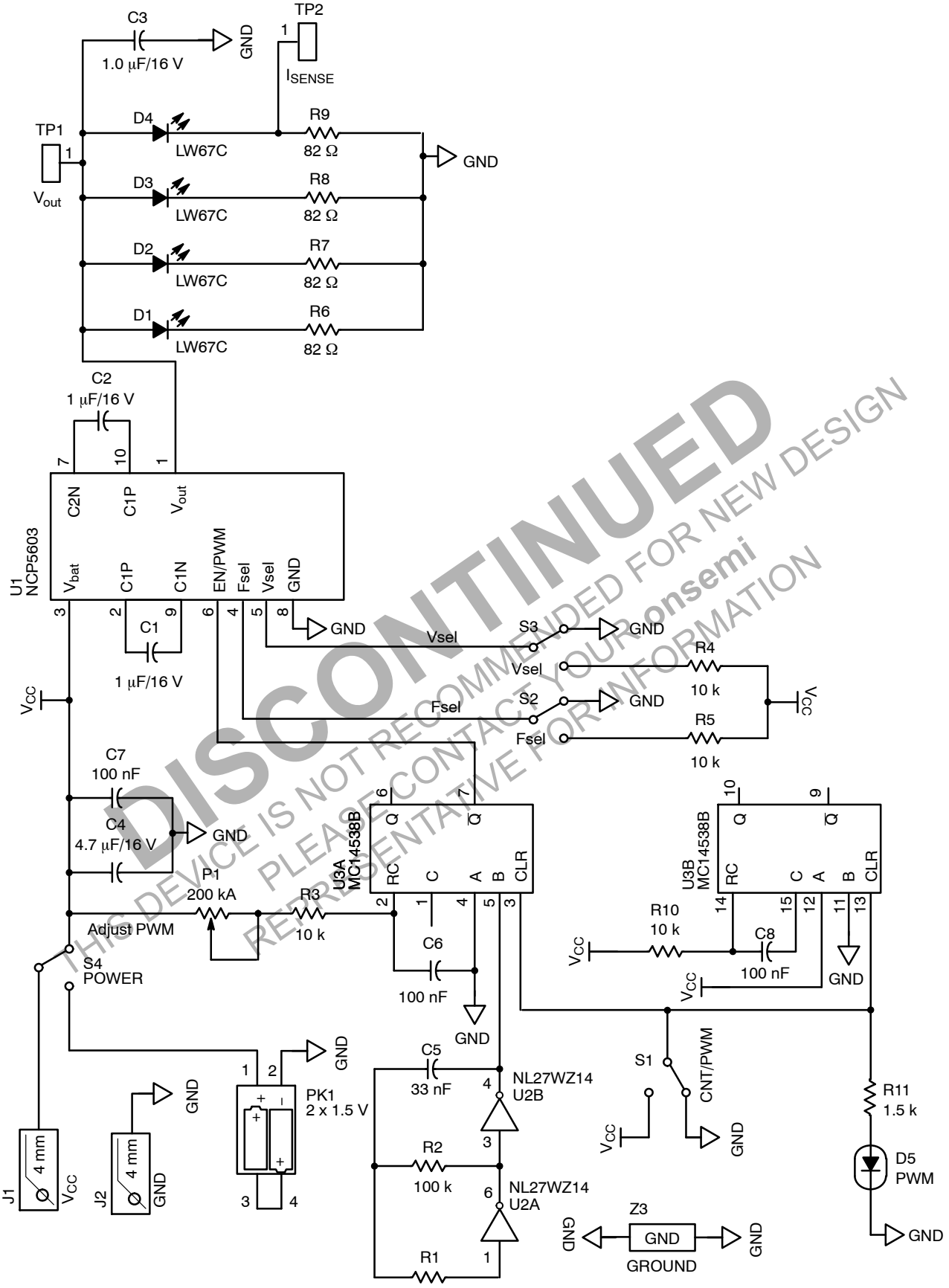


Figure 12. Evaluation Board Schematic Diagram

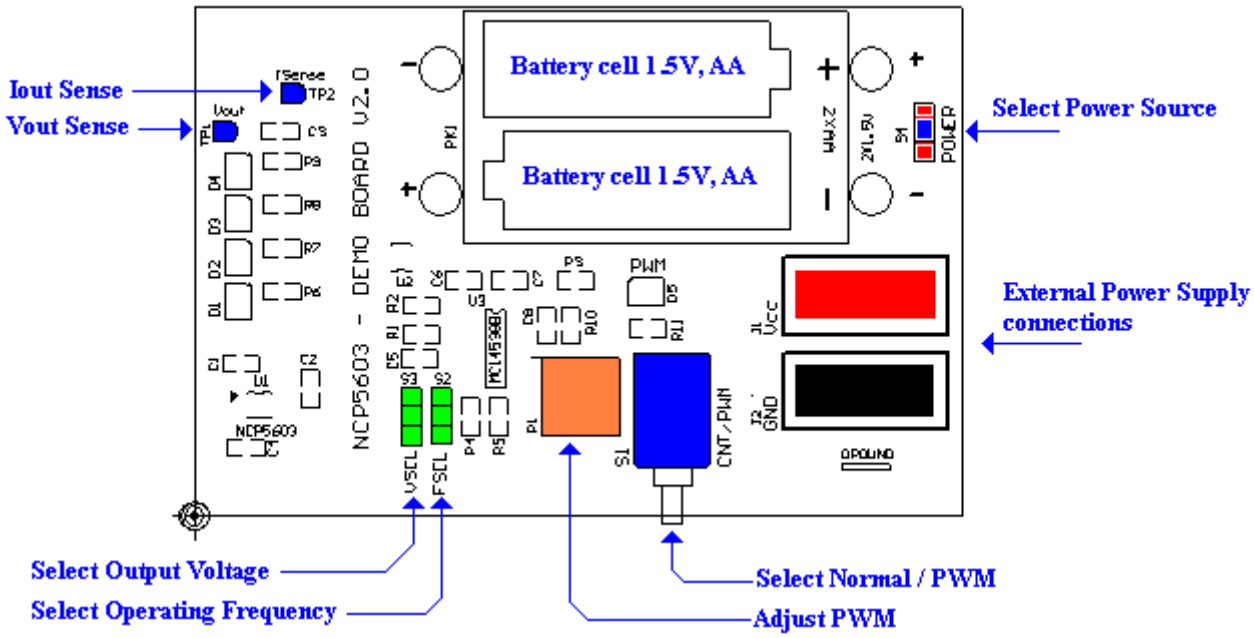
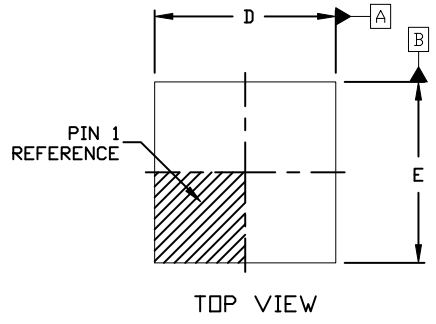


Figure 13. Evaluation Board: Silk View (Top View)

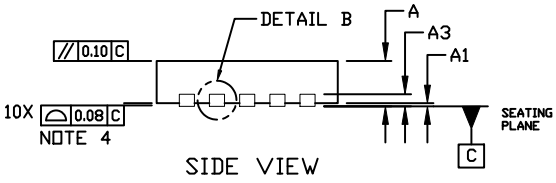
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

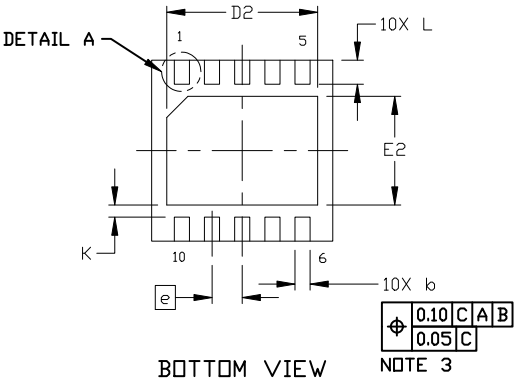
SCALE 2:1



TOP VIEW

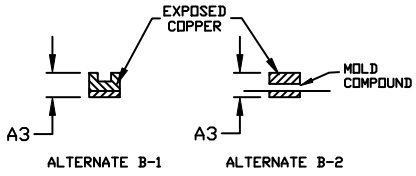


SIDE VIEW

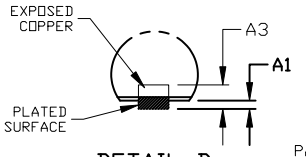


BOTTOM VIEW

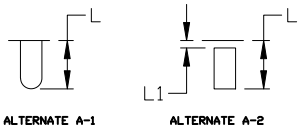
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

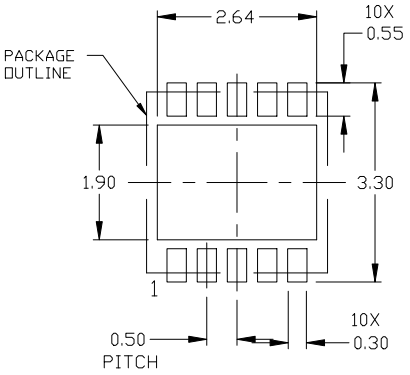


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON03161D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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