MPQ6541-AEC1, MPQ6541A-AEC1

40V, 8A, Three-Phase Power Stage, AEC-Q100 Qualified

DESCRIPTION

The MPQ6541-AEC1 and MPQ6541A-AEC1 are three-phase brushless DC (BLDC) motor drivers with three integrated half-bridges. The three half-bridges consist of six N-channel power MOSFETs. The MPQ6541-AEC1 and MPQ6541A-AEC1 also integrate six pre-drivers, two gate driver power supplies, and three current-sense amplifiers.

The MPQ6541-AEC1 has ENBL and PWM inputs for each half-bridge; the MPQ6541A-AEC1 has separate high-side (HS) and low-side (LS) inputs. Otherwise, these parts are identical. References to the MPQ6541-AEC1 also apply to the MPQ6541A-AEC1, unless otherwise noted.

The MPQ6541-AEC1 can deliver up to 12A of peak current for 1 second, or 8A of continuous current, depending on thermal and PCB conditions. The device uses an internal charge pump to generate the gate driver supply voltage for the high-side MOSFETs (HS-FETs), and a trickle charge circuit that maintains sufficient gate driver voltage to operate at 100% duty cycle.

Internal safety features include thermal shutdown, under-voltage lockout (UVLO), and over-current protection (OCP).

The MPQ6541-AEC1 is available in a TQFN-26 (6mmx6mm) package.

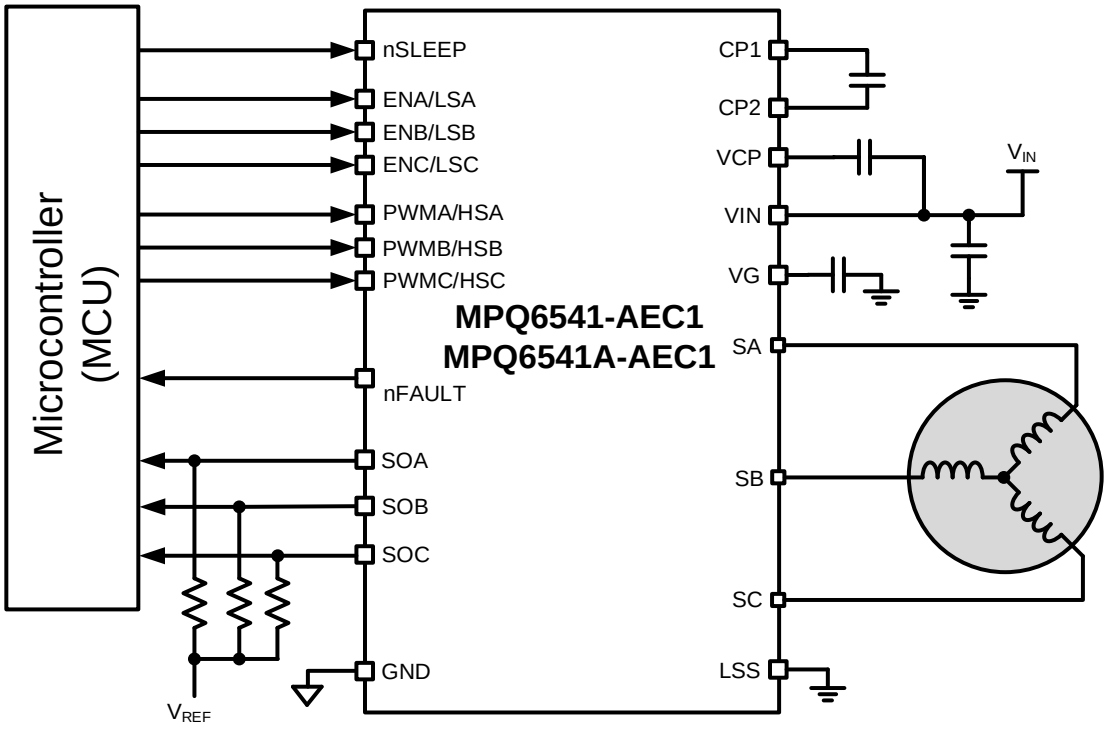
FEATURES

- 4.75V to 40V Operating Supply Voltage
- Three Integrated Half-Bridge Drivers
- 8A of Continuous Output Current
- MOSFET On Resistance: 15mΩ per FET
- MPQ6541-AEC1: PWM and ENBL Inputs
  MPQ6541A-AEC1: HS and LS Inputs
- Internal Charge Pump Supports 100% Duty Cycle Operation
- Automatic Synchronous Rectification
- Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)
- Thermal Shutdown Protection
- Over-Current Protection (OCP)
- Integrated, Bidirectional Current-Sense Amplifiers
- Available in a TQFN-26 (6mmx6mm) Package with Wettable Flank
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Brushless DC (BLDC) Motor Drivers
- Permanent Magnet Synchronous Motor (PMSM) Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ6541GQKTE-AEC1*	TQFN-26 (6mmx6mm)	*See Below*	1
MPQ6541AGQKTE-AEC1**	TQFN-26 (6mmx6mm)	*See Below*	

* For Tape & Reel, add suffix -Z (e.g. MPQ6541GQKTE-AEC1-Z).

** For Tape & Reel, add suffix -Z (e.g. MPQ6541AGQKTE-AEC1-Z).

TOP MARKING (MPQ6541GQKTE-AEC1)

MPSYYWW
MP6541
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP6541-AEC1: Part number
LLLLLLLLL: Lot number
E: Wettable lead flank

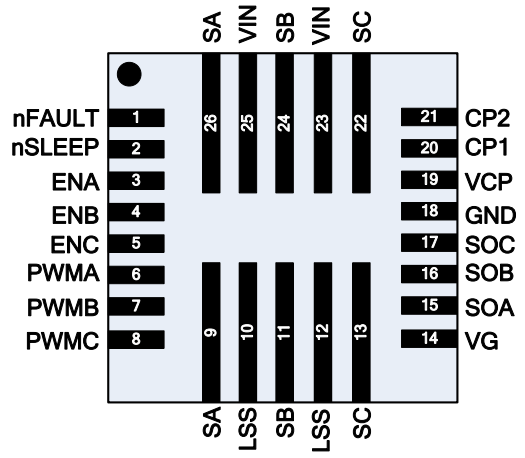
TOP MARKING (MPQ6541AGQKTE-AEC1)

MPSYYWW
MP6541A
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP6541A-AEC1: Part number
LLLLLLLLL: Lot number
E: Wettable lead flank

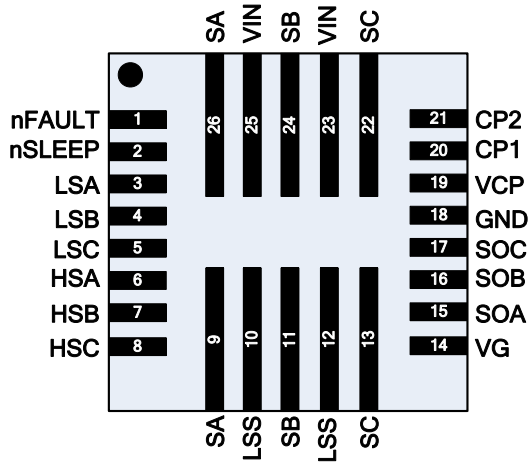
PACKAGE REFERENCE

TOP VIEW



MPQ6541-AEC1, TQFN-26 (6mmx6mm)

TOP VIEW



MPQ6541A-AEC1, TQFN-26 (6mmx6mm)

PIN FUNCTIONS

Pin #	MPQ6541-AEC1 Pin Name	MPQ6541A-AEC1 Pin Name	Description
1	nFAULT		**Fault indication.** nFAULT has an open-drain output that pulls to logic low under fault conditions.
2	nSLEEP		**Sleep mode input.** Pull nSLEEP to logic low to enter low-power sleep mode; pull nSLEEP to logic high for normal operation. nSLEEP has an internal pull-down resistor.
3	ENA	-	**Enable pin for phase A.**
	-	LSA	**Enables the low-side MOSFET (LS-FET) for phase A.**
4	ENB	-	**Enable pin for phase B.**
	-	LSB	**Enables the LS-FET for phase B.**
5	ENC	-	**Enable pin for phase C.**
	-	LSC	**Enables the LS-FET for phase C.**
6	PWMA	-	**PWM input for phase A.**
	-	HSA	**Enables the high-side MOSFET (HS-FET) for phase A.**
7	PWMB	-	**PWM input for phase B.**
	-	HSB	**Enables the HS-FET for phase B.**
8	PWMC	-	**PWM input for phase C.**
		HSC	**Enables the HS-FET for phase C.**
9, 26	SA		**Phase A output.**
10, 12	LSS		**Low-side source connection for phases A, B, and C.** These pins must be connected directly to GND.
11, 24	SB		**Phase B output.**
13, 22	SC		**Phase C output.**
14	VG		**Low-side gate drive output.** Connect a 4.7µF, 10V ceramic capacitor with X7R dielectrics from VG to ground.
15	SOA		**Current-sense output for phase A.**
16	SOB		**Current-sense output for phase B.**
17	SOC		**Current-sense output for phase C.**
18	GND		**Ground.**
19	VCP		**Charge pump output.** Connect a 1µF, 16V ceramic capacitor with X7R dielectrics from VCP to VIN.
20	CP1		**Charge pump capacitor pins.** Connect a 100nF ceramic capacitor with X7R dielectrics rated for V_{IN} (at minimum) from CP1 to CP2.
21	CP2		
23, 25	VIN		**Input supply voltage.**

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +45V
CP2, VCP .....V_{IN} to V_{IN} + 6.5V
SA/B/C .....-0.3V to +45V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
TQFN-26 (6mmx6mm)……5.84W
Storage temperature ..... -55°C to +150°C
Junction temperature .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM) 2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4.75V to 40V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-26 (6mmx6mm)……21.4….12.8..°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, LSS = GND = 0V, unless otherwise noted.

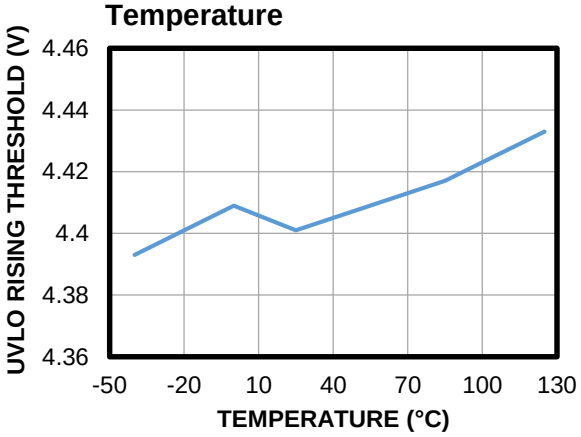
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.75		40	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		4	8	mA
	I_{SLEEP}	nSLEEP = 0		1		µA
Control Logic						
Input logic ‘low’ threshold	V_{IL}				0.8	V
Input logic ‘high’ threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		+20	µA
	$I_{IN(L)}$	V_{IL} = 0V	-20		+20	µA
Power up delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		1		ms
Internal pull-down resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT pull-down R_{ON}	$R_{ON(NFAULT)}$			10		Ω
Protection Circuits						
UVLO threshold	V_{UVLO}	V_{IN} rising	4	4.4	4.8	V
UVLO hysteresis	ΔV_{UVLO}			470		mV
OVP threshold	V_{OVP}	V_{IN} rising	44.5	48	51.5	V
OVP hysteresis	ΔV_{OVP}			1.3		V
HS OCP threshold	$I_{OCP(HS)}$		10	19		A
LS OCP threshold	$I_{OCP(LS)}$		17.5	25		A
OCP deglitch time (5)	t_{OCD}			0.4		µs
OCP retry time	t_{OCR}			2		ms
Thermal shutdown (5)	T_{TSD}			150		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			25		°C
Current-Sense						
Current-sense ratio		A phase	1/13000	1/11600	1/10000	A/A
		B phase	1/13000	1/11500	1/9750	
		C phase	1/12500	1/11000	1/9500	
Current-sense output offset current	I_{SOx}	A phase current = 0A	-35	-5	+25	µA
		B phase current = 0A	-26	-3	+21	
		C phase current = 0A	-33	-5	+26	µA
Current-sense output voltage swing (5)			0		5	V
Current-sense minimum load impedance (5)		Pull-up		1.8		kΩ
		Pull-down		1		
Outputs						
HS-FET on resistance	$R_{ON(HS)}$	I_{OUT} = 1A, T_J = 25°C		15	18	mΩ
LS-FET on resistance	$R_{ON(LS)}$	I_{OUT} = 1A, T_J = 25°C		15	18	
Output rising time (5)		I_{OUT} = 1A		0.45		V/ns
Output falling time (5)		I_{OUT} = 1A		0.85		V/ns
Charge pump output voltage	V_{CP}			V_{IN} + 5		V
V_{CP} switching frequency	f_{CP}			2000		kHz

Note:

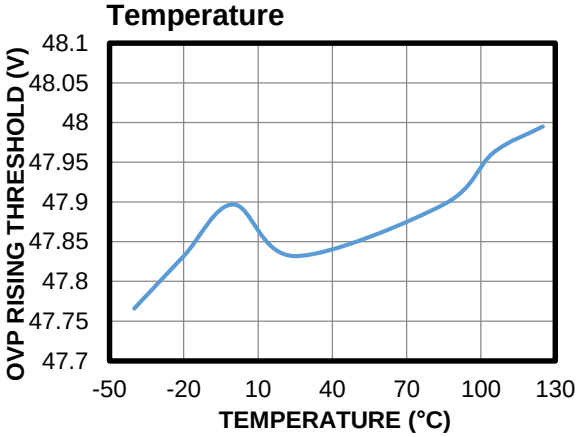
5) Not tested in production.

TYPICAL CHARACTERISTICS

UVLO Rising Threshold vs. Temperature

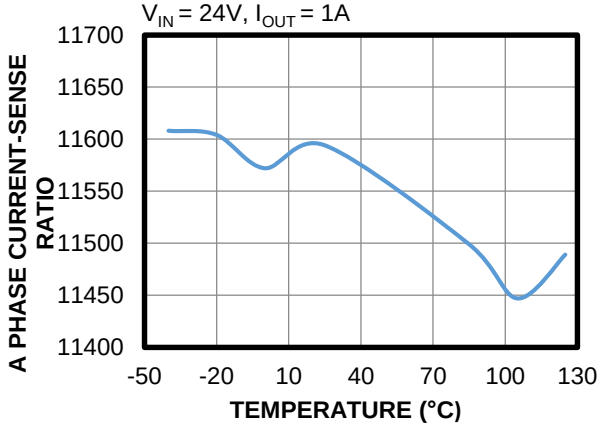


OVP Rising Threshold vs. Temperature



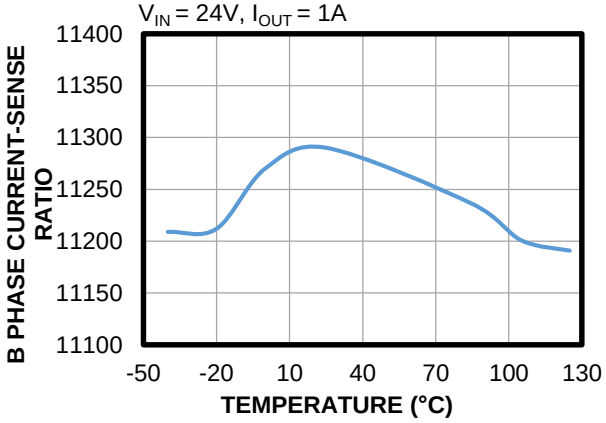
A Phase Current-Sense Ratio vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



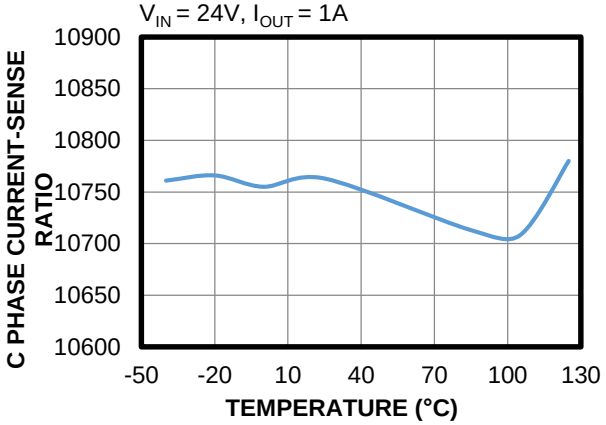
B Phase Current-Sense Ratio vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



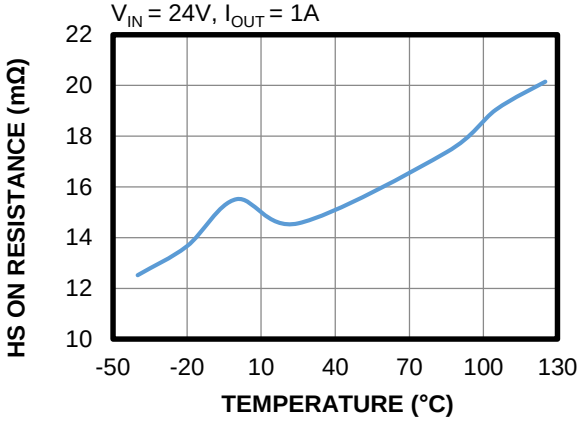
C Phase Current-Sense Ratio vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



HS On Resistance vs. Temperature

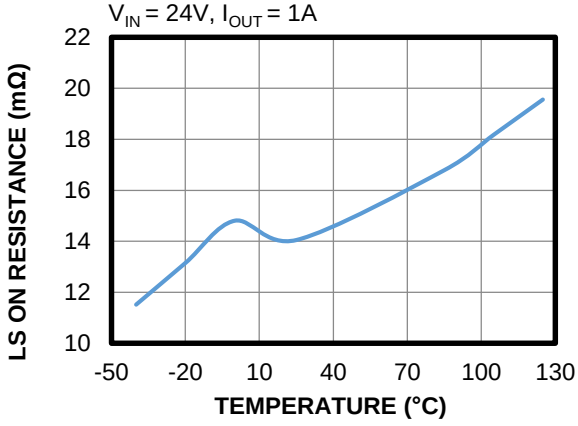
V_{IN} = 24V, I_{OUT} = 1A



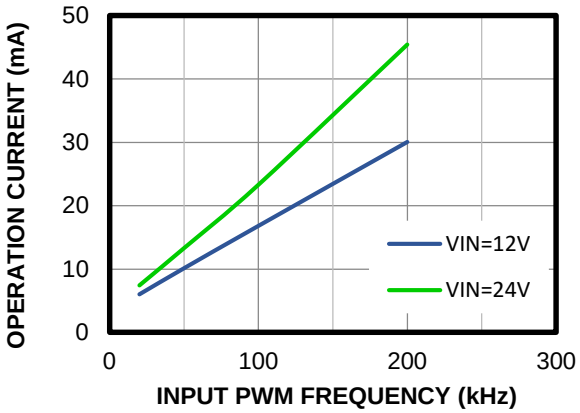
TYPICAL CHARACTERISTICS *(continued)*

LS On Resistance vs. Temperature

V_{IN} = 24V, I_{OUT} = 1A



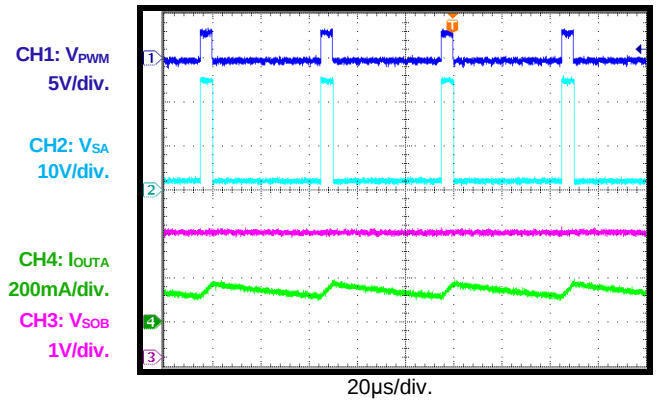
Operation Current vs. Input PWM Frequency



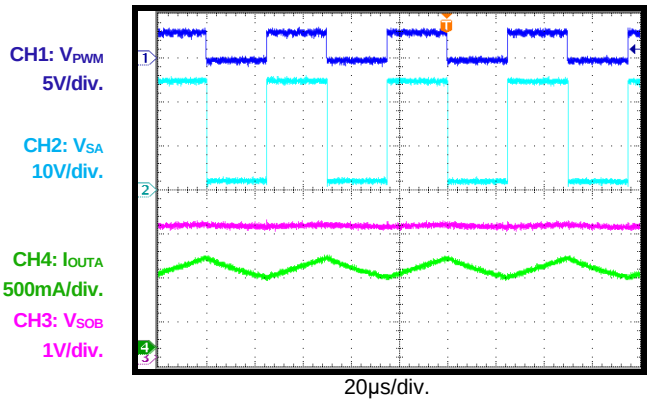
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, A phase switching with a 20kHz frequency, B phase LS on, C phase disabled, V_{REF} = 5V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

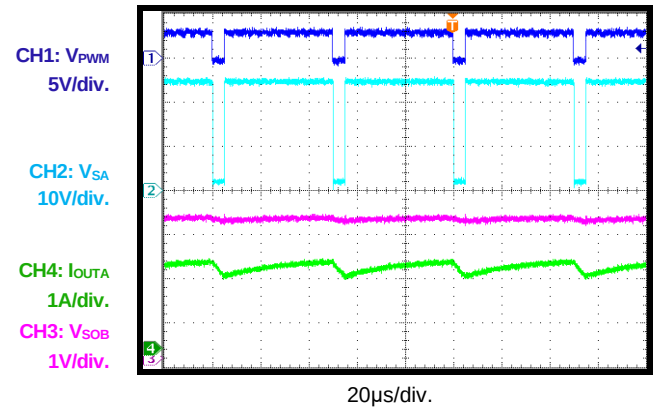
Steady State
Duty cycle = 10%



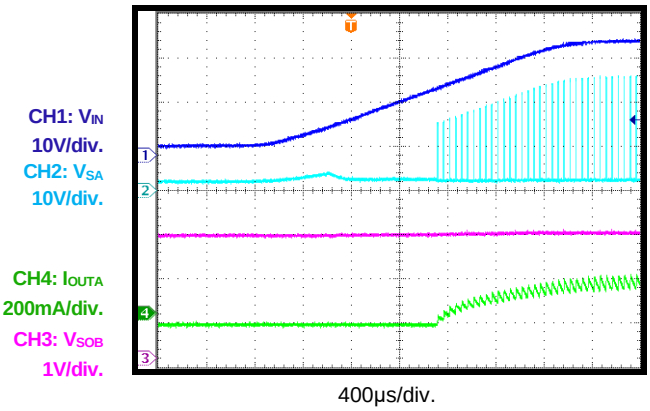
Steady State
Duty cycle = 50%



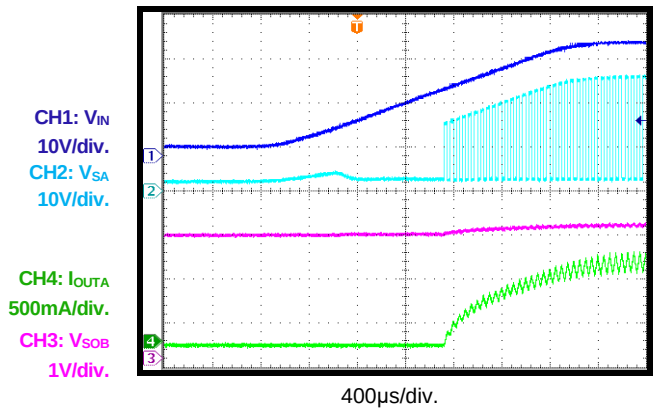
Steady State
Duty cycle = 90%



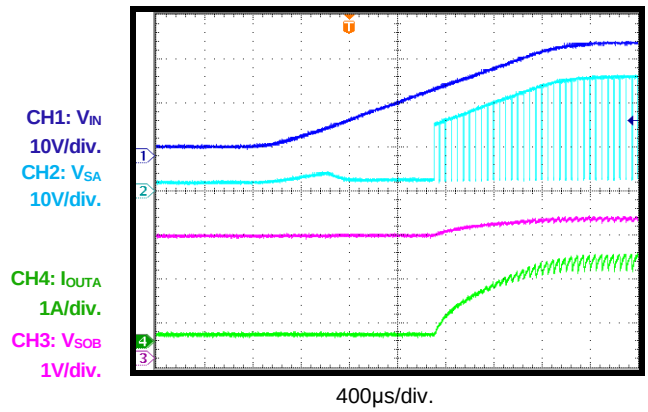
Start-Up
Duty cycle = 10%



Start-Up
Duty cycle = 50%



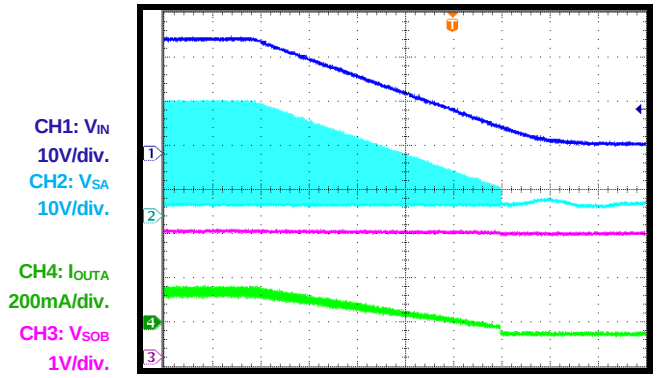
Start-Up
Duty cycle = 90%



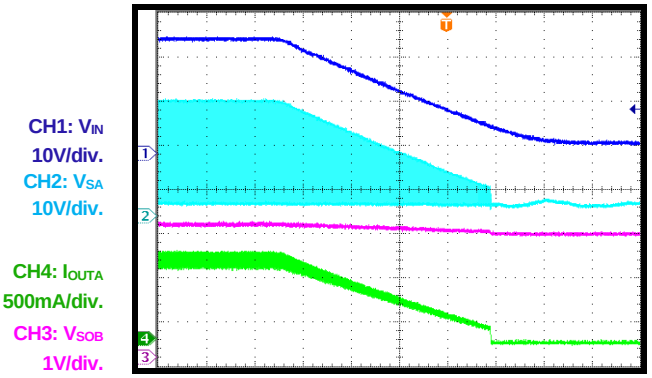
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, A phase switching with a 20kHz frequency, B phase LS on, C phase disabled, V_{REF} = 5V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

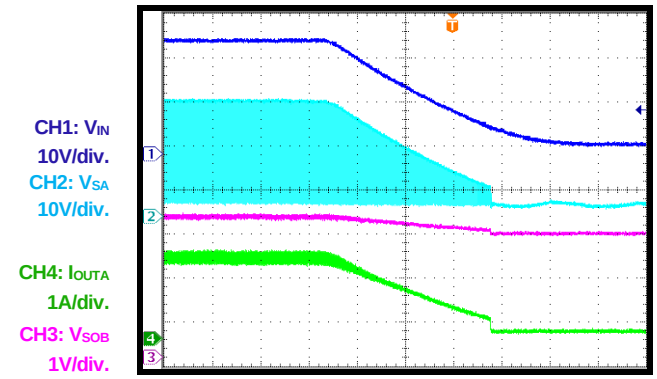
Shutdown
Duty cycle = 10%



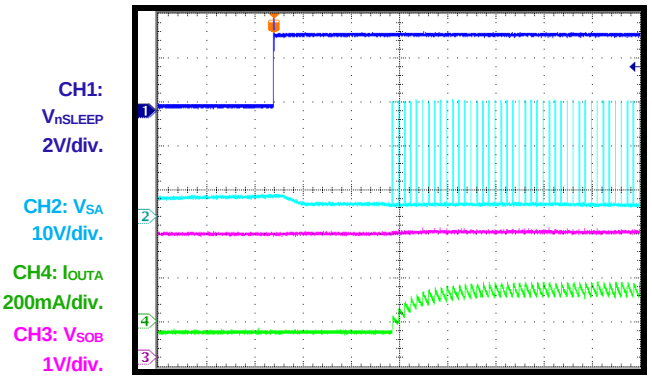
Shutdown
Duty cycle = 50%



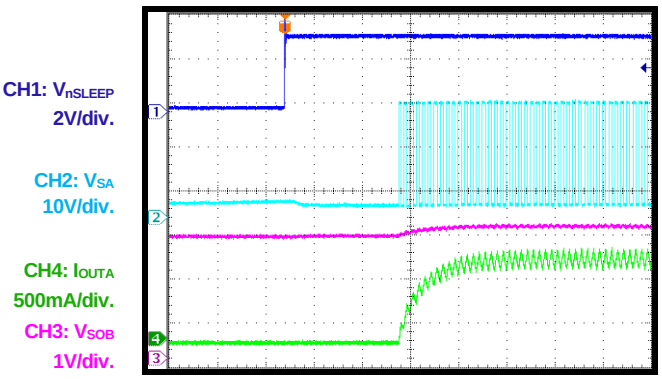
Shutdown
Duty cycle = 90%



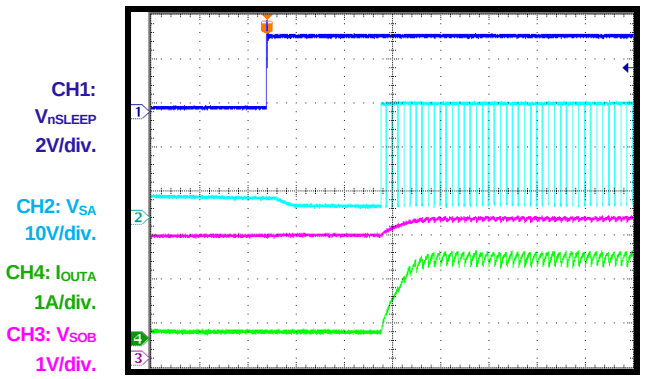
Sleep Recovery
Duty cycle = 10%



Sleep Recovery
Duty cycle = 50%



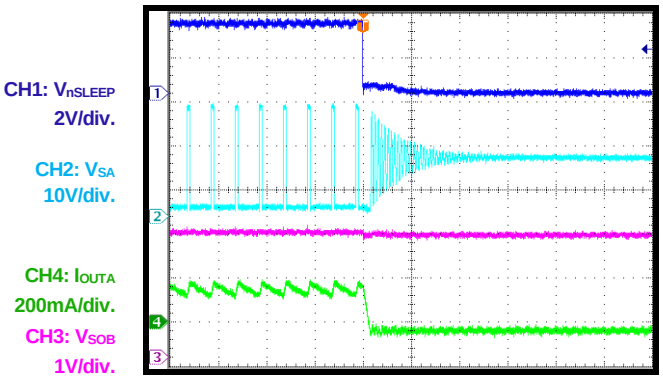
Sleep Recovery
Duty cycle = 90%



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, A phase switching with a 20kHz frequency, B phase LS on, C phase disabled, V_{REF} = 5V, current-sense resistor divider = 5kΩ, T_A = 25°C, resistor + inductor load: 5Ω + 1mH/phase with star connection, unless otherwise noted.

Sleep Entry
Duty cycle = 10%



Sleep Entry
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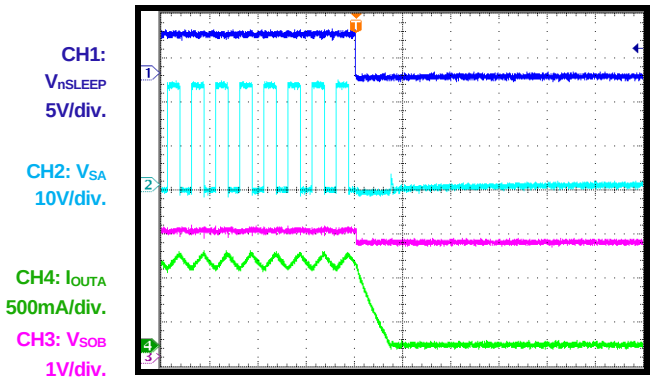

Sleep Entry
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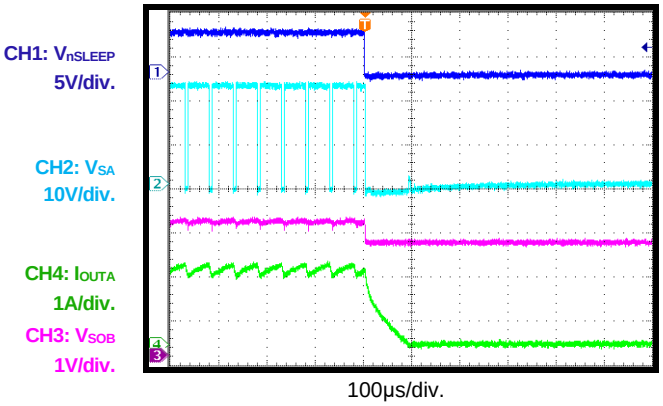


FUNCTIONAL BLOCK DIAGRAM

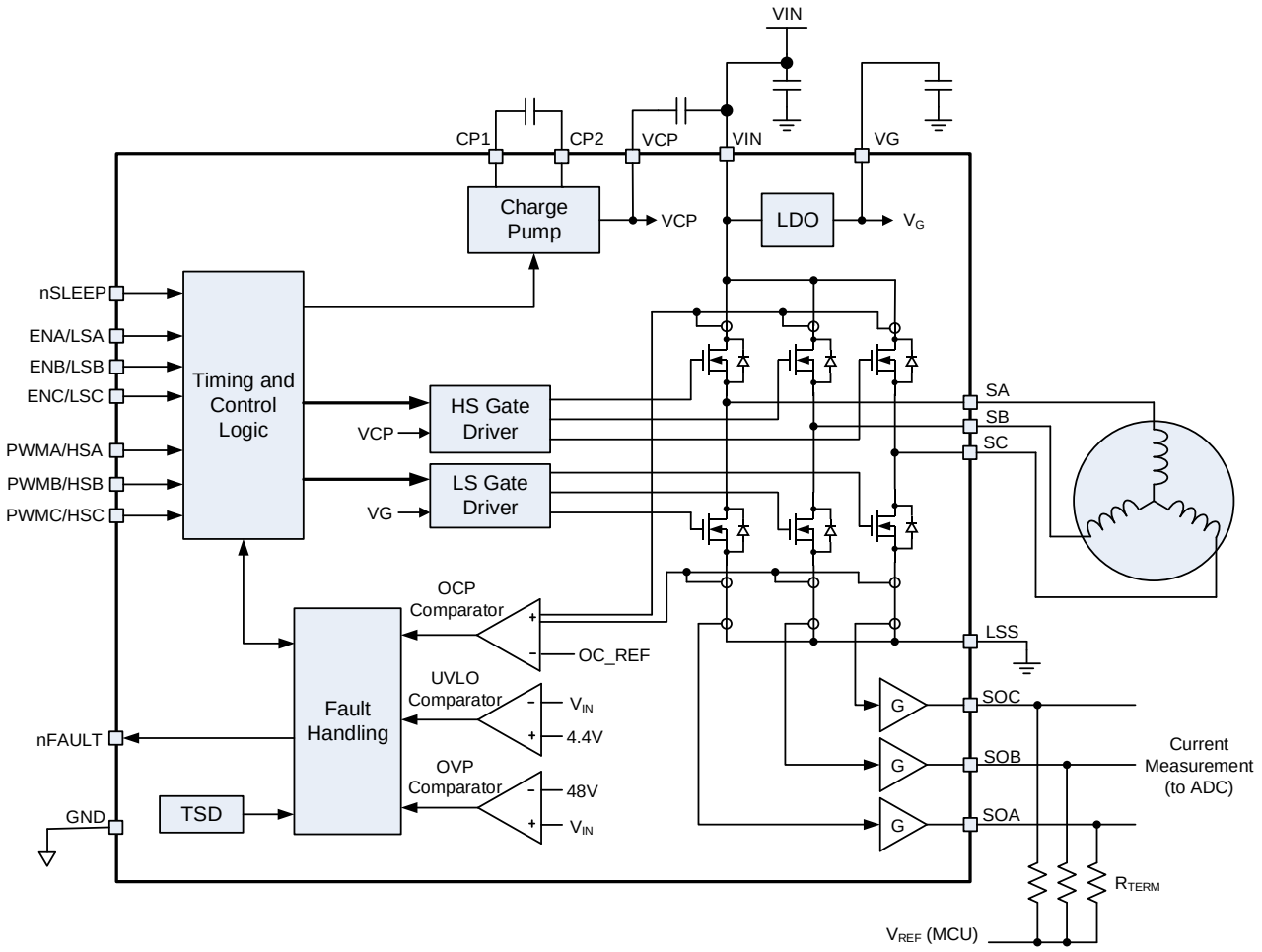


Figure 1: Functional Block Diagram

OPERATION

Input Logic

The MPQ6541-AEC1 has three logic input pins (ENA, ENB, and ENC) that enable corresponding outputs (SA, SB, and SC). When ENx is low, the corresponding output is disabled (output is at high impedance), and the PWM input on that phase is ignored. When ENx is high, the output is enabled, and the PWM input controls the state of the output (see Table 1).

Table 1: Input Logic Truth Table

ENx	PWMx	Sx
High	High	VIN
High	Low	GND
Low	-	High impedance

The MPQ6541A-AEC1 has separate inputs that are used to enable the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) of each phase independently (see Table 2).

Table 2: Input Logic Truth Table

HSx	LSx	Sx
Low	Low	High impedance
Low	High	GND
High	Low	VIN
High	High	High impedance

Note that the logic inputs have internal, 500kΩ pull-down resistors.

nSLEEP Operation

Driving nSLEEP low puts the device into a low-power sleep state. In this state, all the internal circuits are disabled. All inputs are ignored when nSLEEP is active low. When the MPQ6541-AEC1 wakes up from sleep mode, it takes about 1ms before the device responds to the inputs. The nSLEEP input has a 500kΩ pull-down resistor.

Current-Sense Amplifiers

The current flowing in each of the three outputs is sensed by the internal current-sense circuits. Each phase has an output pin that sources or sinks a current proportional to the current flowing in each phase. Note that only the current flowing in the LS-FET is sensed, and this current is sensed in both forward and reverse directions.

To convert this current into a voltage (i.e. to input to an analog-to-digital converter (ADC)), a termination resistor (R_{REF}) is connected between SOx and a reference voltage. When there is no current flowing, the resulting output is equal to the reference voltage. When current is flowing, the voltage (V_{SOUT}) is above or below the reference voltage. V_{SOUT} can be calculated with Equation (1):

$$V_{SOUT} = V_{REF} + (R_{REF} \times I_{LOAD}) / 11{,}000 \quad (1)$$

To terminate the outputs when using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and ground. The resulting ADC code is half-scale at 0A.

Figure 2 shows a simplified drawing of the current measurement circuit.

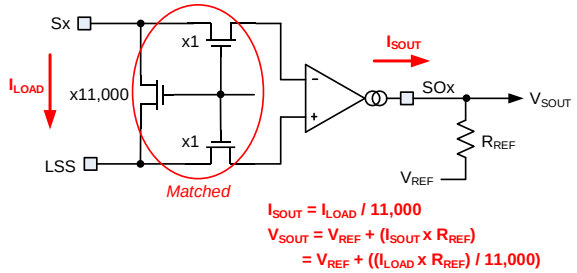


Figure 2: Current Measurement Circuit

Automatic Synchronous Rectification

When driving a current through an inductive load while the output MOSFETs are both turned off, the recirculation current must continue flowing. Typically, this current is passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MPQ6541-AEC1 implements an automatic synchronous rectification feature.

When both the HS-FET and LS-FET are turned off and the voltage on an Sx output pin is driven below ground, the LS-FET turns on until the current flowing through it is close to 0A, or until the HS-FET is commanded to turn on. Similarly, if Sx rises above V_{IN}, the HS-FET turns on until the current is close to 0A, or the LS-FET turns on.

nFAULT Output

The MPQ6541-AEC1 provides an nFAULT output pin that is driven active low if a fault occurs, such

as over-current protection (OCP) or over-temperature protection (OTP). nFAULT is an open-drain output that must be pulled up by an external pull-up resistor.

Input Under-Voltage Lockout (UVLO) Protection

If the VIN voltage (V_{IN}) falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the over-voltage protection (OVP) threshold, all output MOSFETs are disabled. The nFAULT pin is not driven active low. Operation resumes automatically when V_{IN} falls below the OVP threshold.

Thermal Shutdown

If the die temperature exceeds the safe limits, all output MOSFETs are disabled, and nFAULT is driven low. Once the die temperature falls to a safe level, operation resumes automatically.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by disabling its gate driver. If the OC limit is reached and lasts longer than the OC deglitch time, all six output MOSFETs are disabled (outputs have high impedance), and nFAULT is driven low. During this time, synchronous rectification is used to decay the current. Typically, the outputs are disabled for 2ms, and are re-enabled automatically.

OC conditions on both high-side and low-side devices (i.e. a short to ground, supply, or across the motor winding) result in an OC shutdown.

Figure 3 shows a simplified diagram of the OCP circuit for one output.

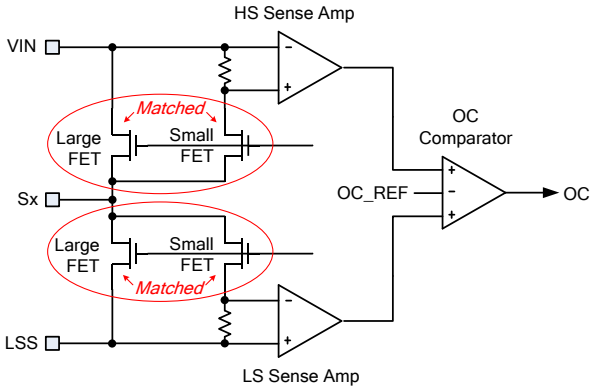


Figure 3: OCP Measurement Circuit

Charge Pump and VG Regulator

An internal LDO regulator generates a low-side gate drive voltage that is about 5.5V. Place a bypass capacitor between 4.7µF and 10µF from VG to ground.

A charge pump generates the gate drive for the HS-FETs. The charge pump requires two external capacitors: a 0.1µF ceramic capacitor rated for at least V_{IN} between the CP1 and CP2 pins, and a 1µF ceramic capacitor rated for at least 10V between VIN and VCP.

APPLICATION INFORMATION

Selecting the Charge Pump External Capacitors

Table 3 lists recommended external charge pump capacitors.

Table 3: External Charge Pump Capacitor Selection

	Min	Typ	Max	Units
CP1 to CP2 capacitor		0.1		µF
CP1 to CP2 capacitor voltage	V_{IN}			V
VCP to VIN capacitor		1		µF
VCP to VIN capacitor voltage	10			V
VG capacitor	4.7		10	µF
VG capacitor voltage	10			V

PCB Layout Guidelines

PCB layout is critical for stable operation. For the best results, refer to Figure 4 and Figure 5, and follow the guidelines below:

1. Place supply bypass and charge pump capacitors as close as possible to the IC (ideally, place them adjacent to the IC pins on the same PCB layer).
2. Supply bypass and charge pump capacitors can also be placed on the opposite side of the PCB directly under the IC, using vias to make connections.
3. Place as much copper as possible on the long pads.
4. Place large copper areas on the pads and on the same outer copper layer as the device.
5. Thermal vias can be placed inside the pad area to move heat to the copper layers.
6. Place the vias just outside the pad area if via-in-pad construction is not possible.

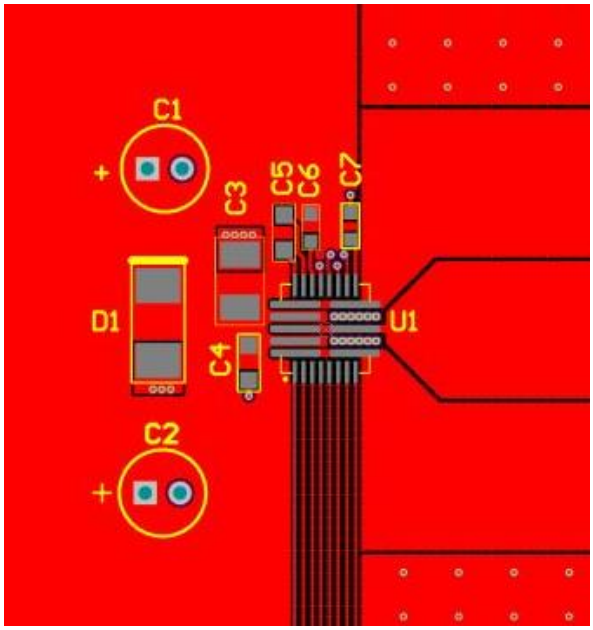


Figure 4: Recommended PCB Layout

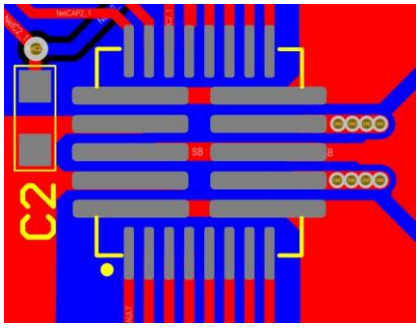


Figure 5: Thermal Vias outside Pads

TYPICAL APPLICATION CIRCUIT

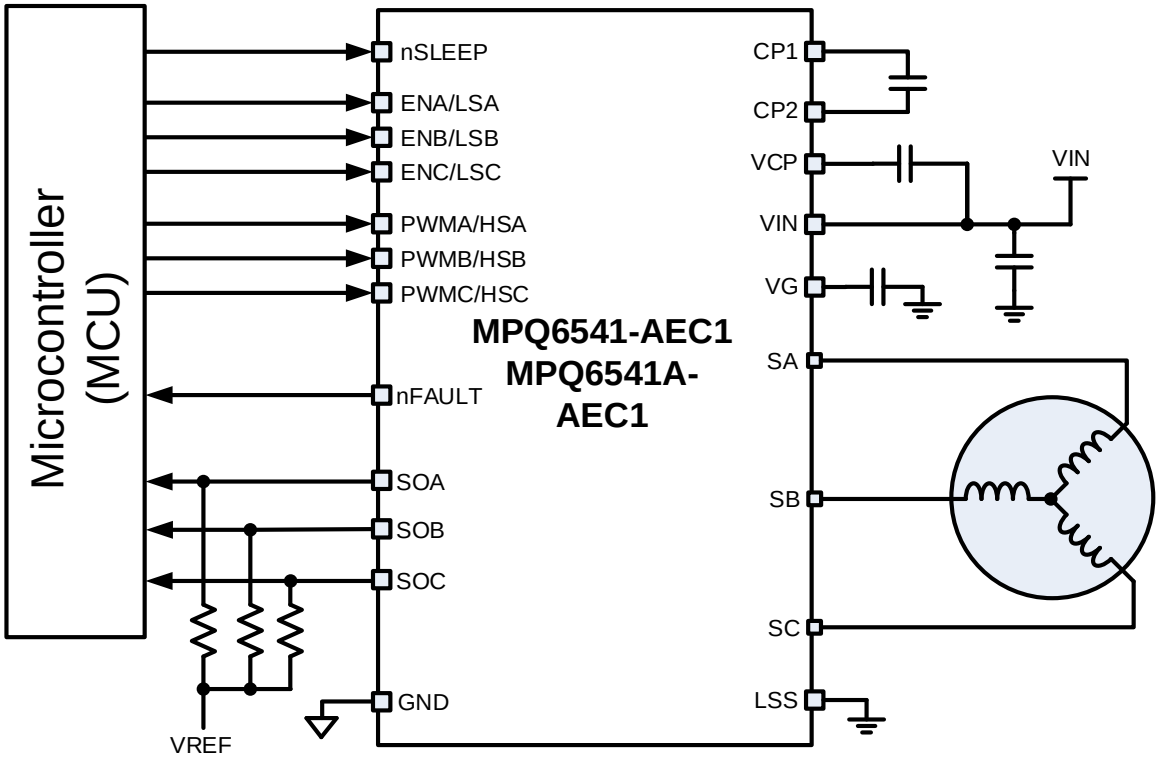
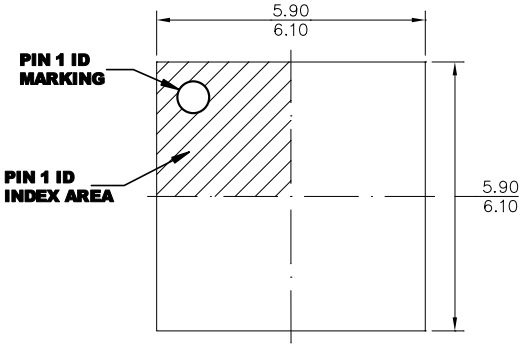


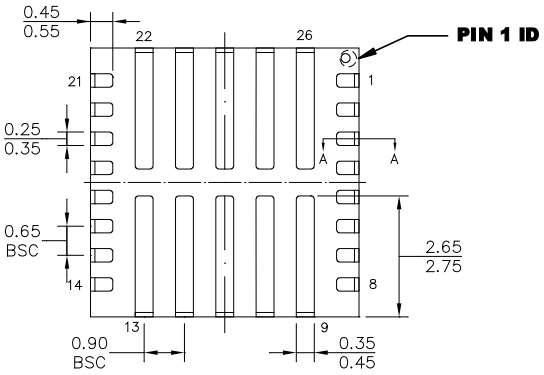
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

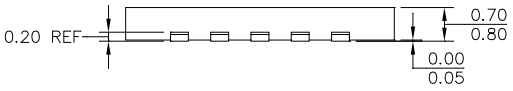
TQFN-26 (6mmx6mm)
Wettable Flank



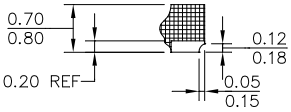
TOP VIEW



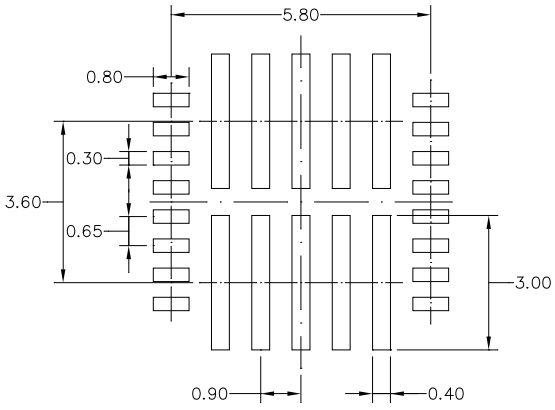
BOTTOM VIEW



SIDE VIEW



SECTION A-A

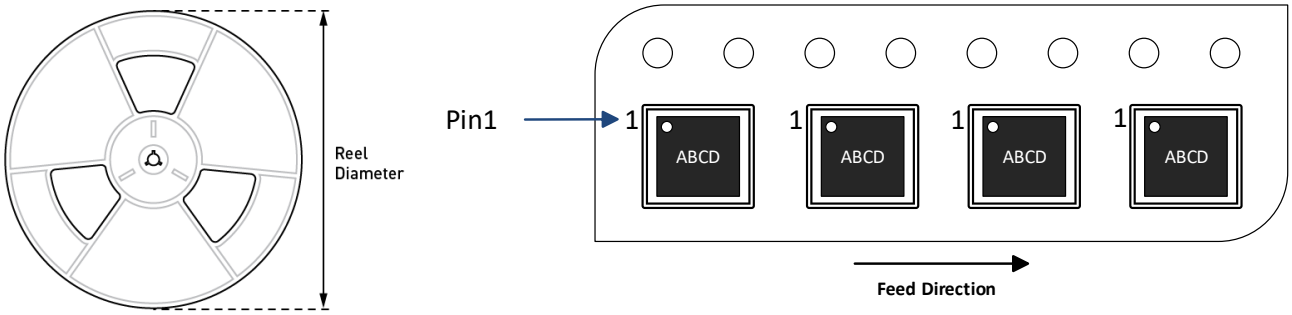


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6541GQKTE-AEC1-Z	TQFN-26 (6mmx6mm)	5000	N/A	13in	12mm	8mm
MPQ6541AGQKTE-AEC1-Z						

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/18/2021	Initial Release	-
1.1	2/24/2023	Added “-AEC1” suffix to part number	All
1.11	5/23/2023	Updated the Typical Application image	2