MP6653A

35V, 1.2A, Single-Phase BLDC Motor Driver with Integrated Hall Sensor and MOSFETs

DESCRIPTION

The MP6653A is a single-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs and an embedded Hall sensor. It can achieve up to 1.2A of peak coil current across a wide 3.5V to 35V input voltage (V_{IN}) range.

The pulse-width-modulation (PWM) signal or the DC voltage (V_{DC}) applied on the PWM pin controls the motor speed. The device also features soft commutation, a configurable Hall offset angle, and a configurable speed curve.

The FG/RD pin is an open-drain output that can be configured for speed detection (FG) or locked rotor detection (RD). It can detect the speed based on the embedded Hall-effect sensor's output, and a locked rotor if locked-rotor protection is triggered.

Rich protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

The MP6653A is available in a TSOT23-6-SL, TSOT23-6-L, or wettable-flank TQFN-6 (2mmx3mm) package.

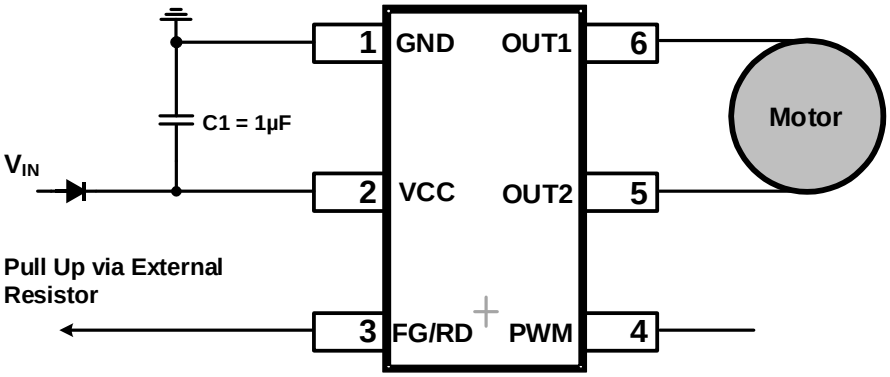
FEATURES

- Wide 3.5V to 35V Operating Input Voltage (V_{IN}) Range
- On-Chip Hall Sensor
- Integrated Power MOSFETs: Total 960mΩ for the High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)
- Selectable Open-Loop or Closed-Loop Speed Control
- Configurable Speed Curve
- Configurable Start and Stop Duty Cycle
- Soft-On and Soft-Off Commutation
- Configurable Soft Acceleration Time
- Configurable Hall Leading/Lag Angle
- 50Hz to 100kHz Pulse-Width Modulation (PWM) Input Frequency or DC Input
- Automatic Reverse Current Block
- 24kHz PWM Output Frequency
- Configurable Current Limit
- Short-Circuit Protection (SCP)
- Over-Voltage Protection (OVP)
- Standby Mode
- Selectable FG or RD Output
- Available in TSOT23-6-SL, TSOT23-6-L, and TQFN-6 (2mmx3mm) WF Packages

APPLICATIONS

- Fans
- Cooling Fans
- General BLDC Motors

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6653AGJS-xxxx**	TSOT23-6-SL	*See Below*	1
MP6653AGJL-xxxx**	TSOT23-6-L		
MP6653AGDTE-xxxx	TQFN-6 (2mmx3mm) with Wettable Flanks		

* For Tape & Reel, add suffix -Z (e.g. MP6653AGJS-xxxx-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” default code.

TOP MARKING (MP6653AGJS)

CEGY

LLL

CEG: Product code of MP6653AGJS
Y: Year code
LLL: Lot number

TOP MARKING (MP6653AGJL)

| CEGY

CEG: Product code of MP6653AGJL
Y: Year code

TOP MARKING (MP6653AGDTE)

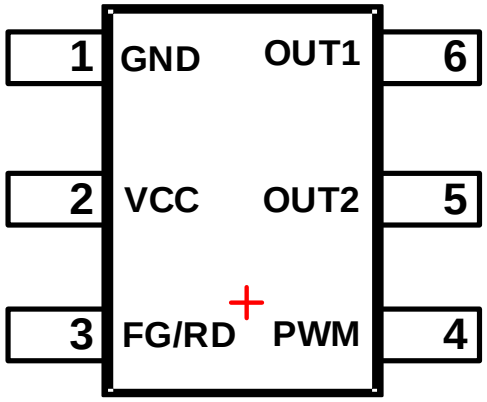
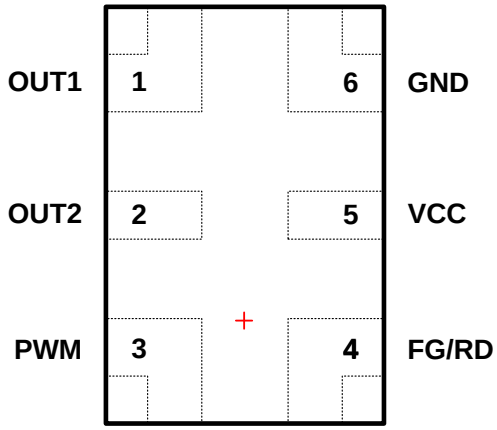
CEG

YWW

LLLL

CEG: Product code of MP6653AGDTE
Y: Year code
WW: Week code
LLLL: Lot number

PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
TSOT23-6-SL, TSOT23-6-L	TQFN-6 (2mmx3mm) with Wettable Flanks

PIN FUNCTIONS

TSOT-6 Pin #	TQFN-6 Pin #	Name	Description
1	6	GND	**Ground.**
2	5	VCC	**Input supply power.** The VCC pin must be bypassed locally.
3	4	FG/RD	**Speed (FG) or rotor-lock (RD) indication.** The FG/RD pin is an open-drain output that is pulled up externally.
4	3	PWM	**Speed control input pin.** The PWM pin supports a 50Hz to 100kHz PWM input frequency or a 0V to 3V DC input. This pin is pulled high internally via a 100kΩ resistor.
5	2	OUT2	**Motor driver output 2.** The OUT2 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.
6	1	OUT1	**Motor driver output 1.** The OUT1 pin is connected to the mid-point of the internal N-channel MOSFET half-bridge.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{CC}), PWM, FG/RD ..... -0.3V to +38V
OUT1, OUT2 ..... -0.3V to V_{CC} + 0.3V
Junction temperature (T_J) ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (2)
TSOT-6 ..... 1.25W
TQFN-6 (2mmx3mm) 1.78W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.5V to 35V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 100 ..... 55... °C/W
TQFN-6 (2mmx3mm) ..... 65 ..... 10... °C/W

Notes:

1) Absolute maximum ratings are rated under room temperature, unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

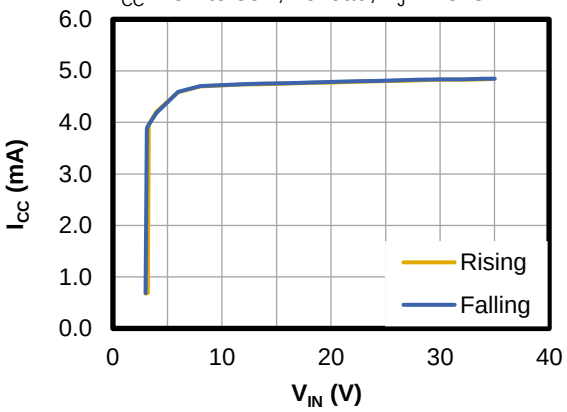
Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{CC} under-voltage lockout (UVLO) rising threshold	V_{CC_UVLO}			3.1	3.4	V
V_{CC} UVLO hysteresis	$V_{CC\_UVLO\_HYS}$			0.4		V
Operating supply current	I_{CC}	PWM = high		5	7	mA
Standby current	I_{STD}	PWM = low		120		µA
Pulse-width modulation (PWM) input high voltage	V_{PWM_H}		2.2			V
PWM input low voltage	V_{PWM_L}				0.8	V
DC input high voltage	V_{DC_H}		2.7	3	3.3	V
DC input low voltage	V_{DC_L}			130		mV
PWM internal pull-up resistance	R_{PWM}			100		kΩ
FG/RD output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA		0.3	0.43	V
Switching frequency	f_{SW}	T_J = 25°C	23.18	24	24.72	kHz
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 100mA		480		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 100mA		480		mΩ
Cycle-by-cycle current limit	I_{OCP}	OCP_SEL = 1		1.2		A
Peak current limit	I_{LIM}			1.8		A
Zero-current detection (ZCD) threshold	I_{ZCD}		-5		+5	mA
Soft-on commutation angle	θ_{SON}	SON[4:0] = 0x10		46.4		deg
Soft-off commutation angle	θ_{SOFF}	SOFF[4:0] = 0x10		46.4		deg
Hall lead/lag angle	θ_{HAL}	HAL_ANG[3:0] = 0xF		21.8		deg
Locked-rotor detection time	t_{RD}			0.6		sec
Locked-rotor retry time	t_{RE}	LOCK_SEL = 0		3.6		sec
Over-voltage protection (OVP) threshold	V_{OVP_H}	OVP_DIS = 0, OVP_H = 1	28	31	34	V
	V_{OVP_L}	OVP_DIS = 0, OVP_H = 0	17	19	21	V
OVP hysteresis	V_{OVP_HYS}			2	3	V
Operating point	B_{OP}			1	2	mT
Release point	B_{RP}		-2	-1		mT
Thermal shutdown threshold	T_{ST}			170		°C
Thermal shutdown hysteresis	T_{ST_HYS}			25		°C

TYPICAL CHARACTERISTICS

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

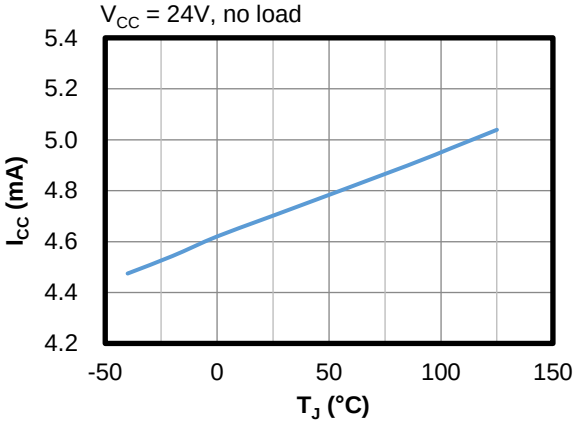
Supply Current vs. Input Voltage

V_{CC} = 3V to 35V, no load, T_J = 25°C

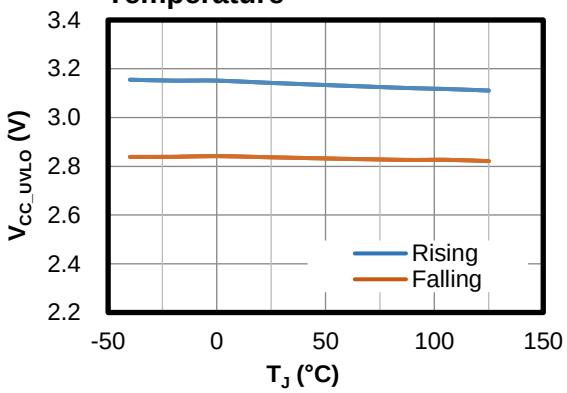


Supply Current vs. Junction Temperature

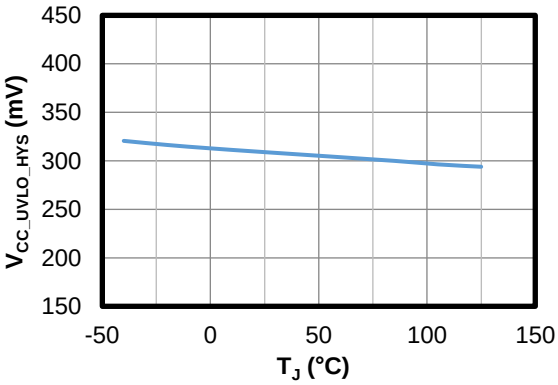
V_{CC} = 24V, no load



V_{CC} UVLO vs. Junction Temperature

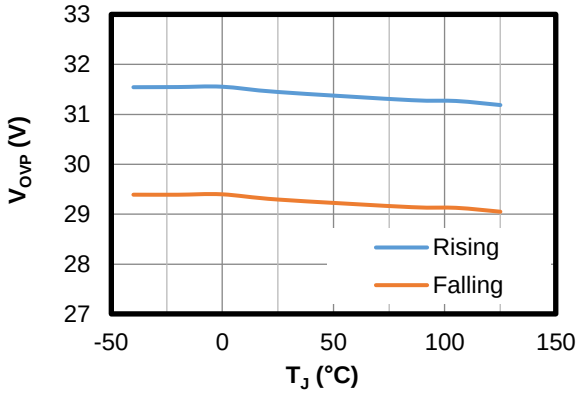


V_{CC} UVLO Hysteresis vs. Junction Temperature



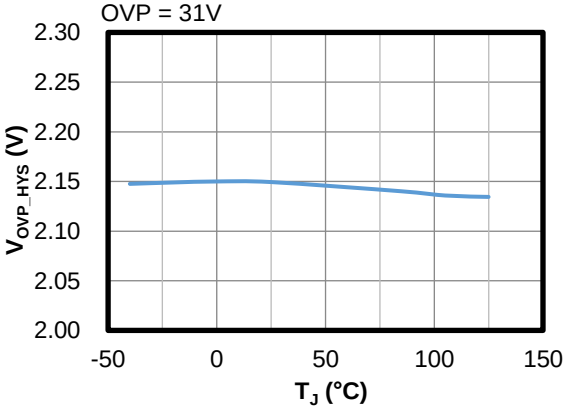
OVP Threshold vs. Junction Temperature

OVP = 31V



OVP Hysteresis vs. Junction Temperature

OVP = 31V

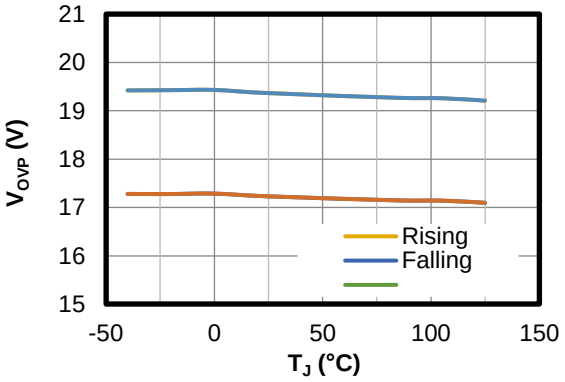


TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

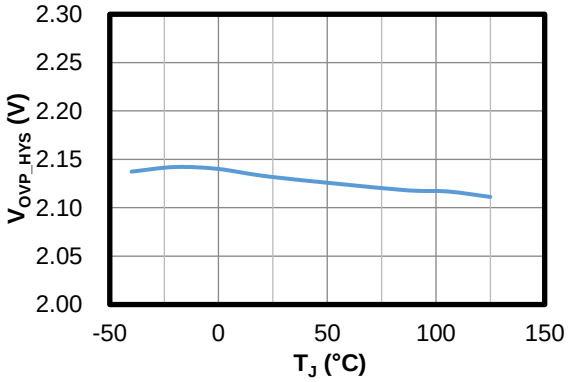
OVP Threshold vs. Junction Temperature

OVP = 19V



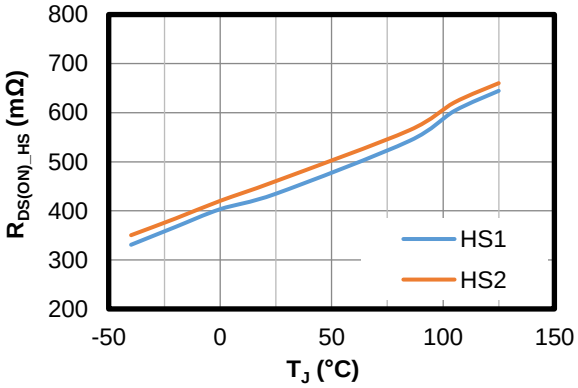
OVP Hysteresis vs. Junction Temperature

OVP = 19V



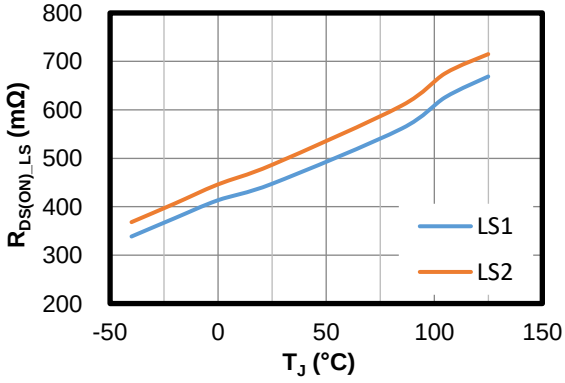
HS-FET On Resistance vs. Junction Temperature

V_{CC} = 24V



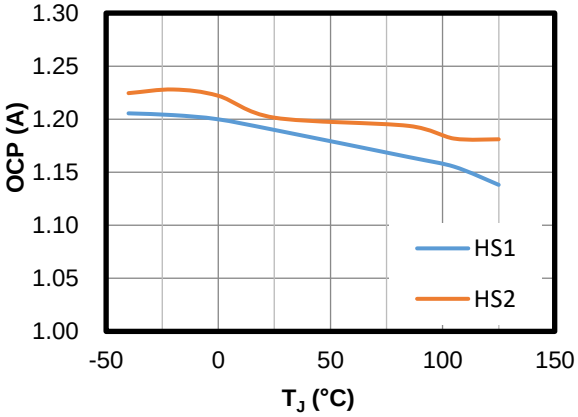
LS-FET On Resistance vs. Junction Temperature

V_{CC} = 24V



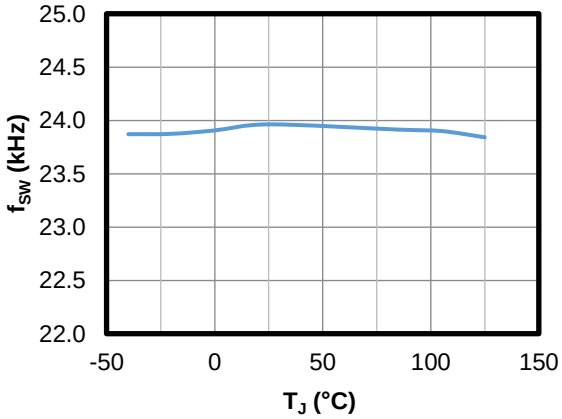
OCP vs. Junction Temperature

V_{CC} = 24V



Switching Frequency vs. Junction Temperature

V_{CC} = 24V

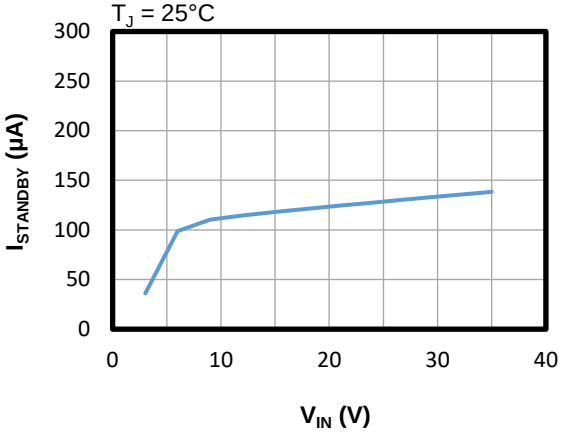


TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

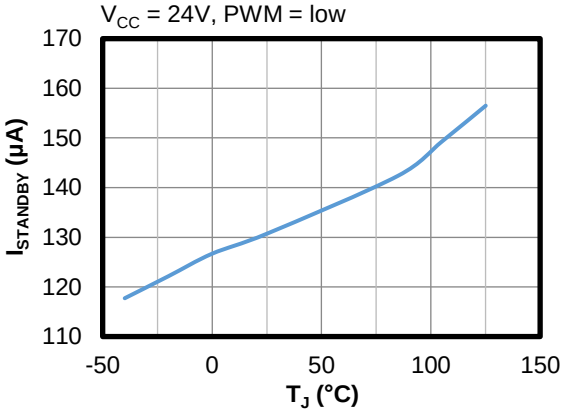
Standby Current vs. Input Voltage

V_{CC} = 3V to 35V, PWM = low, T_J = 25°C



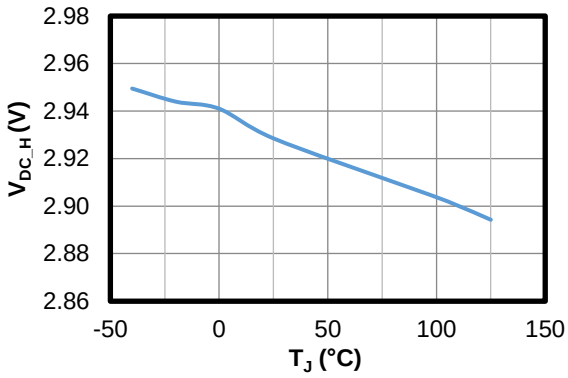
Standby Current vs. Junction Temperature

V_{CC} = 24V, PWM = low



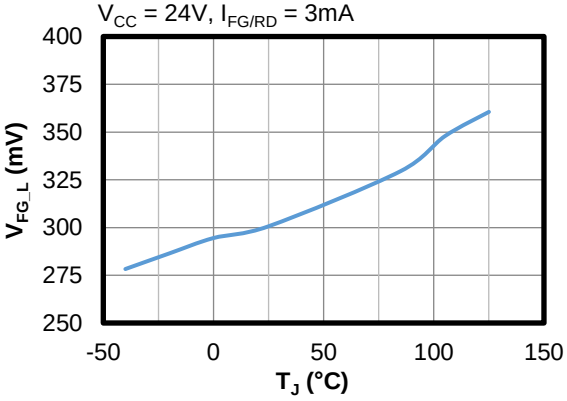
DC Input High Threshold vs. Junction Temperature

V_{CC} = 24V



FG/RD Low-Level Output vs. Junction Temperature

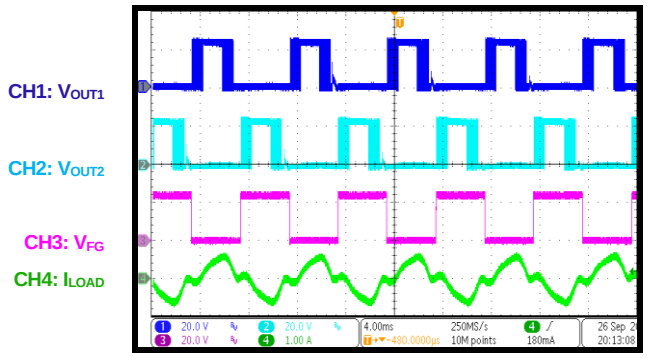
V_{CC} = 24V, $I_{FG/RD}$ = 3mA



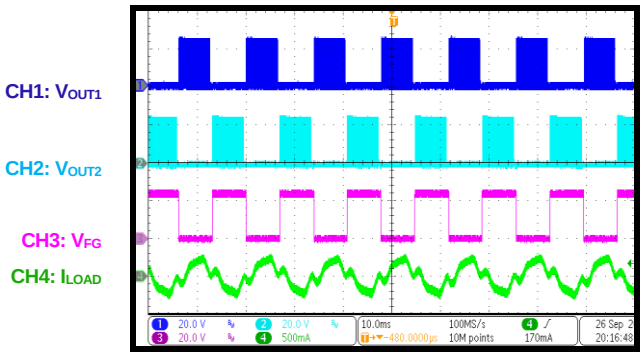
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, 8038 axial fan, 250mA, 4000rpm, T_A = 25°C, unless otherwise noted.

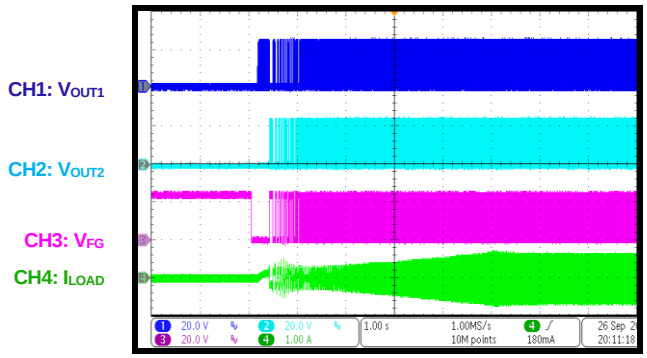
Steady State
PWM duty cycle = 100%



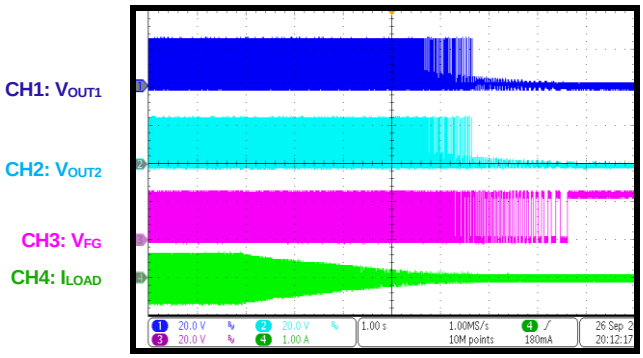
Steady State
PWM duty cycle = 50%



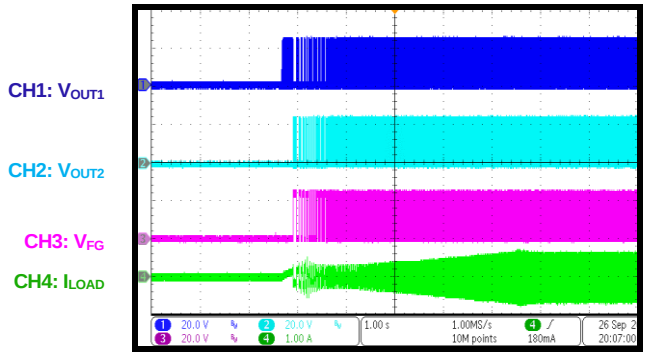
PWM On
PWM duty cycle = 0% to 100%



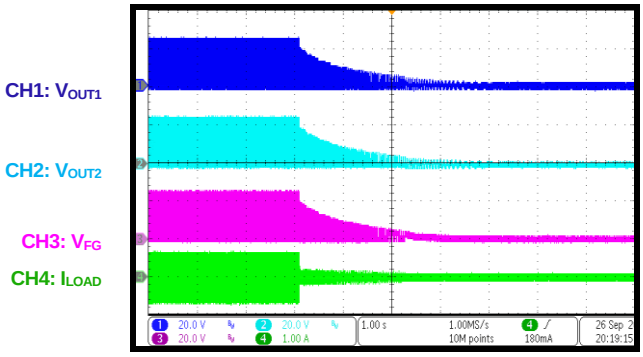
PWM Off
PWM duty cycle = 100% to 0%



Start-Up through VCC
VCC power plugged in



Shutdown through VCC
VCC power is not plugged in

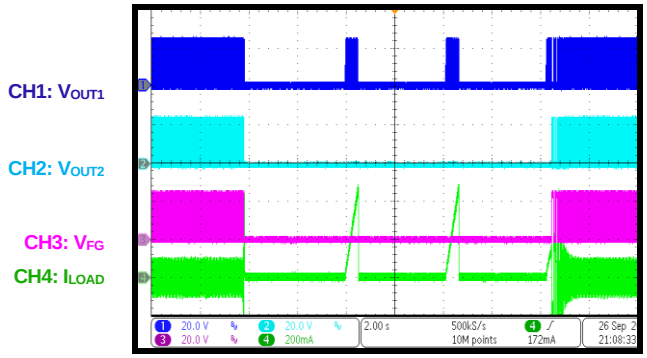


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, 8038 axial fan, 250mA, 4000rpm, T_A = 25°C, unless otherwise noted.

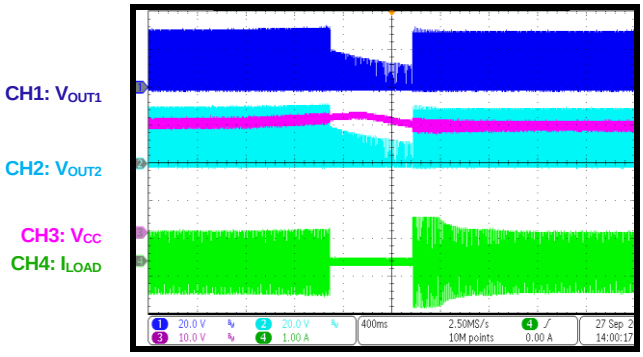
Locked-Rotor Protection

PWM duty cycle = 50%, locked rotor



Over-Voltage Protection

VCC ramps up then down,
OVP threshold = 31V



FUNCTIONAL BLOCK DIAGRAM

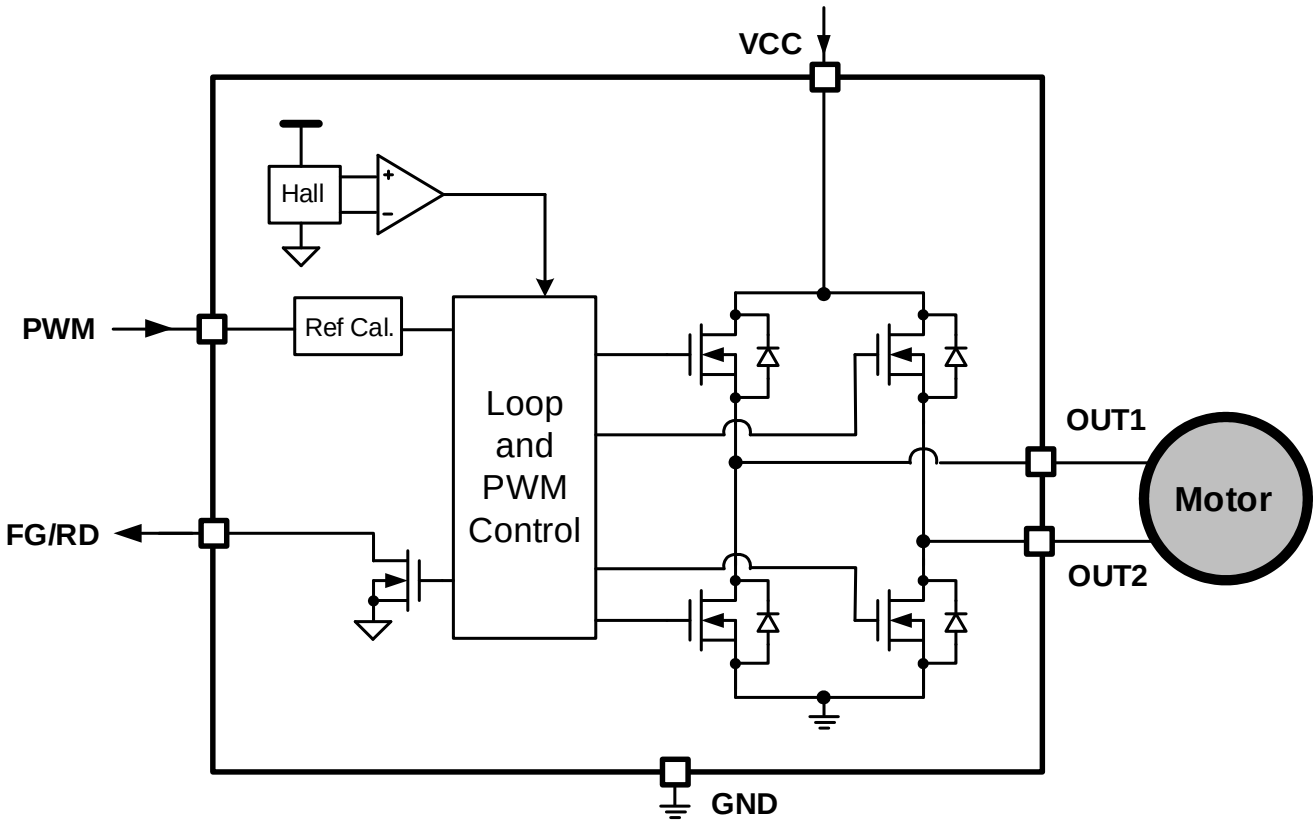


Figure 1: Functional Block Diagram

OPERATION

The MP6653A is a single-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor. The MP6653A controls the motor speed via the pulse-width modulation (PWM) signal or the DC voltage (V_{DC}) on the PWM pin, with closed-loop and open-loop speed control. It features configurable soft-on and soft-off commutation. The Hall-effect offset angle is configurable to optimize performance.
The MP6653A also features a rotational speed (RD) detector. The rotational speed detector is an open-drain output via the FG/RD pin. It outputs a high or low voltage relative to the internal Hall comparator's output.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown.

Speed Control

The PWM pin controls the rotating speed that is selected by the internal register bit via the PWM signal or V_{DC}.

In PWM input mode, the device detects the input PWM duty cycle, and the input PWM duty cycle controls the rotating speed.

In DC input mode, V_{DC} gets converted to a PWM duty cycle to control the rotating speed. There may be an overall up- or down-to-bottom shift in DC input accuracy.

The PWM signal is typically selected by default. The wide 50Hz to 100kHz PWM frequency range can be set via the registers.

If LOW_F = 0, the PWM frequency range is 1kHz to 100kHz and the PWM signal resolution is 163ns. If LOW_F = 1, the PWM frequency range is 50Hz to 2kHz and the PWM signal resolution is 2.6µs.

The MP6653A employs either closed-loop or open-loop speed control, and is configured via the registers.

In open-loop speed control, the OUT1 and OUT2 output duty cycles are adjusted based on the input PWM duty cycle or input V_{DC} on the PWM pin.

In closed-loop speed control, the input PWM duty cycle or input V_{DC} is detected, then gets converts to a reference speed. The motor speed provides feedback to the control loop, and the control loop adjusts the output duty cycle to match the rotating speed with the reference speed.

Starting Duty Cycle

The D0[6:0] bits set the starting duty cycle. When the input duty cycle is below the starting duty cycle, two modes are available depending on register CFR_5 (0Ch), bit[2]:

1. If SPD_ZERO = 0, OUT1 and OUT2 maintain the minimum output duty cycle or the fan maintains the minimum speed set via the S0[7:0] bits.
2. If SPD_ZERO = 1, the MP6653A stops switching and the fan stops.

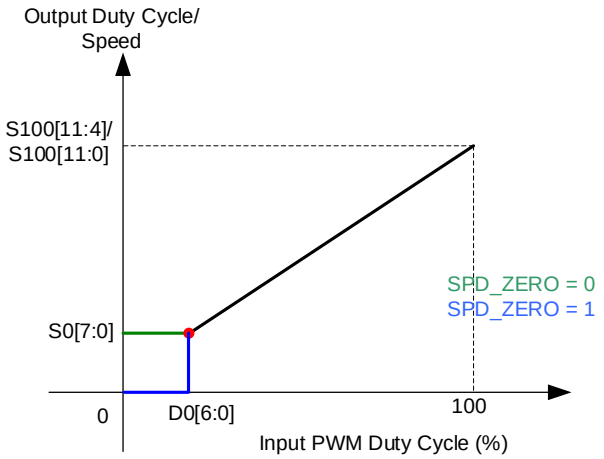


Figure 2: Minimum Speed with SPD_ZERO Setting

Stop Duty Cycle

The MP6653A supports a stop duty cycle. Figure 3 on page 13 shows the stop duty cycle when the input PWM duty cycle is above the stop duty cycle.

The stop duty cycle can be configured via register bits DSTOP[1:0], FIX_DSTOP_S100 (0Eh), bits[5:4]:

- If DSTOP[1:0] = 00, no stops
- If DSTOP[1:0] = 01, the stop duty cycle is 100%

- If DSTOP[1:0] = 10, the stop duty cycle is 95%
- If DSTOP[1:0] = 11, the stop duty cycle is 90%

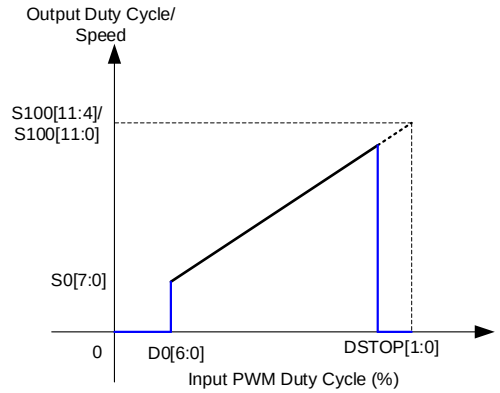


Figure 3: Stop Duty Cycle

OUT1 and OUT2 Normal Operation

In steady-state operation, the MP6653A controls the H-bridge MOSFETs' switching based on the internal Hall sensor's output to reduce speed variation and increase system efficiency. Figure 4 shows the operation with the Hall offset angle.

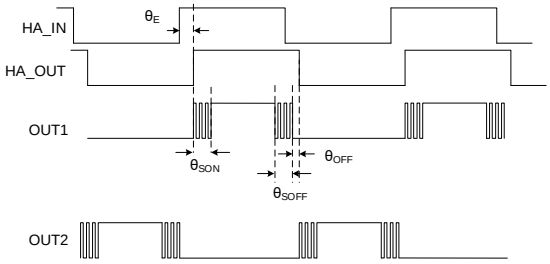


Figure 4: Operation with Hall Offset Angle

Where θ_E is the shifted phase and θ_{SON} is the soft-on and θ_{SOFF} is the soft-off commutation.

The operation sequence is based on the Hall-effect signal coming from the embedded Hall-effect sensor (HA_IN). HA_IN generates a signal with a shifted phase (HA_OUT), and the shifted phase can be configured via the HAL_ANG[3:0] bits.

When the HA_OUT signal is high, OUT2 remains low while OUT1 switches phases. When the HA_OUT signal is low, OUT1 remains low while OUT2 switches phases.

- HAL_ANG[3:0] bits set the Hall offset angle
- HAL_FLAG bits set the Hall offset angle leading/lag direction
- When HAL_ANG[3:0] = 0000, the Hall offset angle is 0

Soft-On Commutation

During soft-on commutation, the switching phase's output duty cycle gradually increases from 0 to the target duty cycle, and the other phase keeps the low-side MOSFETs (LS-FETs) on.

The soft-on commutation angle can be set between 0° and 90° via the SON[4:0] bits.

The high soft-on commutation angle lowers the rotating speed under the same condition.

Soft-Off Commutation

During soft-off commutation, the switching phase's output duty cycle gradually decreases from the target duty cycle to 0, and the other phase keeps the LS-FETs on.

The soft-off commutation angle can be set between 0° and 90° via the SOFF[4:0] bits.

The larger soft-off commutation angle helps eliminate the reverse current and lowers the rotating speed under the same condition.

Soft-On and Soft-Off Commutation Angle Linear Interpolation

The soft-on and soft-off commutation angle can linearly change when the output varies. When the output duty cycle is 100%, the soft-on and soft-off commutation angles can be set via the SON[4:0] and SOFF[4:0] bits, respectively. Figure 5 shows the commutation angle linearly increasing to 90° when the output duty cycle decreases to 0.

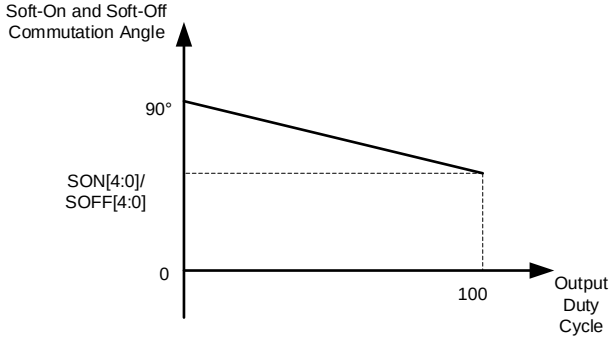


Figure 5: Soft-On and Soft-Off Commutation Angle Linear Interpolation

Configurable Speed Curve

The MP6653A employs a configurable speed curve for the input and output duty cycles.

Figure 6 shows four different, available configurable points, including the starting duty cycle set by the D0[6:0] bits, and the input duty cycle at 100%.

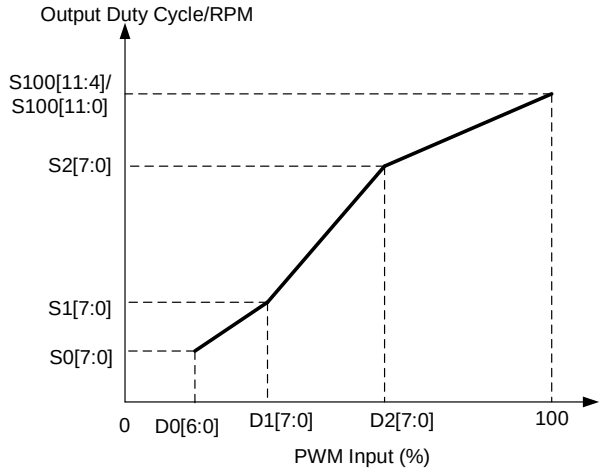


Figure 6: Configuring Speed Curve

D0[6:0] sets the starting duty cycle, and the starting duty cycle = D0[6:0] / 256.

The input duty cycle is set by Dx[7:0] (x = 1, 2), and the input duty cycle = Dx / 256.

In open-loop speed control, Sx[7:0] (x = 0, 1, 2) sets the corresponding output duty cycle, and the output duty cycle = Sx[7:0] / 256.

S100[11:4] sets the output duty cycle at input duty cycle at 100%, and the output duty cycle = S100[11:4] / 256.

In closed-loop speed control, S100[11:0] sets the maximum speed when the input duty cycle is 100%. The electrical speeds are set by the following:

- Speed (rpm) = S100[11:0] x 16

Other electrical speeds are set by Sx[7:0] (x = 0, 1, 2).

Speed (rpm) = S100[11:0] x Sx[7:0] / 256 x 16

Standby Mode

The device employs standby mode when the supply voltage (V_{CC}) exceeds the UVLO rising threshold and the PWM pin is pulled low. The device exits standby mode once the PWM input signal is high or the power is cycled.

Pre-Startup

When the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold and the input PWM duty cycle exceeds the starting duty cycle set via the D0[6:0] bits. the MP6653A enters pre-startup. The output duty cycle increases with a setting slope by ignoring the final steady state output duty cycle. After several Hall cycles, the MP6653A exits pre-startup, then initiates a soft start (SS).

With different pre-startup timer configurations, the MP6653A provides enough torque to power the motor.

Soft Start (SS)

SS initiates after pre-startup. The output duty cycle ramps up and down step by step via the TIME_SS[1:0] bits.

To reduce the input inrush current during start-up, several configurations are available to meet different applications.

The duty cycle drop can be configured as 1x or 2x via the DN_SCALE bit.

Rotor Speed Indicator (FG) or Rotor Dead Lock Indicator (RD)

The FG/RD pin can be configured for speed indication (FG) or locked-rotor detection (RD) via the FGRD[2:0] bits.

- If FGRD[2:0] = 000, FG/RD is 1x the original Hall frequency and outputs 1 pulse in every electrical cycle.
- If FGRD[2:0] = 001, the FG/RD pin is 0.5x the original Hall frequency and outputs 1 pulse in every 2 electrical cycles.
- If FGRD[2:0] = 010, the FG/RD pin is 2x the original Hall frequency and outputs 2 pulses in every electrical cycle.
- If FGRD[2:0] = 011, the FG/RD pin outputs 1 pulse in every electrical cycle during normal operation, and outputs an RD signal for locked-rotor protection. RD_H_L bits set the RD signal output polarity.
- If FGRD[2:0] = 100, the FG/RD pin is set for locked-rotor detection, and the RD_H_L bits set the RD signal output polarity.

- If FGRD[2:0] = 101, the FG/RD pin is set as the fault indicator and outputs a signal if a fault is detected.
- If FGRD[2:0] = 110, the FG/RD pin is set as the external Hall signal input. The external Hall sensor replaces the internal Hall sensor for operation.

Protection Circuits

The MP6653A features rich protection features, including over-voltage protection (OVP), under-voltage lockout (UVLO), over-current protection (OCP), and thermal shutdown (TSD).

Over-Current Protection (OCP)

During normal switching, if the current flowing through the H-bridge HS-FET exceeds the threshold set via the OCP_SEL bit after a blanking time, the HS-FET turns off and resumes switching in the next switching cycle. The OCP threshold can be set to 0.6A or 1.2A via OCP_SEL bit.

Short-Circuit Protection (SCP)

If the current is not limited via cycle-by-cycle limiting, there is also a peak current limit. This is also called short-circuit protection (SCP). If the current reaches the peak current limit threshold (typically 1.8A), all MOSFETs turn off. The device restarts and resumes normal operation after a lock-retry time set via the LOCK_SEL bit.

Thermal Shutdown (TSD)

The MP6653A integrates thermal monitoring. If the die temperature exceeds 170°C, the switching MOSFETs' half-bridges turn off. Once the die temperature drops to the thermal shutdown (TSD) falling threshold, the device restarts and resumes normal operation.

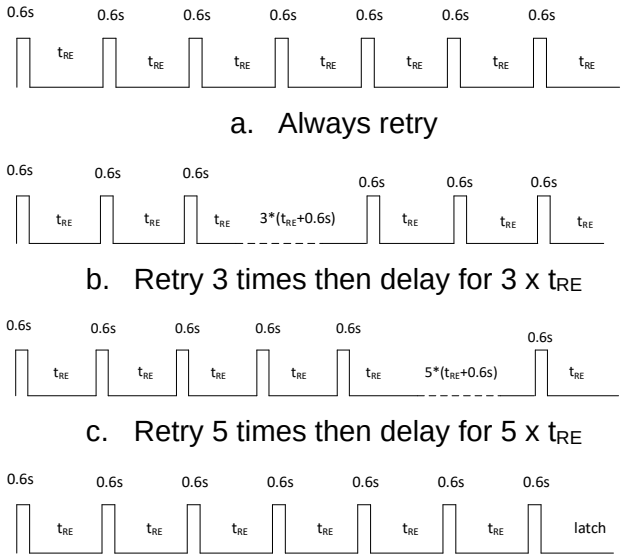
Under-Voltage Lockout (UVLO)

If V_{CC} falls below the UVLO falling threshold, all circuitry in the device is disabled and internal logic resets. Once V_{CC} exceeds the UVLO rising threshold, the device restarts and resumes normal operation.

Locked-Rotor Protection (RD)

The internal Hall signal detects whether locked-rotor protection (RD) is triggered. If the MP6653A cannot detect a Hall signal edge during the detection time (typically 0.6s), then RD triggers and both the LS-FETs' H-bridges turn on. The IC automatically attempts to restart after a lock-retry time (typically 3.6s or 8.4s) set via the LOCK_SEL bit.

The MP6653A supports several retry times; the lock-retry time can be set to be longer via register configuration (see Figure 7).



a. Always retry

b. Retry 3 times then delay for 3 x t_{RE}

c. Retry 5 times then delay for 5 x t_{RE}

d. Retry 7 times then latch

Figure 7: Locked-Rotor Protection and Retry Times

The FG/RD pin only releases after RD releases and 3 Hall signal edges are detected.

Over-Voltage Protection (OVP)

The MP6653A employs two over-voltage (OV) thresholds for different applications.

If V_{CC} exceeds its OV threshold (typically 19V/31V), then the OUT1/2 output is disabled. Once V_{CC} falls below the OVP falling threshold (typically 17V/28V) and a Hall edge is detected during the OVP interval, the device restarts and resumes normal operation.

Fault Diagnosis

The OCP, SCP, TSD, OVP, and RD protections have relative fault bits to indicate the fault. The fault bit(s) can be reset after being read.

Test Mode and Factory Mode

The MP6653A supports test mode to configure the internal registers. All internal registers can be read and written in test mode. After finalizing the design, the non-volatile memory (NVM) configures the register values.

REGISTER MAP

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	S0[7:0]							
01h (OTP/REG)	S1[7:0]							
02h (OTP/REG)	S2[7:0]							
03h (OTP/REG)	S100[11:4]							
04h (OTP/REG)	D1[7:0]							
05h (OTP/REG)	D2[7:0]							
06h (OTP/REG)	RD_H_L	D0[6:0]						
07h (OTP/REG)	OVP_H	FAST_DN	PWM_POL	SON[4:0]				
08h (OTP/REG)	SINE	SPD_SEL[1:0]		SOFF[4:0]				
09h (OTP/REG)	WAIT_DIS	T_PRE[1:0]		HAL_FLAG	HAL_ANG[3:0]			
0Ah (OTP/REG)	RESERVED	INT_EN	RESERVED	LOCK_SEL	OCP_SEL	ASYNC	PWM_WAIT	TADV_EN
0Bh (OTP/REG)	OVP_DIS	TADV[1:0]		TIME_SS[1:0]		FGRD[2:0]		
0Ch (OTP/REG)	PWM_DC	CLOSE	LOW_F	LOCK_BHV[1:0]		SPD_ZERO	COA_SLOW	DN_SCALE
0Dh (OTP/REG)	KI[6:0]							ZCD_POS
0Eh (OTP/REG)	FIX_ST[1:0]		DSTOP[1:0]		S100[3:0]			
14h (REG)	OCP	SCP	OVP	TSD	RD	RESERVED		
15h (REG)	RESERVED	LOCK_ DIS	RESERVED					
16h (REG)	RESERVED	OTP_PAGE[1:0]	RESERVED					

SPEED_CURVE_1 (00h)

The SPEED_CURVE_1 command configures the output duty cycle or speed when the input pulse-width modulation (PWM) duty cycle is set by D0[6:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S0[7:0]	0x20	Sets the output duty cycle or speed when the input PWM duty cycle is set by D0[6:0]. In open-loop control, sets the output duty cycle when the input PWM duty cycle is set by D0[6:0]. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S0[7:0] / 256 In closed-loop control, sets the speed reference when the input PWM duty cycle is set by D0[6:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S0[7:0] / 256 x S100[11:0] x 16

SPEED_CURVE_2 (01h)

The SPEED_CURVE_2 command configures the output duty cycle or speed when the input PWM duty cycle is set by D1[7:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S1[7:0]	0x60	Sets the output duty cycle or speed when the input PWM duty cycle is set by D1[7:0]. In open-loop control, sets the output duty cycle when the input PWM duty cycle is set by D1[7:0]. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S1[7:0] / 256 In closed-loop control, sets the speed reference when the input PWM duty cycle is set by D1[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S1[7:0] / 256 x S100[11:0] x 16

SPEED_CURVE_3 (02h)

The SPEED_CURVE_3 command configures the output duty cycle or speed when the input PWM duty cycle is set by D2[7:0].

Bits	Access	Bit Name	Default	Description
7:0	R/W	S2[7:0]	0xC0	Sets the output duty cycle or speed when the input PWM duty cycle is set by D2[7:0]. In open-loop control, sets the output duty cycle when the input PWM duty cycle is set by D2[7:0]. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S2[7:0] / 256 In closed-loop control, sets the speed reference when the input PWM duty cycle is set by D2[7:0]. The electrical speed can be calculated with the following equation: Speed (rpm) = S2[7:0] / 256 x S100[11:0] x 16

SPEED_CURVE_4 (03h)

The SPEED_CURVE_4 command configures the output duty cycle or speed when the input PWM duty cycle is 100%.

Bits	Access	Bit Name	Default	Description
7:0	R/W	S100[11:4]	0xFF	Sets the output duty cycle or the 8 most significant bits (MSB) for the speed when the input PWM duty cycle is 100%. Open-loop control sets the output duty cycle when the input PWM duty cycle is 100%. The output duty cycle can be calculated with the following equation: Output Duty Cycle = S100[11:4] / 256 Closed-loop control sets the maximum speed reference when the input PWM duty cycle is 100%. Combined with S100[3:0], the maximum electrical speed can be calculated with the following equation: Max Speed (rpm) = S100[11:0] x 16

SPEED_CURVE_5 (04h)

The SPEED_CURVE_5 command configures the input duty cycle 1 (D1).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D1[7:0]	0x60	Sets the input duty cycle for curve configuration. The input PWM duty cycle can be calculated with the following equation: Input PWM Duty Cycle = D1[7:0] / 256

SPEED_CURVE_6 (05h)

The SPEED_CURVE_6 command configures the input duty cycle 2 (D2).

Bits	Access	Bit Name	Default	Description
7:0	R/W	D2[7:0]	0xC0	Sets the input duty cycle for curve configuration. The input PWM duty cycle can be calculated with the following equation: Input PWM Duty Cycle = D2[7:0] / 256

RD_D0 (06h)

The RD_D0 command sets the RD/FT output polarity and the starting corner duty cycle.

Bits	Access	Bit Name	Default	Description
7	R/W	RD_H_L	0	Selects RD/FT output polarity. 0: The output is low if a protection is triggered (default) 1: The output is high if a protection is triggered
6:0	R/W	D0[6:0]	0x20	Sets the starting corner duty cycle for curve configuration. The starting corner PWM duty cycle can be calculated with the following equation: Starting Duty Cycle = D0[6:0] / 256

CFR_1 (07h)

The CFR_1 command controls the function register 1, which sets the over-voltage protection (OVP) threshold, fast-off, input PWM polarity, and soft-on commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_H	1	Selects the OVP threshold. 0: 19V 1: 31V (default)
6	R/W	FAST_DN	0	Enables fast-off. 0: Disables fast-off (default) 1: Enables fast-off when PWM is off. The IC quickly stops switching if the input duty cycle drops below the starting duty cycle
5	R/W	PWM_POL	0	Selects the input PWM polarity. 0: Positive duty cycle (default) 1: Negative duty cycle
4:0	R/W	SON[4:0]	0x10	Sets the soft-on commutation angle. 00000: 2.9° 00001: 5.8° 11111: 90° The soft-on commutation angle can be calculated with the following equation: Soft-On Angle = (SON[4:0] + 1) x 2.9° 2.9° per step.

SOFF_CLK (08h)

The SOFF_CLK command configures the soft-on and soft-off mode, digital clock, and soft-off commutation angle.

Bits	Access	Bit Name	Default	Description
7	R/W	SINE	0	Selects soft-on and soft-off mode. 0: Linear (default) 1: Sine
6:5	R/W	SPD_SEL[1:0]	00	Selects the digital clock. A higher frequency can result in a higher calculation resolution. However, it also leads to a higher minimum speed. The bits below indicate the supported minimum electrical speeds: 00: 200rpm (default electrical speed) 01: 800rpm 10: 1600rpm 11: 3200rpm
4:0	R/W	SOFF[4:0]	0x10	Sets the soft-off commutation angle. 00000: 2.9° 00001: 5.8° 11111: 90° The soft-off commutation angle can be calculated with the following equation: Soft-off angle = (SOFF[4:0] + 1) x 2.9° 2.9° per step.

CFR_2 (09h)

The CFR_2 command controls function register 2, which sets the waiting function, pre-startup time, and Hall offset angle.

Bits	Access	Bit Name	Default	Description
7	R/W	WAIT_DIS	0	Disables the waiting function at start-up. 0: Enabled (default) 1: Disabled
6:5	R/W	T_PRE[1:0]	01	Selects the pre-startup time. 00: 21.33ms/step 01: 10.67ms/step (default) 10: 5.36ms/step 11: 2.73ms/step
4	R/W	HAL_FLAG	0	Sets the Hall offset angle lag/lead. 0: Lag (default) 1: Lead
3:0	R/W	HAL_ANG[3:0]	0000	Sets the Hall offset angle. 0000: 0° (default) 0001: 1.4° 1111: 21° The Hall offset angle can be calculated with the following equation: Hall Offset Angle = HAL_ANG[3:0] x 1.4° 1.4° per step.

CFR_3 (0Ah)

The CFR_3 command controls function register 3, which sets the soft-on and soft-off angle, lock-retry time, current limit, asynchronized rectification, waiting function, and advanced turn-off.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	INT_EN	0	Enables soft-on and soft-off commutation angle linear interpolation. 0: Disables the soft-on/soft-off commutation angle, which linearly increases to 90° when the duty cycle drops (default) 1: Enables the soft-on/soft-off commutation angle, which linearly increases to 90° when the duty cycle drops
5	R	RESERVED	1	Reserved.
4	R/W	LOCK_SEL	0	Sets the locked-rotor protection retry time. 0: 3.6s (default) 1: 8.4s
3	R/W	OCP_SEL	1	Sets the current limit threshold. 0: 0.6A 1: 1.2A (default)
2	R/W	ASYNC	0	Enables asynchronized rectification. 0: Disabled (default) 1: Enabled

1	R/W	PWM_WAIT	0	Enables the waiting function at PWM on start-up. 0: Disabled (default) 1: Enabled
0	R/W	TADV_EN	1	Enables advanced turn-off. 0: Disables advanced turn-off 1: Enables advanced turn-off (default)

CFR_4 (0Bh)

The CFR_4 command controls function register 4, which sets over-voltage protection (OVP), advanced soft-off angle, soft-start time (t_{SS}), and the FG/RD pin.

Bits	Access	Bit Name	Default	Description
7	R/W	OVP_DIS	0	Enables OVP. 0: Enables OVP (default) 1: Disables OVP
6:5	R/W	TADV[1:0]	00	Selects the advanced off angle. 00: Automatic (default) 01: 5.6° 10: 11.2° 11: 22.5°
4:3	R/W	TIME_SS[1:0]	01	Selects t_{SS}, the time during which the output duty cycle transitions from 0% to 100%. 00: 2.73s 01: 5.46s (default) 10: 8.19s 11: 10.92s
2:0	R/W	FGRD[2:0]	000	Selects the FG/RD pin function. 000: 1 x FG (default) 001: 0.5 x FG 010: 2 x FG 011: FG + RD where the FG signal is the output during normal operation, and the RD signal is the output if locked-rotor protection is detected 100: RD where the RD signal polarity is set via the RD_H_L bit 101: FT where the fault signal is the output if a fault is detected, and the FT polarity is set via the RD_H_L bit 110: HALL_IN where the FG/RD pin is set as the external Hall input pin

CFR_5 (0Ch)

The CFR_5 command controls function register 5, which sets the PWM/DC input, closed-loop and open-loop speed control, PWM frequency, deadlock protection mode, coasting down threshold, zero-speed, and output duty cycle ramping down scale.

Bits	Access	Bit Name	Default	Description
7	R/W	PWM_DC	0	Selects the DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
6	R/W	CLOSE	0	Enables closed-loop speed control. 0: Open-loop speed control (default) 1: Closed-loop speed control

5	R/W	LOW_F	0	Selects the low-frequency PWM input. 0: The high frequency is selected between 1kHz and 100kHz (default) 1: The low frequency is selected between 50Hz and 2kHz
4:3	R/W	LOCK_BHV[1:0]	00	Selects deadlock protection mode. 00: Always retry (default) 01: Retries for 3 times, then the lock-retry time is 3x 10: Retries for 5 times, then the lock-retry time is 5x 11: Retries for 7 times, then the device latches
2	R/W	SPD_ZERO	1	Enables zero speed. 0: Keeps minimum speed when the input duty cycle below the duty cycle set by D0[6:0] 1: Stops when the input duty cycle below the duty cycle set by D0[6:0] (default)
1	R/W	COA_SLOW	0	Selects the coasting down speed threshold (electrical speed). The IC remains coasting until the fan rotation's coasting down speed drops below the speed threshold during start-up. 0: 1400rpm (default) 1: 700rpm
0	R/W	DN_SCALE	0	Selects the PWM output duty cycle ramping down scale as the output duty cycle drops from 100% to 0%. 0: 1 x TIME_SS[1:0] (default) 1: 2 x TIME_SS[1:0]

KI_ZCD (0Dh)

The KI_ZCD command sets the integral parameter for closed-loop speed control and the zero-current detection (ZCD) active angle position.

Bits	Access	Bit Name	Default	Description
7:1	R/W	KI[6:0]	0x10	Sets the integral parameter for closed-loop speed control.
0	R/W	ZCD_POS	0	Sets the ZCD active angle position. 0: ZCD is active once soft-on commutation ends (default) 1: ZCD is active after 90°

FIX_DSTOP_S100 (0Eh)

The FIX_DSTOP_S100 command sets the initial output duty cycle, stop input duty cycle, and maximum speed reference.

Bits	Access	Bit Name	Default	Description
7:6	R/W	FIX_ST[1:0]	00	Selects the initial output duty cycle at start-up. 00: The initial output duty cycle is 0% (default) 01: The initial output duty cycle is 12.5% 10: The initial output duty cycle is 25% 11: The initial output duty cycle is 50%
5:4	R/W	DSTOP[1:0]	00	Selects the stop input duty cycle. When the input PWM duty cycle is equal to or exceeds the selected stop input duty cycle, the IC stops switching. 00: Does not stop (default) 01: 100% 10: 95% 11: 90%

3:0	R/W	S100[3:0]	0000	Sets the maximum speed reference when the input PWM duty cycle is 100% for closed-loop control. Combined with S100 [11:4], SPEED_CURVE_4 (03h), bits[7:0], the maximum electrical speed can be calculated with the following equation: Max speed (rpm) = S100[11:0] x 16

FAULT_BIT(14h)

The FAULT_BIT command indicates faults, including the cycle-by-cycle current limit (I_{OCP}), peak current limit (I_{LIMIT_PEAK}), input over-voltage (OV) conditions, thermal shutdown, and locked-rotor protection.

Bits	Access	Bit Name	Default	Description
7	R	OCP	0	Indicates an I_{OCP} fault. 0: I_{OCP} is not triggered 1: I_{OCP} is triggered
6	R	SCP	0	Indicates an I_{LIMIT_PEAK} fault. 0: I_{LIMIT_PEAK} is not triggered 1: I_{LIMIT_PEAK} is triggered
5	R	OVP	0	Indicates an input OV fault. 0: Input OVP is not triggered 1: Input OVP is triggered
4	R	TSD	0	Indicates a thermal shutdown fault. 0: Thermal shutdown protection is not triggered 1: Thermal shutdown protection is triggered
3	R	RD	0	Indicates a locked-rotor fault. 0: Rotor deadlock protection is not triggered 1: Rotor deadlock protection is triggered
2:0	R	RESERVED	000	Reserved.

LOCK_DIS (15h)

The LOCK_DIS command enables locked-rotor protection.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6	R/W	LOCK_DIS	0	Enables locked-rotor protection. 0: Enables locked-rotor protection 1: Disables locked-rotor protection
5:0	R	RESERVED	0x00	Reserved.

OTP_PAGE (16h)

The OTP_PAGE command sets the one-time programmable (OTP) memory page indicator.

Bits	Access	Bit Name	Default	Description
7	R	RESERVED	0	Reserved.
6:5	R	OTP_PAGE[1:0]	00	Sets the OTP page indicator. 00: No OTP page is configured 01: First OTP page is configured 10: Second OTP page is configured
4:0	R	RESERVED	0x00	Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{IN}) and reduce noise at the input. C_{IN} must have a low impedance at the switching frequency (f_{SW}).

Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics. The ceramic capacitance is dependent on the V_{DC} rating. If the ceramic capacitor is biased to its V_{DC} rating, then its capacitance drops below 50%.

Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient. In some applications, an additional, large electrolytic capacitor may be required to absorb the motor's energy.

Selecting the Input Snubber

Due to the C_{IN} energy charge and discharge during phase commutation, I_{IN} has switching cycle ringing. If necessary, place an RC snubber and a 2Ω resistor in series with a 1µF capacitor in parallel with C_{IN}. This effectively prevents switching cycle ringing.

Hall Position

Figure 8 shows the embedded Hall sensor cell location.

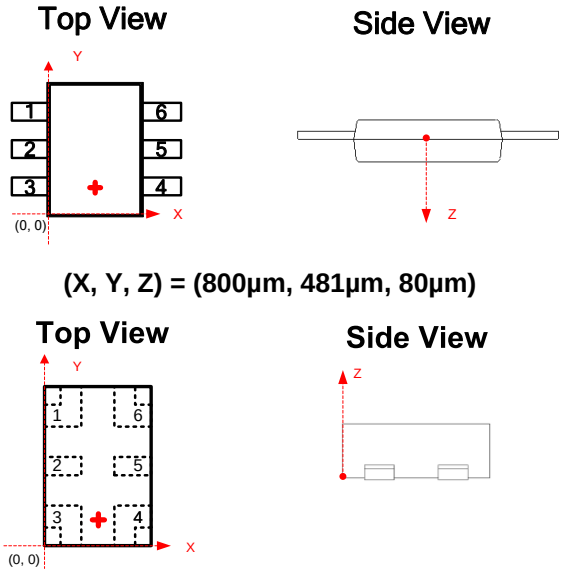


Figure 8: Hall Sensor Position

Selecting an Input Clamping Circuit

A voltage-clamping circuit may be required to prevent V_{IN} from being charged by the energy store in the motor. A 15V SOD-123 Zener diode or TVS diode is typically sufficient for most 12V applications and a 28V SOD-123 Zener diode or TVS diode is typically sufficient for most 24V applications. Use a higher clamping voltage if a higher V_{IN} range is applied.

Selecting the Reverse Blocking Diode

If the fan experiences a reverse plug-in or reverse voltage applied on the input terminal, a reverse blocking diode is required to avoid damage. The reverse blocking diode prevents the bus voltage from charging via the fan's reverse current.

The blocking diode's reverse voltage rating must be greater than the maximum operating voltage under all conditions.

System-Level ESD

Some fan products must pass system-level ESD testing. System-level ESD follows the IEC 61000-4-2 standards. There are differences between human body mode (HBM) ESD and system-level ESD (IEC 61000-4-2). Figure 9 shows the equivalent HBM ESD circuit.

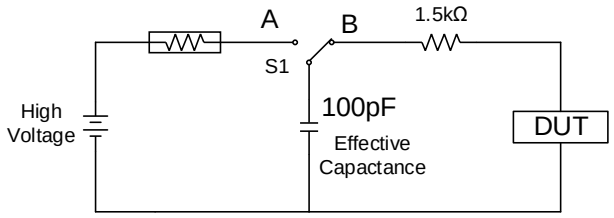


Figure 9: HBM ESD Equivalent Circuit

Figure 10 shows the equivalent system-level ESD circuit.

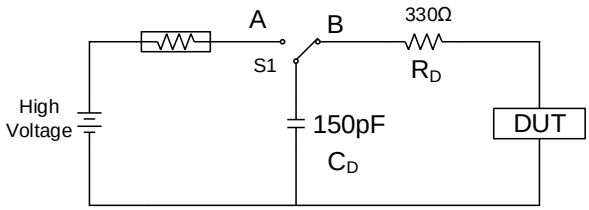


Figure 10: System-Level ESD Equivalent Circuit

Compared to the HBM ESD, the discharge capacitance in the system-level ESD exceeds the HBM's effective capacitance, and the

system-level ESD discharge resistance is much smaller. Hence, the system-level ESD discharging energy is much greater than the HBM ESD.

If a high level system-level ESD is required, an external circuit may be required to enhance ESD capability.

Figure 11 shows an external ESD-enhanced circuit using a Zener/ESD diode.

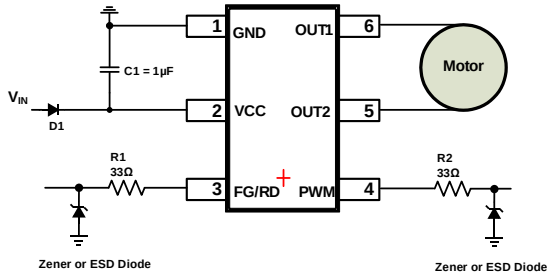


Figure 11: Enhanced ESD using Zener Diode or ESD Diode

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and follow the guidelines below:

1. To improve EMI performance, a 0402 capacitor is required (C2). Place the capacitor as close to the VCC and GND pins as possible.
2. Place the input capacitor (C1) close to the VCC and GND pins.

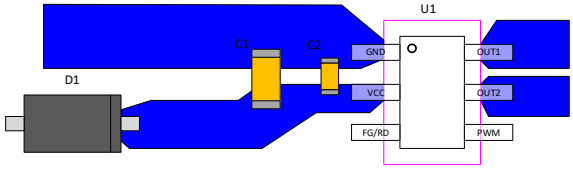


Figure 12: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

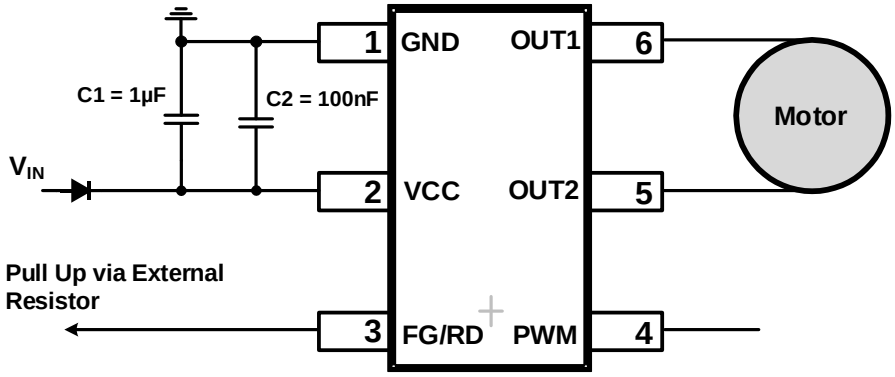


Figure 14: Typical Application Circuit

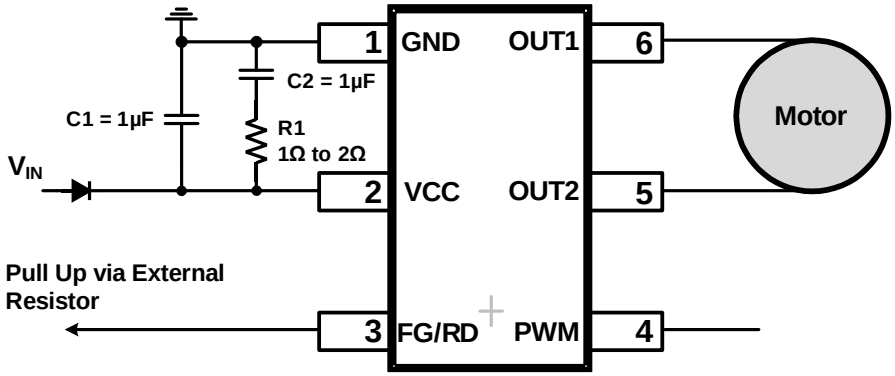


Figure 15: Typical Application Circuit with RC Snubber

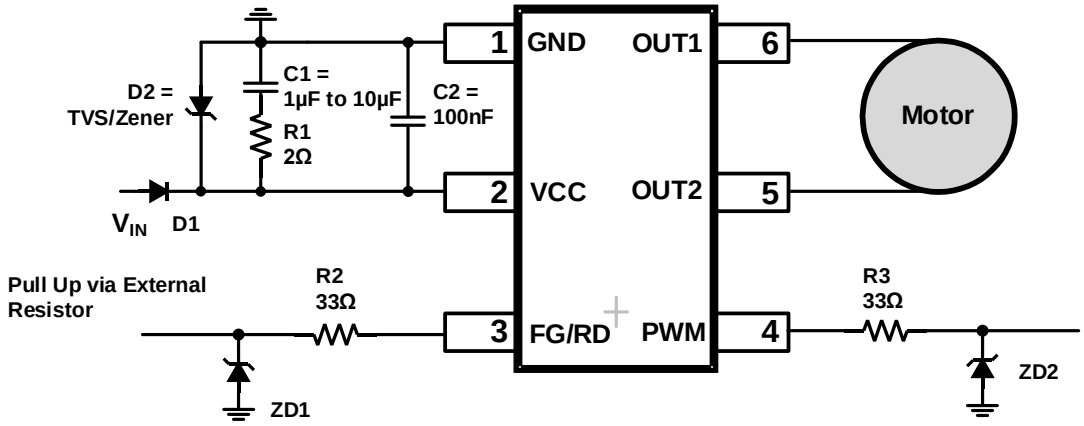
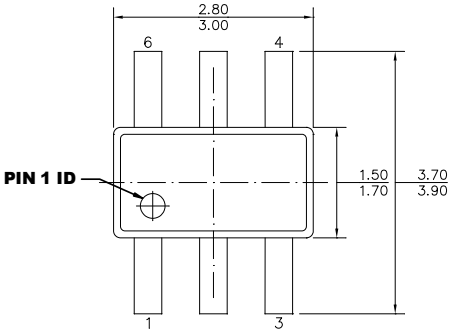


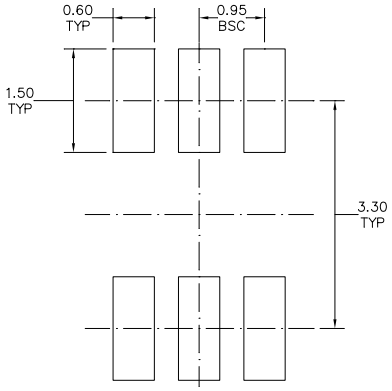
Figure 16: Typical Application Circuit with Voltage Clamping and Enhanced ESD

PACKAGE INFORMATION

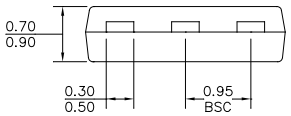
TSOT23-6-SL



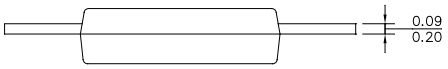
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



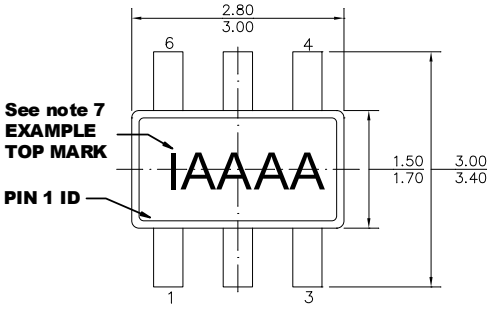
SIDE VIEW

NOTE:

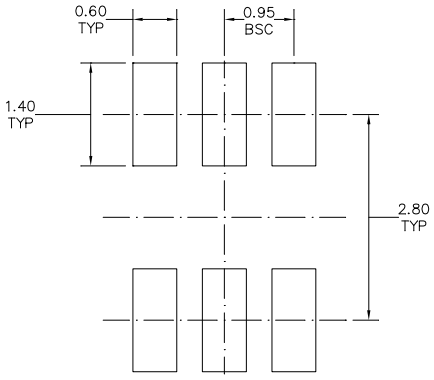
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

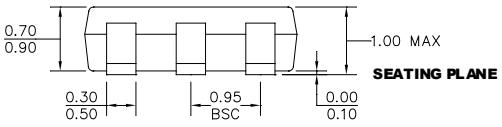
TSOT23-6-L



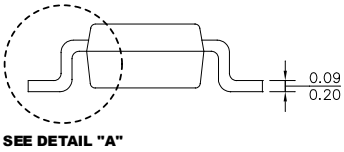
TOP VIEW



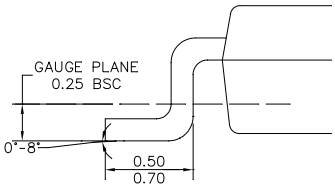
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



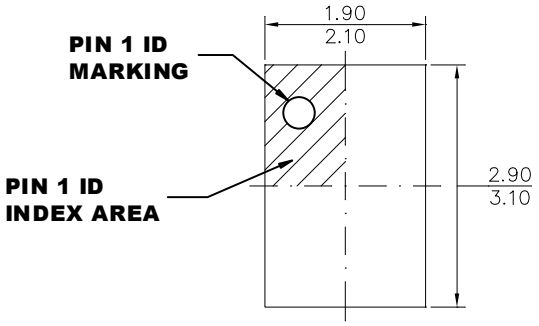
DETAIL "A"

NOTE:

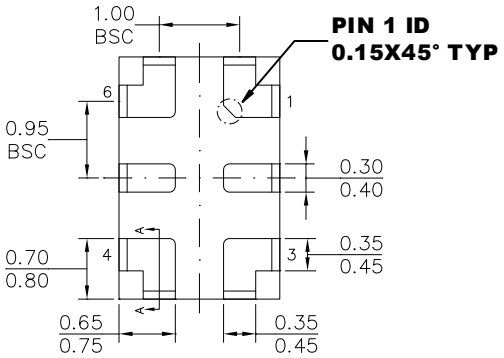
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

PACKAGE INFORMATION *(continued)*

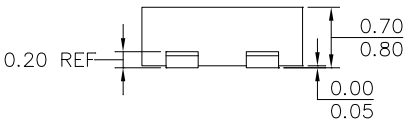
TQFN-6 (2mmx3mm)
Wettable Flank



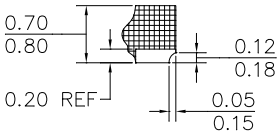
TOP VIEW



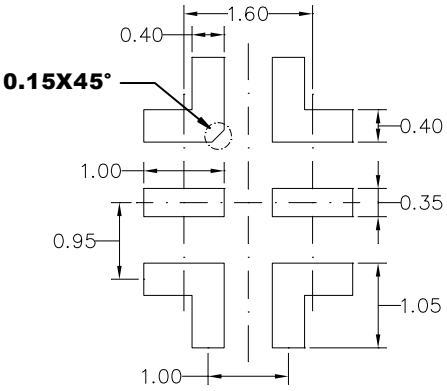
BOTTOM VIEW



SIDE VIEW



SECTION A-A

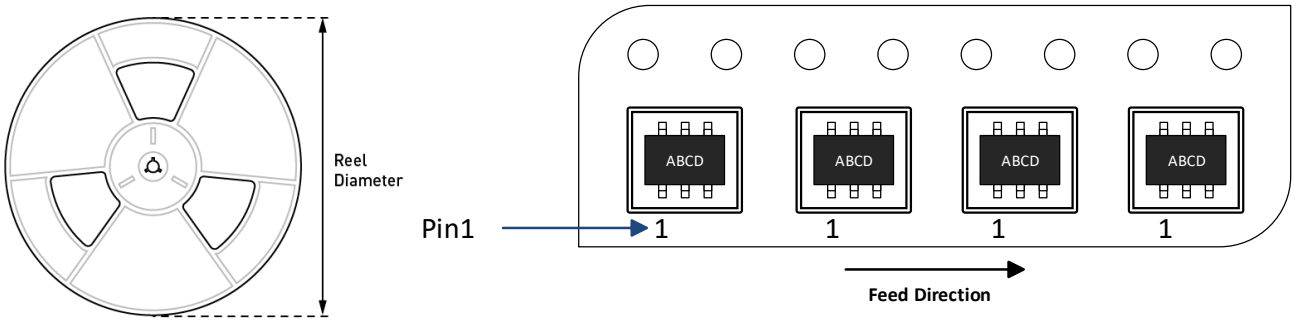


RECOMMENDED LAND PATTERN

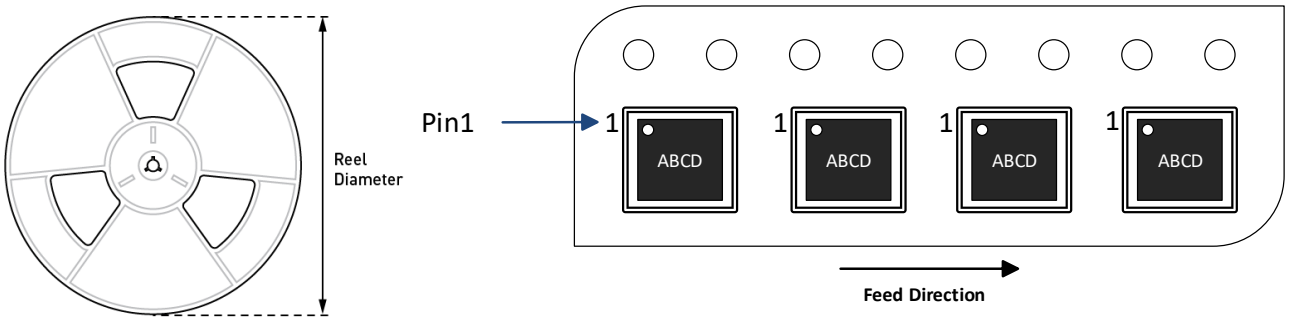
NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6653AGJS-xxxx-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MP6653AGJL-xxxx-Z	TSOT23-6-L	5000	N/A	N/A	13in	12mm	8mm



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6653AGDTE-xxxx-Z	TQFN-6 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/8/2024	Initial Release	-