MP6632

50V, Three-Phase BLDC Motor Driver with 1A Gate Driver

DESCRIPTION

The MP6632 is a three-phase brushless DC (BLDC) motor driver controller with up to 1A of driving current. It drives three-phase BLDC motors, with a 6V to 50V input voltage (V_{IN}) range.

The MP6632 controls the motor speed through the pulse-width modulation (PWM) signal or the DC signal on the PWM/DC pin with closed-loop/open-loop speed control. The device features a built-in, configurable speed curve function. It also features a sinusoidal drive for maximum torque, as well as low speed ripple and noise across the full speed range.

The MP6632 provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the Hall comparator's output. Direction control is achieved via the DIR pin's input.

Rich protections include under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6632 is available in a QFN-32 (4mmx4mm) package.

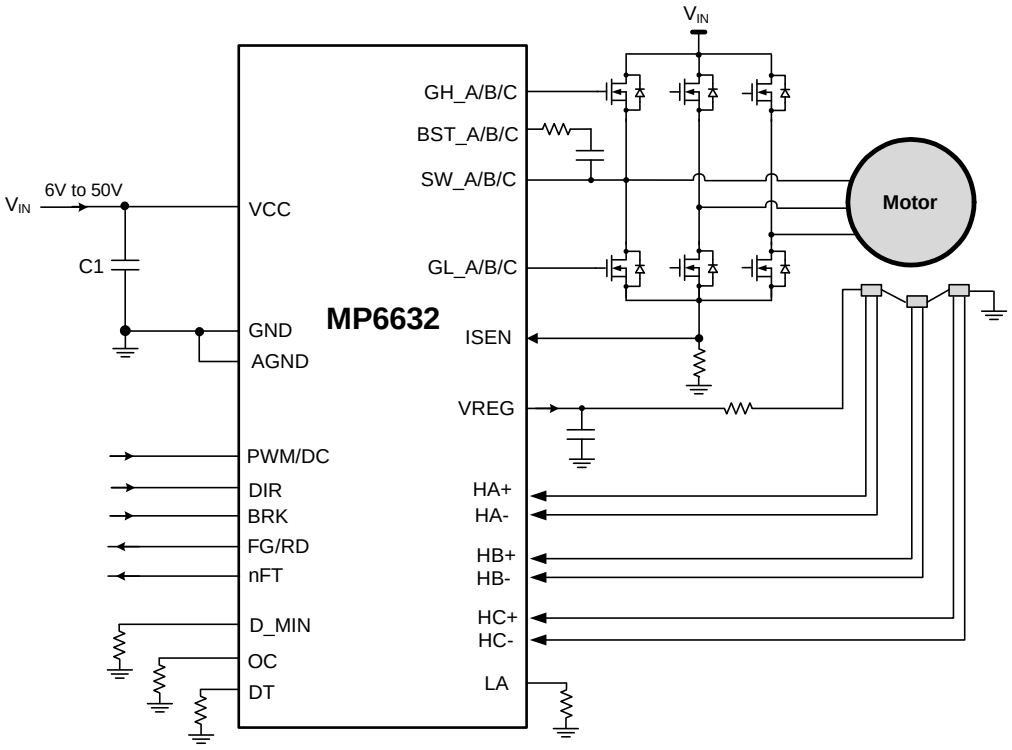
FEATURES

- 6V to 50V Input Voltage (V_{IN}) Range
- Up to 1A of Driving Current Capability
- Sinusoidal Drive
- Trapezoidal Drive
- Supports 0V to 3.3V DC Input or 50Hz to 100kHz Pulse-Width Modulation (PWM) Input
- Supports External Triple-Hall or Single-Hall Input
- Closed-Loop/Open-Loop Speed Control
- Direction/Brake Input
- Power-Save Mode
- Lock Protection
- Over-Current Protection (OCP)
- Rotational Speed Indicator
- 25kHz/50kHz Switching Frequency (f_{SW})
- Soft Start (SS) for Low Noise
- Available in a QFN-32 (4mmx4mm) Package

APPLICATIONS

- General Three-Phase Brushless DC (BLDC) Motors
- Fans
- Pumps

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6632GR-xxxx**	QFN-32 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6632GR-xxxx-Z).

** “xxxx” is the configuration code identifier. The first four digits of the suffix (“xxxx”) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for the non-default function option. “0000” is the default function value.

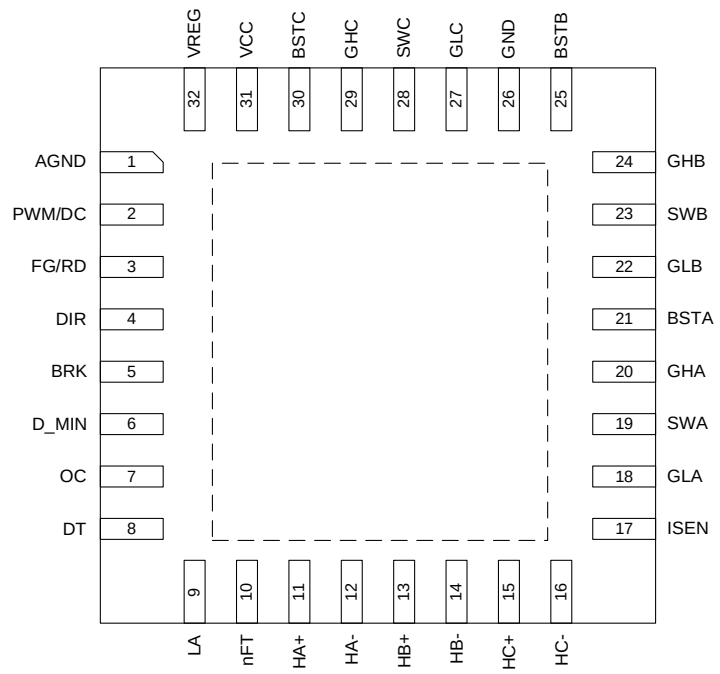
TOP MARKING

MPSYWW
MP6632
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP6632: First four digits of the part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-32 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground.**
2	PWM/DC	**Rotational speed control input.** The PWM/DC pin is connected to an internal low-dropout (LDO) regulator via an 85kΩ internal pull-up resistor. When PWM_DC = 0, apply a 50Hz to 100kHz pulse-width modulation (PWM) signal for speed control. When PWM_DC = 1, apply a 0V to 3.3V DC voltage for speed control.
3	FG/RD	**Speed or rotor lock indication.** The FG/RD pin can be used for speed indication (FG) or rotor deadlock indication (RD). FG/RD is an open-drain pin. Pull up this pin externally.
4	DIR	**Direction control.** Pull down the DIR pin internally via a resistor. Pull DIR low for forward rotation (A→B→C); pull DIR high for reverse rotation (A→C→B).
5	BRK	**Brake.** Pull the BRK pin high to brake the motor. Pull down BRK internally via a resistor.
6	D_MIN	**Input starting duty configuration.** Connect a resistor between the D_MIN pin and GND to set the starting duty. If D_MIN is floated, the starting duty is set via the internal register bits.
7	OC	**Over-current configuration.** Connect a resistor between the OC pin and GND to set the over-current threshold. If OC is floated, the over-current threshold is set via the internal register bits.
8	DT	**Dead time configuration.** Connect a resistor between the DT pin and GND to set the dead time (t_{DEAD}) of the high-side (HS) gate driver and low-side (LS) gate driver. If DT is floated, t_{DEAD} is set via the internal register bits.
9	LA	**Leading angle configuration.** Connect a resistor between the LA pin and GND to set the leading angle. If the LA pin is floated, the leading angle is set via the internal register bits.
10	nFT	**Fault indicator output.** If a fault is triggered, pull the nFT pin active low. nFT is an open-drain output. Pull up this pin externally.
11	HA+	**Phase A positive Hall input terminal.**
12	HA-	**Phase A negative Hall input terminal.** The HA- pin is active only in differential mode.
13	HB+	**Phase B positive Hall input terminal.**
14	HB-	**Phase B negative Hall input terminal.** The HB- pin is active only in differential mode.
15	HC+	**Phase C positive Hall input terminal.**
16	HC-	**Phase C negative Hall input terminal.** The HC- pin is active only in differential mode.
17	ISEN	**Current sense.** The ISEN pin senses the bus current via the sensing resistor.
18	GLA	**Phase A LS gate driver.**
19	SWA	**Phase A switching node.**
20	GHA	**Phase A HS gate driver.**
21	BSTA	**Phase A HS gate driver bootstrap (BST).**
22	GLB	**Phase B LS gate driver.**
23	SWB	**Phase B switching node.**
24	GHB	**Phase B HS gate driver.**
25	BSTB	**Phase B HS gate driver BST.**
26	GND	**Ground.**
27	GLC	**Phase C LS gate driver.**
28	SWC	**Phase C switching node.**
29	GHC	**Phase C HS gate driver.**
30	BSTC	**Phase C HS gate driver BST.**
31	VCC	**Input voltage supply.**
32	VREG	**10V reference output.**

ABSOLUTE MAXIMUM RATINGS (1)

VCC .....-0.3V to +55V
SWA, SWB, SWC .....-0.3V to V_{CC} + 0.3V
GHA, GHB, GHC, BSTA, BSTB, BSTC .....
……-0.3V to SWA/SWB/SWC + 13V
PWM/DC, VREG, GLA, GLB, GLC .....
……-0.3V to +13V
All other pins .....-0.3V to +6.5V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-32 (4mmx4mm) 2.97W
Junction temperature (T_J) .....150°C
Supply voltage (V_{CC}) .....5.5V to 55V
Operating temperature..... -40°C to +125°C

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM).....2000V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....6V to 50V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-32 (4mmx4mm)…...…....42…….9....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC}= 12V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			5	5.2	V
Input UVLO hysteresis				0.5		V
Operating supply current	I_{CC}			5		mA
Standby current	$I_{STANDBY}$	Pull the PWM/DC pin low for 100ms			200	uA
Logic Input Threshold						
DIR input high voltage	V_{DIR_H}		2			V
DIR input low voltage	V_{DIR_L}				0.8	V
DIR pull-down resistance	R_{DIR}			100		kΩ
BRK input high voltage	V_{BRK_H}		2			V
BRK input low voltage	V_{BRK_L}				0.8	V
BRK pull-down resistance	R_{BRK}			100		kΩ
PWM input high voltage	V_{PWM_H}	PWM_DC = 0	2			V
PWM input low voltage	V_{PWM_L}	PWM_DC = 0			0.8	V
PWM pull-up resistance	R_{PWM}	PWM_DC = 0		85		kΩ
DC input high voltage	V_{DC_H}	PWM_DC = 1, T_A = 25°C	3.2	3.3	3.4	V
DC input low voltage	V_{DC_L}	PWM_DC = 1		6		mV
Logic Output Voltage						
FG/RD output low-level voltage	V_{FG_L}	I_{FG} = 3mA			0.3	V
nFT output low-level voltage	V_{nFT}	I_{nFT} = 3mA			0.3	V
Reference						
VREG output voltage			9.5	10	10.5	V
VREG load regulation		I_{VREG} = 30mA		9.95		V
Bias output current (D_MIN, LA, OC, and DT pins)	I_{BIAS}		47.5	50	52.5	μA
D_MIN duty threshold	D_{MIN}	R_{D_MIN} = 10kΩ		15.6		%
Leading angle		R_{LA} = 10kΩ		18.8		deg
Gate Driver						
High-side (HS) gate driver high output voltage	V_{GATE_HS}			9.4		V
Low-side (LS) gate driver high output voltage	V_{GATE_LS}			10		V
Gate frequency	f_{SW}	T_A = 25°C	24.4	25	25.8	kHz
Gate sourcing current (5)	I_{SO}			1		A
Gate sinking current (5)	I_{SI}			1		A
Gate pull-up resistance	R_{UP}	T_A = 25°C			7	Ω
Gate pull-down resistance	R_{DOWN}	T_A = 25°C			5	Ω
Dead time	t_{DT}	R_{DT} = 28kΩ		300		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_A = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Hall Signal						
Hall input differential-mode voltage	V_{H_DM}	HLOGIC = 0, differential input mode	±30			mV
Hall input common-mode voltage	V_{H_CM}	HLOGIC = 0, differential input mode	0		4	V
Hall input offset voltage	V_{HO}	HLOGIC = 0, V_{HCM} = 1V, differential mode		±1		mV
Hall input hysteresis voltage	V_{H_HYS}	HLOGIC = 0, V_{HCM} = 1V, differential mode		±13		mV
Hall input logic high threshold	V_{HALL_H}	HLOGIC = 1, logic input mode	2			V
Hall input logic low threshold	V_{HALL_L}	HLOGIC = 1, logic input mode			0.8	V
Protection						
Over-current protection (OCP) threshold		R_{OC} = 28kΩ	90	100	110	mV
Locked-rotor detection time	t_{RD}			0.5		s
Locked-rotor retry time	t_{RD_R}			4.5		s
Thermal shutdown threshold				170		°C
Thermal shutdown hysteresis				30		°C

Note:

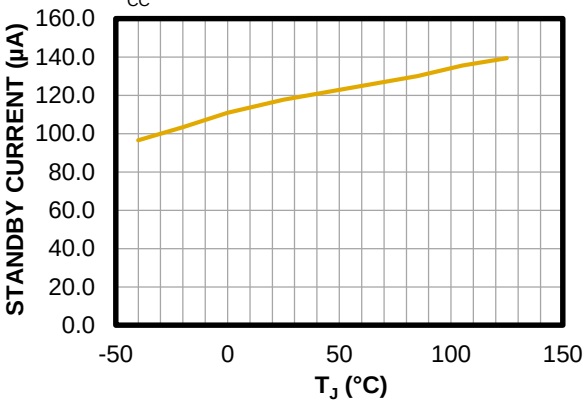
5) Guaranteed by design.

TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_A = -40°C to +125°C, unless otherwise noted.

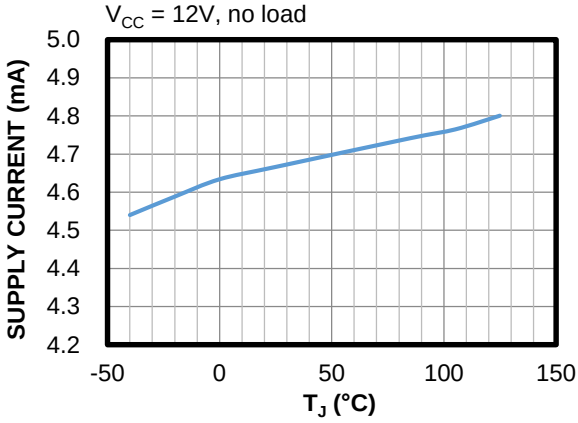
Standby Current vs. Junction Temperature

V_{CC} = 12V

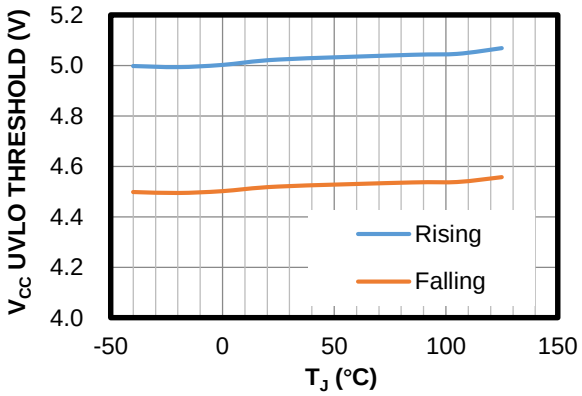


Supply Current vs. Junction Temperature

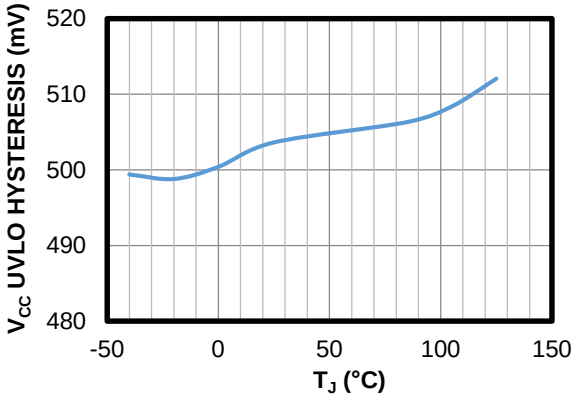
V_{CC} = 12V, no load



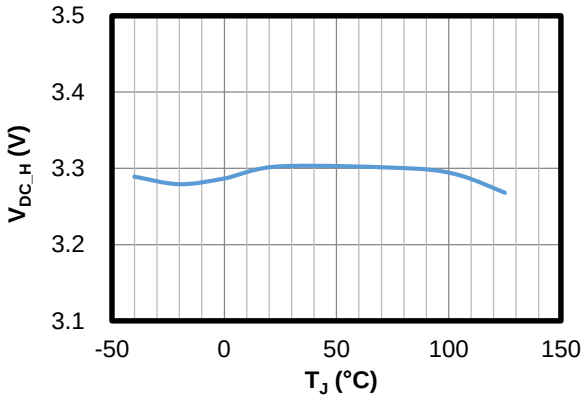
V_{CC} UVLO Threshold vs. Junction Temperature



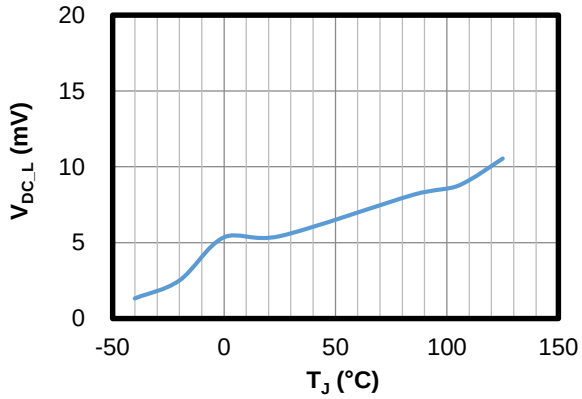
V_{CC} UVLO Hysteresis vs. Junction Temperature



DC Input High Voltage vs. Junction Temperature



DC Input Low Voltage vs. Junction Temperature

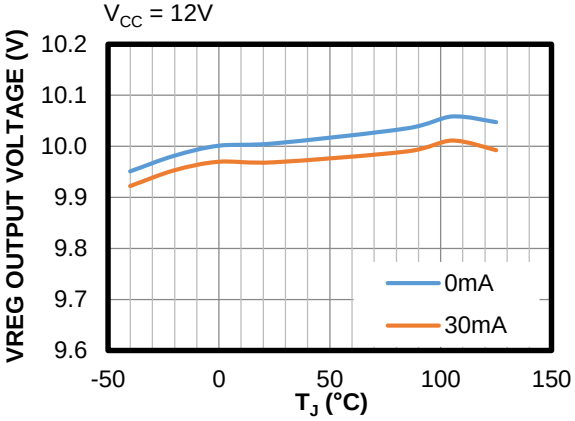


TYPICAL CHARACTERISTICS *(continued)*

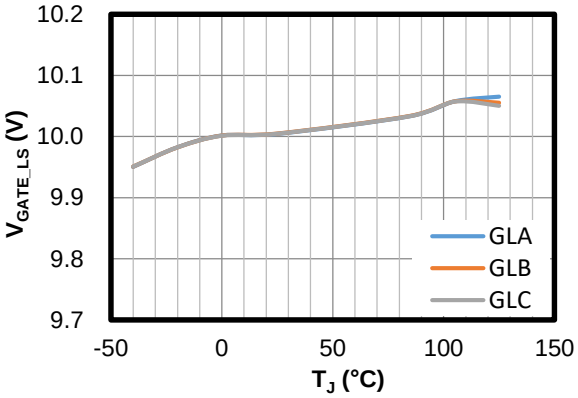
V_{CC} = 12V, T_A = -40°C to +125°C, unless otherwise noted.

VREG Output Voltage vs. Junction Temperature

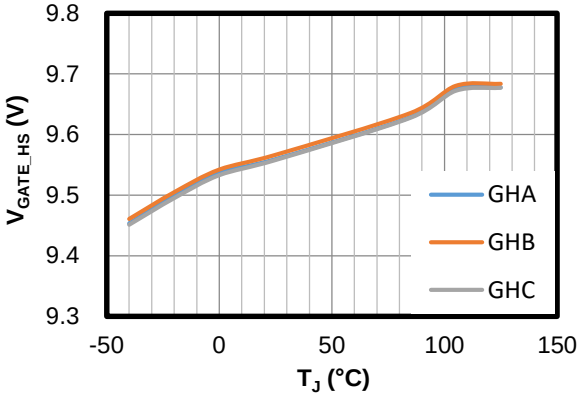
V_{CC} = 12V



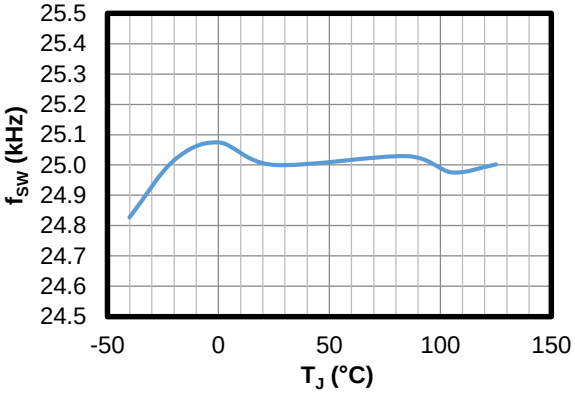
LS Gate Driver High Output Voltage vs. Junction Temperature



HS Gate Driver High Output Voltage vs. Junction Temperature

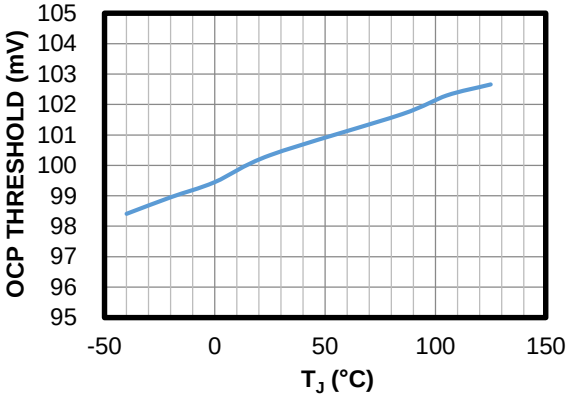


Gate Frequency vs. Junction Temperature



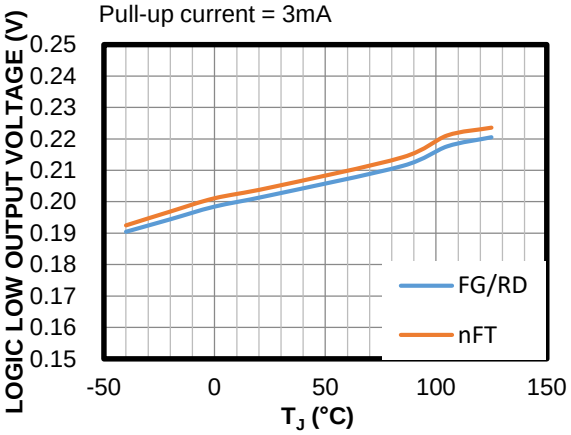
OCP Threshold vs. Junction Temperature

R_{OC} = 28kΩ



Logic Low Output Voltage vs. Junction Temperature

Pull-up current = 3mA

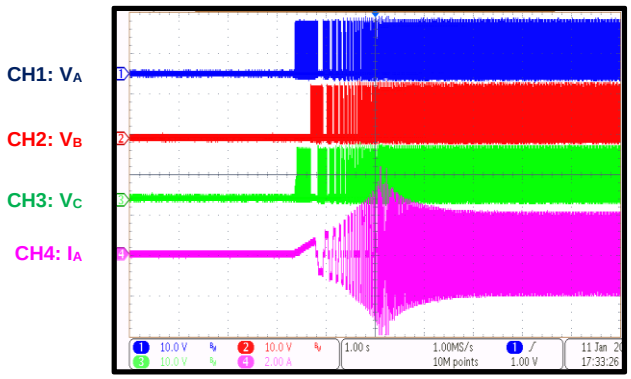


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

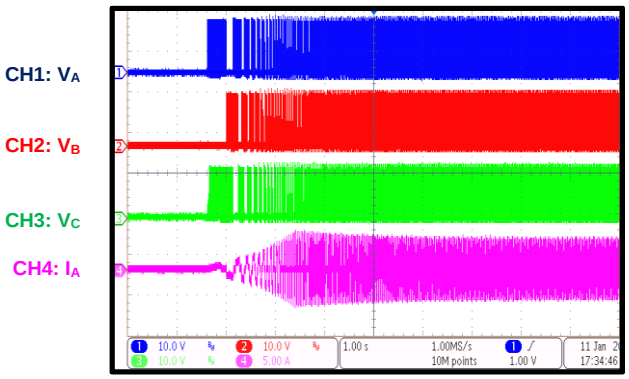
PWM On

PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = low, CCW trapezoid



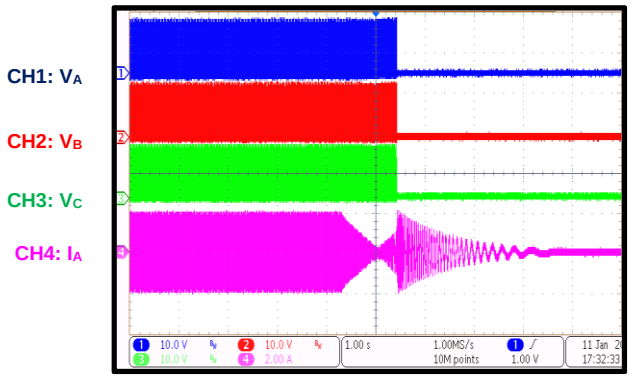
PWM On

PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = high, CW trapezoid



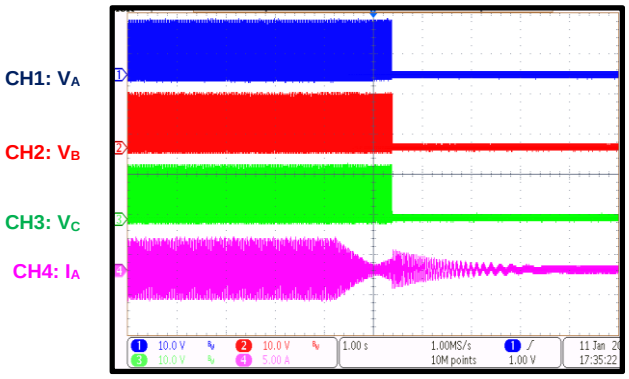
PWM Off

PWM duty = 100% to 0%, DIR = low, triple Hall-effect sensor, CCW trapezoid



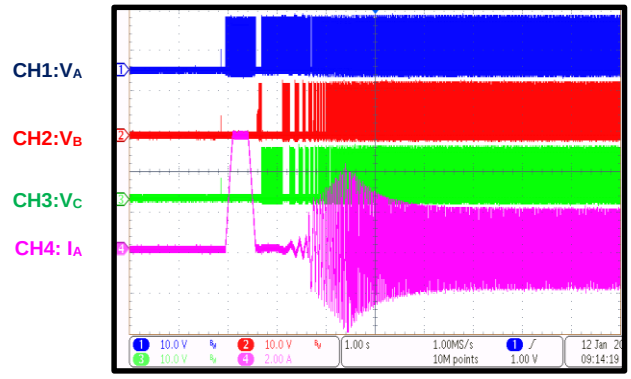
PWM Off

PWM duty = 100% to 0%, DIR = high, triple Hall-effect sensor, CW trapezoid



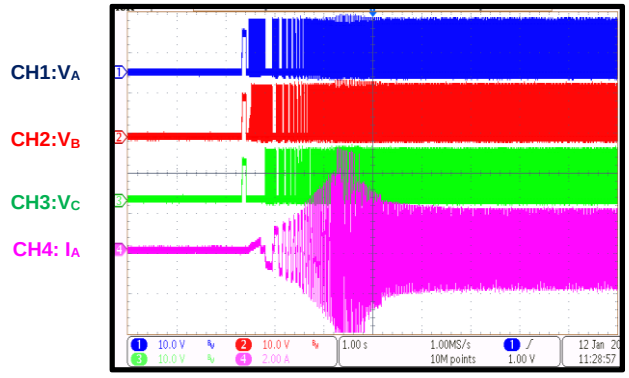
Start-Up through VCC

V_{CC} = 0V to 12V, PWM duty = 100%, single Hall-effect sensor, DIR = low, CCW



Start-Up through VCC

V_{CC} = 0V to 12V, PWM duty = 100%, triple Hall-effect sensor, DIR = low, CCW

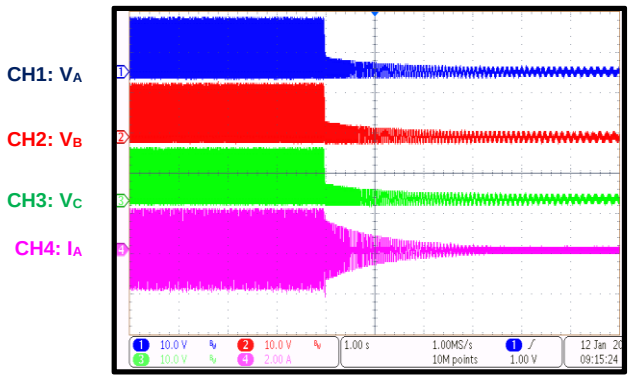


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

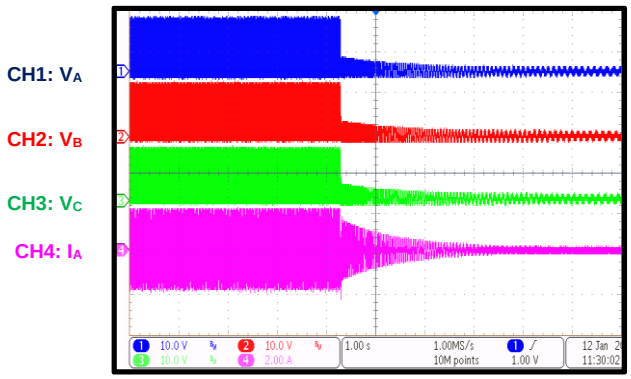
Shutdown through VCC

V_{CC} = 12V to 0V, PWM duty = 100%, single Hall-effect sensor, DIR = low, CCW



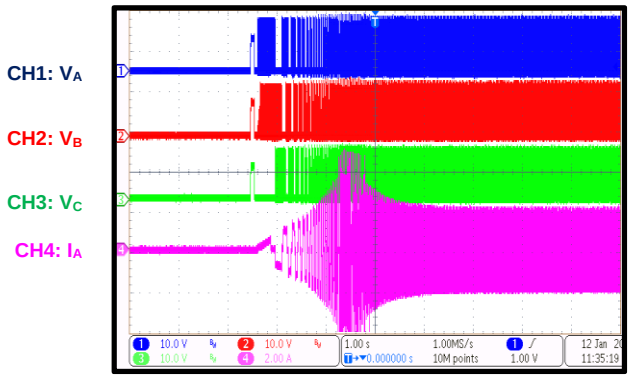
Shutdown through VCC

V_{CC} = 12V to 0V, PWM duty = 100%, triple Hall-effect sensor, DIR = low, CCW



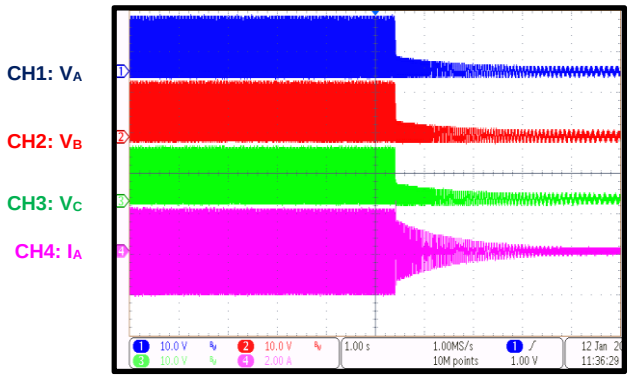
Start-Up through VCC

V_{CC} = 0V to 12V, PWM duty = 100%, triple Hall-effect sensor, DIR = low, CCW trapezoid



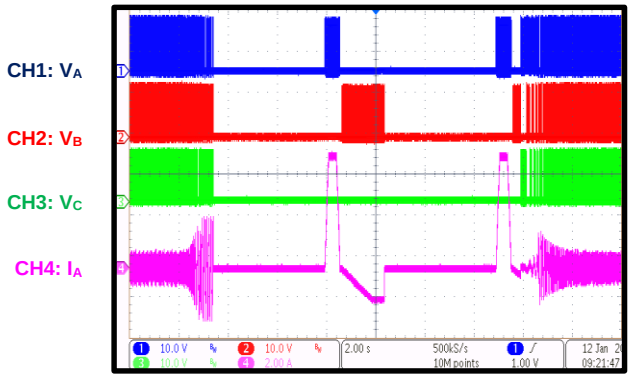
Shutdown through VCC

VCC = 12V to 0V, PWM duty = 100%, triple Hall-effect sensor, DIR = low, CCW trapezoid



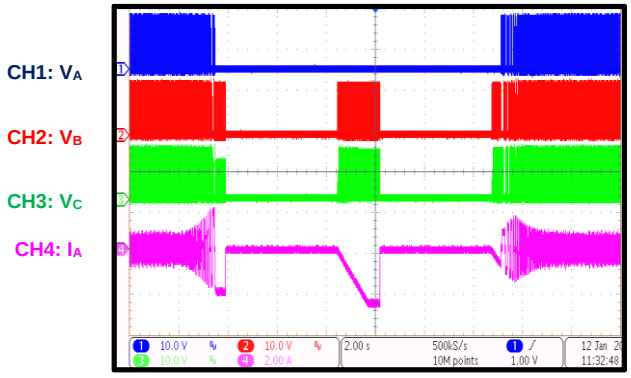
Rotor Lock and Retry

PWM duty = 40%, single Hall-effect sensor, lock rotor then release



Rotor Lock and Retry

PWM duty = 40%, triple Hall-effect sensor, lock rotor then release



FUNCTIONAL BLOCK DIAGRAM

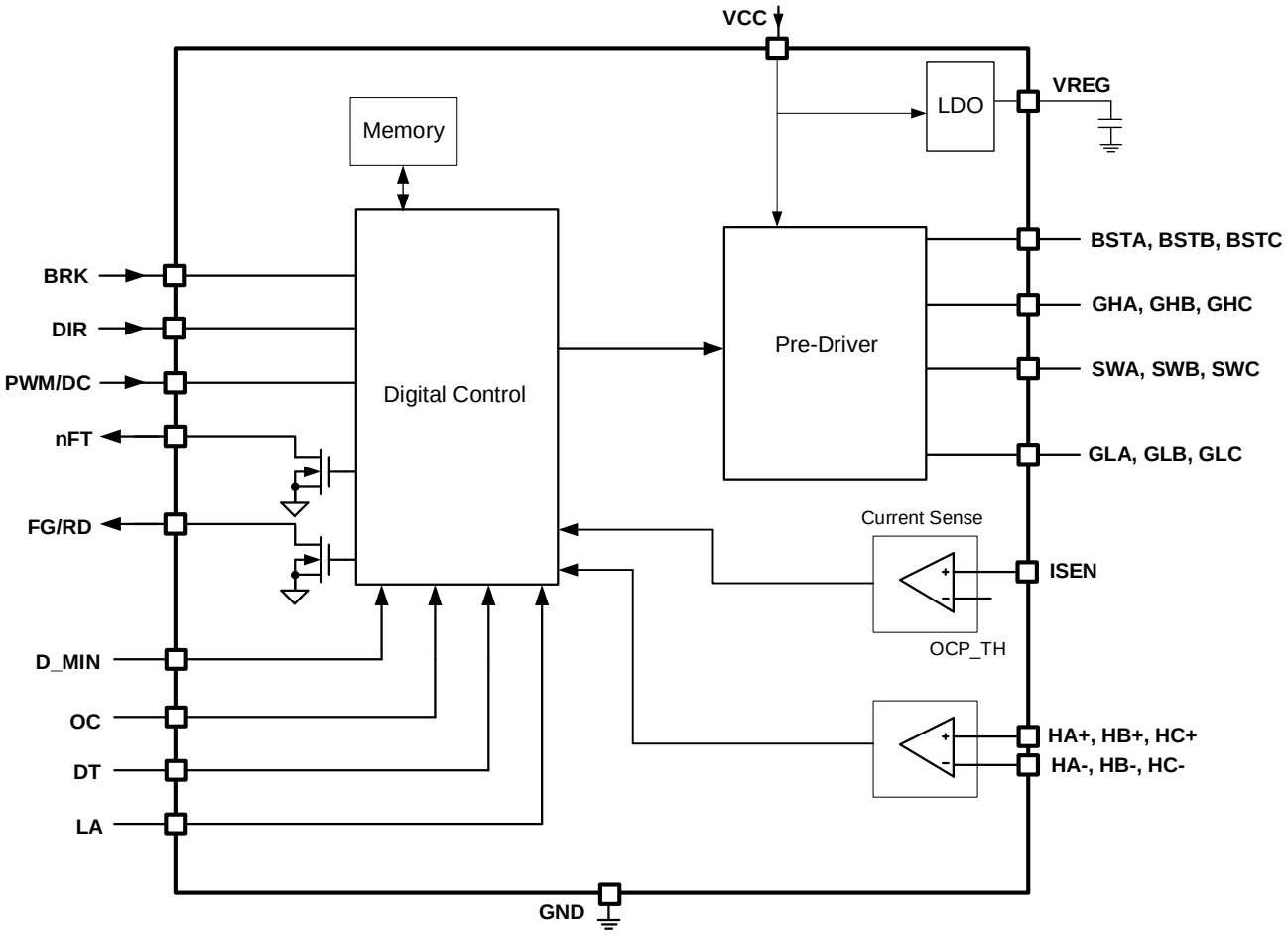


Figure 1: Functional Block Diagram

OPERATION

The MP6632 is a three-phase brushless DC (BLDC) motor driver controller. The MP6632 controls the motor speed via the pulse-width modulation (PWM) signal or the DC voltage on the PWM/DC pin with closed-loop/open-loop speed control and a built-in, configurable speed curve function. The device features sinusoidal control to optimize efficiency and speed ripple across the full speed range.

The MP6632 supports either a sinusoidal drive or trapezoidal drive via the register setting based on the external Hall-effect sensor's signal.

Figure 2 shows the sinusoidal drive.

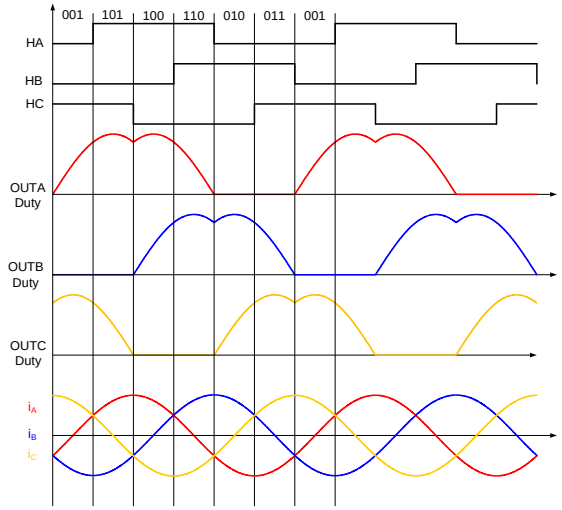


Figure 2: Sinusoidal Drive

Figure 3 shows the trapezoidal drive.

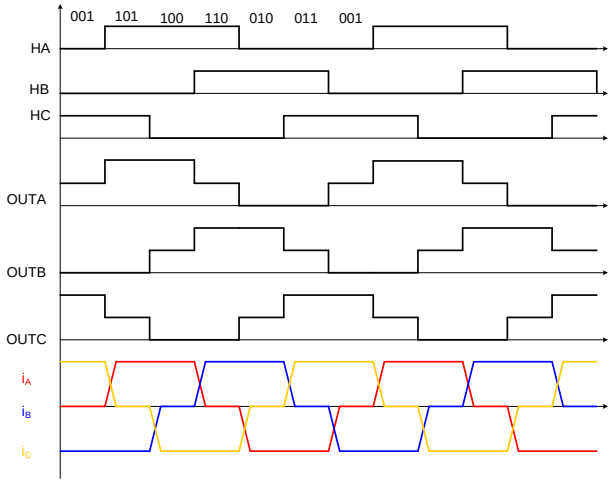


Figure 3: Trapezoidal Drive

The MP6632 also provides rotational speed detection. The FG/RD pin is the rotational speed detector and is an open-drain output. FG/RD outputs a high or low voltage relative to the external Hall-effect sensor's signal. Direction control is achieved via the DIR pin's input, and the BRK pin brakes the motor.

Rich protections include under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

Speed Control

The PWM/DC pin controls the motor speed via the PWM signal or the DC voltage.

If PWM_DC = 1, the motor speed is controlled via the DC voltage on the PWM/DC pin. The external DC voltage is linearly converted to an input PWM duty cycle internally. The DC voltage range is 0V to 3.3V.

If PWM_DC = 0, the motor speed is controlled via the input PWM signal duty cycle. The input PWM signal frequency is between 50Hz and 100kHz. The supported PWM signal frequency range can be selected via the register bit.

Open-Loop/Closed-Loop Speed Control

The MP6632 supports open-loop or closed-loop speed control, which is configured by register bits OPEN_L and CLOSE_H.

In closed-loop mode (OPEN_L = 0, CLOSE_H = 1), the MP6632 internally detects the Hall signal speed and feedback to the control loop, then adjusts the output PWM duty in a closed loop. By doing this, the motor speed follows the reference exactly.

In open-loop mode (OPEN_L = 1), the OUTA, OUTB, and OUTC output duty cycles directly depend on the PWM input duty.

In mixed mode (OPEN_L = 0, CLOSE_H = 0), the MP6632 operates in closed-loop mode when the PWM input duty is below 87.5%, and operates in open-loop mode when input duty exceeds 87.5%.

Starting Duty and Minimum Speed

The input starting duty can be configured by the internal register or the resistance on the external D_MIN pin (R_{D_MIN}). If D_MIN is floated,

the starting duty is set via the internal register. Otherwise, the starting duty is set via the resistance on D_MIN.

When the MP6632 is enabled, the voltage on D_MIN (V_{D_MIN}) is detected and then sets the starting duty cycle. The starting duty cycle remains constant until the power is reset.

Table 1 shows the starting duty set via R_{D_MIN}.

Table 1: Starting Duty Set via R_{D_MIN}

R_{D_MIN} (kΩ)	DIN_MIN Starting Duty (%)
0	0
2	3.125
4	6.25
6	9.375
8	12.5
10	15.625
12	18.75
14	21.875
16	25
20	28.125
24	31.25
28	34.375
32	37.5
38	40.625
44	43.75
50	46.875

When the PWM input duty is below the starting duty configured by register bits SPD_ZERO and MAX_EN, there are three operation modes:

1. If SPD_ZERO = 0 and MAX_EN = 0, the speed maintains the minimum speed.
2. If SPD_ZERO = 0 and MAX_EN = 1, the speed rises to the maximum speed.
3. If SPD_ZERO = 1 and MAX_EN = x, the speed is at 0.

Speed Curve Configuration

The SPD_MAX registers configure the speed when the input PWM duty is at 100%. Otherwise, the MP6632 provides a five-point curve configuration function where the output speed can be configured when the input duty is 37.5%, 50%, 62.5%, 75%, or 87.5%. Linear interpolation occurs between the adjacent duty cycles.

Figure 4 shows the curve configuration when SPD_ZERO = 1.

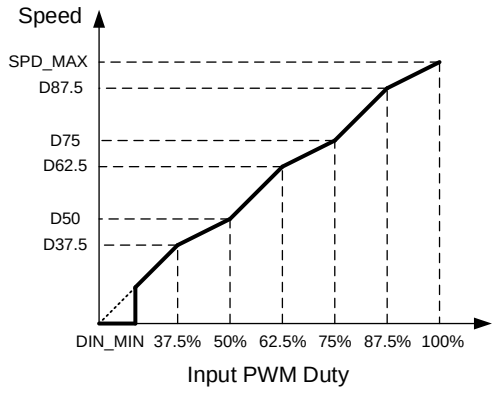


Figure 4: Curve Configuration when SPD_ZERO = 1

Figure 5 shows the curve configuration when SPD_ZERO = 0.

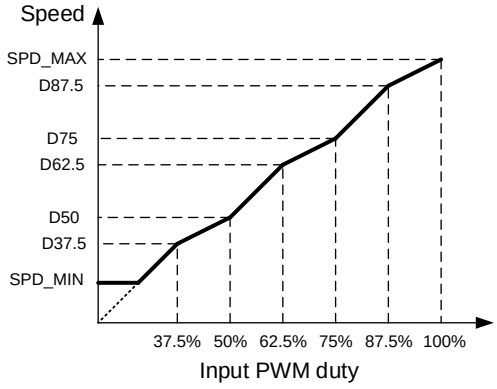


Figure 5: Curve Configuration when SPD_ZERO = 0

The DIN_MIN register sets the starting duty, and the SPD_MIN register sets the minimum output duty (open-loop control) and minimum speed (closed-loop control).

Single-Hall or Triple-Hall Input Mode

The MP6632 supports either a single or triple Hall-effect sensor. If a single Hall-effect sensor is employed, the Hall selecting bit must set the single Hall sensor, and Hall C is used as the control.

Direction Control

The direction is controlled by the DIR pin's polarity. When DIR is pulled low, the MP6632 operates in forward rotation in the following sequence: A → B → C → A…

When DIR is pulled high, the MP6632 operates in reverse rotation in the following sequence: A → C → B → A...

Alignment

In single Hall sensor applications, the MP6632 aligns the rotor at the beginning of start-up in certain angles depending on the Hall sensor signals. A set vector is given for a configurable time to pull the rotor to the initial position. Then the MP6632 enters pre-startup.

The alignment time is selectable by the register, where the default time is 320ms.

Pre-Startup Time

Once the alignment time completes, the MP6632 gradually increases the output duty cycle before the speed is controlled by the input PWM duty cycle. This is triggered by the timer set via the register bits TPRE[1:0]. This process avoids start-up current when the fan is at a standstill and provides robust start-up.

A longer pre-startup time leads to lower soft pre-start current, but increases pre-startup time.

Soft-Start Time

To reduce the input inrush current during start-up, the MP6632 provides the reference speed's configurable soft-start time (t_{SS}) by setting register bits T_SS[1:0]. This time can be configured from 1.3s to 10.4s.

Closed-Loop Integrator Gain

In closed-loop mode, the closed-loop integrator gain depends on the register bits KI[7:0] and KP[7:0].

Higher KI and KP values lead to faster loop response when the loop is steady.

Setting the Switching Frequency

The operating switching frequency (f_{SW}) can be configured to 25KHz/50kHz by the SW_SEL register.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall change signal for speed indication. Different FG signal frequencies are provided based on the application type. Triple Hall sensor applications include 1x, 1/2x and 3x Hall frequencies. Single Hall sensor applications include 1x, 1/2x, and 1/4x Hall frequencies. The frequencies are selected via the register bits FGRD[1:0].

FG is an open-drain output that must be pulled up externally during normal operation.

Dead Time

A dead time (t_{DEAD}) is required to prevent shoot-through during any phase of the bridge. t_{DEAD} for all three phases is set via a single dead time resistor (R_{DT}) on the DT pin or the internal register. t_{DEAD} is selectable with 8 different options.

Table 2 shows t_{DEAD} set by R_{DT}.

Table 2: Dead Time Set via R_{DT}

R_{DT} (kΩ)	t_{DEAD} (ns)
0	800
4	700
8	600
12	500
16	400
24	300
32	200
44	100

Leading Angle

The leading angle can be configured via an external resistor on the LA pin (R_{LA}) or the internal register. The leading angle ranges between 0° and 60°.

The leading angle compensation is active only in the sinusoidal drive. There is no leading angle compensation function in the trapezoidal drive.

Table 3 on page 16 shows the leading angle set by R_{LA}.

Table 3: Leading Angle Set by R_{LA}

R_{LA} (kΩ)	Leading Angle
0	Auto
2	3.75°
4	7.5°
6	11.25°
8	15°
10	18.75°
12	22.5°
14	26.25°
16	30°
20	33.75°
24	37.5°
32	45°
38	48.75°
44	52.5°
50	56.25°
Float	Internal register

Standby Mode

The MP6632 integrates standby mode to reduce power consumption.

If PWM_DC = 0, the input PWM duty remains low for longer than 100ms, and there is no gate driver output. The MP6632 then enters standby mode where most of the internal circuitry turn off, including the VREG LDO regulator.

Rotor Deadlock Protection

If the motor rotor is locked and the Hall signal edge is not detected during the 0.5s detection time, then all the low-side (LS) gate drivers output high, and all the LS-FETs turn on and auto-restart after 4.5s. The MP6632 then tries to recover. During locked-rotor fault status, nFT remains low. Once the fault is removed, nFT is pulled high again.

Over-Current Protection (OCP)

The MP6632 senses the bus current via the sense resistor during normal switching. If the bus current exceeds the threshold set via the OC pin or the OCP_SEL register after the deglitch time, all the LS-FETs turn on immediately. The MP6632 resumes normal switching in the next switching cycle. If the over-current fault lasts longer than the time set via the register bits PTIME[2:0], all the gate drivers are disabled. OCP can be configured to latch-off mode or retry mode. In addition, OCP can be configured to decrease the output duty cycle.

Table 4 shows the OCP threshold set via the OC resistor (R_{OC}).

Table 4: OCP Threshold Set via R_{OC}

R_{OC} (kΩ)	OCP Threshold (mV)
0 to 6	Disabled
16 to 28	100
8 to 14	50
32 to 80	200

Thermal Shutdown

The MP6632 also provides thermal monitoring. If the die temperature exceeds 175°C, then all the gate drivers are disabled. Once the die temperature drops below 150°C, normal operation automatically resumes. nFT is pulled low when thermal shutdown is triggered.

Under-Voltage Lockout (UVLO)

If the voltage on the VCC pin (V_{CC}) falls below the UVLO threshold, all circuitry in the device is disabled, and the internal logic resets. when Once V_{CC} exceeds the UVLO threshold the device resumes normal operation.

REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPD_MAX[7:0]							
01h (OTP/REG)	SPD_MAX[15:8]							
02h (OTP/REG)	SPD_MIN[7:0]							
03h (OTP/REG)	HI_FREQ	BRK_MD	DIN_MIN[5:0]					
04h (OTP/REG)	WAIT_TM[1:0]		WAIT_PWM	MAX_EN	CLOSE_H	OPEN_L	LOCK_SEL[1:0]	
05h (OTP/REG)	DST	T_SS[1:0]		TPRE[1:0]		SPD_ZERO	SINGLE	FSINE
06h (OTP/REG)	OCP_BH	SINE	PWM_DC	FGRD[1:0]		OCP_TH[1:0]		TPOS
07h (OTP/REG)	PWM_L	SW_SEL	THETA_COMP[5:0]					
08h (OTP/REG)	KI[7:0]							
09h (OTP/REG)	KP[7:0]							
0Ah (OTP/REG)	RESERVED							
0Bh (OTP/REG)	D37.5							
0Ch (OTP/REG)	D50							
0Dh (OTP/REG)	D62.5							
0Eh (OTP/REG)	D75							
0Fh (OTP/REG)	D87.5							
10h (OTP/REG)	RESERVED	MIN_SEL	DT[2:0]			PTIME[2:0]		
11h (OTP/REG)	RESERVED	WAIT_BH	WAIT_SEL	WAIT_EN	MOD	OC_RTY	HLOGIC	RESERVED
12h (OTP/REG)	OCP_RED	RESERVED	HAL_POL	INTP_EN	RESERVED	LOCK_LF	OCP_LF	RESERVED

MAX_SPEED_1 (00h)

The MAX_SPEED_1 command sets the maximum speed in closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[7:0]	0xFF	Sets the maximum speed when the input duty is 100%. 8-bit least significant bit (LSB). Electrical speed = 7.5rpm / LSB.

MAX_SPEED_2 (01h)

The MAX_SPEED_2 command sets the maximum speed in closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[15:8]	0x08	Sets the maximum speed when the input duty is 100%. 8-bit most significant bit (MSB). Combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).

MIN_SPEED (02h)

The MIN_SPEED command sets the minimum speed in closed-loop speed control or the minimum output duty in open-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MIN[7:0]	0x20	Sets the minimum speed or minimum output duty. In closed-loop mode, this bit sets the minimum speed (electrical speed), depending on the HI_FREQ bit, where: HI_FREQ = 0, 60rpm / LSB HI_FREQ = 1, 480rpm / LSB In open-loop mode, this bit sets the minimum output duty, where minimum output duty = SPD_MIN[7:0] / 255 and the default is 12.5%.

CFR_1 (03h)

The CFR_1 command refers to the control function register and sets the switching frequency (f_{SW}), brake mode, and starting duty.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	HI_FREQ	0	Selects the high frequency. 0: High frequency is not selected (default) 1: High frequency is selected The SW bit must be set to 1 if HI_FREQ = 1.
6	OTP/REG	BRK_MD	0	Selects the brake action after the BRK pin is pulled high. 0: The reference duty cycle reduces to DIN_MIN, then turns on the low-side MOSFETs (LS-FETs) 1: Turns on the LS-FETs
5:0	OTP/REG	DIN_MIN[5:0]	0x10	Sets the starting duty, where the starting duty = DIN_MIN / 128 and the default is 12.5%.

CFR_2 (04h)

The CFR_2 command sets the wait status, maximum speed below starting duty, open-loop/closed-loop speed control, and lock protection time.

Bits	Access	Bit Name	Default	Description
7:6	OTP/REG	WAIT_TM[1:0]	00	Selects the waiting time or speed threshold at start-up. Combined with WAIT_SEL, these bits can select the fixed time that the IC waits before output switching or the motor speed threshold at which the IC starts driving the motor. When LOCK_SEL = 00, the waiting time or speed threshold can be selected as follows: If WAIT_SEL = 1, wait for a fixed time. The time setting is WAIT_TM = 00: 1.2s, 01: 1.8s, 10: 3s, 11: 4.2s. If WAIT_SEL = 0, wait for the motor speed to drop to a certain speed, where WAIT_TM = 00: 1000rpm (electrical speed), 01: 600rpm, 10: 150rpm, 11: 60rpm. This is also related to the LOCK_SEL register setting. If LOCK_SEL = 01, the wait time is doubled, and the corresponding speed threshold is reduced to half of its default speed. If LOCK_SEL = 1x, the wait time is increased by four times, and the speed threshold is reduced to a fourth of its default speed.
5	OTP/REG	WAIT_PWM	0	Enables the wait function for the PWM on/off control. 0: Disable the wait function for the PWM on/off control 1: Enable the wait function for the PWM on/off control
4	OTP/REG	MAX_EN	0	Enables the maximum speed when PWM input duty < DIN_MIN. 0: Disabled (default) 1: Maximum output speed or maximum output duty when PWM input duty < DIN_MIN This is active only when SPD_ZERO = 0.
3	OTP/REG	CLOSE_H	0	Enables closed-loop speed control when the PWM input duty > 87.5%. 0: Open-loop speed control when the PWM input duty > 87.5% (default) 1: Closed-loop speed control when the PWM input duty > 87.5%
2	OTP/REG	OPEN_L	1	Enables open-loop speed control. 1: Open-loop speed control (default) 0: Closed-loop speed control when the PWM input duty < 87.5%
1:0	OTP/REG	LOCK_SEL	00	Selects the lock detection time and retry time. 00: The detection time is 0.5s, and the retry time is 4.5s 01: The detection time is 1s, and the retry time is 9s 1x: The detection time is 2s, and the retry time is 18s

START_HALL (05h)

The START_HALL command sets the start-up, Hall-effect sensor, and dynamic operation.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	DST	0	Sets the duty limit at pre-startup. 0: 50% 1: 93%
6:5	OTP/REG	T_SS[1:0]	00	Sets the soft dynamic time. The output duty reference time ranges from 0% to 100%. 00: 1.3s (default) 01: 2.6s 10: 5.2s 11: 10.4s
4:3	OTP/REG	TPRE[1:0]	10	Pre-startup time bits. The output duty's time duration increases by 1 step. 00: 2.5ms 01: 5ms 10: 10ms (default) 11: 20ms
2	OTP/REG	SPD_ZERO	1	Enables zero speed. 0: Maintain the minimum speed when PWM input duty cycle < DIN_MIN 1: Stop when PWM input duty cycle< DIN_MIN
1	OTP/REG	SINGLE	0	Selects the number of Hall sensors. 0: Triple Hall sensor application (default) 1: Single Hall sensor application
0	OTP/REG	FSINE	0	Selects the sinusoidal drive or trapezoidal drive based on the dynamic load. This bit is active only when the sinusoidal drive is selected (SINE = 1). 0: Trapezoidal drive with dynamic load 1: Sinusoidal drive with dynamic load

CFR_3 (06h)

The CFR_3 command sets the over-current protection (OCP), driving mode, pulse-width modulation (PWM) input and FG/RD output, and alignment time.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OCP_BH	0	Enables over-current protection (OCP) actions. 0: Turn on the LS-FETs 1: Float
6	OTP/REG	SINE	1	Selects the sinusoidal drive or trapezoidal drive. 0: Trapezoidal drive 1: Sinusoidal drive
5	OTP/REG	PWM_DC	0	Selects the DC input or pulse-width modulation (PWM) input for the PWM/DC pin. 0: PWM input (default) 1: DC input
4:3	OTP/REG	FGRD[1:0]	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 10: 1/4x for single Hall sensor applications, 3x for triple Hall sensor applications 11: RD
2:1	OTP/REG	OCP_TH[1:0]	11	Selects the OCP threshold. 00: Disabled 01: 50mV 10: 100mV 11: 200mV
0	OTP/REG	TPOS	0	Sets the alignment time in single Hall sensor applications. 0: 320ms (default) 1: 650ms

PWM_SW_COMP (07h)

The PWM_SW_COMP command sets the PWM frequency range, f_{SW}, and the compensation angle.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	PWM_L	0	Selects the input PWM frequency. 0: 1kHz to 100kHz 1: 50Hz to 2kHz
6	OTP/REG	SW_SEL	0	Selects the output f_{SW}. 0: 25kHz (default) 1: 50kHz
5:0	OTP/REG	THETA_COMP [5:0]	0x01	Sets the leading compensation angle (active only in sinusoidal drive). 0x00: Auto compensation The non-zero value sets the fixed leading angle compensation. Leading compensation angle = THETA_COMP[5:0] x 15 / 16°

KI (08h)

The KI command configures the integral parameter for closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	KI[7:0]	0x01	Sets the integral parameter for closed-loop speed control.

KP (09h)

The KP command configures the gain parameter during closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	KP[7:0]	0x01	Sets the gain during closed-loop speed control.

SPEED_CURVE_1 (0Bh)

The SPEED_CURVE_1 command configures the speed when the input PWM duty cycle is at 37.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D37.5[7:0]	0x60	Sets the speed or output duty when the input PWM duty = 37.5%. For open-loop control, set the output duty when the input PWM duty = 37.5%. Output duty = D37.5[7:0] / 256. For closed-loop control, set the reference speed when the input PWM duty = 37.5%. Speed = D37.5[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_2 (0Ch)

The SPEED_CURVE_2 command configures the speed when the input PWM duty cycle is at 50%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D50[7:0]	0x80	Sets the speed or output duty when the input PWM duty = 50%. For open-loop control, set the output duty when the input PWM duty = 50%. Output duty = D50[7:0] / 256. For closed-loop control, set the reference speed when the input PWM duty = 50%. Speed = D50[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_3 (0Dh)

The SPEED_CURVE_3 command configures the speed when the input PWM duty cycle is at 62.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D62.5[7:0]	0xA0	Sets the speed or output duty when the input PWM duty = 62.5%. For open-loop control, set the output duty when the input PWM duty = 62.5%. Output duty = D62.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 62.5%. Speed = D62.5[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_4 (0Eh)

The SPEED_CURVE_4 command configures the speed when the input PWM duty cycle is at 75%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D75[7:0]	0xC0	Sets the speed or output duty when the input PWM duty = 75%. For open-loop control, set the output duty when the input PWM duty = 75%. Output duty = D75[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 75%. Speed = D75[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_5 (0Fh)

The SPEED_CURVE_5 command configures the speed when the input PWM duty cycle is at 87.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D87.5[7:0]	0xE0	Sets the speed or output duty when the input PWM duty = 87.5%. For open-loop control, set the output duty when the input PWM duty = 87.5%. Output duty = D87.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 87.5%. Speed = D87.5[7:0] / 256 x SPD_MAX[15:8].

GATE_DRIVE_PT (10h)

The GATE_DRIVE_PT command sets the minimum on time, dead time (t_{DEAD}), and protection time.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	00	Reserved.
6	OTP/REG	MIN_SEL	0	Selects the minimum on time of the LS-FETs. 0: 400ns 1: 800ns
5:3	OTP/REG	DT[2:0]	000	Selects the dead time (t_{DEAD}). 000: 800ns 001: 700ns 010: 600ns 011: 500ns 100: 400ns 101: 300ns 110: 200ns 111: 100ns
2:0	OTP/REG	PTIME[2:0]	010	Selects the protection time. 000: 80ms 001: 160ms 010: 240ms 011: 320ms 100: 400ms 101: 480ms 110: 560ms 111: 640ms

CFR_4 (11h)

The CFR_4 command sets the wait configuration, SVPWM mode, OCP, and Hall sensor logic.

Bits	Access	Bit Name	Default	Description

7	N/A	RESERVED	0	Reserved.
6	OTP/REG	WAIT_BH	0	Selects coasting or brake during waiting. 0: Coasting during wait 1: Brake during wait
5	OTP/REG	WAIT_SEL	0	Selects the waiting function at start-up. 0: Coasting until the speed drops below the speed threshold during start-up (default) 1: Coasting for a fixed time during start-up
4	OTP/REG	WAIT_EN	1	Enables wait at start-up. 0: Directly start up without wait 1: Wait until the speed drops to a set threshold or wait for a fixed time during start-up
3	OTP/REG	MOD	0	Selects the SVPWM modulation. 0: 5-segment SVPWM (000 as zero vector) 1: 7-segement SVPWM (000, 111 as zero vector)
2	OTP/REG	OC_RTY	0	Disables entering retry state during OCP. 0: Enter retry state during OCP 1: Do not enter retry state during OCP
1	OTP/REG	HLOGIC	0	Selects the input Hall-effect sensor signal. 0: Differential input 1: High/low logic input
0	N/A	RESERVED	0	Reserved.

CFR_5 (12h)

The CFR_5 command sets OCP, Hall sensor polarity, leading angle interpolation, and lock protection.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OC_RED	0	Enables reduced output duty cycle during OCP. 0: Disabled 1: Enabled
6	N/A	RESERVED	0	Reserved.
5	OTP/REG	HAL_POL	0	Selects the input polarity of the Hall sensor signal. 0: Original 1: Inverse of the input Hall sensor signal.
4	OTP/REG	INTP_EN	1	Enables leading angle linear interpolation. 0: Disable leading angle linear interpolation, where the compensation leading angle is fixed 1: Enable leading angle linear interpolation, where the compensation leading angle varies with the output duty cycle Leading angle = output duty x THETA_COMP This is active only during fixed leading angle compensation.
3	N/A	RESERVED	00	Reserved.
2	OTP/REG	LCK_LF	0	Enables latch-off mode for rotor-lock protection. 0: Disabled 1: Enabled
1	OTP/REG	OCP_LF	0	Enables latch-off mode for OCP. 0: Disabled 1: Enabled
0	N/A	RESERVED	0	Reserved.

APPLICATION INFORMATION

Selecting the VCC Input

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible to maintain a stable input voltage (V_{IN}) and reduce input switching voltage noise and ripple. The impedance of C_{IN} must be low at the switching frequency (f_{SW}).

It is recommended to place an electrolytic capacitor parallel to the ceramic capacitors with X7R dielectrics. The voltage rating must exceed the maximum V_{IN}.

A voltage-clamping TVS diode is recommended to avoid high voltage spikes that result when the energy stored in the motor charges back to C_{IN}.

Selecting the MOSFETs

Six external N-channel MOSFETs are required for normal operation.

The drain-source breakdown voltage of the MOSFETs must exceed the supply voltage. Due to the voltage spike caused by parasitic inductance, the voltage margin must be considered to prevent damage to the MOSFETs being damaged from the voltage spikes. Typically, a minimum 10V to 15V margin is recommended. The voltage spike is related with the PCB layout and current. Additional margin is required for higher-current applications or suboptimal PCB layout.

The on resistance ($R_{DS(ON)}$) refers to the resistance when the MOSFET is fully turned on. A lower $R_{DS(ON)}$ indicates lower power consumption and less generated heat. $R_{DS(ON)}$ must be selected to ensure that the heat can be dissipated safely. An external heat sink or special PCB layout can be used for heat dissipation.

Selecting the External Capacitor

A locally bypass capacitor is required for the VREG pin to provide power for the gate driver. A 1µF or higher ceramic capacitor with X7R or X5R dielectrics is recommended.

The bootstrap (BST) capacitor (C_{BST}) is the power supply for the high-side (HS) gate driver. A 1µF or higher ceramic capacitor with X7R or X5R dielectrics is recommended. In addition, a 2.2Ω or higher resistor in series with C_{BST} is recommended.

Hall Sensor Connection

This operation is based on the Hall sensor signal from the external Hall-effect sensor. The MP6632 supports either the Hall elements with differential inputs or a Hall-sensor IC with high/low logic inputs configured via the register bit HLOGIC.

Hall Elements Connection at HLOGIC = 0

If HLOGIC = 0, the Hall input is selected as differential input, the MP6632 supports Hall elements with differential inputs. The Hall element has two outputs connected to HA+/HB+/HC+ and HA-/HB-/HC- as the differential inputs.

Figure 6 shows the Hall sensors connected in series.

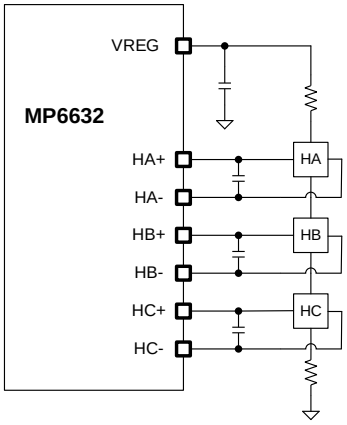


Figure 6: Series Hall Elements Connection

The voltage range of HA+/HB+/HC+ and HA-/HB-/HC- are recommended to be within the Hall sensor's common-mode voltage. Otherwise, the wrong result may occur where the comparator's high output becomes low, or vice versa.

Figure 7 shows the Hall sensors connected in parallel.

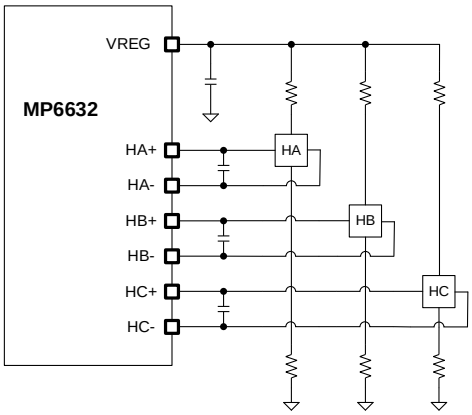


Figure 7: Parallel Hall Elements Connection

The voltage range of HA+/HB+/HC+ and HA-/HB-/HC- must be within the Hall sensor's common-mode voltage. Otherwise, the wrong result may occur where the comparator's high output becomes low, or vice versa.

Figure 8 shows that the supply voltage of the Hall element can be an LDO regulator.

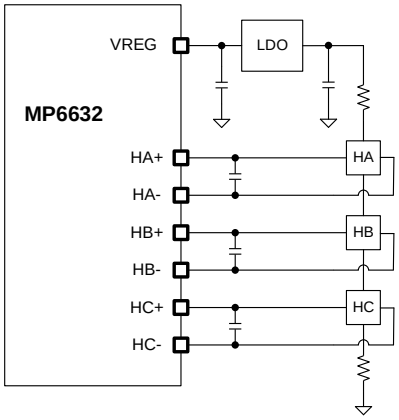


Figure 8: Hall Sensor Supplied by the LDO

Hall-Sensor IC Connection at HLOGIC = 0

In Hall differential input mode, the MP6632 can support a Hall-sensor IC with HA-/HB-/HC- connected to a bias voltage, which must be within the Hall sensor's common-mode voltage.

The voltage range of HA+/HB+/HC+ and HA-/HB-/HC- must also be within the Hall sensor's common-mode voltage. Otherwise, the wrong result may occur where the comparator's high output becomes low, or vice versa.

Figure 9 shows the Hall-sensor IC connection in differential mode.

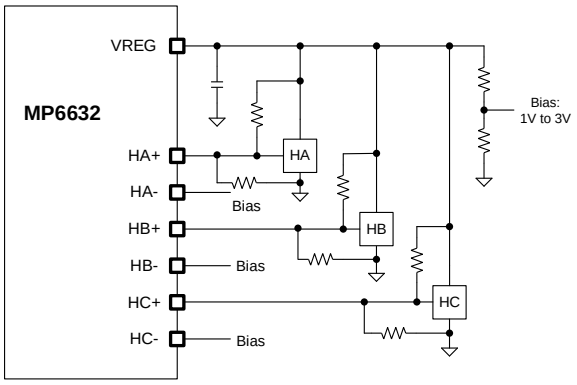


Figure 9: Hall-Sensor IC Connection with Differential Input Mode

Hall-Sensor IC Connection at HLOGIC = 1

If the Hall input mode is configured as the high/low logic input mode via HLOGIC = 1, the Hall-sensor IC is used as the Hall sensor. Connect the Hall-sensor IC's output to HA+/HB+/HC+ and float HA-/HB-/HC-.

Figure 10 shows the Hall-sensor IC connection configured as the Hall sensor high/low logic input.

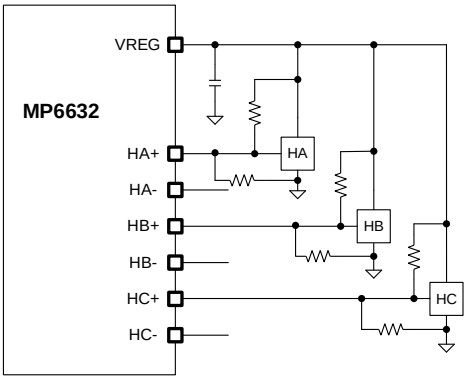


Figure 10: Hall-Sensor IC Connection with High/Low Logic Input Mode

Hall Sensor Placement Example

The MP6632 supports either a single or triple Hall-effect sensor. Consider the Hall sensor placement for a 4-pole, 6-slot motor. There are two conditions to evaluate:

1. When the current flows into the stator phase winding, the south magnetic field is generated (see Figure 11 on page 28).

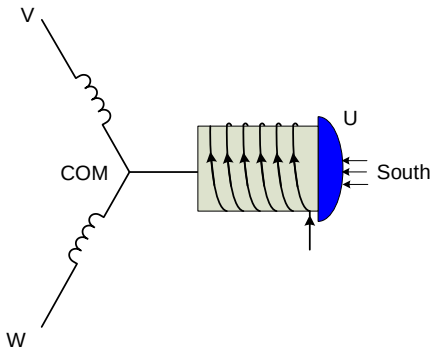


Figure 11: South Magnetic Field with Winding Direction

2. If the Hall sensor output is high when the north pole is close to the Hall sensor's branded side (see Figure 12).

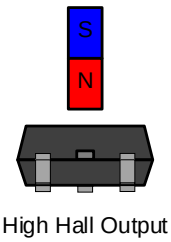


Figure 12: High Hall Output with Approaching North Pole

If either both or none of the conditions are satisfied, then the following Hall sensor placement is recommended:

- Hall A is aligned with phase A and phase C's central lines.
- Hall B is aligned with phase A and phase B's central lines.
- Hall C is aligned with phase B and phase C's central lines.

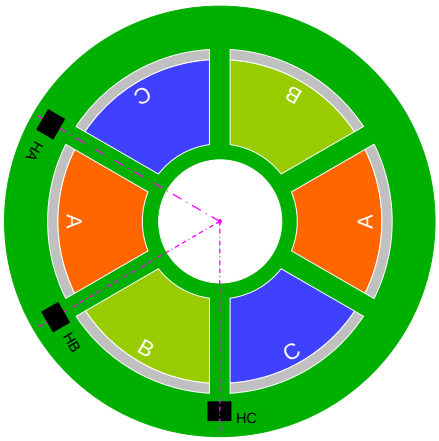


Figure 13: Hall Sensor Placement Option 1

If one of these conditions is not satisfied, then the Hall sensor polarity can be configured to inverse by the register bit HAL_POL using the Hall placements in Figure 13.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and good performance. Refer to Figure 15 and follow the guidelines below:

1. Place C_{IN} as close to the VCC and GND pins as possible.
2. Place the VREG bypass capacitor as close to the VREG and GND pins as possible.
3. Place a capacitor for each Hall input signal to filter the signal from the external Hall sensor. The capacitor must be placed as close to IC as possible.
4. Two-wire routing is recommended. Place the Hall signal's two wires close to each other to avoid noise coupling.
5. Place a capacitor close to the ISEN pin for noise filtering.
6. It is recommended to use a ceramic capacitor for each half bridge to reduce the switching noise and minimize the switching loop trace.
7. Figure 14 shows an example dual MOSFETs with an SOIC-8 package.

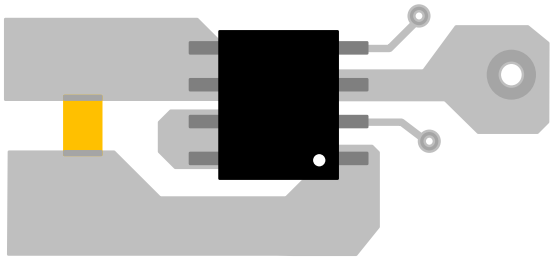


Figure 14: A Bypass Capacitor for Each Half Bridge

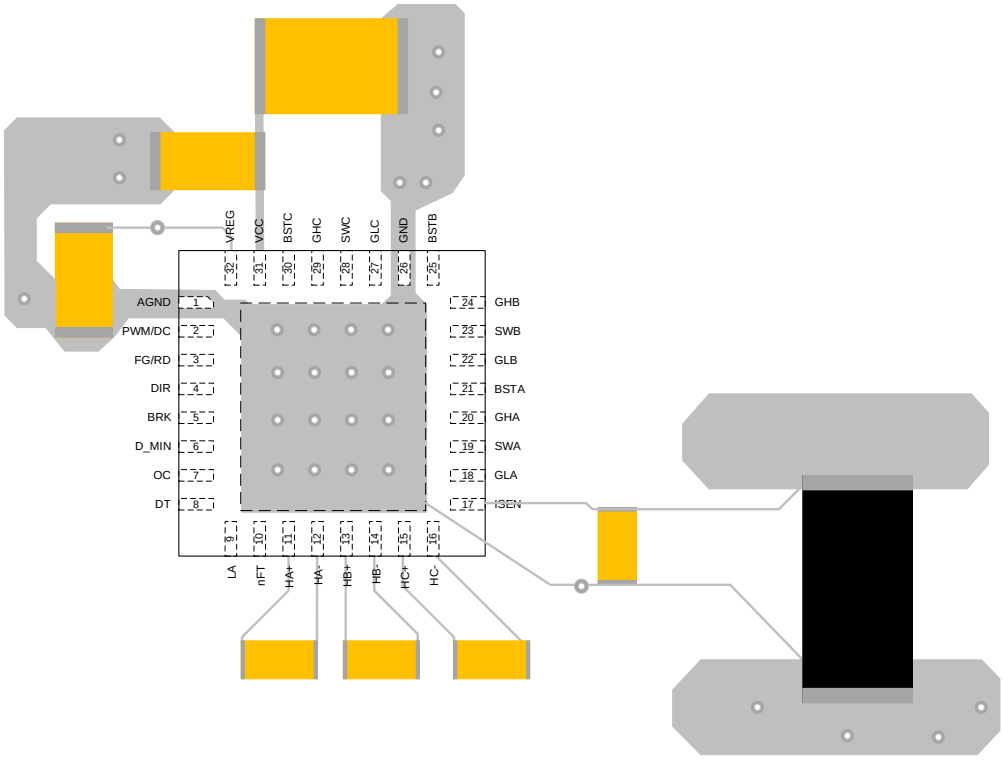


Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

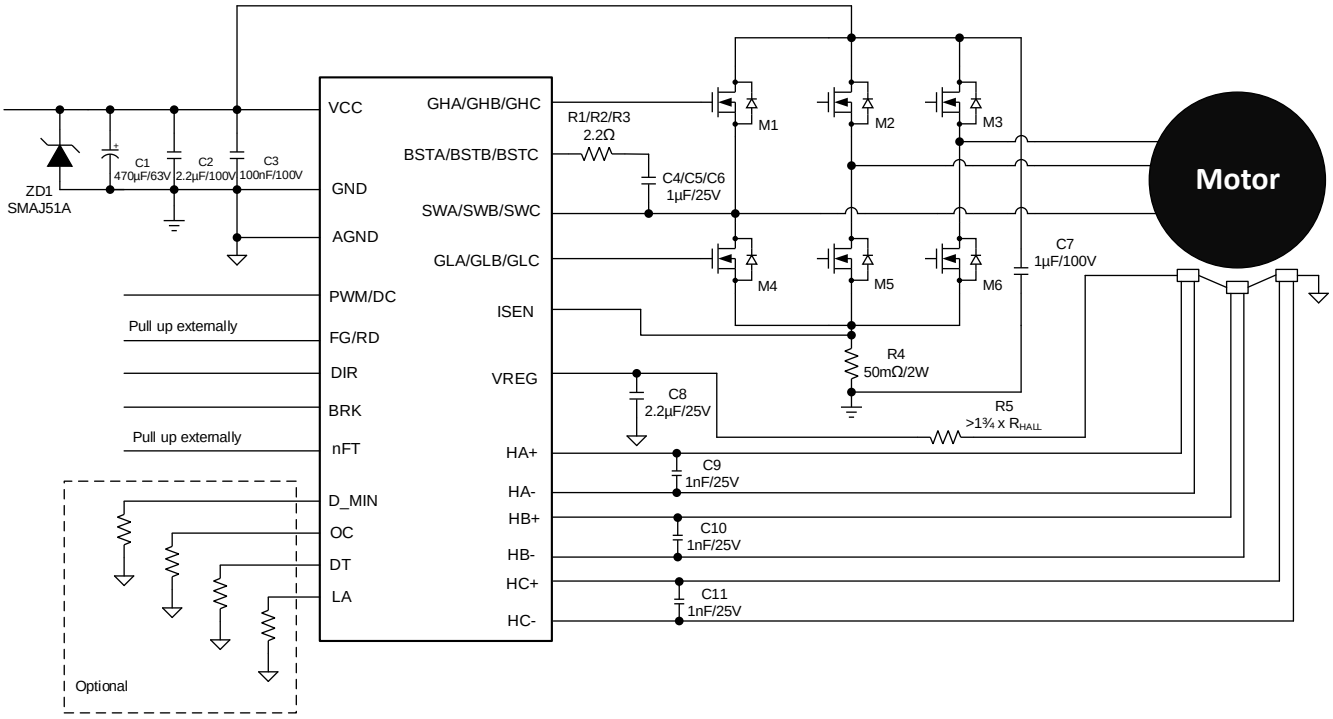
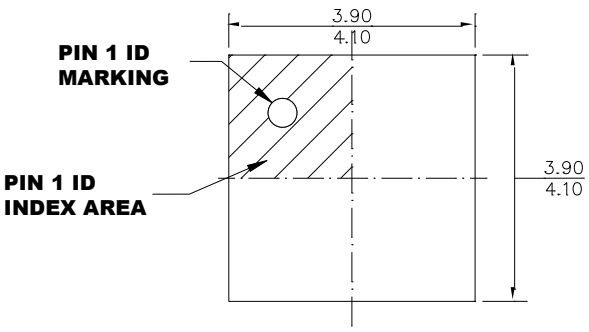


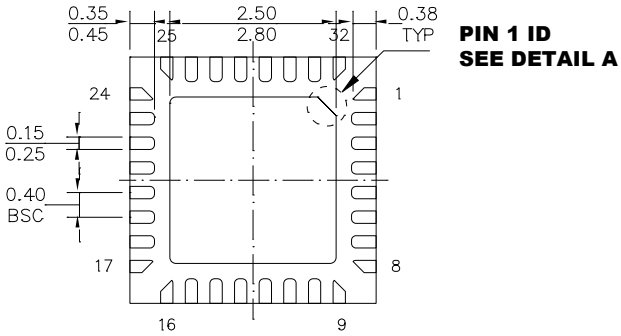
Figure 16: Typical Application Circuit

PACKAGE INFORMATION

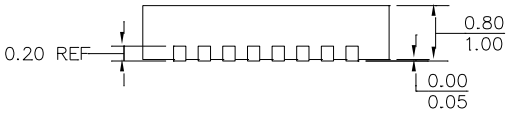
QFN-32 (4mmx4mm)



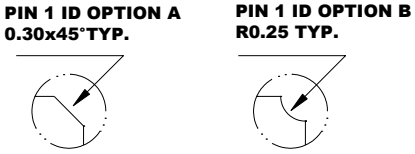
TOP VIEW



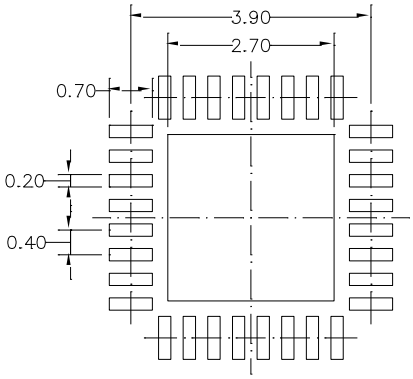
BOTTOM VIEW



SIDE VIEW



DETAIL A

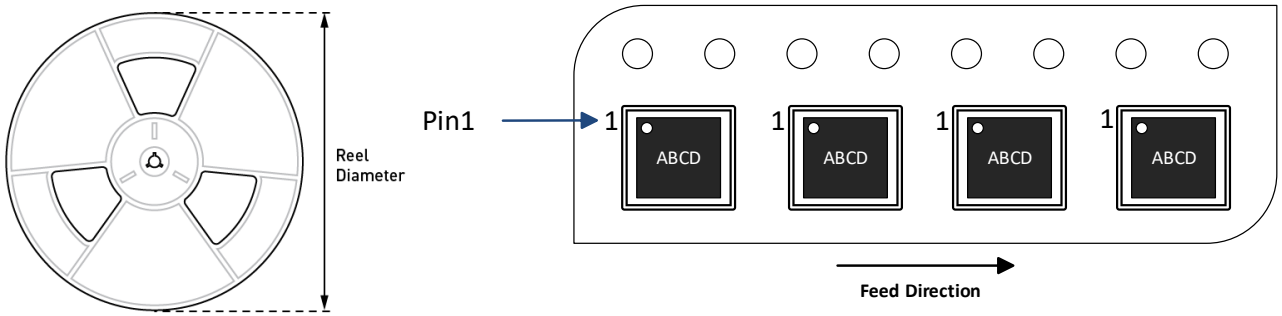


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6632GR-xxxx-Z	QFN-32 (4mmx4mm)	5000	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/7/2023	Initial Release	-