MP6604A

Simple, Dual H-Bridge Motor Driver with Separate Input and Enable Pins

DESCRIPTION

The MP6604A is a dual H-bridge motor driver IC that can drive stepper motors, brushed DC motors, and other loads.

The device operates across a 4.5V to 45V input voltage (V_{IN}) range, and can deliver up to 2.5A of output current (I_{OUT}) per phase.

Internal safety and diagnostic features include over-current protection (OCP), input over-voltage protection (OVP), and input under-voltage lockout (UVLO) protection, and thermal shutdown.

The MP6604A has separate IN and EN pins for each output pin.

The MP6604A is available in QFN-28 (4mmx5mm) and TSSOP-28EP packages.

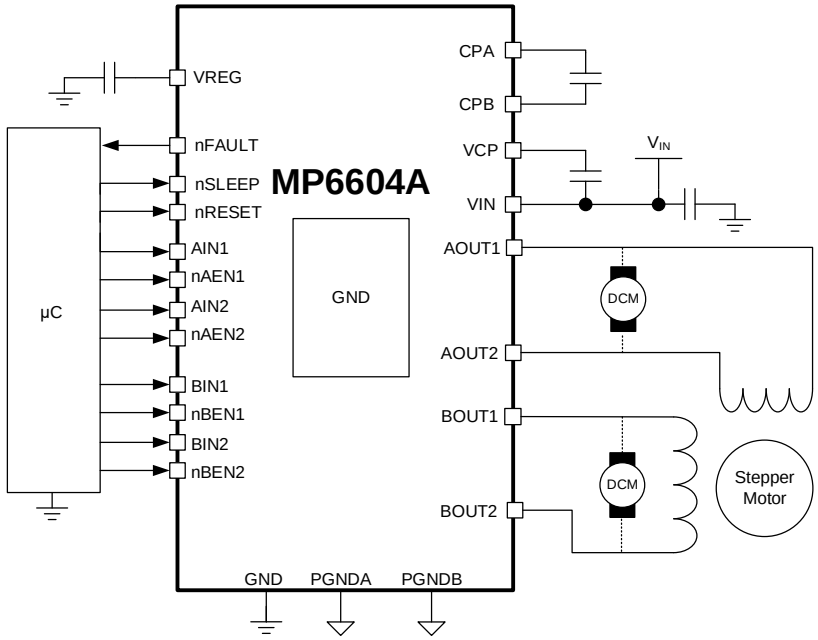
FEATURES

- 4.5V to 45V Operating Input Voltage (V_{IN}) Range
- 2.5A Maximum Output Current (I_{OUT})
- Dual H-Bridge or Quad Half-Bridge Driver
- 150mΩ Low On Resistance (per MOSFET)
- Protection Functions:
  - Over-Current Protection (OCP)
  - Over-Voltage Protection (OVP)
  - Under-Voltage Lockout Protection (UVLO)
  - Thermal Shutdown
  - Fault Indication Output
- Available in QFN-28 (4mmx5mm) and TSSOP-28EP Packages

APPLICATIONS

- Bipolar Stepper Motors
- Stage Lighting
- 3D Printers
- Laser Printers and Copiers
- Textile Machines

TYPICAL APPLICATION

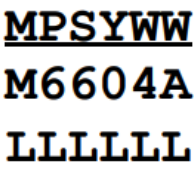


ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6604AGV	QFN-28 (4mmx5mm)	*See Below*	2
MP6604AGF	TSSOP-28EP	*See Below*	2a

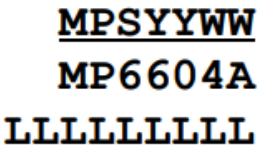
* For Tape & Reel, add suffix -Z (e.g. MP6604AGV-Z).

TOP MARKING (MP6604AGV)



MPS: MPS prefix
Y: Year code
WW: Week code
M6604A: Part number
LLLLLL: Lot number

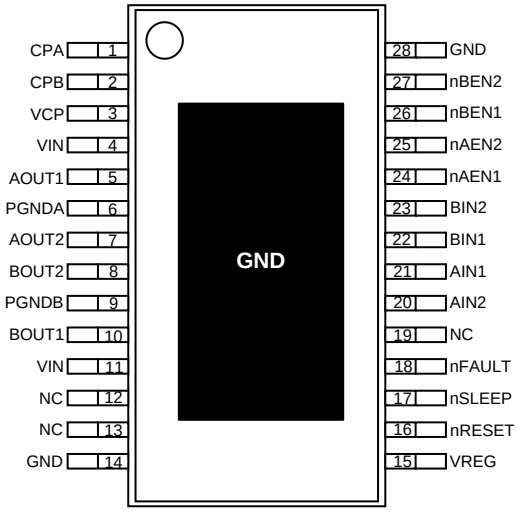
TOP MARKING (MP6604AGF)



MPS: MPS prefix
YY: Year code
WW: Week code
MP6604A: Part number
LLLLLLLLL: Lot number

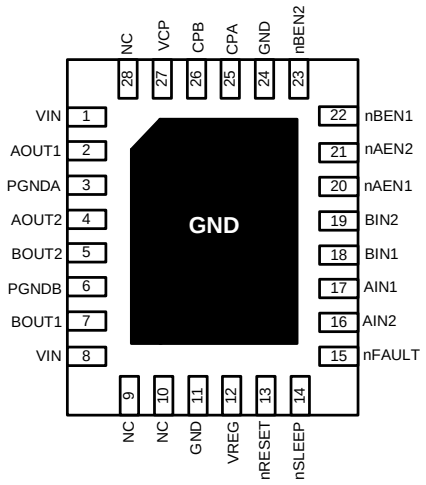
PACKAGE REFERENCE

TOP VIEW



MP6604AGF
TSSOP-28EP

TOP VIEW



MP6604AGV
QFN-28 (4mmx5mm)

PIN FUNCTIONS

Pin #		Name	Description
QFN-28 (4mmx 5mm)	TSSOP-28EP		
1, 8	4, 11	VIN	**Input supply voltage.** Decouple the VIN pin to ground using a ≥100nF ceramic capacitor. Additional bulk capacitance may be required.
2	5	AOUT1	**Bridge A output terminal 1.**
3	6	PGNDA	**Power ground for H-bridge A outputs.**
4	7	AOUT2	**Bridge A output terminal 2.**
5	8	BOUT2	**Bridge B output terminal 2.**
6	9	PGNDB	**Power ground for H-bridge B outputs.**
7	10	BOUT1	**Bridge B output terminal 1.**
11, 24	14, 28	GND	**Signal ground.**
12	15	VREG	**Internal regulator.** Connect a 1µF ceramic capacitor with X7R dielectrics between the VREG and GND pins. This capacitor should be rated for ≥16V.
13	16	nRESET	**Reset input.** Pull the nRESET pin low to reset the protection circuits and disable the outputs. nRESET has an internal pull-down resistor.
14	17	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin low to enter low-power sleep mode. nSLEEP has an internal pull-down resistor.
15	18	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. nFAULT requires an external pull-up resistor if used. If a fault occurs, nFAULT is pulled low.
16	20	AIN2	**Control input of AOUT2.** The AIN2 pin has an internal pull-down resistor.
17	21	AIN1	**Control input of AOUT1.** The AIN1 pin has an internal pull-down resistor.
18	22	BIN1	**Control input of BOUT1.** The BIN1 pin has an internal pull-down resistor.
19	23	BIN2	**Control input of BOUT2.** The BIN2 pin has an internal pull-down resistor.
20	24	nAEN1	**AOUT1 enable.** Pull nAEN1 low to enable the corresponding output (AOUT1). nAEN1 has an internal pull-down resistor.
21	25	nAEN2	**AOUT2 enable.** Pull nAEN2 low to enable the corresponding output (AOUT2). nAEN2 has an internal pull-down resistor.
22	26	nBEN1	**BOUT1 enable.** Pull nBEN1 low to enable the corresponding output (BOUT1). nBEN1 has an internal pull-down resistor.
23	27	nBEN2	**BOUT2 enable.** Pull nBEN2 low to enable the corresponding output (BOUT2). nBEN1 has an internal pull-down resistor.
25	1	CPA	**Charge pump capacitor terminal A.** Connect a 100nF ceramic capacitor rated for the input voltage (V_{IN}) between the CPA and CPB pins.
26	2	CPB	**Charge pump capacitor terminal B.** Connect a 100nF ceramic capacitor rated for V_{IN} between the CPA and CPB pins.
27	3	VCP	**Charge pump output.** Connect a 1µF ceramic capacitor between the VCP and VIN pins. This capacitor should be rated for ≥16V.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +48V
V_{AOUT1}, V_{AOUT2}, V_{BOUT1}, V_{BOUT2}.....-0.7V to +48V
V_{CP}, V_{CPB} ..... …V_{IN} to V_{IN} + 6.5V
PGNDx to GND.....-0.3V to +0.3V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-28 (4mmx5mm)…….3.125W
TSSOP-28EP……..……...3.9W
Storage temperature..... -55°C to +150°C
Junction temperature (T_J) .....150°C
Lead temperature (solder) .....260°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM).....±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4.5V to 45V
PGNDx to GND.....-0.2V to +0.2V
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm).....40.....9.....°C/W
TSSOP-28EP.....32.....6.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input voltage	V_{IN}		4.5		45	V
Quiescent current	I_Q	nSLEEP is high, no load		2.8		mA
Sleep mode I_Q	I_{SLEEP}	nSLEEP is low		0.9	10	µA
Internal MOSFETs						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	I_{OUT} = 1A, T_J = 25°C		135	170	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	I_{OUT} = 1A, T_J = 25°C		150	185	mΩ
Body diode forward voltage	V_F	I_{OUT} = 1A			1.1	V
Control Logic Inputs						
Input logic low voltage	V_{IL}				0.8	V
Input logic high voltage	V_{IH}		2			V
Input logic high current	I_{IN_H}	V_{IN} = 5V	-100		+100	µA
Input logic low current	I_{IN_L}	V_{IN} = 0V	-20		+20	µA
Internal pull-down resistance	R_{PD}	Pulled down to GND		100		kΩ
nFAULT Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 5V			1	µA
Protection Circuits						
V_{IN} under-voltage lockout (UVLO) rising threshold	V_{UVLO}				4.5	V
V_{IN} UVLO hysteresis	ΔV_{UVLO}			300		mV
V_{IN} over-voltage protection (OVP) threshold	V_{OVP}		45		48	V
Over-current protection (OCP) threshold	I_{OCP1}	Sink	3	4.5		A
	I_{OCP2}	Source	3	4.5		A
OCP deglitch time	t_{OCP}			1		µs
Thermal shutdown threshold	T_{TSD}			165		°C
Thermal shutdown hysteresis	ΔT_{TSD}			15		°C
Timing						
AINx/BINx high to AOUTx/ BOUTx high delay time	t1		40		360	ns
AINx/BINx low to AOUTx/ BOUTx low delay time	t2		40		360	ns
Output rise time	t3		1		55	ns
Output fall time	t4		1		165	ns
Dead time (DT)					80	ns

TIMIMG DIAGRAM (5)

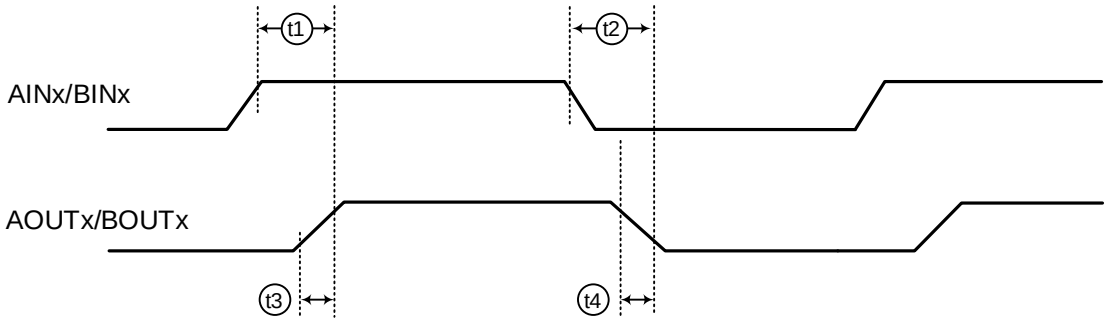


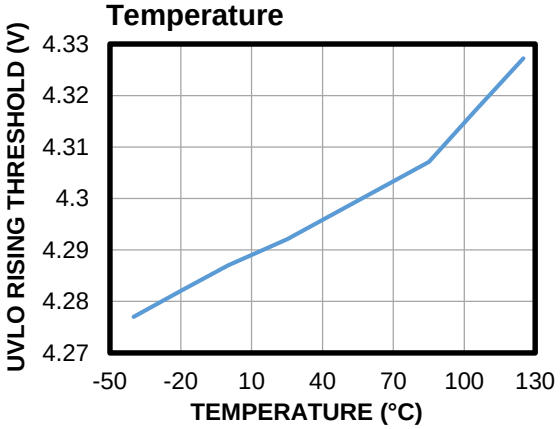
Figure 1: Timing Diagram

Note:

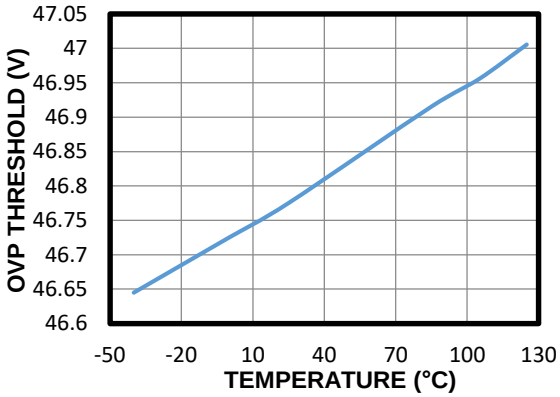
5) V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

TYPICAL CHARACTERISTICS

UVLO Rising Threshold vs. Temperature

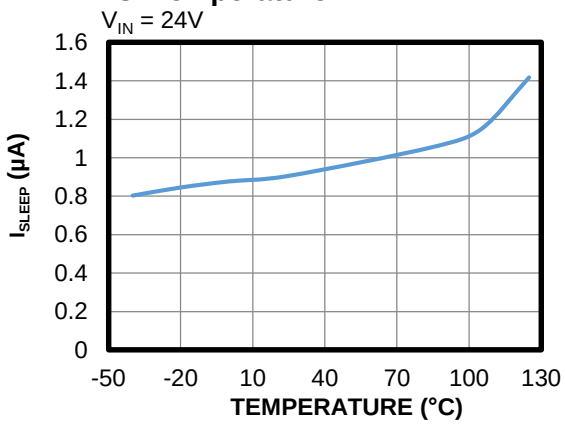


OVP Threshold vs. Temperature



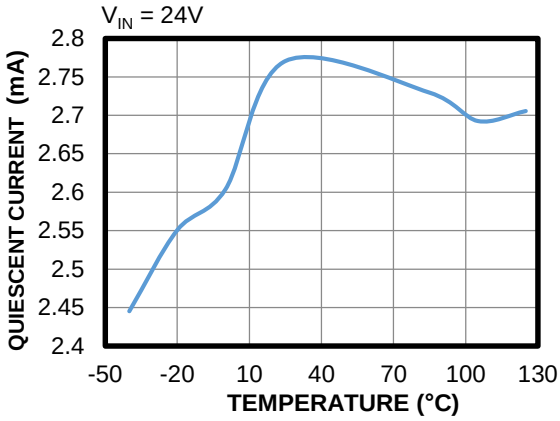
Sleep Mode Quiescent Current vs. Temperature

V_{IN} = 24V



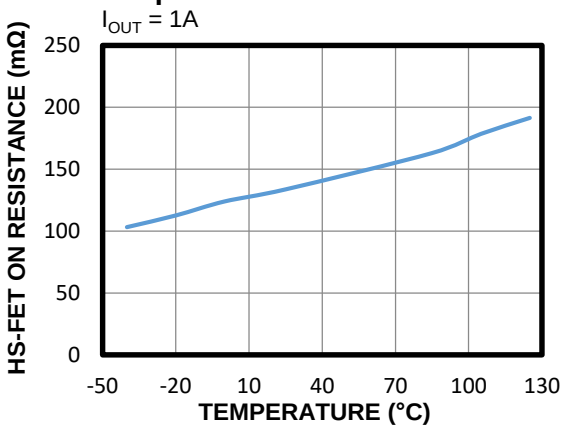
Quiescent Current vs. Temperature

V_{IN} = 24V



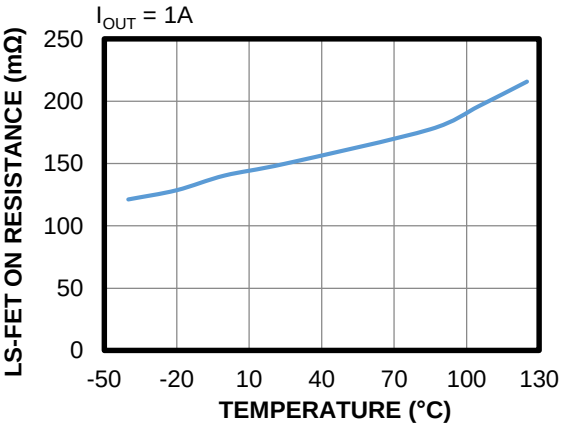
HS-FET On Resistance vs. Temperature

I_{OUT} = 1A



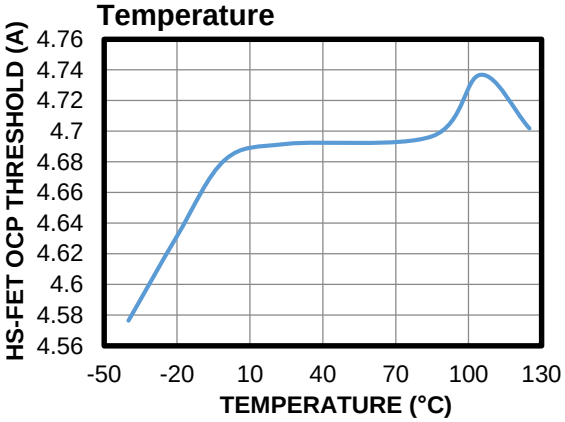
LS-FET On Resistance vs. Temperature

I_{OUT} = 1A

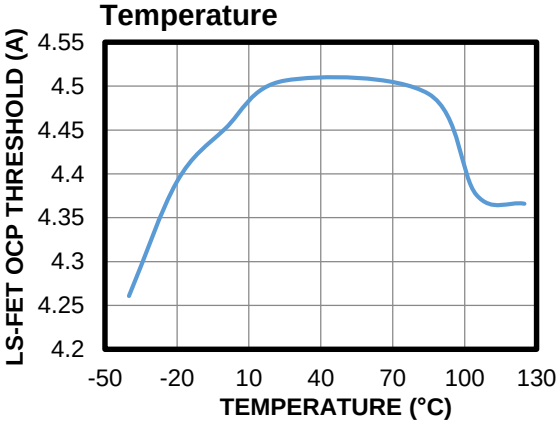


TYPICAL CHARACTERISTICS *(continued)*

HS-FET OCP Threshold vs. Temperature



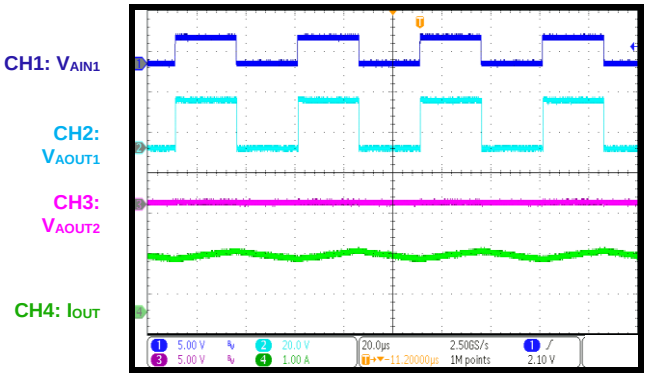
LS-FET OCP Threshold vs. Temperature



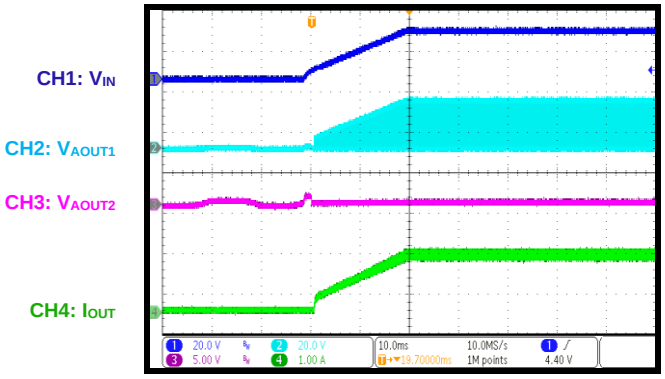
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, AOUT1 is enabled, f_{SW} = 20kHz, AOUT2's LS-FET is on, T_A = 25°C, resistor + inductance = 8Ω + 1.5mH between AOUT1 and AOUT2, unless otherwise noted.

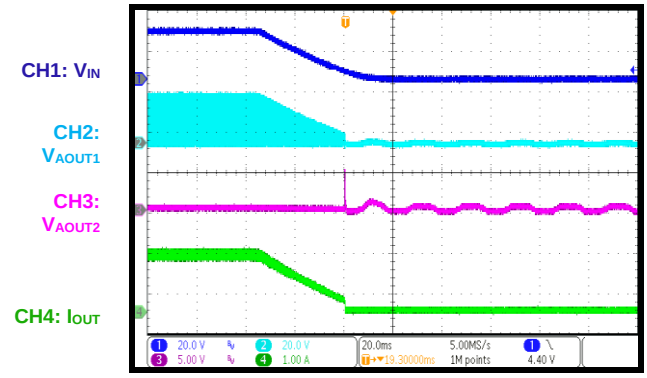
Steady State
50% duty cycle



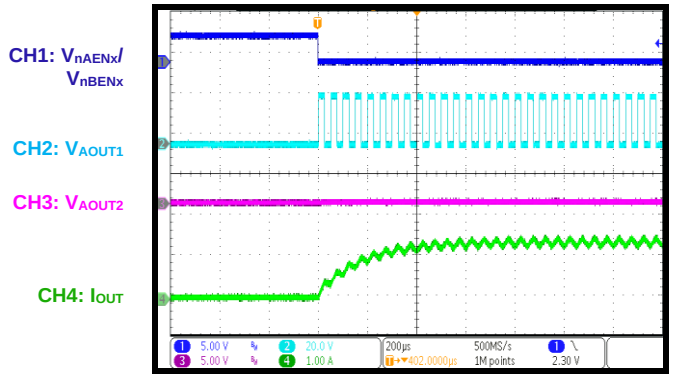
Power Ramps Up
50% duty cycle



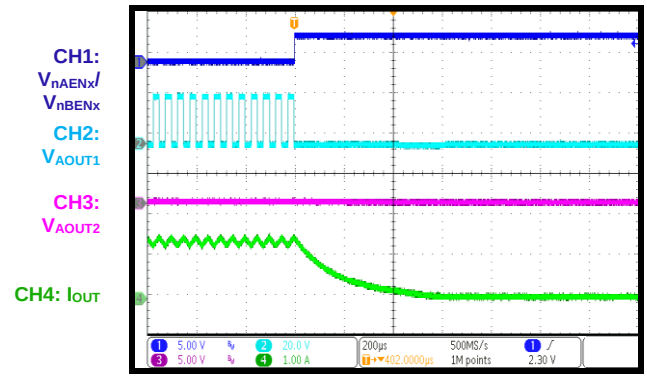
Power Ramps Down
50% duty cycle



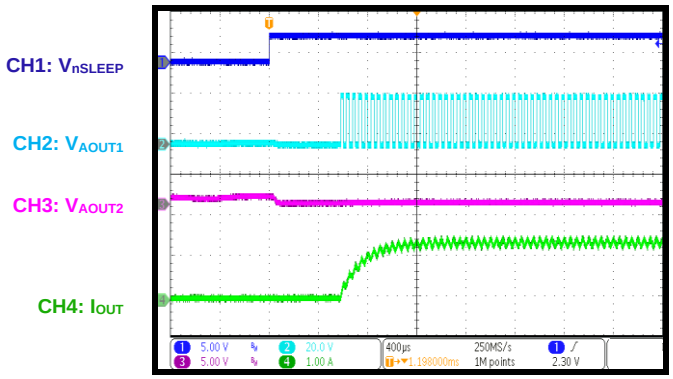
Start Up through nAENx/nBENx
50% duty cycle



Shutdown through nAENx/nBENx
50% duty cycle



Sleep Mode Recovery
50% duty cycle

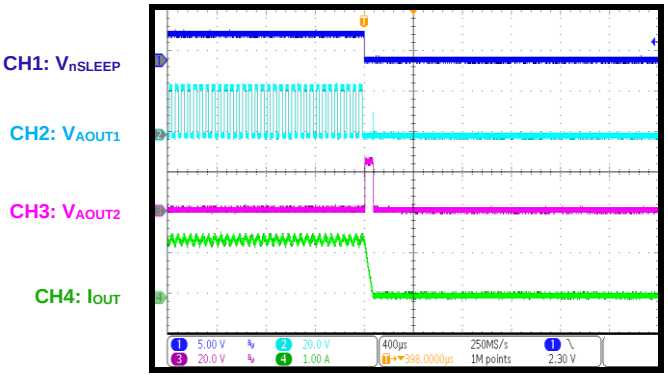


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, AOUT1 is enabled, f_{SW} = 20kHz, AOUT2's LS-FET is on, T_A = 25°C, resistor + inductance = 8Ω + 1.5mH between AOUT1 and AOUT2, unless otherwise noted.

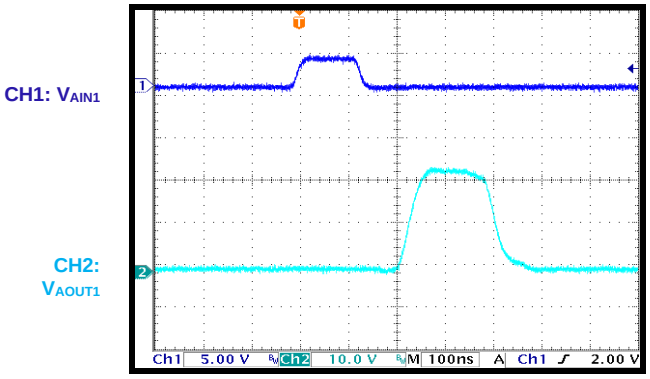
Sleep Mode Entry

50% duty cycle



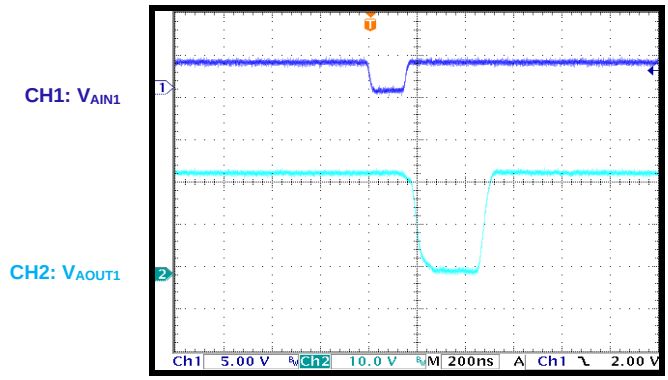
HS-FET Minimum On Time

No load



LS-FET Minimum On Time

No load



FUNCTIONAL BLOCK DIAGRAM

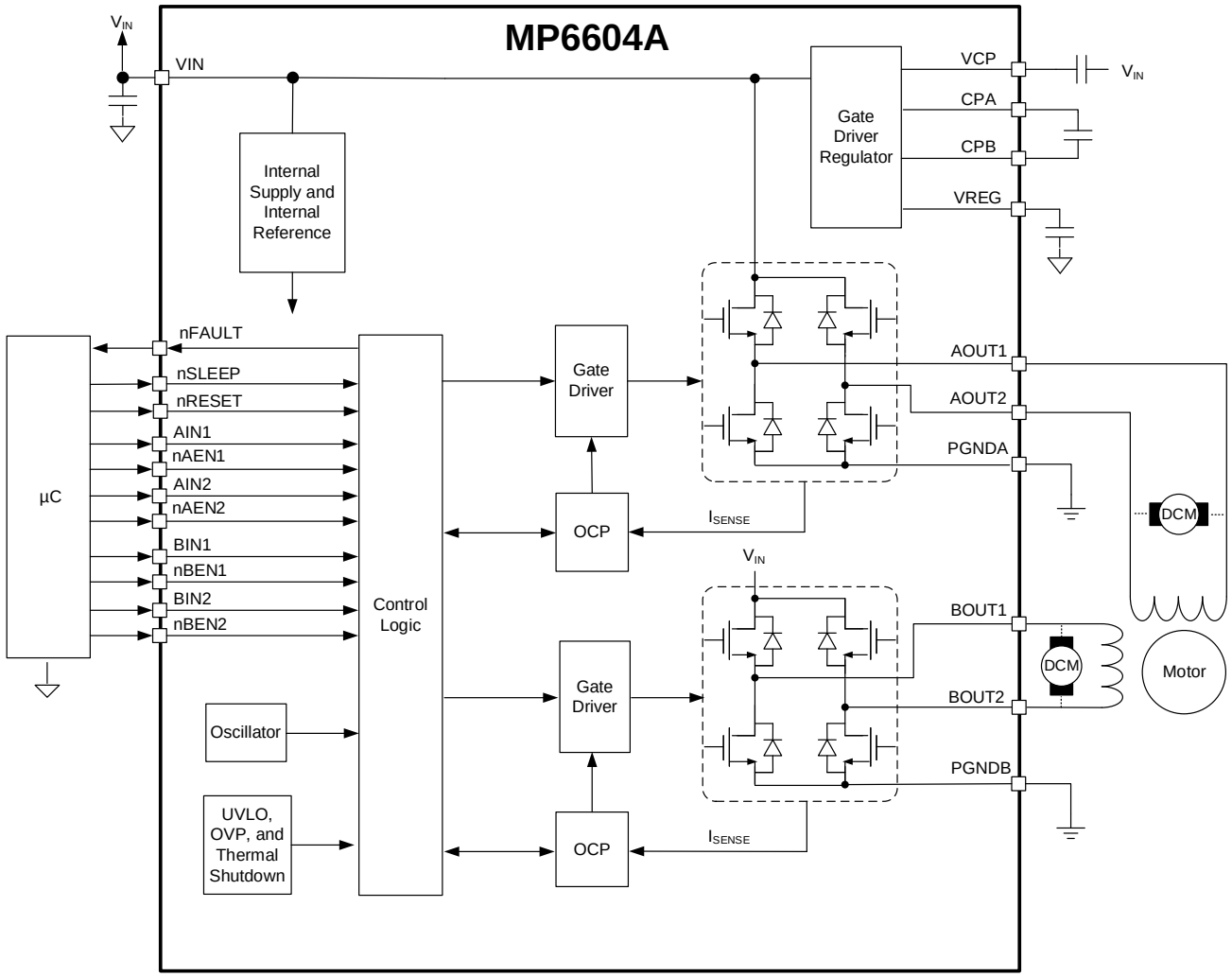


Figure 2: Functional Block Diagram

OPERATION

The MP6604A is a general-purpose dual H-bridge motor driver that integrates eight N-channel power MOSFETs connected as four half H-bridges, with a 2.5A current capability. It operates across a wide 4.5V to 45V input voltage (V_{IN}) range.

The MP6604A is designed to drive bipolar stepper motors, brushed DC motors, solenoids, or other loads.

nSLEEP and nRESET Operation

Pull nSLEEP low to have the device enter low-power sleep mode. In sleep mode, the gate driver charge pump turns off, and all of the internal circuitry and H-bridge outputs are disabled. All of the inputs are ignored while nSLEEP is pulled low.

There is a delay time (600µs) between when the part exits sleep mode and when the part starts driving the motor to allow the internal circuitry to stabilize. The nSLEEP pin has an internal pull-down resistor.

Pull nRESET low to reset a latched protection [e.g. over-current protection (OCP) or over-voltage protection (OVP)] and to have the outputs enter a high-impedance (Hi-Z) state.

Input Interface

The MP6604A integrates four half H-bridges that operate independently from one another.

Each output has its own input (AINx/BINx) and enable (AENx/BENx) pins for each output pin (AOUTx/BOUTx). Table 2 shows the MP6604A's pin logic.

Table 2: MP6604A Pin Logic

AENx/ BENx	AINx/ BINx	AOUTx/ BOUTx
High	x (6)	Hi-Z
Low	Low	Low
Low	High	High

All of the logic inputs have internal pull-down resistors.

Note:

6) "x" denotes high or low.

Automatic Synchronous Rectification

If both the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) are off, recirculation current should continue to flow while driving current through an inductive load. This current passes through the MOSFET body diodes. The MP6604A employs automatic synchronous rectification to reduce excess power dissipation in the body diodes.

If both the HS-FET and LS-FET are off, and the voltage on an AOUTx/BOUTx (V_{AOUTx}/V_{BOUTx}) pin is pulled below GND, then the LS-FET turns on until its current reaches 0A, or until the HS-FET is commanded to turn on. Similarly, if V_{AOUTx}/V_{BOUTx} exceeds V_{IN}, then the HS-FET turns on until its current reaches 0A, or until the LS-FET is commanded to turn on.

Internal Supplies (VREG and VCP)

The internal regulator (VREG) provides a 5V supply for the low-side (LS) gate driver. The other internal regulator (VCP) provides a supply 5V above V_{IN} for the high-side (HS) gate driver. VREG and VCP require external capacitors.

Connect a 1µF capacitor between the VREG pin and GND. Connect a 1µF capacitor between the VCP and VIN pins. Both capacitors should have X7R dielectrics, and should be rated for ≥16V.

The charge pump's flying capacitor (connected between the CPA and CPB pins) should be a 100nF ceramic capacitor with X7R dielectrics, and should be rated for at least the maximum V_{IN}.

Fault Reporting

The MP6604A's nFAULT pin reports whether an over-current (OC), over-temperature (OT), or over-voltage (OV) fault has occurred. nFAULT is an open-drain output that is pulled low if a fault occurs. If used, nFAULT should be pulled high via an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry disables the gate driver to limit the current flowing through the MOSFETs. If the current exceeds the OCP threshold for longer

than the OCP deglitch time (t_{OCP}), then all of the MOSFETs in the H-bridge are disabled, and nFAULT is pulled low. The driver turns on again once the device is reset by pulling the nRESET pin low, or by cycling the power on VIN. An OC fault on either the HS-FET or LS-FET (e.g. an excessive current to ground, to the supply, or across the motor winding) can cause an OC shutdown.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the OVP threshold, then the H-bridge output is disabled, and nFAULT is pulled low. The driver turns on again once the device is reset by pulling the nRESET pin low, or by cycling the power on VIN.

V_{IN} Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops below the under-voltage lockout (UVLO) threshold, then all of the IC's circuitry is disabled, and the internal logic is reset. Once V_{IN} exceeds the UVLO threshold, the part resumes normal operation.

Thermal Shutdown

If the die temperature the thermal shutdown threshold (165°C), then all of the MOSFETs in the H-bridge are disabled, and nFAULT is pulled low. Once the die temperature drops to 150°C, the part resumes normal operation .

APPLICATION INFORMATION

External Component Selection

Bypass the VIN pins to GND using a ≥100nF ceramic capacitor with X7R dielectrics. Place this capacitor as close to the IC as possible. Place an additional 1µF to 10µF ceramic capacitor near the ≥100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an additional electrolytic bulk capacitor may be required to stabilize V_{IN}.

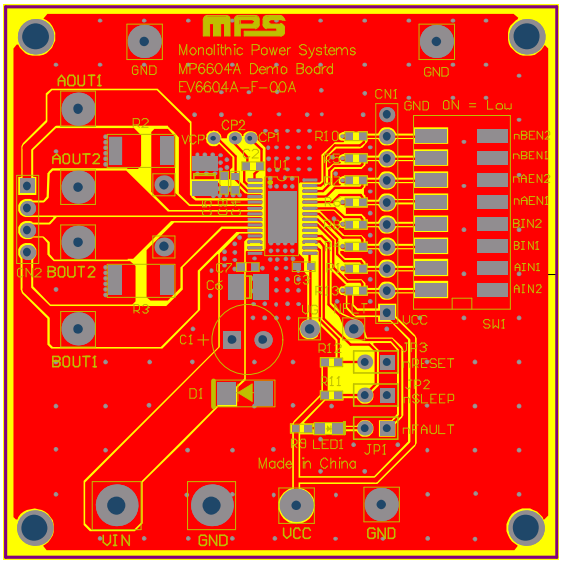
Connect a 100nF ceramic capacitor rated for V_{IN} between the CPA and CPB pins. Connect a 1µF ceramic capacitor between the VIN and VCP pins. This capacitor should be rated for ≥16V.

Connect a 1µF ceramic capacitor with X7R dielectrics between the VREG and GND pins. This capacitor should be rated for ≥16V.

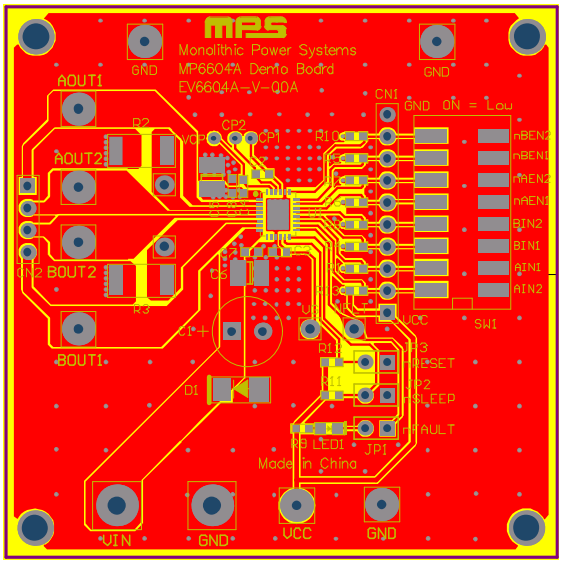
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the VIN bypass capacitor and charge pump capacitor as close to the IC as possible. Place these capacitors adjacent to the pins on the same PCB layer. Each VIN pin should have a bypass capacitor.
2. Place as much copper as possible on the long pads.
3. Place large copper areas on the pads, on the same outer copper layer as the device.
4. Solder the thermal pad directly to the copper on the PCB.
5. Add multiple thermal vias to improve thermal dissipation.



Recommended PCB Layout for the MP6604AGF



Recommended PCB Layout for the MP6604AGV

Figure 3: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

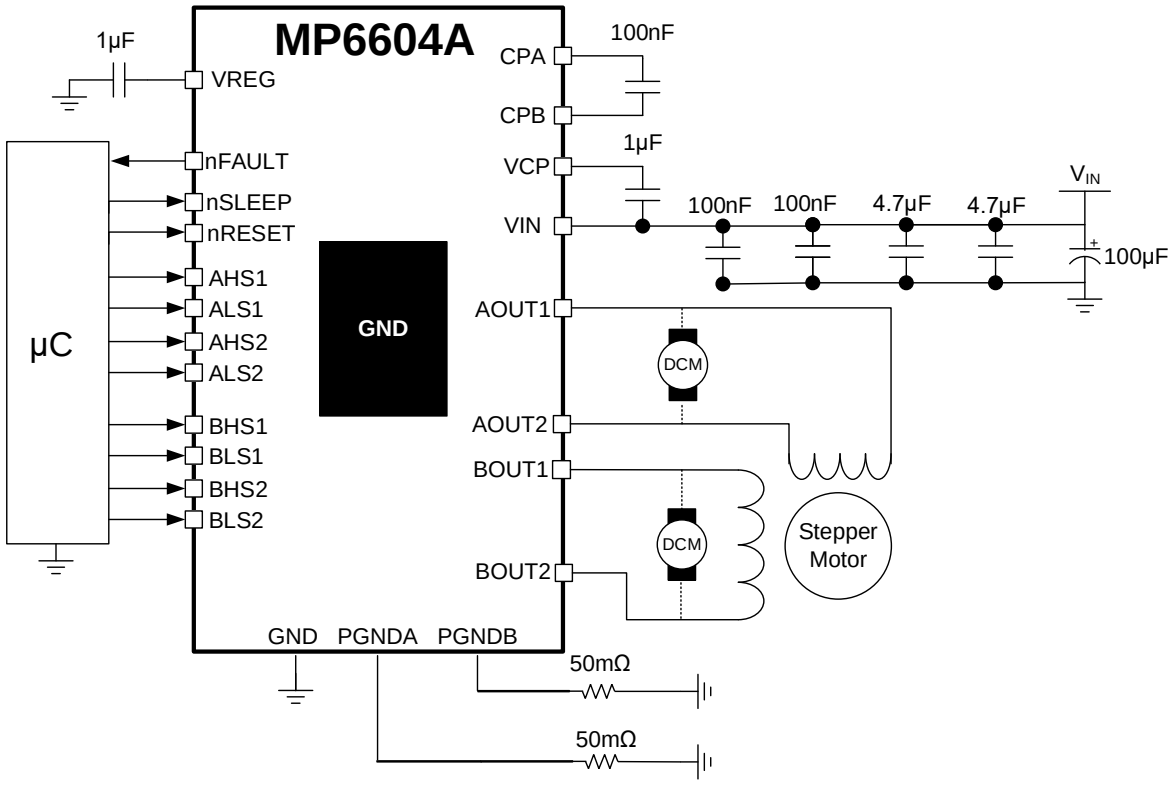
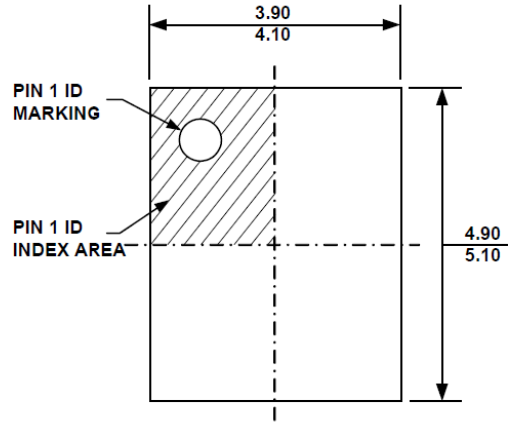


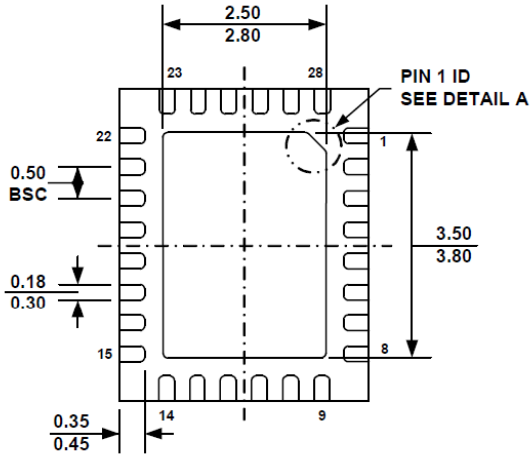
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

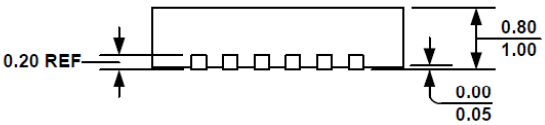
QFN-28 (4mmx5mm)



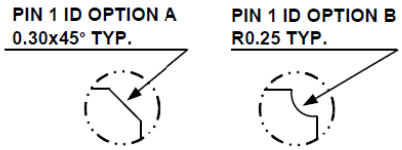
TOP VIEW



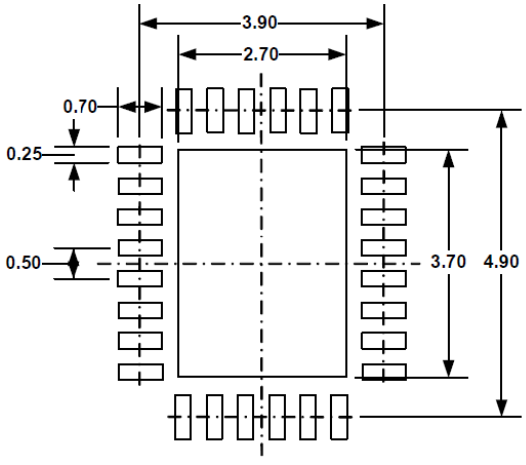
BOTTOM VIEW



SIDE VIEW



DETAIL A



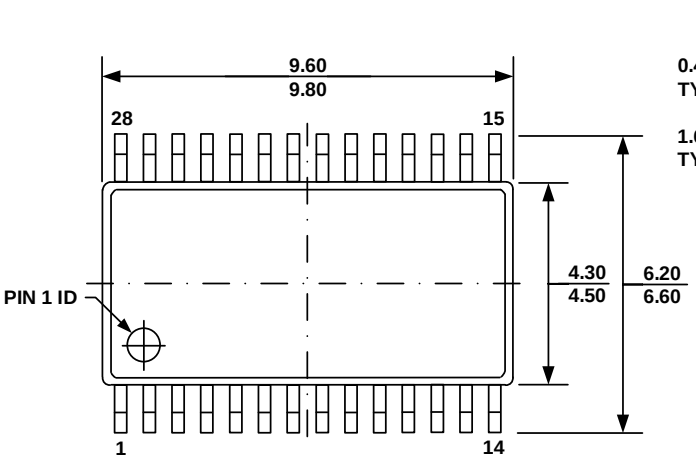
RECOMMENDED LAND PATTERN

NOTE:

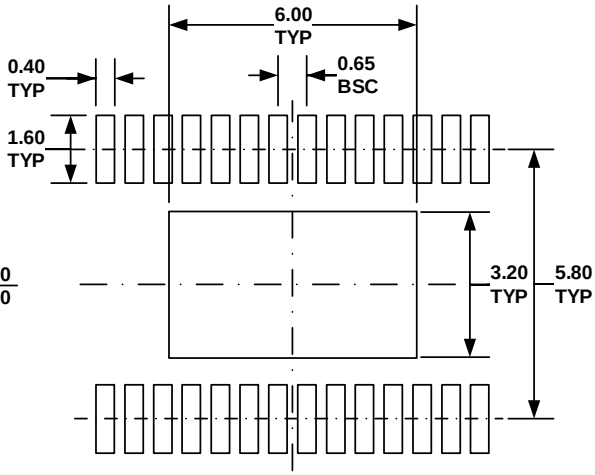
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VHGD-3.
5) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

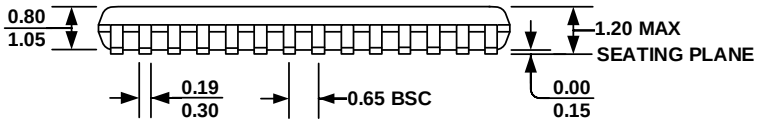
TSSOP-28EP



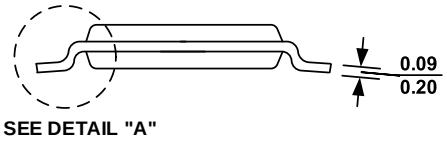
TOP VIEW



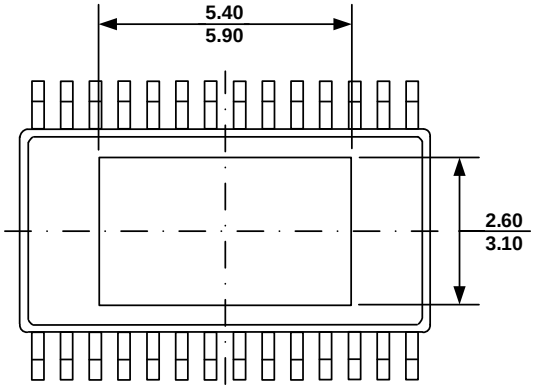
RECOMMENDED LAND PATTERN



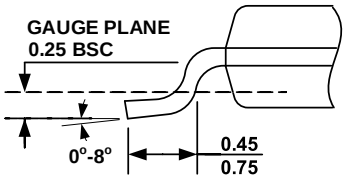
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

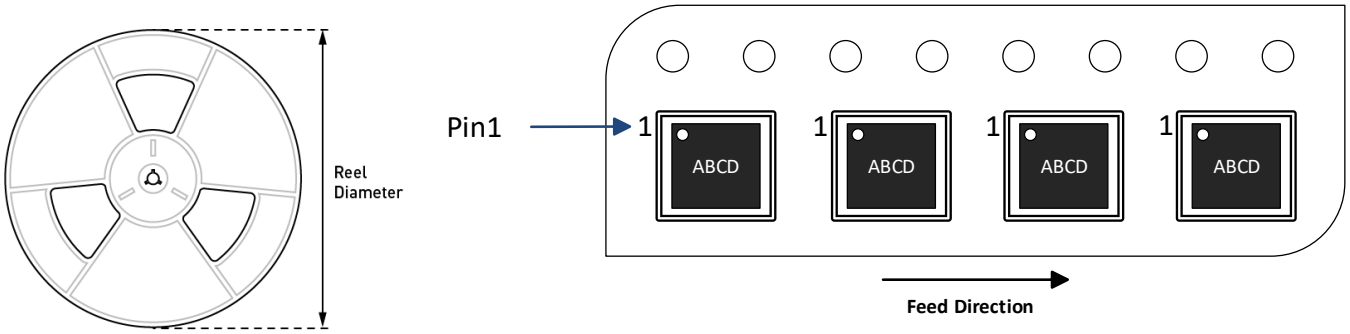


DETAIL “A”

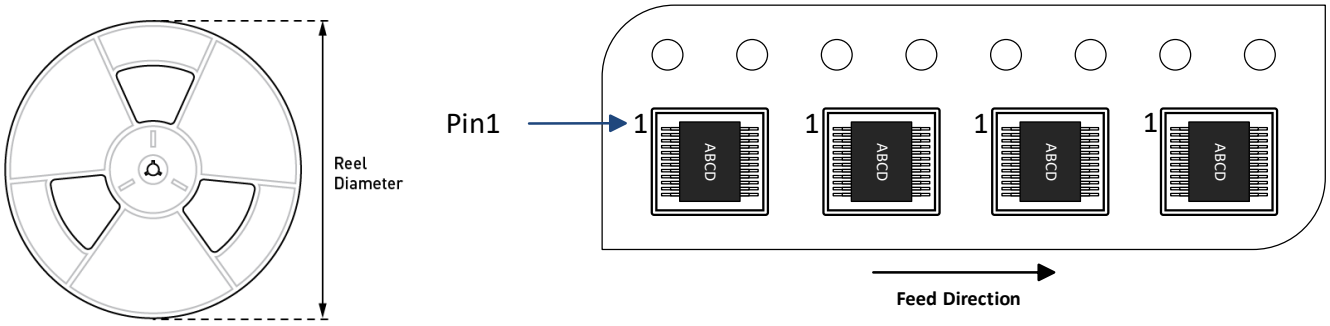
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITIES (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.1 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6604AGV-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6604AGF-Z	TSSOP-28EP	2500	50	N/A	13in	16mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/20/2022	Initial Release	-
1.1	5/12/2023	Updated the MSL rating for the MP6604AGV to “2” in the Ordering Information section	2