MP5098A

Dual E-Fuse with SAS Function and Reverse Current Blocking

DESCRIPTION

The MP5098A is a dual 5V/12V e-fuse that protects circuitry on the output from transients on the input. It also prevents shorts at the output and limits the input inrush current during system start-up.

The SAS and EN pins control the dual e-fuse's on/off logic. For each channel, the SS pin controls the device's start-up time. The reverse current blocking function is integrated for 5V devices. The maximum load at the output is current-limited. The current limit magnitude is internally fixed and can be trimmed.

An internal, integrated low-dropout (LDO) regulator provides 5V/10mA load capability for system use.

The MP5098A requires a minimal number of external components and is available in a space-saving TQFN-10 (2mmx3mm).

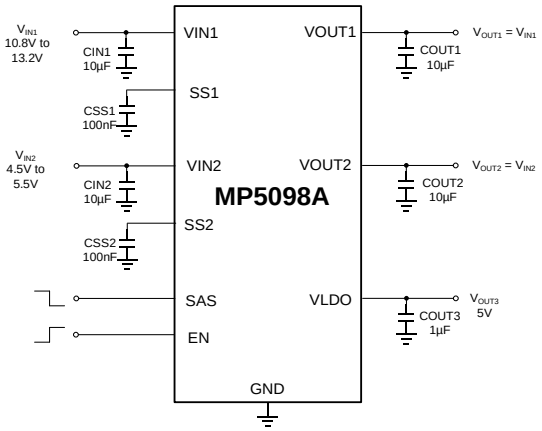
FEATURES

- Integrated 5V/12V Input Dual E-Fuse
- Up to 18V Absolute Maximum Input Voltage (V_{IN}) for Both E-Fuses
- Reverse Current Blocking for the 5V Channel
- Negative Voltage Protection for Both E-Fuses
- Integrated, Dual-Channel Current Limit Switch
- Low 44mΩ On Resistance ($R_{DS(ON)}$) for Both Power FETs
- 3A, ±10% Current Limit for 5V V_{IN} Channel
- 4.5A, ±10% Current Limit for 12V V_{IN} Channel
- 5.7V Typical Over-Voltage Protection (OVP) Threshold for 5V V_{IN} Channel
- 15V Typical OVP Threshold for 12V V_{IN} Channel
- Integrated 10mA Low-Dropout (LDO) Regulator
- Latch-Off Thermal Shutdown
- Available in a TQFN-10 (2mmx3mm) Package

APPLICATIONS

- Hard Disk Drives (HHDs)
- Solid-State Drives (SSDs)
- Hot-Swap Applications

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5098AGDT	TQFN-10 (2mmx3mm)	*See Below*	1

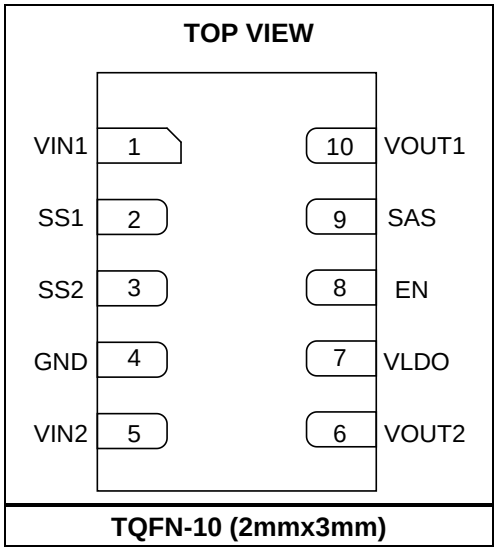
* For Tape & Reel, add suffix -Z (e.g. MP5098AGDT-Z).

TOP MARKING

BLF
YWW
LLL

BLF: Product code of MP5098AGDT
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



TQFN-10 (2mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN1	**Channel 1 supply voltage.** The typical input voltage (V_{IN}) of channel 1 is 12V. A ceramic capacitor is required to decouple the input rail. Connect VIN1 using a wide PCB trace.
2	SS1	**Channel 1 soft start pin.** Connect a capacitor from SS1 to ground to set the soft-start time (t_{SS}).
3	SS2	**Channel 2 soft start pin.** Connect a capacitor from SS2 to ground to set t_{SS}.
4	GND	**System ground.**
5	VIN2	**Channel 2 supply voltage.** The typical V_{IN} of channel 2 is 5V. A ceramic capacitor is required to decouple the input rail. Connect VIN2 using a wide PCB trace.
6	VOUT2	**Channel 2 output terminal**
7	VLDO	**Output terminal for the internal, 5V LDO.**
8	EN	**Enable pin for both channel 1 and channel 2.** EN is a digital input that turns the e-fuses on or off. Float EN or pull EN high to turn on the e-fuses; drive it low to turn off the e-fuses.
9	SAS	**SAS control pin.** Pull this pin logic active low. When EN and SAS are both pulled high, the e-fuses are forced to turn off.
10	VOUT1	**Channel 1 output terminal.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN1}, V_{OUT1} ..... -0.3V to +18V
Negative input transient (1ms) ..... -3V
Positive input transient (100ms) 22V
V_{IN2}, V_{OUT2} ..... -0.3V to +18V
All other pins..... -0.3V to +7V
Junction temperature ..... -40°C to +150°C
Lead temperature ..... 260°C
Continuous power dissipation (2) (4).....3.1W

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM).....2kV

Recommended Operating Conditions (3)

CH1 continuous voltage..... 10.8V to 13.2V
CH2 continuous voltage..... 4.5V to 5.5V
CH1 output voltage ..... 10.8V to 13.2V
CH2 output voltage ..... 4.5V to 5.5V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

TQFN-10 (2mmx3mm)		
EV5098A-D-00A (4)	40	4 °C/W
JESD51-7 (5) (6)	70	5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV5098A-D-00A, 2-layer PCB (54mmx46mm).
5) Measured on JESD51-7, 4-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, C_{OUT1} = C_{OUT2} = 10µF, T_J = -40°C to +125°C (7), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent current	I_{Q_CH1}	EN = high, I_{12V} = 0A		150		µA
	I_{Q_CH2}	EN = high, I_{5V} = 0A		120		µA
Shutdown current	I_{SD_CH1}	EN = low		60		µA
	I_{SD_CH2}	EN = low		65		µA
Power FET						
On resistance	$R_{DS(ON)\_CH1}$	T_J = 25°C		44		mΩ
		T_J = 125°C			88	mΩ
	$R_{DS(ON)\_CH2}$	T_J = 25°C		44		mΩ
		T_J = 125°C			88	mΩ
Turn-on delay (8)	t_{UVLO_DELAY}	Under-voltage lockout (UVLO) delay		100		ms
	t_{EN_DELAY}	EN delay, from EN high to SS		200		µs
LDO						
Output voltage	V_{LDO}	I_{LDO} = 0A, T_J= 25°C	4.8	5	5.2	V
		I_{LDO} = 10mA, T_J= 25°C	4.7	4.9	5.1	V
Soft-start time (8)	t_{SS}	V_{LDO} rise from 0% to 90%, T_J = 25°C		830		µs
Current limit (8)	I_{LIMIT}	I_{LDO} ramp up, T_J = 25°C		30		mA
Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP)						
UVLO rising threshold	V_{UVLO_CH1}		8.35	8.6	8.85	V
	V_{UVLO_CH2}		3.9	4	4.1	V
UVLO hysteresis	$V_{UVLOHYS\_CH1}$			800		mV
	$V_{UVLOHYS\_CH2}$			300		mV
Output over-voltage clamp voltage	V_{OVLO_CH1}		13.8	15	16	V
	V_{OVLO_CH2}		5.5	5.7	5.9	V
Output over-voltage response time (8)	$t_{OUT\_OV\_CH1}$	C_{OUT} = 10µF, add a 30Ω load resistor, V_{IN1} = 12V to 18V/10µs		1		µs
	$t_{OUT\_OV\_CH2}$	C_{OUT} = 10µF, add a 10Ω load resistor, V_{IN2} = 5V to 7V/10µs		1		µs
Enable (EN) Control						
EN high input voltage	V_{EN_H}		1.4			V
EN low input voltage	V_{EN_L}				0.4	V
EN turn-off delay time (8)	t_{OFF_DELAY}				1	µs
EN pull-up resistance	R_{EN}		2			MΩ
SAS high input voltage	V_{SAS_H}		1.4			V
SAS low input voltage	V_{SAS_L}				0.5	V
SAS pull-down resistance	R_{SAS}		2			MΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, C_{OUT1} = C_{OUT2} = 10µF, T_J =-40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft Start (SS)						
SS current	I_{SS_CH1}		4.3	5.7	7.2	µA
	I_{SS_CH2}		4.3	6.1	8	µA
Current Limit						
Current limit at normal operation	I_{LIMIT_CH1}		-10%	4.5	+10%	A
	I_{LIMIT_CH2}		-10%	3	+10%	A
Current limit response time [8]	t_{CL_CH1}			15		µs
	t_{CL_CH2}			15		µs
Secondary current limit [8]	$I_{LIMIT\_H\_CH1}$			8		A
	$I_{LIMIT\_H\_CH2}$			8		A
Hiccup mode on time	t_{HICP_ON}			2		ms
Hiccup mode off time	t_{HICP_OFF}			200		ms
Over-Temperature Protection (OTP)						
Thermal shutdown [8]	T_{SD}			150		°C

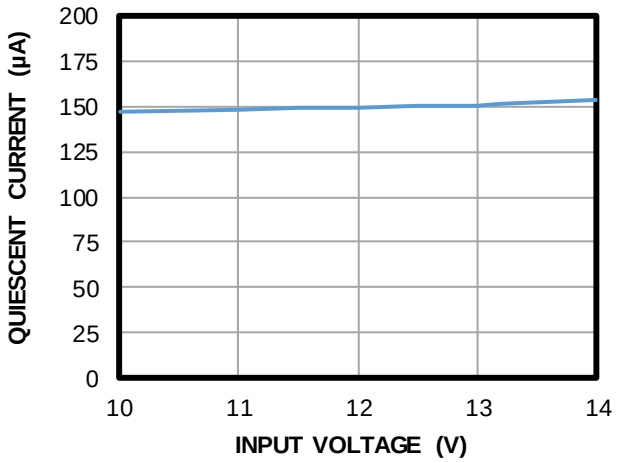
Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization.

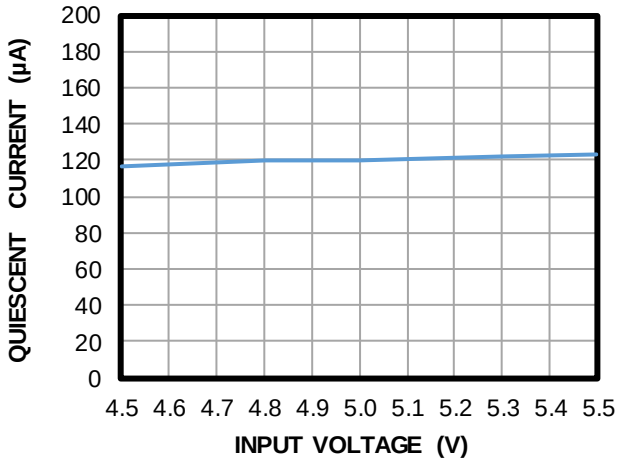
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage (12V E-Fuse)

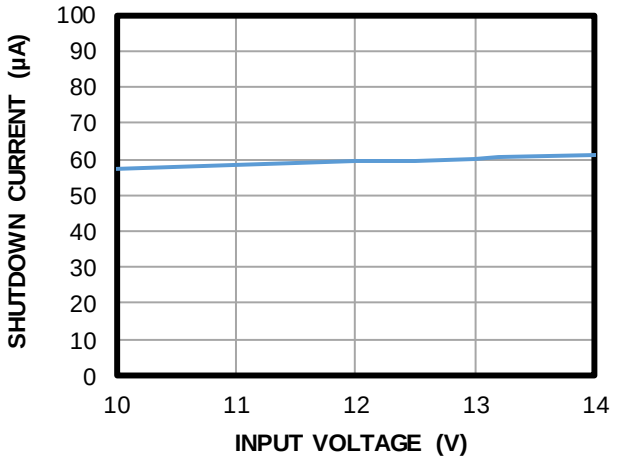


Quiescent Current vs. Input Voltage (5V E-Fuse)



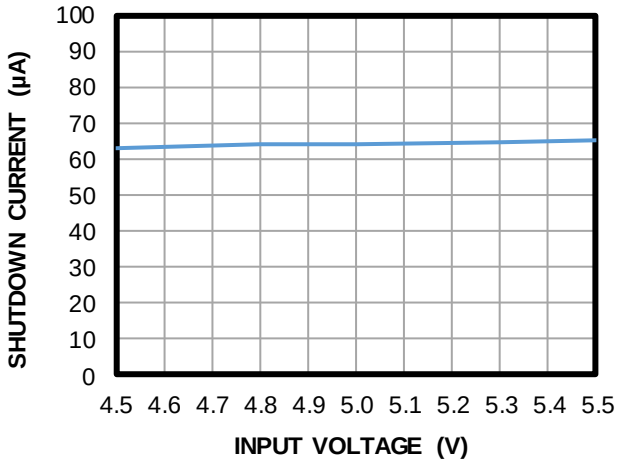
Shutdown Current vs. Input Voltage (12V E-Fuse)

V_{EN} = 0V

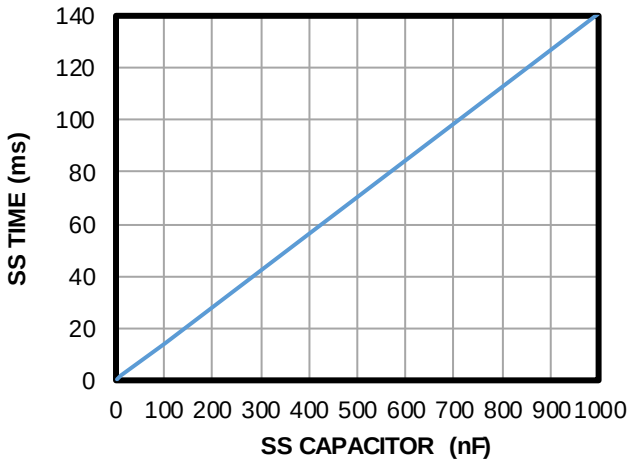


Shutdown Current vs. Input Voltage (5V E-Fuse)

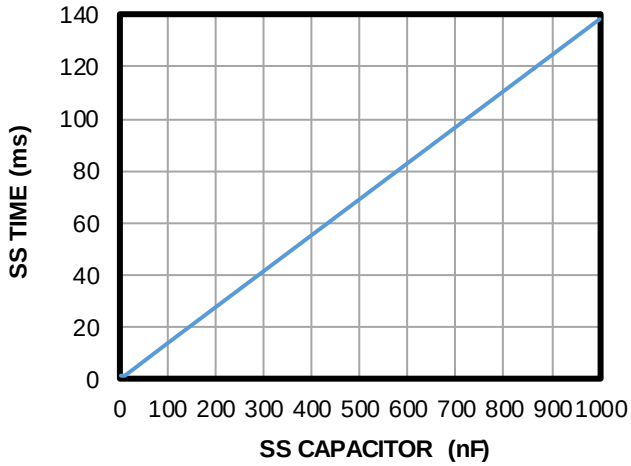
V_{EN} = 0V



SS Time vs. SS Capacitor (12V E-Fuse)



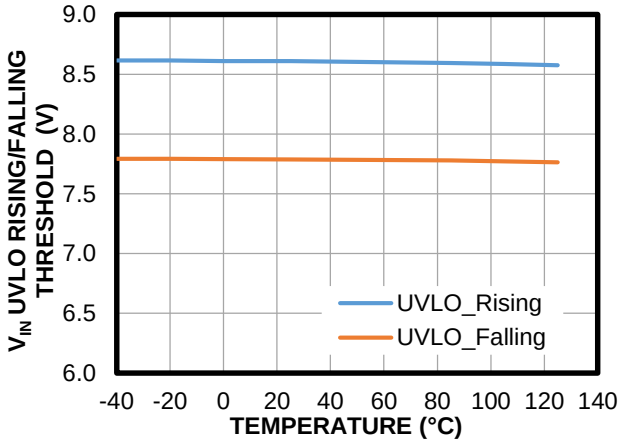
SS Time vs. SS Capacitor (5V E-Fuse)



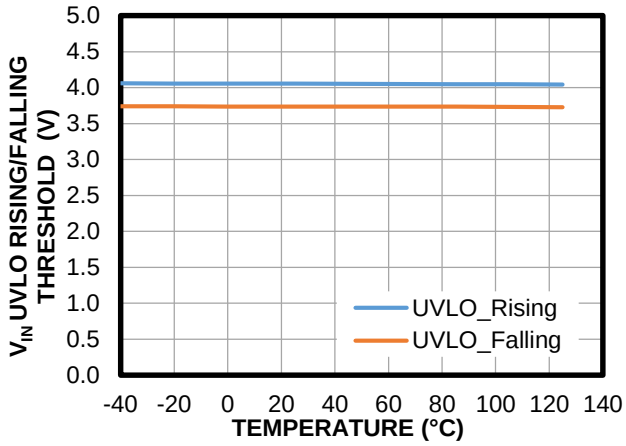
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

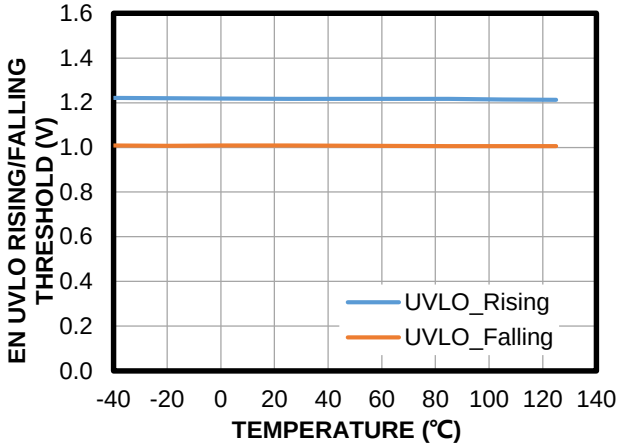
V_{IN} UVLO Rising/Falling Threshold vs. Temperature (12V E-Fuse)



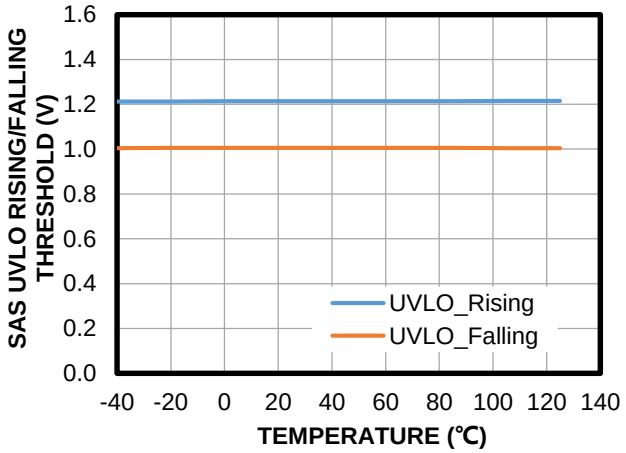
V_{IN} UVLO Rising/Falling Threshold vs. Temperature (5V E-Fuse)



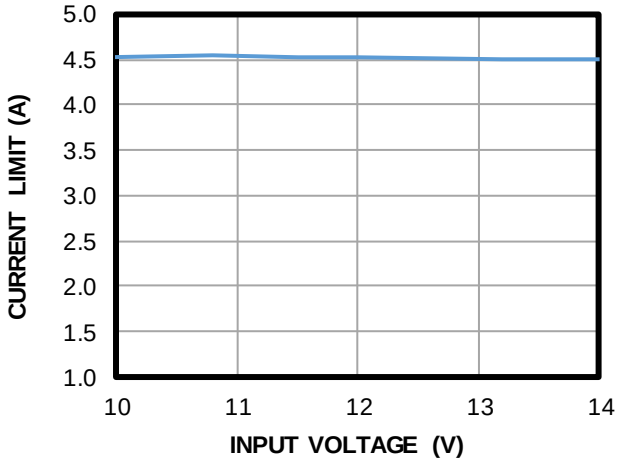
EN UVLO Rising/Falling Threshold vs. Temperature (12V E-Fuse)



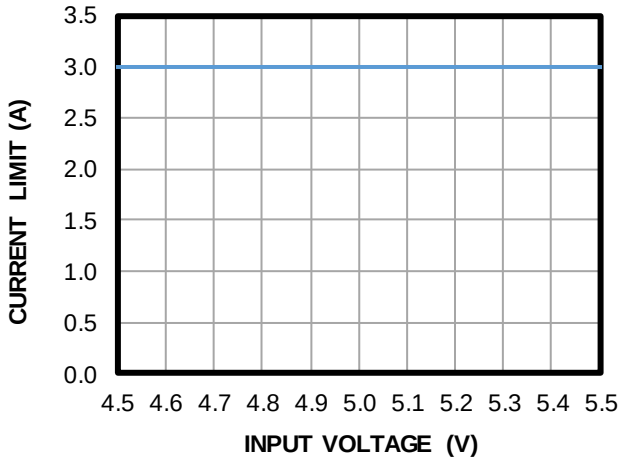
SAS UVLO Rising/Falling Threshold vs. Temperature (5V E-Fuse)



Current Limit vs. Input Voltage (12V E-Fuse)



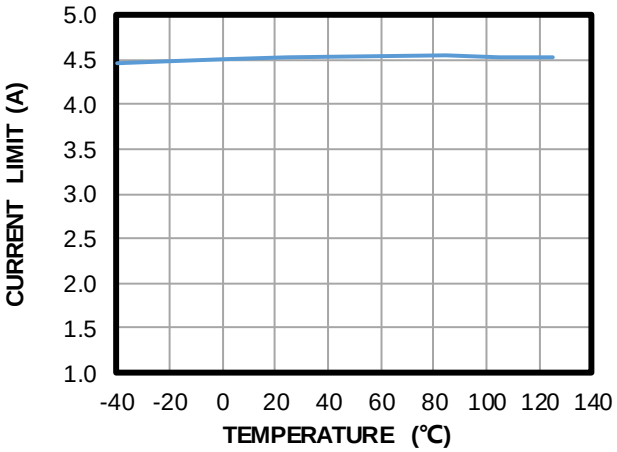
Current Limit vs. Input Voltage (5V E-Fuse)



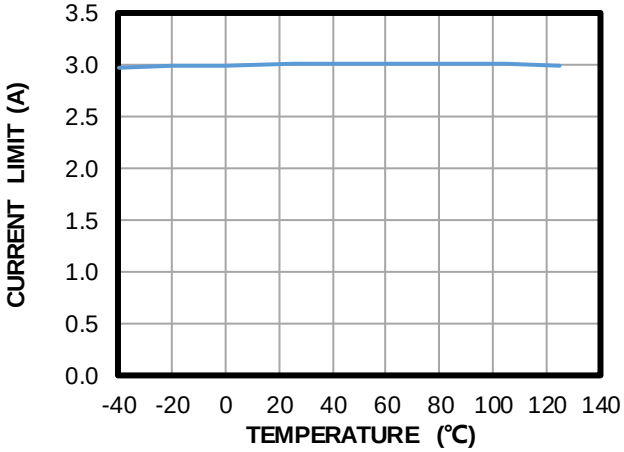
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

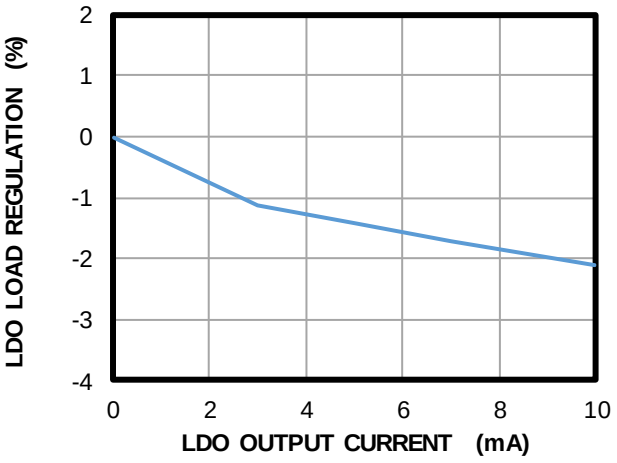
Current Limit vs. Temperature (12V E-Fuse)



Current Limit vs. Temperature (5V E-Fuse)



LDO Load Regulation vs. LDO Output Current

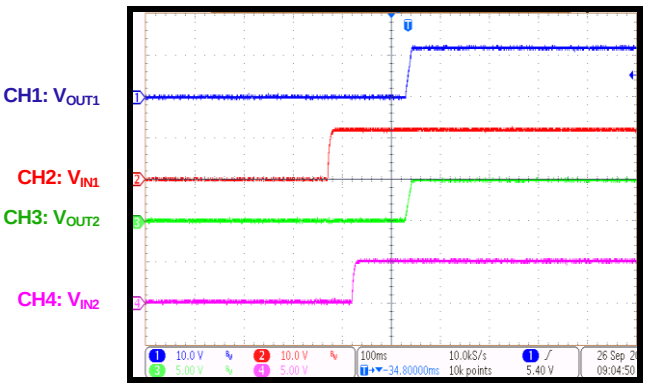


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

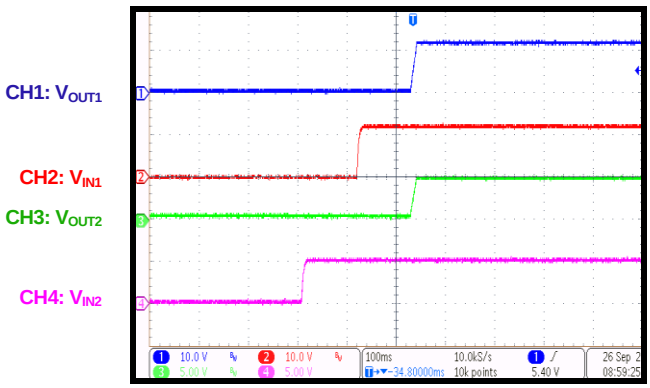
CH1/CH2 Start-Up Logic

CH1 starts up first, I_{OUT1} = I_{OUT2} = 0A



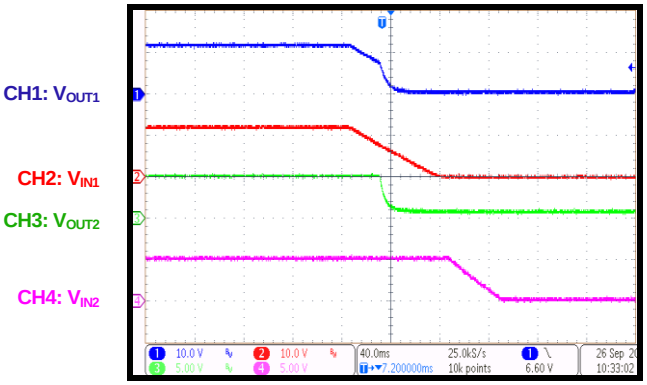
CH1/CH2 Start-Up Logic

CH2 starts up first, I_{OUT1} = I_{OUT2} = 0A



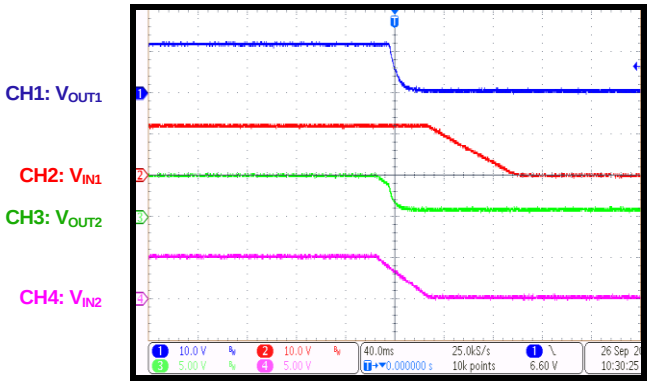
CH1/CH2 Shutdown Logic

CH1 shuts down first, I_{OUT1} = I_{OUT2} = 0A



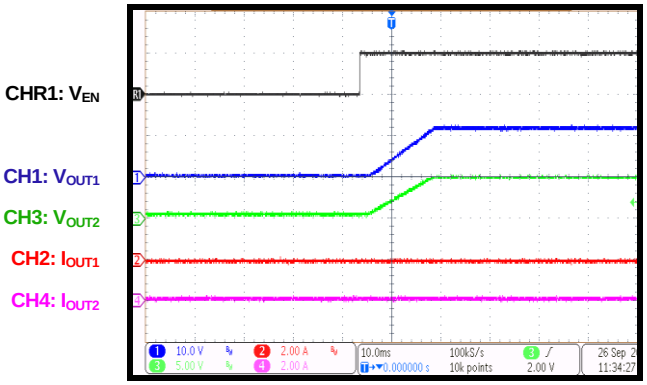
CH1/CH2 Shutdown Logic

CH2 shuts down first, I_{OUT1} = I_{OUT2} = 0A



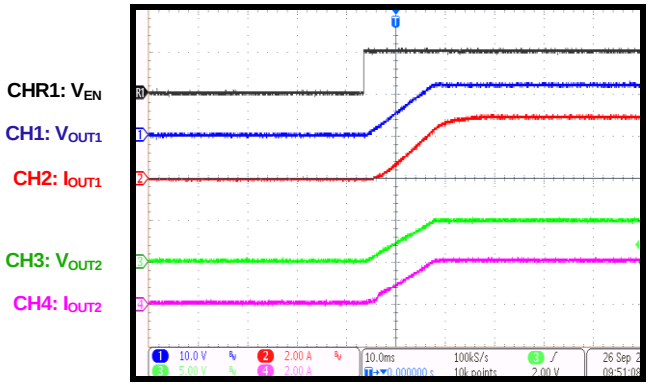
CH1/CH2 EN On Logic

I_{OUT1} = I_{OUT2} = 0A



CH1/CH2 EN On Logic

I_{OUT1} = 3A, I_{OUT2} = 2A

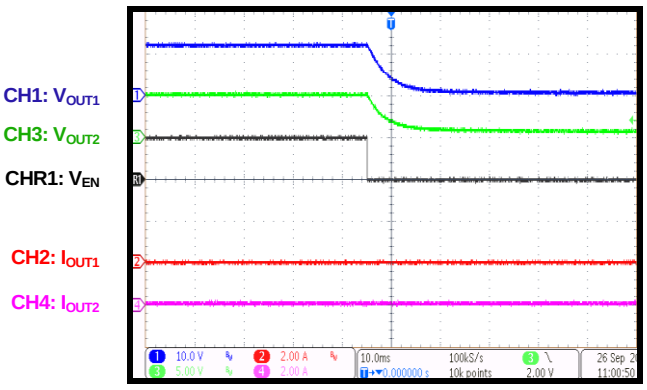


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

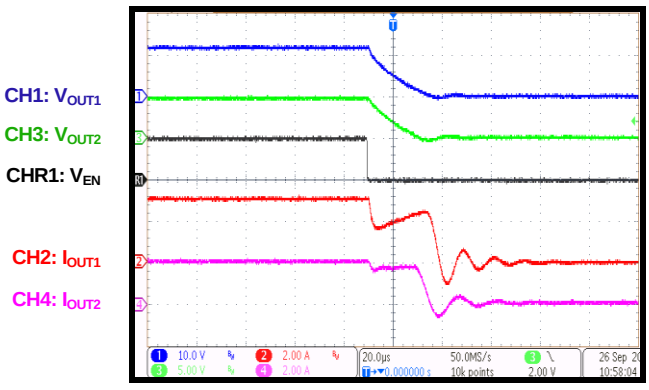
CH1/CH2 EN Off Logic

I_{OUT1} = I_{OUT2} = 0A



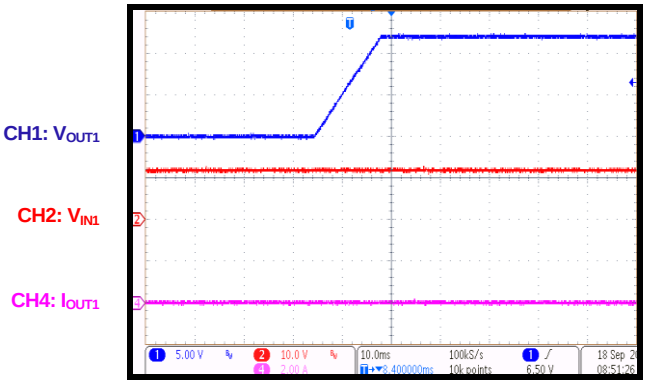
CH1/CH2 EN Off Logic

I_{OUT1} = 3A, I_{OUT2} = 2A



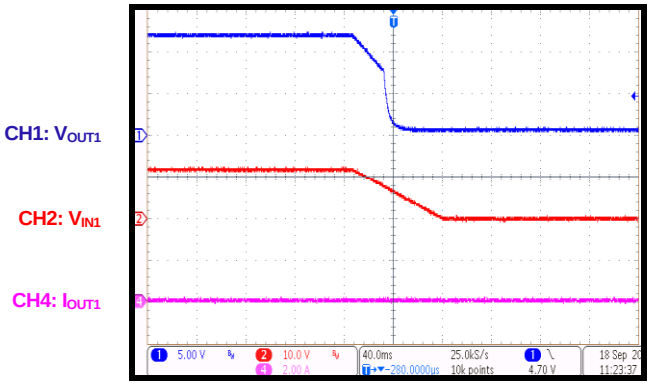
Start-Up through VIN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



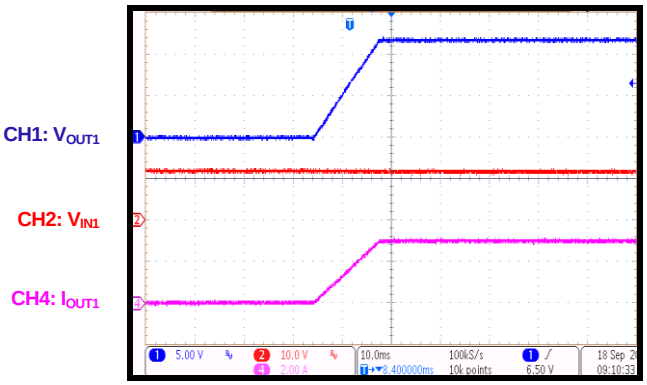
Shutdown through VIN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



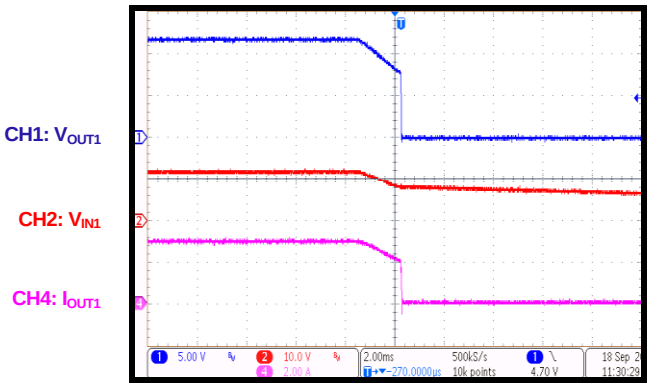
Start-Up through VIN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



Shutdown through VIN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A

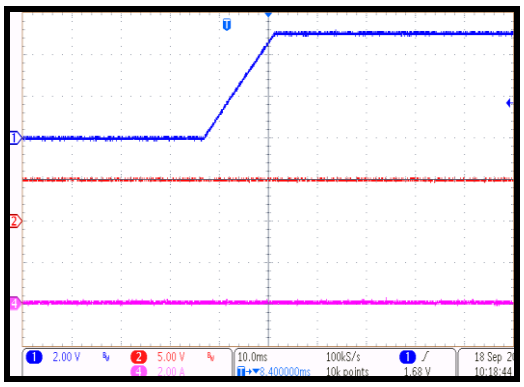


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

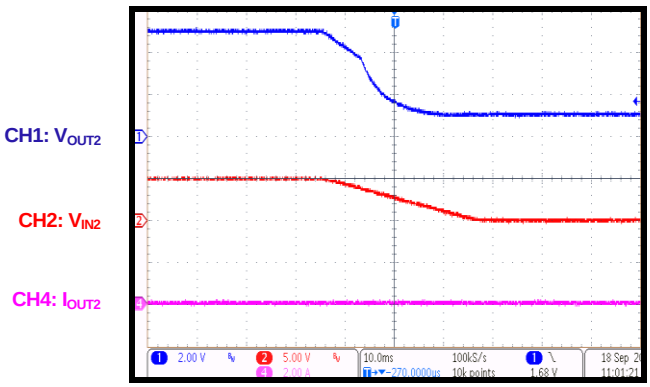
Start-Up through VIN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



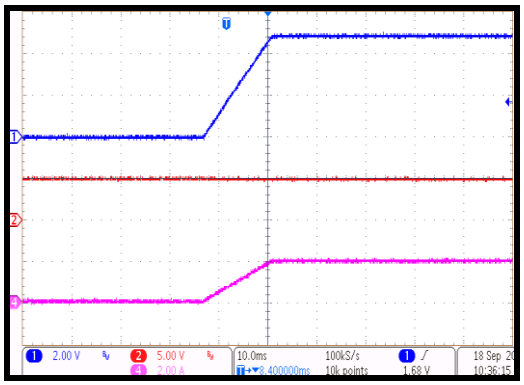
Shutdown through VIN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



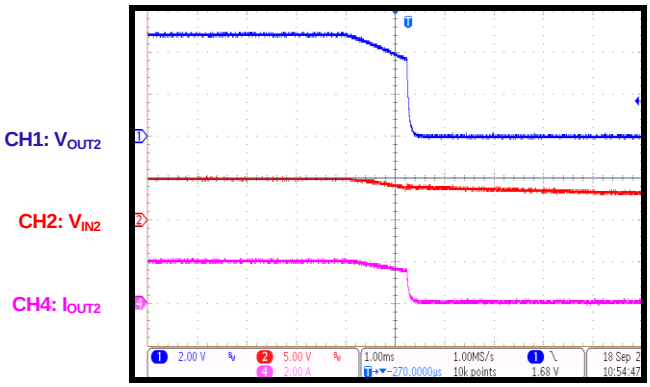
Start-Up through VIN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



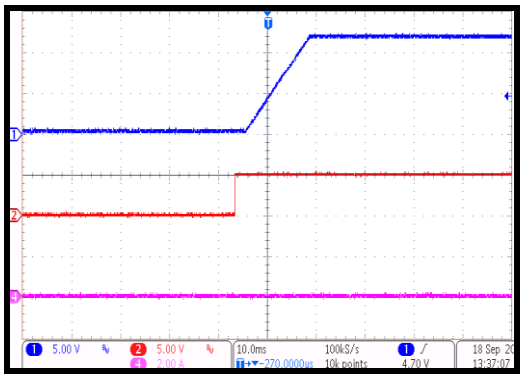
Shutdown through VIN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



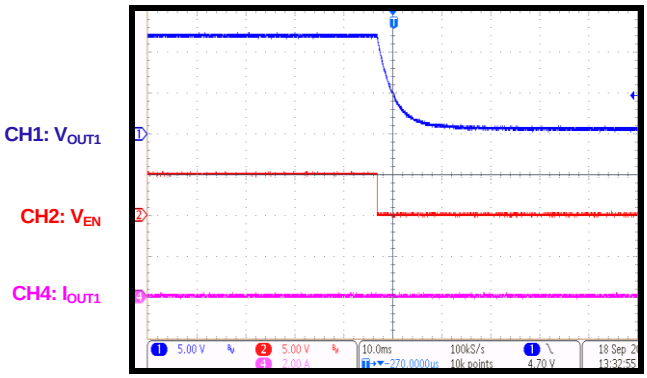
Start-Up through EN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



Shutdown through EN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A

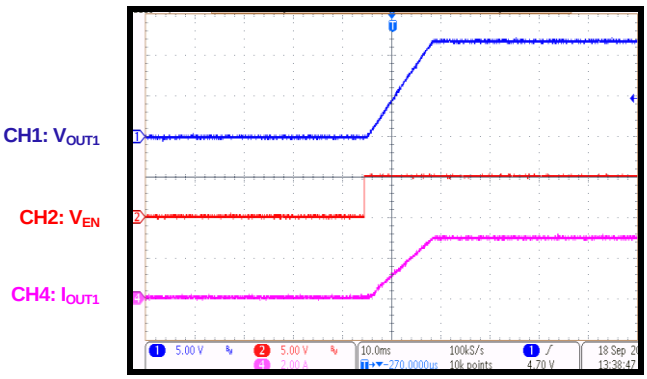


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

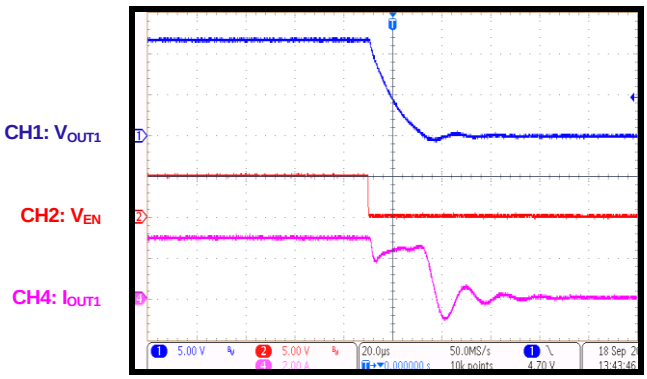
Start-Up through EN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



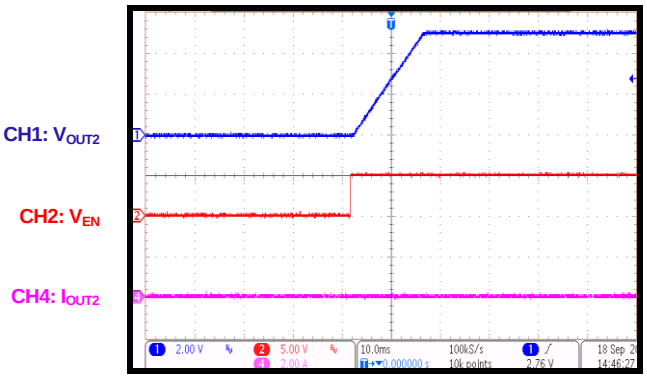
Shutdown through EN (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



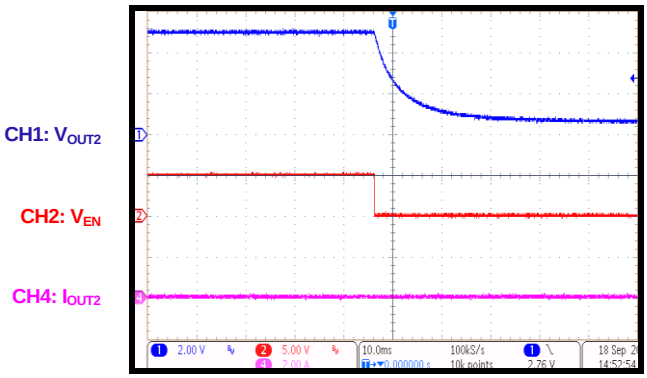
Start-Up through EN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



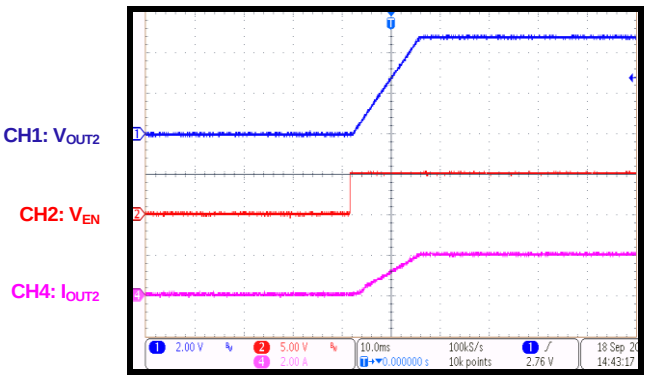
Shutdown through EN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



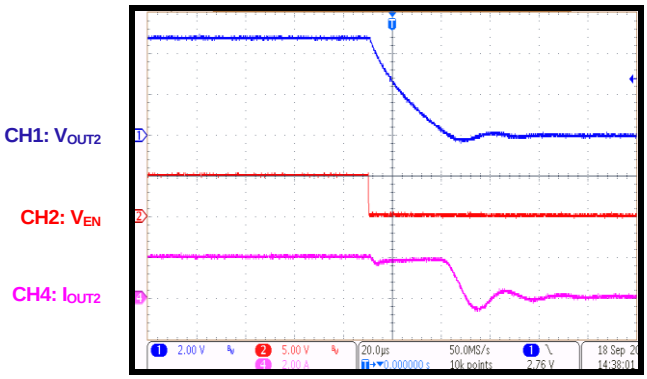
Start-Up through EN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



Shutdown through EN (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

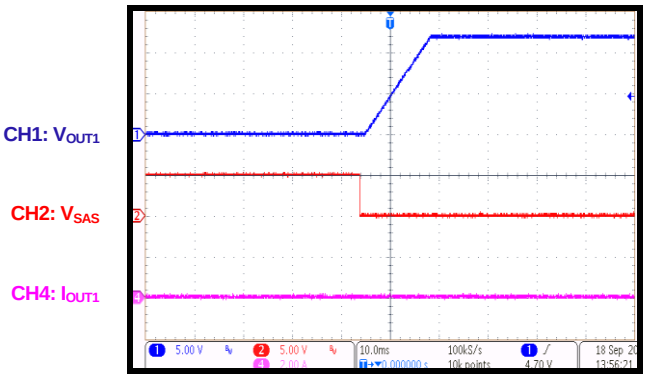


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

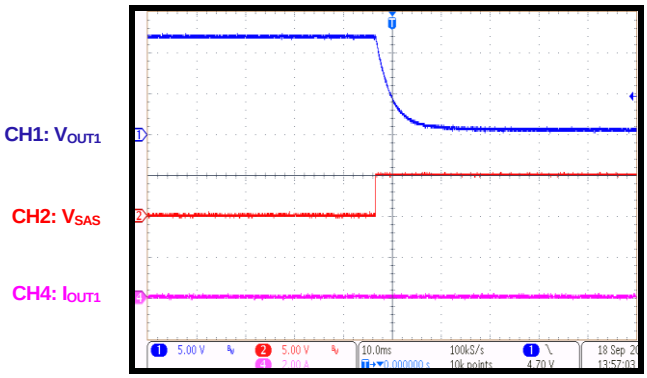
Start-Up through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



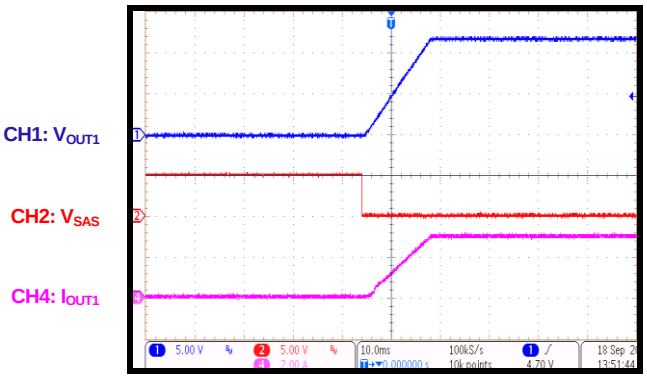
Shutdown through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 0A



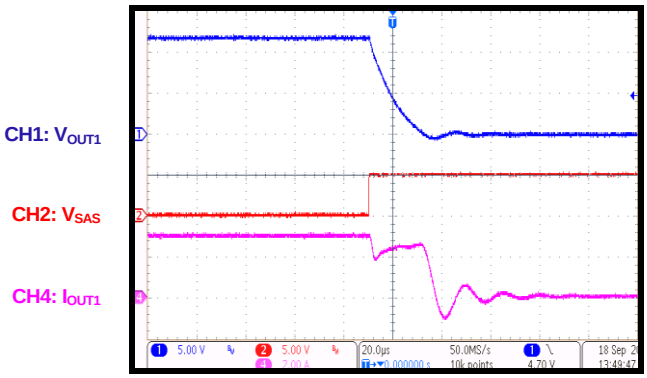
Start-Up through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



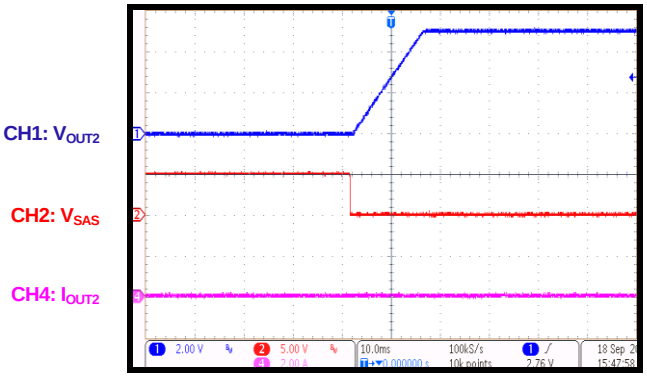
Shutdown through SAS (12V E-Fuse)

V_{IN2} = 5V, I_{OUT1} = 3A



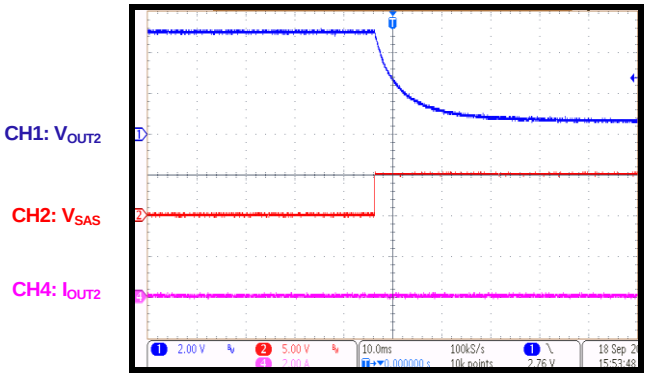
Start-Up through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A



Shutdown through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 0A

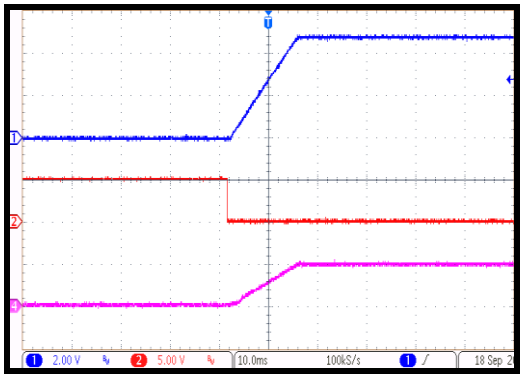


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

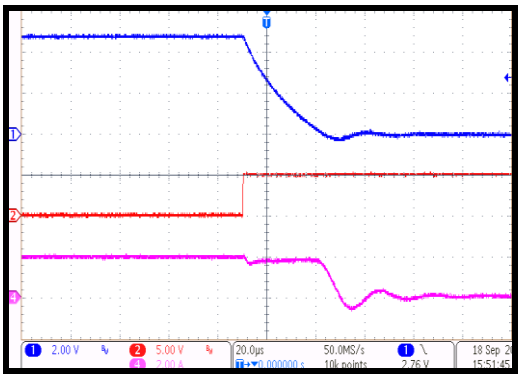
Start-Up through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A



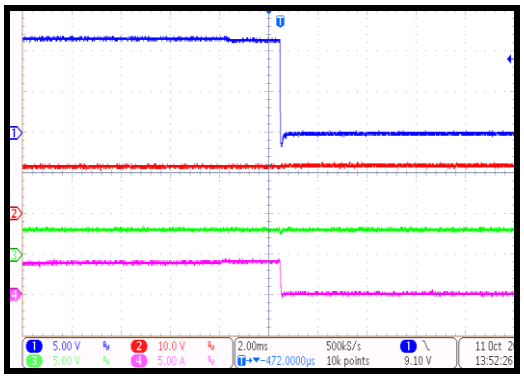
Shutdown through SAS (5V E-Fuse)

V_{IN1} = 12V, I_{OUT2} = 2A

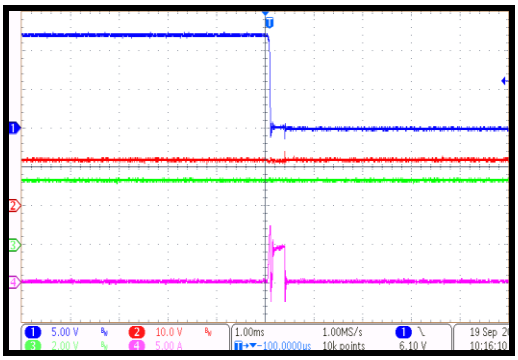


Current Limit (12V E-Fuse)

Increase I_{OUT} slowly

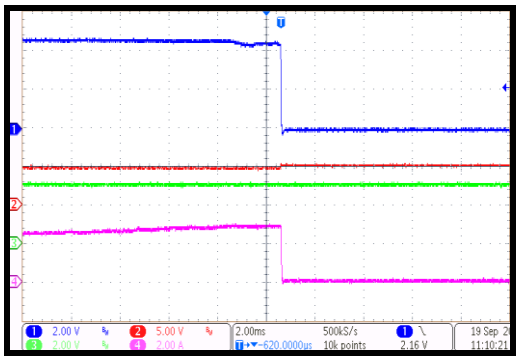


Short Circuit during Normal Operation (12V E-Fuse)

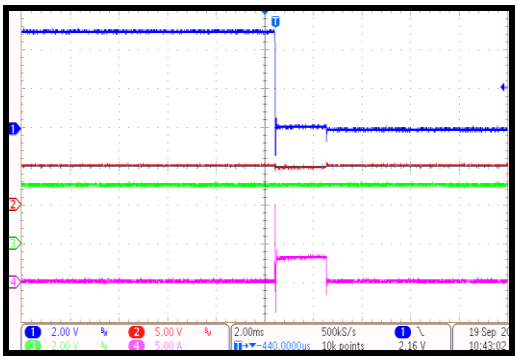


Current Limit (5V E-Fuse)

Increase I_{OUT} slowly



Short Circuit during Normal Operation (5V E-Fuse)

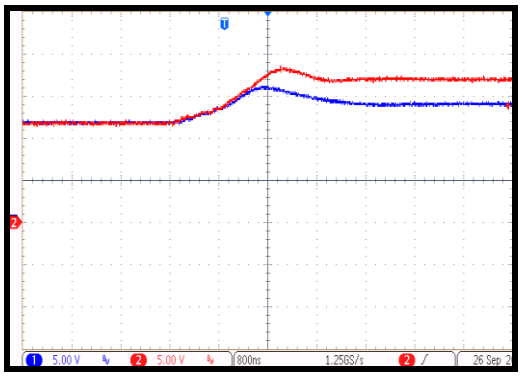


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, T_A = 25°C, unless otherwise noted.

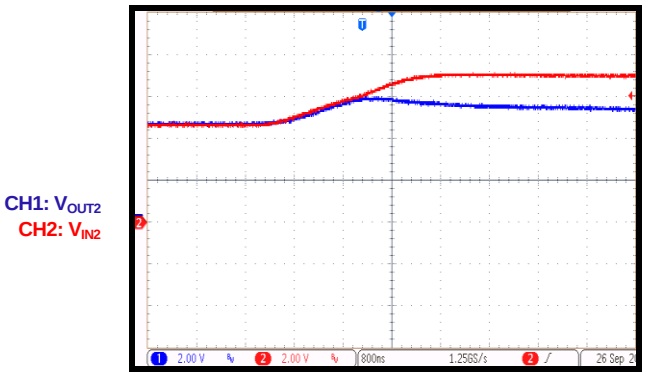
Output Over-Voltage Protection (12V E-Fuse)

V_{IN1} = 12V to 17V, I_{OUT1} = 0.4A



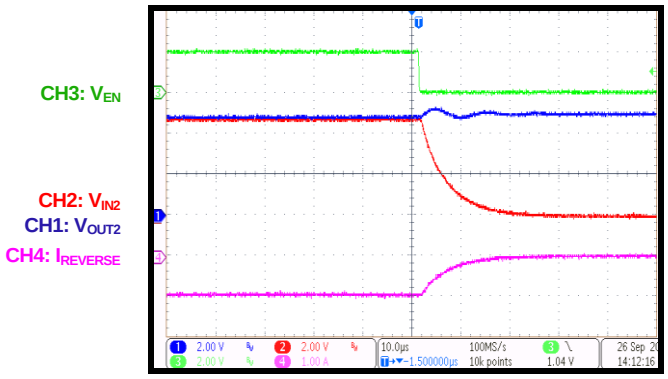
Output Over-Voltage Protection (5V E-Fuse)

V_{IN2} = 5V to 7V, I_{OUT2} = 0.4A



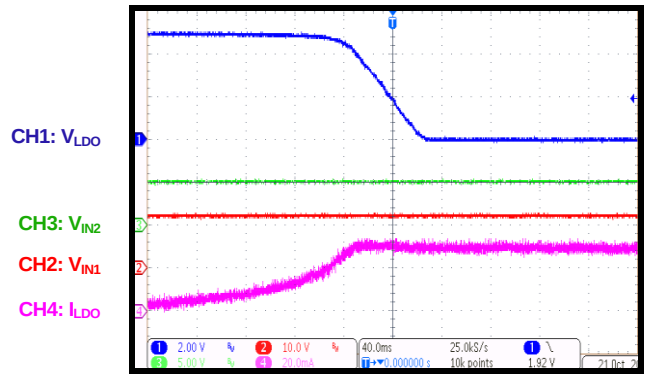
Reverse Protection (5V E-Fuse)

Increase $I_{REVERSE}$ slowly



Current Limit (LDO)

Increase I_{LDO} slowly



FUNCTIONAL BLOCK DIAGRAM

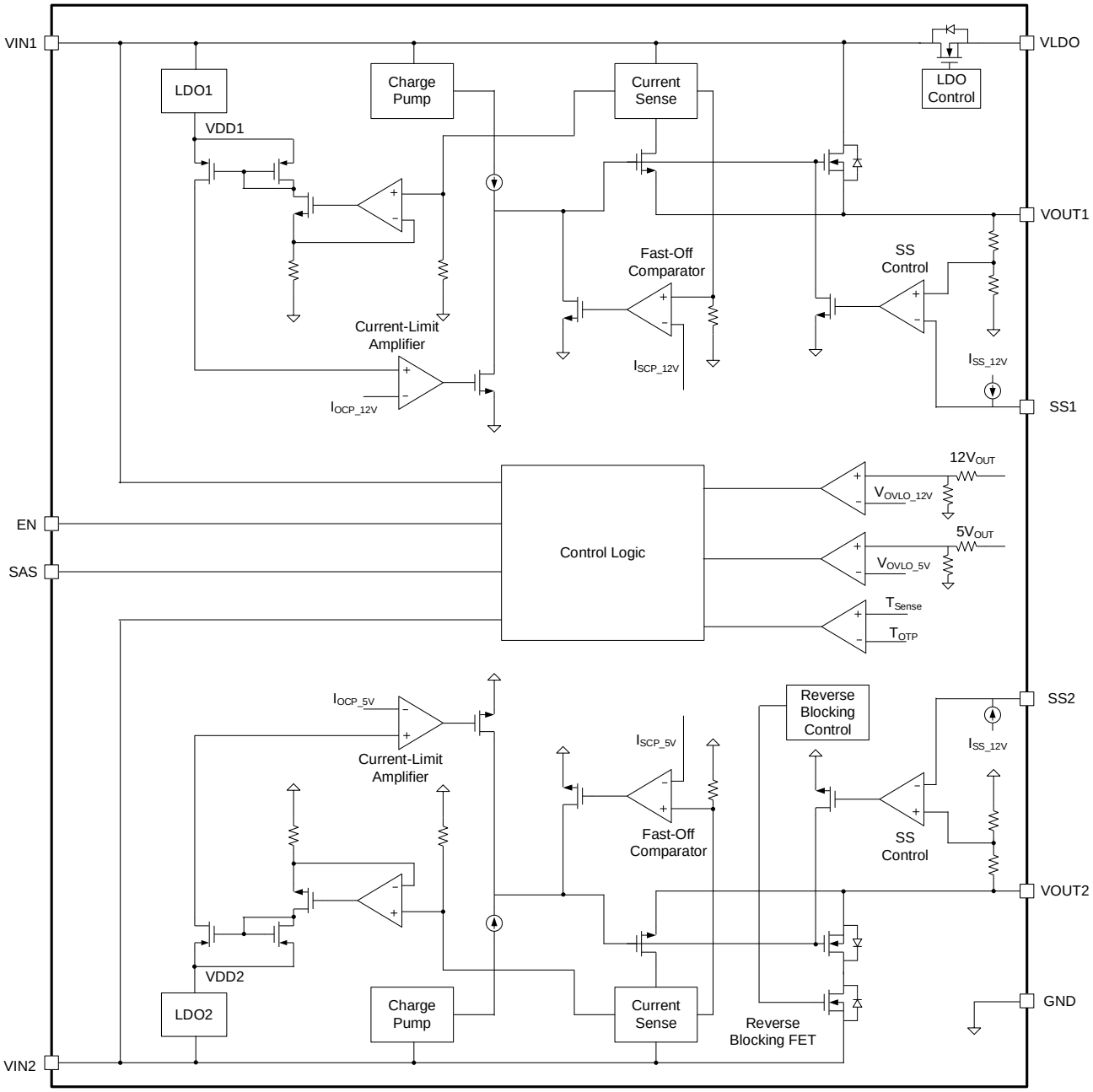


Figure 1: Functional Block Diagram

OPERATION

The MP5098A is a dual 5V/12V e-fuse integrated into a small TQFN-10 (2mmx3mm) package. The device protects circuitry on the output from transients on the input. It also prevents shorts at the output and limits the input inrush current during system start-up. The 5V and 12V channels provide load currents up to 3A and 4.5A, respectively.

Under-Voltage Lockout (UVLO)

The MP5098A's channel 1 can be used in the 12V input supply system, and channel 2 can be used in the 5V input supply system. High energy transients occur during normal operation or during hot swap. These transients depend on the parasitic inductance and resistance of the wire, as well as a capacitor at the VCC node. If a power clamp (e.g. TVS or TransZorb) diode is not used, the e-fuse must be able to withstand the transient voltage. The MP5098A integrates a high-voltage MOSFET and also uses a high-voltage circuit for the VCC node to guarantee safe operation. When V_{IN1} rises to the channel 1 UVLO rising threshold (8.6V) and V_{IN2} rises to the channel 2 UVLO rising threshold (4V), the whole chip turns on; once one of the channels shuts down, the whole chip turns off.

Soft Start (SS)

Connect a capacitor to the SS pin to set the soft-start time (t_{SS}). A constant current source charges the SS capacitor (C_{SS}) and results in a linear ramping voltage on the SS pin. The output voltage (V_{LDO}) rises at a similar slew rate to the SS voltage.

t_{SS} is a function of C_{SS}. $t_{DV/DT}$ can be calculated with Equation (1):

$$t_{DV/DT}(ms) = \frac{\frac{V_{IN}}{V_{CLAMP}}(V) \times C_{SS}(nF)}{I_{SS}(\mu A)} \quad (1)$$

Where $t_{DV\ /\ DT}$ = t_{SS} from 0% to 100% V_{LDO}, V_{CLAMP} is the output over-voltage clamp voltage, V_{IN} is the input voltage, and I_{SS} is the SS current.

Current Limit

The MP5098A provides a constant current limit. Once the current limit threshold is reached, the internal circuit regulates gate voltage to constantly hold the current in power FET. The current limit is 4.5A for the 12V rail and 3A for the 5V rail.

Short-Circuit Protection (SCP)

If the load current rapidly increases due to a short-circuit event, the current may exceed the current limit threshold before the control loop is able to respond. If the current reaches a secondary current limit level of 8A, a fast turn-off circuit activates to turn off the power FET (see Figure 1 on page 16). The fast turn-off circuit limits the peak current through the switch, which prevents V_{IN} from dropping drastically. The total short circuit response time is shorter than 1µs. After the FET switches off, the part restarts. During the restart process, if the short still exists, the MP5098A regulates the gate voltage to hold the current at a normal current limit level. The IC enters hiccup mode with a 200ms off time.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. All the FETS shut down when the silicon die temperature exceeds 150°C.

Reverse Behavior

The 5V channel uses the EN and SAS pins with its internal, back-to-back, N-channel MOSFETs to protect the reverse current between V_{OUT} and V_{IN} during shutdown. After a (maximum) delay time of 1µs, the MOSFET turns off. Figure 2 shows the reverse behavior.

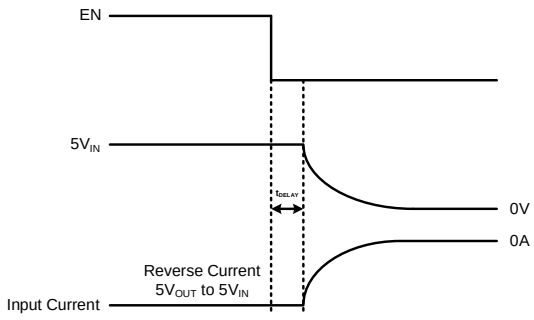


Figure 2: Reverse Behavior

Start-Up Sequence Control

When both channel 1 and channel 2 exceed the UVLO threshold, the 5V LDO output ramps up in 1ms, and the output is charged by the SS slew rate.

The EN and SAS logics control the start-up sequences for channel 1 and channel 2.

There is a 100ms between when the input voltage is ready and the output voltage begins ramping up.

If EN is pulled high and SAS is pulled low for 100ms while V_{IN} exceeds the UVLO threshold, channel 1 and channel 2 ramp up under the control of the 100ms delay (see Figure 3).

If EN is pulled high and SAS is pulled low 100ms after V_{IN} exceeds the UVLO threshold, channel 1 and channel 2 ramp up under the control of EN and SAS (see Figure 4).

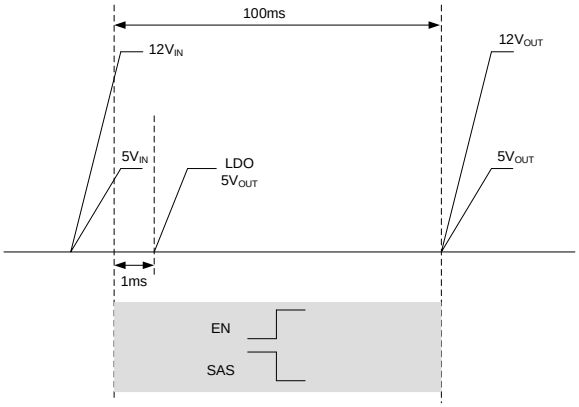


Figure 3: Start-Up Sequence under 100ms Delay

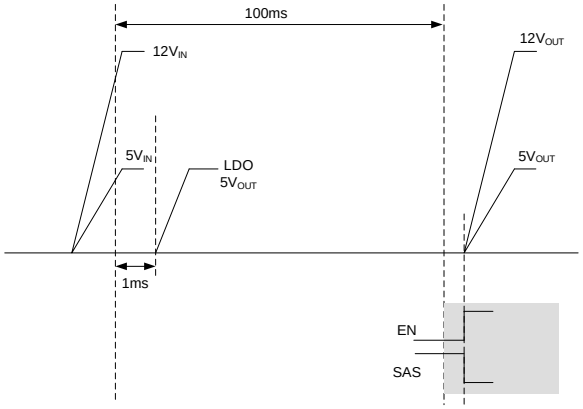


Figure 4: Start-Up Sequence under EN and SAS

APPLICATION INFORMATION

Design Example

Table 1 shows a design example following the application guidelines for the specifications below.

Table 1: Design Example

V_{IN1}	V_{OUT1}	V_{IN2}	V_{OUT2}
12V	12V	5V	5V

Figure 6 on page 20 shows the detailed application circuit. The typical performance and waveforms are shown in the Typical Performance Characteristics section on page 6. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical for improved performance. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high-current paths (VIN and VOUT) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VIN and GND pins.
3. Connect the VIN and VOUT pads to large VIN and VOUT planes, respectively, to improve thermal performance.
4. Place C_{SS} close to the SS pin.

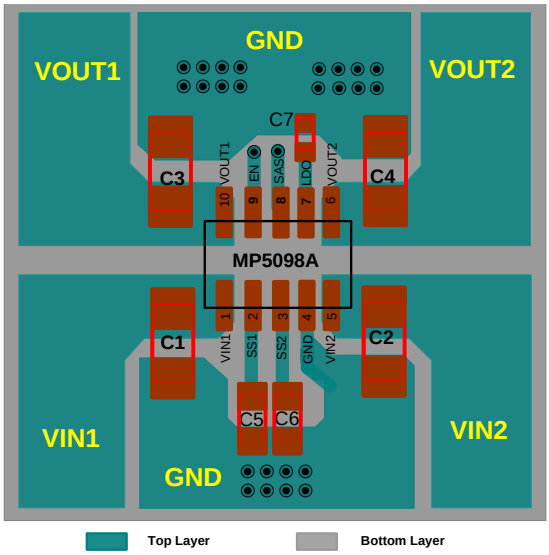


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

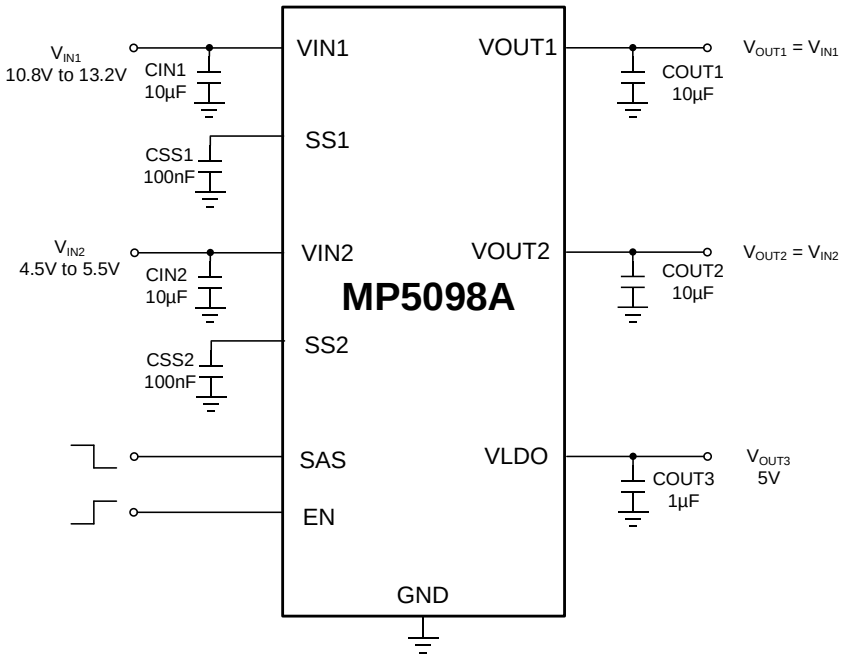
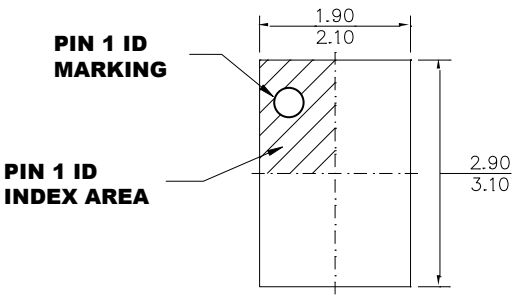


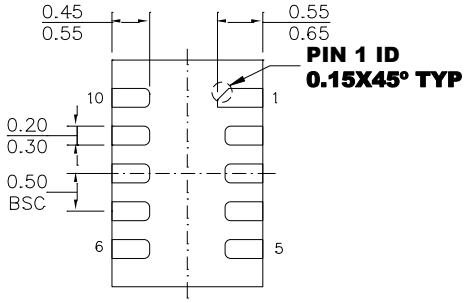
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

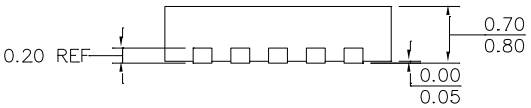
TQFN-10 (2mmx3mm)



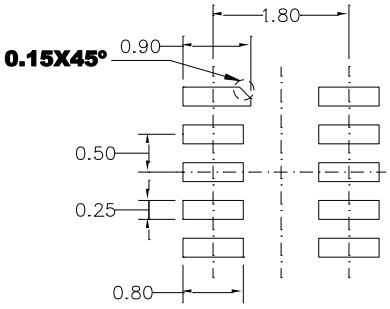
TOP VIEW



BOTTOM VIEW



SIDE VIEW

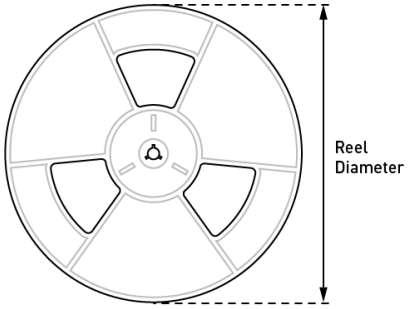


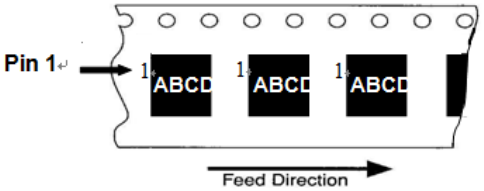
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5098AGDT-Z	TQFN-10 (2mmx3mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/02/2021	Initial Release	-